# XM981A Series

ETR08005-001

## 60V 6A buck Charge pump-based DCDC Converter Module

## ■GENERAL DESCRIPTION

XM981A series is an Ultra-thin High Efficiency integrated power module which combines a 72W buck charge pump-based DC-DC converter with components.

This Module is a buck charge pump that outputs one-quarter of the input voltage, only three peripheral components are required to provide output power with a maximum efficiency of 96.5%.

Input voltage range is 20V to 60V, the maximum output current is 6A. It perfectly supports 12V intermediate bus from 48V systems.

Compared to DC/DC converters that use inductors, the XM981A is ideal for applications that require high efficiency in a small footprint and low profile.

The XM981A also supports parallel connection, allowing up to 4 parallel connections (6A x 4 parallel = 24A), making it usable in applications requiring higher power.

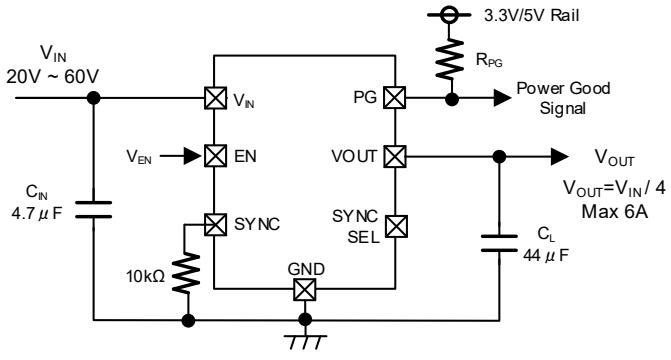
## ■APPLICATIONS

- Data center/server
- Networking equipment
- Base station
- Optical equipment
- Test equipment
- LED signage
- PoE equipment
- 48V/12V medium-size bus

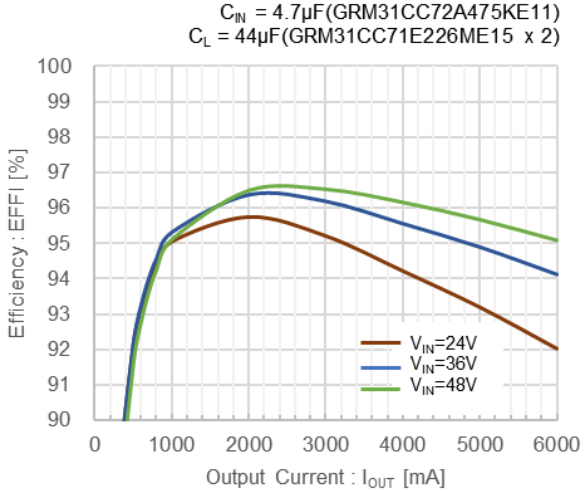
## ■FEATURES

| | |
|---|---|
| Input Voltage Range | : 20V ~ 60V |
| Output Voltage | : $V_{IN}$ / 4 |
| Output Current | : 6A<br>* When operating in parallel:<br>Max. 24A = 6A x 4 parallel |
| Oscillation Frequency | : 270kHz |
| Efficiency | : 96.5% @ $V_{IN}$=48V, $I_{OUT}$=2.4A |
| Protection Functions | : Thermal shutdown function<br>Current Limit<br>Short-Circuit Protection<br>Soft-Start Time-out<br>Output under-voltage protection |
| Functions | : Parallel operation (Max. 4 parallel)<br>Soft-Start,<br>Power Good, UVLO |
| Output Capacitor | : Ceramic Capacitor |
| Operating Ambient Temperature | : -40℃ ~ 105℃ |
| Package | : LGA-52C01 (11.5 x 9.5 x 2.1mm) |
| Environmentally | : EU RoHS Compliant, Pb Free |

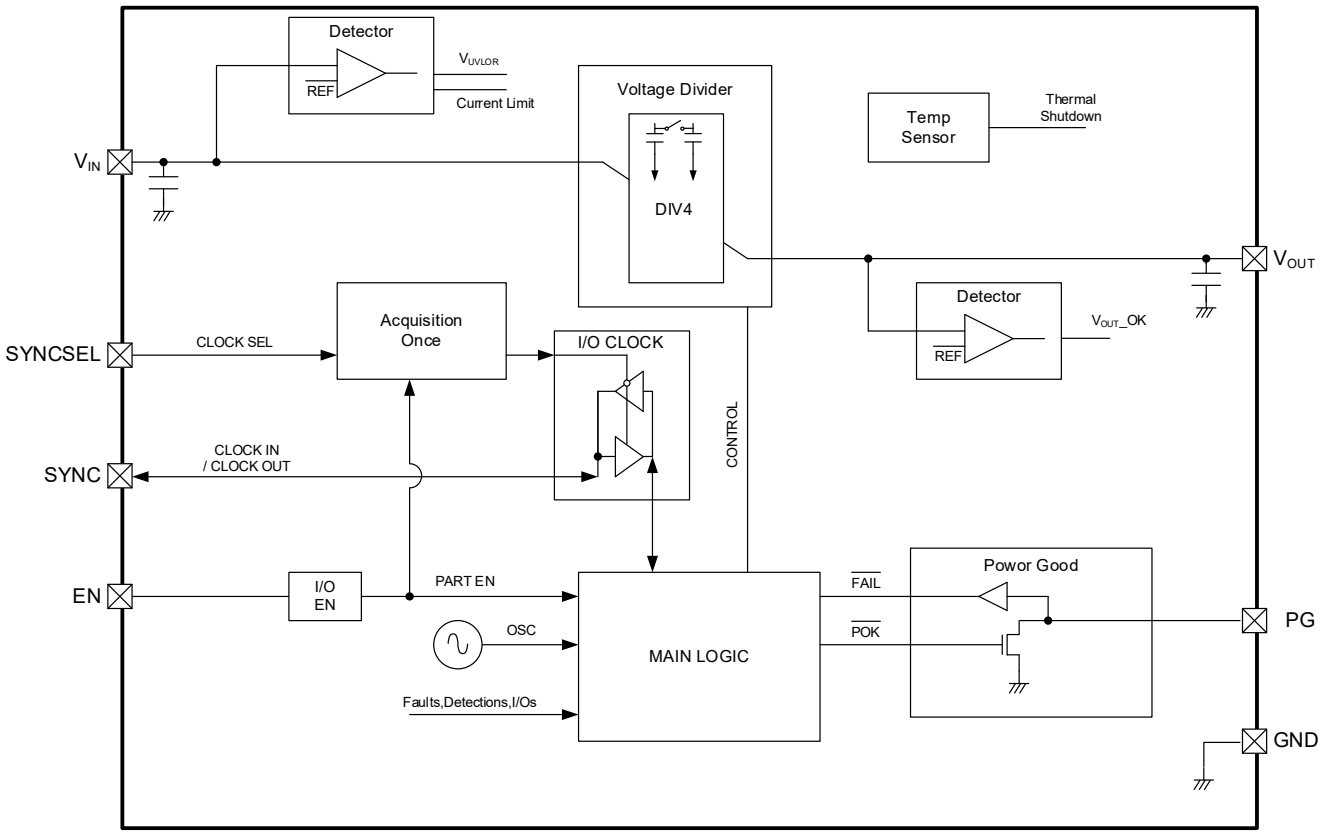
## ■TYPICAL APPLICATION




## ■TYPICAL PERFORMANCE CHARACTERISTICS



## ■BLOCK DIAGRAM




## ■PRODUCT CLASSIFICATION

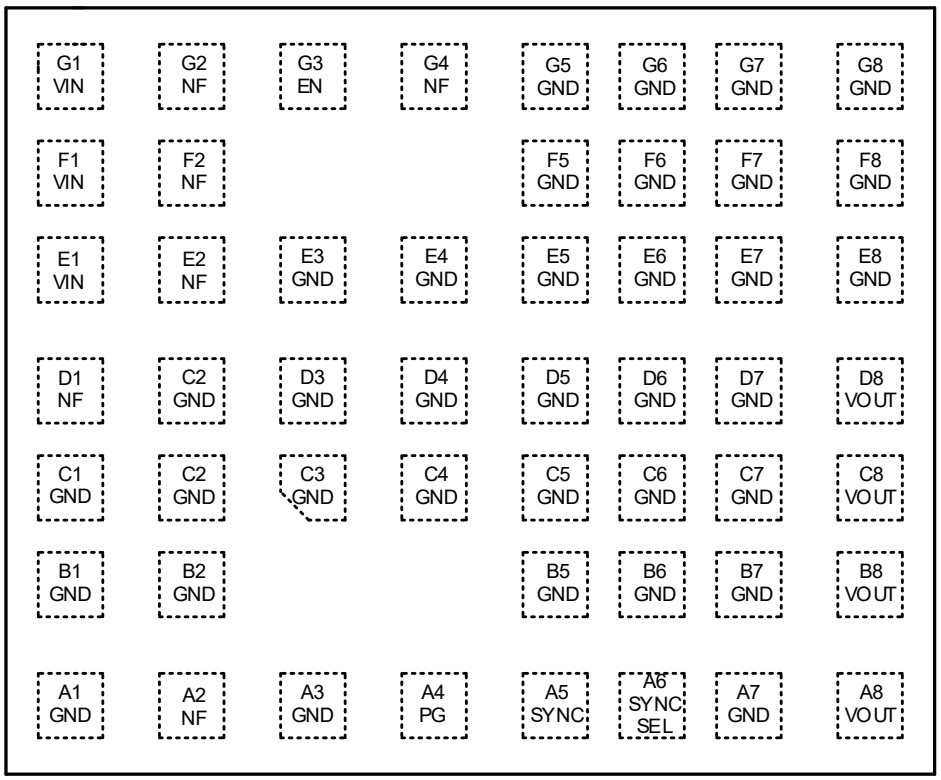
●Ordering Information

XM981A①②③④⑤⑥-⑦

| DESIGNATOR | ITEM | SYMBOL | DESCRIPTION |
|---|---|---|---|
| ① | Type | B | - |
| ② | $V_{OUT}$ | 4 | $V_{OUT} = V_{IN} / 4$ |
| ③④ | Switching Frequency | 03 | 270kHz |
| ⑤⑥-⑦ (*1) | Packages (Order Unit) | 12-G | LGA-52C01 (400pcs/Reel) |

(*1) The “-G” suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

## ■PIN CONFIGURATION




LGA-52C01
(Top View)

## ■PIN ASSIGNMENT

| PIN NUMBER | PIN NAME | FUNCTIONS |
|---|---|---|
| A1, A3, A7, B1, B2, B5-7, C1-7, D2-7, E3-8, F5-8, G5-8 | GND | Ground for power and thermal. |
| E1, F1, G1 | $V_{IN}$ | Power input terminal |
| A8, B8, C8, D8 | $V_{OUT}$ | Power output terminal |
| G3 | EN | Part enable pin.<br>Do not leave this terminal open. |
| A5 | SYNC | CLOCK IN / OUT terminal.<br>Direction is configurable by SYNCSEL terminal potential. |
| A6 | SYNCSEL | SYNC terminal control.<br>“L”=CLOCK OUT, “OPEN”=CLOCK IN. |
| A4 | PG | Power good pin. Connecting a 10kΩ resistor from PG to an external bus voltage between 3.0V and 5.5V. |
| A2, D1, E2, F2, G2 | NF | Do not connect pins electrically. Those pins must connect to the board with solder but must be left floating electrically each other. |

(*1) Connect all GND pins to GND.

(*2) All pins should be soldered to the board for heat dissipation.

## ■FUNCTION

EN function

| PIN NAME | SIGNAL | STATUS |
|---|---|---|
| EN | L | Stand-by |
| | H | Active |
| | OPEN | Undefined State (*1) |

(*1) Please do not leave the EN pin open.

Power Good function

| $V_{IN}$ | EN | STATE | PG |
|---|---|---|---|
| $V_{IN} \leqq V_{UVLOD}$ | X | Undefined State | Undefined State |
| $V_{IN} > V_{UVLOD}$ | "L" | Shutdown | "H" (High impedance) |
| | "H" | Normal operation | "H" (High impedance) |
| | | Start-up | "L" (Low Impedance) |
| | | From shutdown state to 60ms | "L" (Low Impedance) |
| | | Others | "L" (Low Impedance) |

SYNC / SYNCSEL

| Purpose | SYNCSEL | SYNC | DESCRIPTION |
|---|---|---|---|
| Single use | OPEN | 10kΩ Pull-Down Resistor to GND | Standalone use : Operates with internal clock when SYNCSEL=OPEN. |
| Clock input device in parallel operation | OPEN | CLOCK Input | Parallel operation : Operates synchronously with an external clock. |
| Clock output device in parallel operation | GND | CLOCK Output | Parallel operation : Outputs an internal clock. |

## ■ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATINGS | UNITS |
|---|---|---|---|
| $V_{IN}$ Pin Voltage | $V_{IN}$ | -0.3 ~ 61.0 | V |
| EN Pin Voltage | $V_{EN}$ | -0.3 ~ $V_{IN}$ + 0.3 | V |
| SYNC Pin Voltage | $V_{SYNC}$ | -0.3 ~ 5.5 | V |
| SYNCSEL Pin Voltage | $V_{SYNCSEL}$ | -0.3 ~ 5.5 | V |
| PG Pin Voltage | $V_{PG}$ | -0.3 ~ 5.5 | V |
| $V_{OUT}$ Pin Voltage | $V_{OUT}$ | -0.3 ~ $V_{IN}$ / 4 + 0.1 | V |
| Output Current | Iout | 0 ~ 8.0 | A |
| Junction Temperature | Tj | -40 ~ 120 | ℃ |
| Storage Temperature | Tstg | -55 ~ 125 | ℃ |

All voltages are described based on the GND pin.

## ■Package Thermal Characteristics

| PARAMETER | **SYMBOL** | TYP. | UNITS |
|---|---|---|---|
| Junction-case-top at Heat Junction | $\Theta_{jc\text{-}top}$ | 15.9 | ℃/W |
| Junction-case-bottom at Heat Junction | $\Theta_{jc\text{-}bottom}$ | 4.7 | ℃/W |

## ■RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|
| Input Voltage | $V_{IN}$ | 20.0 | - | 60.0 | V |
| EN Pin Voltage | $V_{EN}$ | 0 | - | $V_{IN}$ | V |
| Output Current (*1) | Iout | 0 | - | 6.0 | A |
| SYNC Pin Voltage | $V_{SYNC}$ | OPEN or Connect to the SYNC pin of the parallel devices. | | | - |
| SYNCSEL Pin Voltage | $V_{SYNCSEL}$ | OPEN or GND | | | - |
| PG Pull-up Voltage | $V_{PG}$ | 3.0 | - | 5.5 | V |
| PG Pull-up Resistance Value | $R_{PG}$ | 4.7 | 10 | 47 | kΩ |
| Operating Ambient Temperature | Topr | -40 | - | 105 | ℃ |
| Input Capacitor (Effective Value) | $C_{IN}$ | 1.2 (*3) | - | 1000 (*4) | μF |
| Output Capacitance (Effective Value) | $C_L$ | 12 | | 400 | μF |
| Total Output Capacitance with Parallel Operation (Effective Value) | | 12 x n (*2) | | | |

All voltages are described based on the GND pin.

(*1) Please refer to the temperature derating curve (see characteristic example).

(*2) n: Number of parallel devices

(*3) Some ceramic capacitors have an effective capacitance that is significantly lower than the nominal value due to the applied DC bias and ambient temperature. For the input / output capacitance of this IC, use an appropriate ceramic capacitor according to the DC bias usage conditions (ambient temperature, input / output voltage) so that the effective capacitance value is equal to or higher than the recommended component.

## ■ELECTRICAL CHARACTERISTICS

Ta=25℃

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Input Voltage | $V_{IN}$ | | 20.0 | - | 60.0 | V |
| $V_{IN}$ Start-up Slew Rate(2) | $V_{IN\_SR}$ | | 0.2 | - | - | V/ms |
| UVLO Release Voltage | $V_{UVLOR}$ | $I_{OUT}$=0A | - | 18.1 | - | V |
| UVLO Detect Voltage | $V_{UVLOD}$ | $I_{OUT}$=0A | - | $V_{UVLOD}$ - 0.9 | - | V |
| Quiescent Current | $I_q$ | $V_{IN}$=48V, No load | - | 11 | - | mA |
| Shutdown Current | $I_{STB}$ | $V_{IN}$=48V, EN=0V | - | 0.15 | - | μA |
| EN “H” Voltage (1) | $V_{ENH}$ | | 2.6 | - | $V_{IN}$ | V |
| EN “L” Voltage (1) | $V_{ENL}$ | | GND | - | 0.6 | V |
| EN Input Rising Duration (1) | $t_{R\_EN}$ | 0V to $V_{ENH}$ | - | - | 1 | ms |
| EN “H” Current | $I_{ENH}$ | EN=$V_{IN}$=48V, Ta=125℃, No Load | - | 42 | - | μA |
| PG Output Pulldown “L” Level (1) | $V_{PGL}$ | $I_{PG}$=20mA | - | - | 0.25 | V |
| PG Detect Voltage | $V_{PGD}$ | $V_{OUT}$ rising, No fault | - | 0.95 x $V_{IN}$/4 | - | V |
| PG Released Voltage | $V_{PGR}$ | $V_{OUT}$ falling after PG=”H” | - | 0.8 x $V_{IN}$/4 | - | V |
| SYNCSEL “L” Voltage (1) | $V_{SYNCSELL}$ | | GND | - | 0.4 | V |
| Output Voltage | $V_{OUT}$ | $V_{IN}$=48V, Full load condition, DC | - | 0.96 x $V_{IN}$/4 | - | V |
| Output Current (Continuous) (3) | $I_{OUT}$ | Inside recommended OP range | - | - | 6.0 | A |
| Equivalent Output Resistance (3) | $R_{OUT}$ | $V_{IN}$=48V, $I_{OUT}$=6A | | 0.08 | | Ω |
| Efficiency Peak | $EFF_{\_PK}$ | $V_{IN}$=48V, $I_{OUT}$=2.4A | - | 96.5 | - | % |
| Efficiency Full Load | $EFF_{\_FULL}$ | $V_{IN}$=48V, $I_{OUT}$=6A | - | 95.0 | - | % |
| Switching Frequency | fosc | | - | 270 | - | kHz |
| Soft-start Input Current Limit (2) | $I_{IN\_SS}$ | | - | 134 | - | mA |
| Soft-start Timeout Duration (2) | $t_{TO\_SS}$ | | - | 100 | - | ms |
| Output Current (Start-up) (2) | $I_{OUT\_START}$ | | - | - | 20 | mA |
| Thermal Shutdown Temperature (1) | $T_{TSD}$ | Temperature rising | 125 | 150 | - | ℃ |
| Thermal Shutdown Hysteresis | $T_{HYS}$ | | - | 16 | - | ℃ |
| Current Limit | $I_{LIM}$ | | - | 10 | - | A |
| Short Circuit Protection | $I_{SHORT}$ | | - | 15 | - | A |

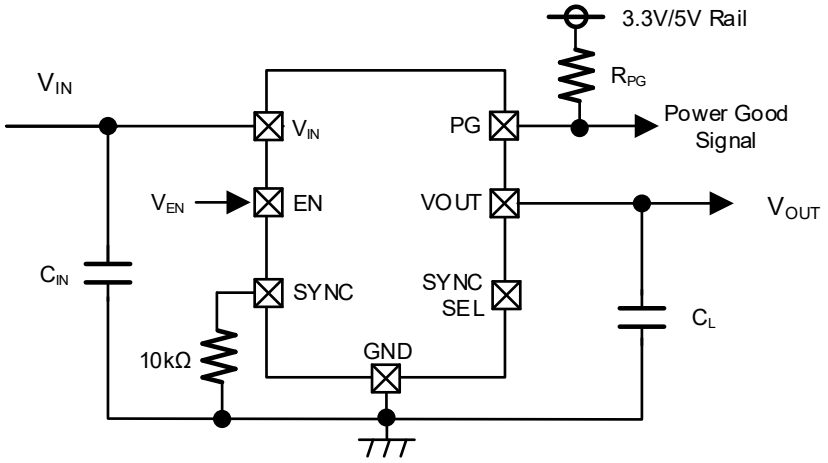
Measuring Conditions: Unless otherwise stated, $V_{IN}$=48V, $I_{OUT}$=6A

(1) Design value

(2) Depending on the output current, startup failure may occur due to soft-start timeout.
Equipment powered by the XM981A should be started after the PG signal goes to "H".

(3) $R_{OUT}$ = ($V_{IN}$ / 4 - $V_{OUT}$) / $I_{OUT}$

# ■TYPICAL APPLICATION CIRCUIT/ COMPONENT SELECTION EXAMPLES




【Typical Examples】

| | MANUFACTURER | PRODUCT NUMBER | VALUE | SIZE(L×W×T) |
|---|---|---|---|---|
| $C_{IN1}$ (*1) | | | - | |
| $C_{IN2}$ | Murata | GRM31CC72A475KE11 | 4.7μF | 3.2 x 1.6 x 1.6mm |
| $C_L$ | Murata | GRM31CC71E226ME15 | 22μF x 2 | 3.2 x 1.6 x 1.6mm |
| $R_{PG}$ | - | - | 10kΩ | - |

(*1) If there is a non-negligible parasitic impedance between the input line and module, $C_{IN1}$ may be required to reduce the impedance. A conductive polymer capacitor is typically used. It is not necessary to place it near the input pin of the converter.

(*2) Some ceramic capacitors have an effective capacitance that is significantly lower than the nominal value due to the applied DC bias and ambient temperature. For the input / output capacitance of this IC, use an appropriate ceramic capacitor according to the DC bias usage conditions (ambient temperature, input / output voltage) so that the effective capacitance value is equal to or higher than the recommended component.

**Input capacitor: $C_{IN2}$**

The input capacitor should be placed as close to the module as possible to reduce any parasitic inductance effects. The ripple voltage on Vin will affect the output voltage.

**Output capacitor: $C_L$**

The output capacitor is used to reduce the ripple on Vout. Increasing the output capacitance will reduce the ripple voltage on Vout, but it will increase the soft-start period, which may cause the XM981A to time out during soft-start, resulting in a startup failure.

**PG resistor**

Connect a pull-up resistor to the PG pin. Apply a pull-up voltage between 3.0V and 5.5V.

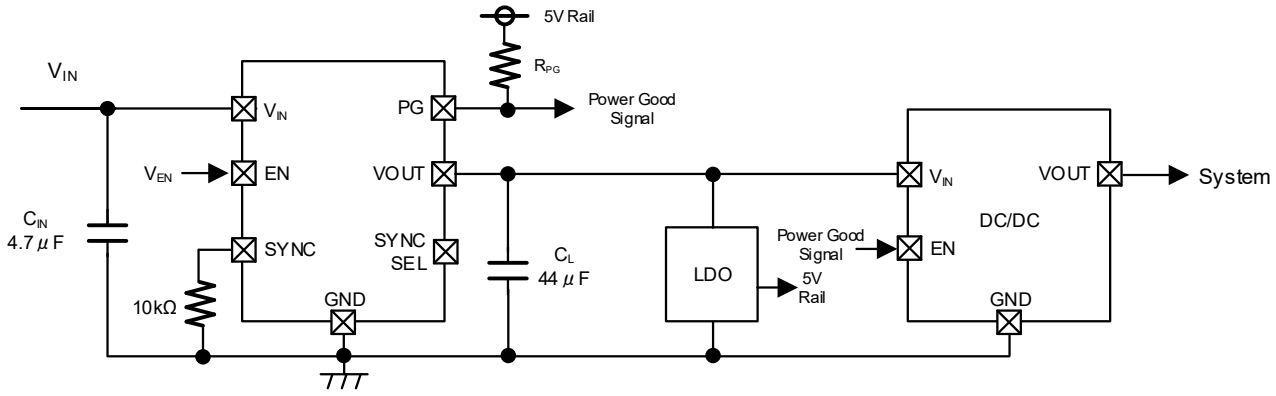
If you do not have an external 3.3V/5.0V power supply, use a voltage regulator to generate 3.3V or 5.0V from the output voltage of the XM981A and use that as a pull-up power supply.

The output voltage can also be divided by resistors to create a pull-up power supply.

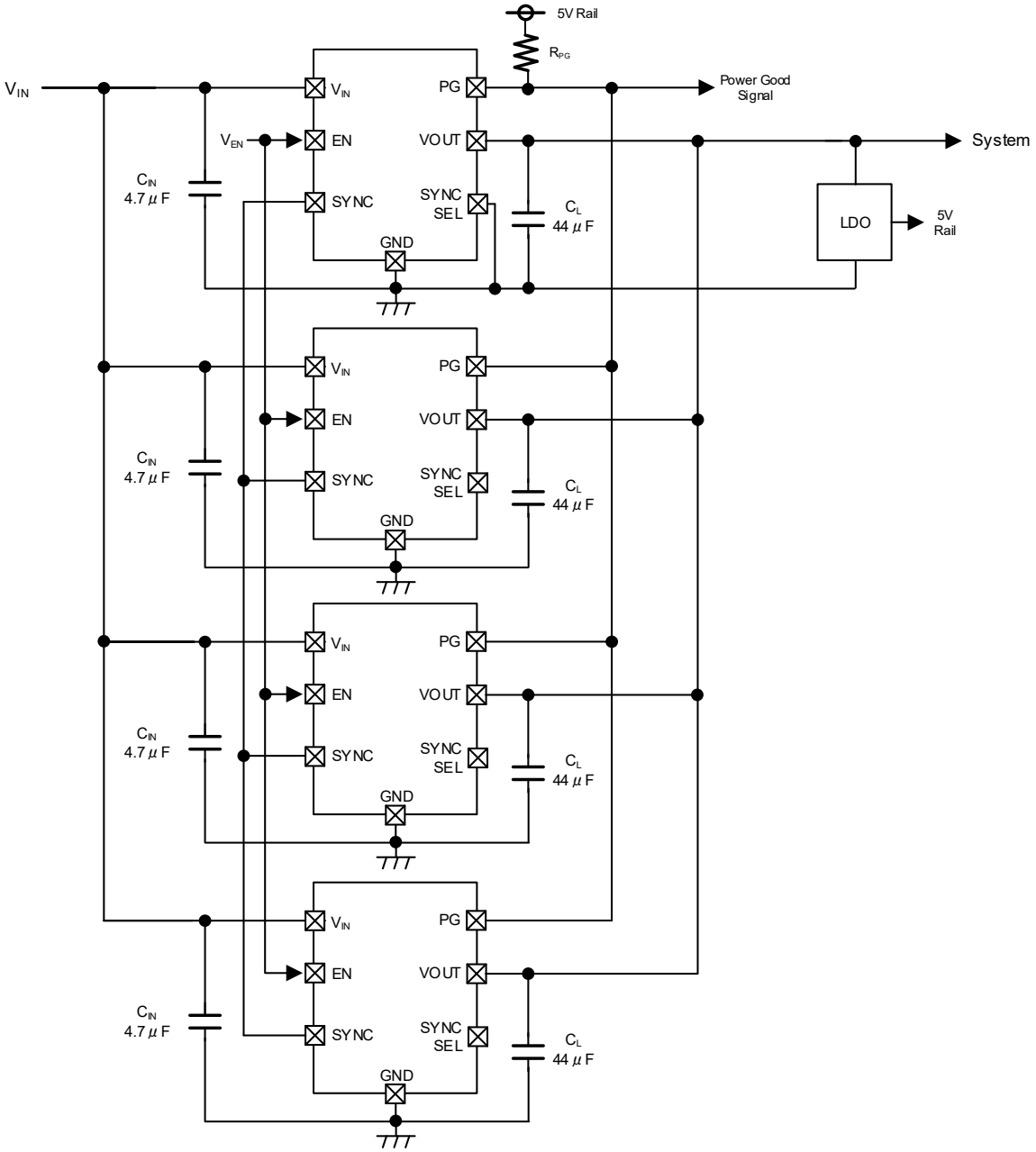
However, when using voltage division by resistors, the output voltage depends on the input voltage, so it is not possible to support all operating voltages from 20V to 60V input. Depending on the input voltage range to be used, the output voltage should be divided and used as the pull-up voltage.

## ■Application Circuit Examples

(a) When used alone




(b) During parallel operation

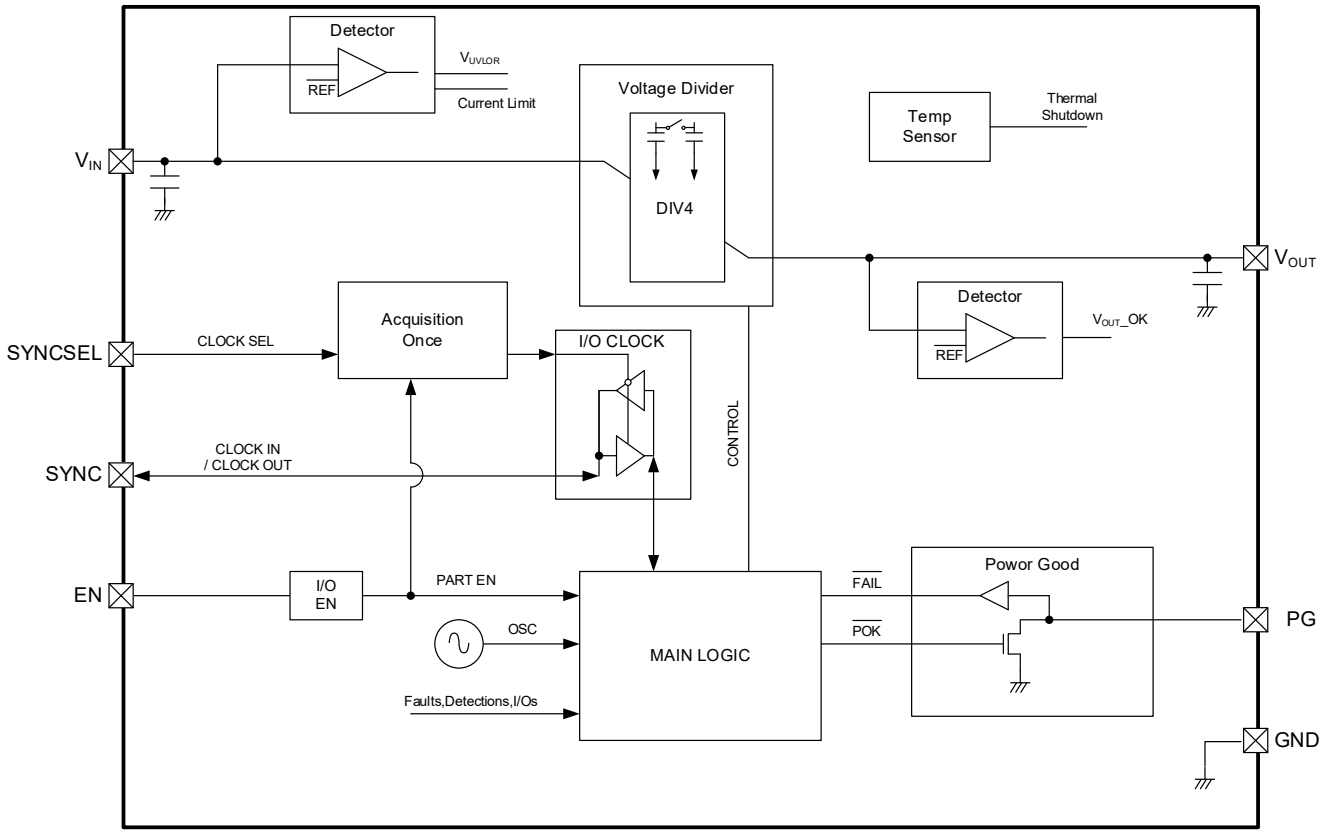


# ■OPERATIONAL EXPLANATION

XM981A is a divide-by-4, two-phase charge pump-based DC-DC converter. It outputs 1/4 of the input voltage, any change in input voltage will be reflected in the output. It does not have an output voltage regulation function.

Input voltage is 20V~60V, maximum output current is 6A.

The XM981A also supports parallel connection, allowing up to 4 parallel connections (6A x 4 parallel = 24A), making it ideal for intermediate buses that require high power and high efficiency.



## ■OPERATIONAL EXPLANATION

＜Normal operation/Full power mode＞

After startup mode is complete, the device transitions to full power mode. In full power mode, the output current can be supplied up to 6A.

When a protection function is activated, the device transitions to shutdown mode or startup mode.

＜EN Function＞

When a “L” voltage ($V_{ENL}$) is applied to the EN pin, the device enters a stand-by mode and current consumption is reduced to $I_{STB}$ (TYP. 0.15μA). In the stand-by mode, the internal circuit stops and no output voltage is output.

When a "H" voltage ($V_{ENH}$) is applied to the EN pin, the UVLO is released.
When the device enters the active state, it enters start-up mode and begins to increase the output voltage.

When operating multiple XM981As in parallel, connect all EN pins to a single enable signal.

| PIN NAME | SIGNAL | STATUS |
|---|---|---|
| EN | L | Stand-by |
| | H | Active |
| | OPEN | Undefined State |

＜UVLO＞

The UVLO function monitors the $V_{IN}$ pin voltage.

When the $V_{IN}$ pin voltage reaches or exceeds the UVLO release voltage $V_{UVLOD}$=18.1V(TYP.), XM981A enters the active state.

After shifting to the active state, if the $V_{IN}$ pin voltage falls or lower than the UVLO detection voltage $V_{UVLOR}$= $V_{UVLOD}$ - 0.9V(TYP.), the device shifts to the shutdown state.

# ■OPERATIONAL EXPLANATION

＜Start-up mode/Soft-start mode＞

Once UVLO is released and shifted to the active state, the output voltage rises through the following startup sequence.

(1) Shift to active state by UVLO release.

(2) Samples the SYNCSEL pin to determine whether the SYNC pin is CLOCK IN or CLOCK OUT.

(3) Pre-charge

Before enabling the soft-start switching sequence, the XM981A pre-charges the internal flying capacitors to make a balanced state based upon the divider ratio.

This is done so that when the soft-start mode begins, the flying capacitor voltage is at the set output voltage. Note that the adaptive pre-charge system takes pre-charging time depending on the output voltages.

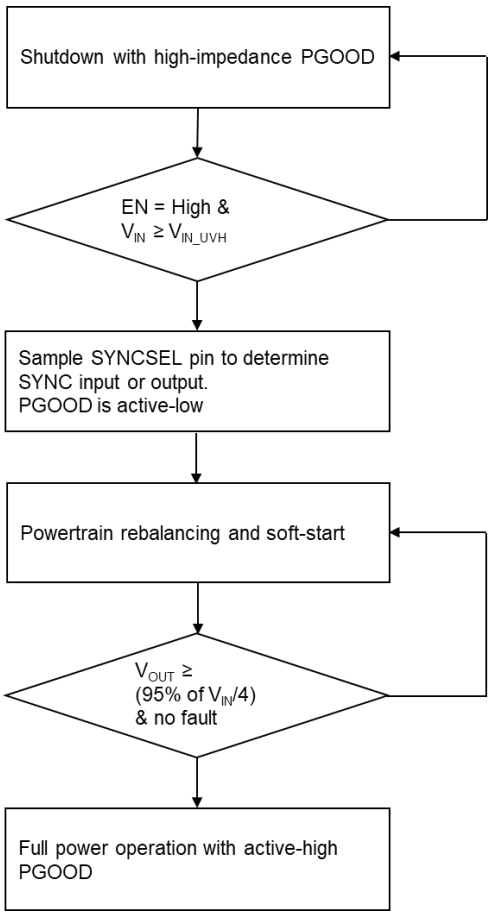
The output voltage may not rise monotonically during the pre-charge period.

(4) Soft-start mode

After the pre-charge is completed, the device enters soft-start mode and charges the output capacitor at 134mA typical value input current. When the output voltage reaches the PG detect voltage $V_{PGD}$=0.95 x ($V_{IN}$/4) (TYP.), the device exits soft start mode and shifts to full power mode.

When the soft-start mode is completed, the PG pin becomes "H (High impedance)".

If the load current is large or the output capacitance is large during soft-start mode, the output voltage may not rise to the PG detect voltage (0.95 x ($V_{IN}$/4)) during the soft-start timeout duration $t_{TO\_SS}$=100ms (TYP.) period. In that case, the soft-start timeout is detected and latched off. The EN pin must be toggled to restart from latch-off.




Start-up sequence

## ■OPERATIONAL EXPLANATION

＜Power Good＞

Functions for monitoring output status and module status.

The power good pin is a bi-directional open drain pin. The PG pin must be pulled up externally.

When the output voltage is above the PG detect voltage ($V_{PGD}$=0.95 x ($V_{IN}$/4) (TYP.)), the PG pull-down FET is turned off to allow the external pull-up resistor to pull up the PG voltage.

When the PG pin goes high, the full power mode is enabled, and the device is ready to support full load current.

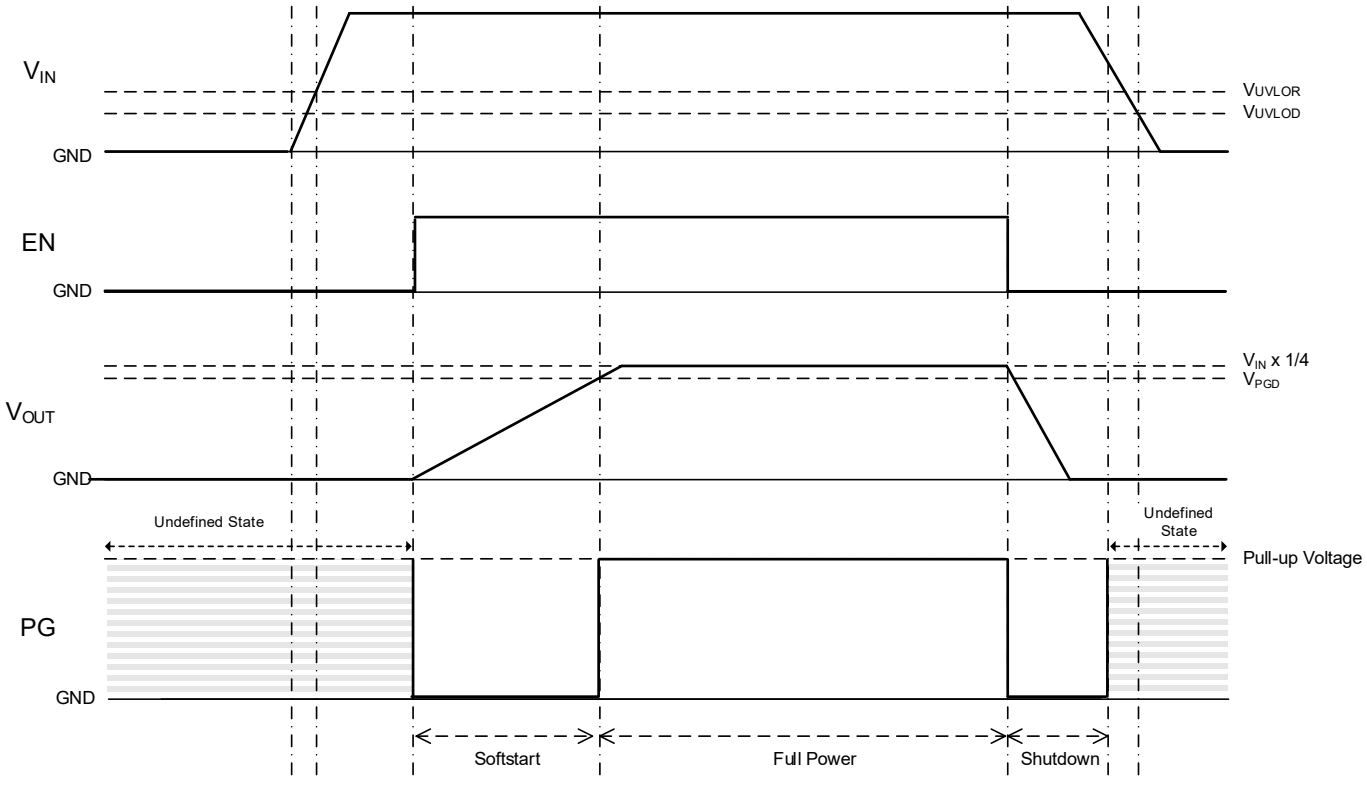
If another device or digital I/O is also pulling down on this pin, the XM981A remains in soft-start mode, and high-power mode is not enabled.

When multiple XM981As are used in parallel, all their PG pins must be connected. In this case, the XM981A will not start operating in full power mode until all XM981As have completed their boot preparation.

In the event of a fault at one or more parallel XM981As, the PG pin will be pulled low.

Note that the PG pin of a disabled device will not be pulled low if the device is not enabled. In effect, if EN="L", the PG pin should be ignored.

| $V_{IN}$ | EN | STATE | PG |
|---|---|---|---|
| $V_{IN} \leqq V_{UVLOD}$ | X | Undefined State | |
| $V_{IN} > V_{UVLOD}$ | "L" | Shutdown | "H" (High impedance) |
| | "H" | Normal operation | "H" (High impedance) |
| | | Start-up | "L" (Low Impedance) |
| | | From shutdown state to 60ms | "L" (Low Impedance) |
| | | Others | "L" (Low Impedance) |




PG Sequence Diagram

# ■OPERATIONAL EXPLANATION

＜SYNCSEL, SYNC Pin : External/Internal Clock Modes＞

SYNCSEL Pin

The SYNCSEL pin allows you to select whether the SYNC pin is used to output the internal clock signal or to input an external clock signal.

When using the XM981A alone, set SYNCSEL = “OPEN” to output the internal clock signal.

For parallel operation, SYNCSEL pin on one of the paralleled modules should be GND to provide the clock for the others, the other paralleled modules should be left floating to receive the shared clock to get all synced up.

The SYNCSEL pin is sampled before the charge pump is enabled and determines the configuration of the SYNC pin, which is not designed to be driven dynamically and should not be changed during power-on.

| Purpose | SYNCSEL | SYNC | DESCRIPTION |
|---|---|---|---|
| Single use | OPEN | 10kΩ Pull-Down Resistor to GND | Standalone use : Operates with internal clock when SYNCSEL=OPEN. |
| Clock input device in parallel operation | OPEN | CLOCK Input | Parallel operation : Operates synchronously with an external clock . |
| Clock output device in parallel operation | GND | CLOCK Output | Parallel operation : Outputs an internal clock. |

SYNC Pin

The charge pump is operated at a half frequency of the SYNC pin input/output clock.

Because XM981A internal components are optimized for efficiency with the internal oscillator frequency, injecting an external clock is not recommended for single-unit applications.

If configured to use an external clock (SYNCSEL=”OPEN”), and the external clock stops or is not present for some reason, an internal watchdog detects the missing clock and causes XM981A to swap back to use of the internal clock source. When the expected external clock source resumes, the XM981A reverts to using the external clock.

When the SYNCSEL pin is tied to GND, the internal clock is present on the SYNC pin.

Since the SYNC pin is high impedance and can be affected by external noise, in the event that an external clock out function is not being used in the application, it is recommended that the SYNCSEL pin is left to float, and the SYNC pin is tied to GND by a resistor.

## ■OPERATIONAL EXPLANATION

＜Protection Functions＞

To protect both systems and the internal circuit of XM981A, there are multiple fault detection circuits built in.

**PROTECTIONS**

| DETECTOR / CONDITION | LATCHED OFF /AUTOMATIC RETRY | OUTLINE |
|---|---|---|
| Thermal Shutdown | Automatic retry | PG goes low and the power stage switches off until the temperature reduces under the $T_{TSD}$. At this point, the device automatically restarts. |
| UVLO | Automatic retry | PG goes low and the device shuts down until $V_{IN}$ rises above $V_{UVLOR}$. When $V_{IN}$ rises, the device restarts. |
| Current Limit | Automatic retry | If the load current exceeds the over-current limit, PG goes low and the charge pump is disabled for a certain period to cool down. After the cooldown period, it automatically restarts. |
| Short Circuit Protection | Latched off | If the load current exceeds the short-current limit, the device is immediately latched off and shuts down. EN must be toggled to restart the device. |
| Soft-Start timeout | Latched off | If $V_{OUT}$ does not reach the target voltage during the soft-start timeout period, the device shuts down and EN must be toggled to restart it. |
| PG held “L” | Automatic retry | If the device is operating at full power and if PG is pulled down externally, the device enters soft-start mode and restarts. |
| $V_{OUT}$ under-voltage | Automatic retry | If the output voltage is under the $V_{PGR}$, the PG pin is pulled low. The device will shut down and enter a cooldown period. After the cool down period the device will restart. |

# ■OPERATIONAL EXPLANATION

＜Thermal Shutdown＞

The junction temperature is monitored to protect the module from thermal breakdown.

When the junction temperature reaches $T_{TSD}$ (TYP. 150℃), the thermal shutdown is activated, the shutdown sequence is entered, and PG becomes “L”. When the junction temperature falls to the thermal shutdown release temperature $T_{TSD}$-$T_{HYS}$ (TYP. 134℃) by stopping the current supply, the output voltage is turned on by the soft-start sequence.

＜UVLO＞

If the input voltage is insufficient, it is unlikely that the XM981A will be able to support the full load current, so input voltage is monitored to prevent it from operating in this condition.

The XM981A monitors the $V_{IN}$ pin voltage and enters the active state when the $V_{IN}$ pin voltage becomes equal or more than the UVLO release voltage $V_{UVLOR}$=18.1V(TYP.). After the active state, when the $V_{IN}$ pin voltage falls below the UVLO detector threshold $V_{UVLODR}$= $V_{UVLOR}$ - 0.9V(TYP.), the XM981A enters the shutdown state.

＜Current Limiting / Short Circuit Protection＞

The current limit function operates by detecting the current drawn from $V_{IN}$, and when the output current exceeds $I_{LIM}$ (TYP. 10A), the current limit function operates. Furthermore, when the output current exceeds $I_{SHORT}$ (TYP. 15A), the short circuit protection operates.

Current Protection

If the output current exceeds the over current protection threshold of 10A typical, then when triggered, the device will enter a cool-down period and after this automatically restart. During this time the PG pin is pulled low.

Short-circuit Protection

If the output current exceeds 15A typical, the device immediately shuts down and latches off.
During this time, the PG pin is pulled down. Then the XM981A is latched off until EN is toggled.
To restart the device, the EN pin must be toggled.

＜Output Under-voltage protection＞

Output under-voltage protection monitors the average value of output voltage. When the output voltage falls below $V_{OUT\_UVP}$ (TYP. 0.8 x $V_{IN}$/4), output under-voltage protection is activated and the XM981A enters a cool-down period. The XM981A will then automatically restart.

It is important that external components are chosen so that expected load transients do not drop below $V_{OUT\_UVP}$ (TYP. 0.8 x $V_{IN}$/4).

＜Soft-start･Timeout＞

To enter the soft-start mode and keep PG="L", if the output voltage does not rise to the PG detect voltage(0.95 x ($V_{IN}$/4)) within the soft-start timeout $t_{TO\_SS}$=100ms (TYP.) period, soft-start timeout is activated.

The soft-start timeout causes power to the load to be stopped and XM981A enters a controlled shutdown sequence. The device then latches off, and EN must be toggled to restart it.

＜PG Low Detection＞

Stand alone

When XM981A is ready for full power, PG goes high and stays high for as long as the single XM981A remains enabled and fault-free.

In parallel operation

In parallel operation, the PG signal must be connected in a wired OR configuration with the other PG pin.

When all devices are ready for full power, the PG signal goes high. In the event of a fault, the PG signal is pulled low and switches off all the parallel devices.

EN must be toggled to restart the devices.

＜In Parallel Operation＞

The output power can be increased by operating the XM981A in parallel in a multi-device configuration. Up to four devices can be operated in parallel. In parallel operation mode, the following points should be noted.

Current Balance / Thermal Balance

As with DC/DC converters using standard inductors, current and heat balance must be considered when using parallel charge pumps. In XM981A, the output voltage is not regulated because the input voltage is divided by the output voltage. Therefore, the output voltage drops based on the equivalent output resistance ($R_{OUT}$).

When an output current flows through the parallel charge pumps, the output voltage of each module starts to drop. The voltage drop from the set output voltage ($V_{IN}$ /4) is ($R_{OUT}$ + parasitic resistance) x $I_{OUT}$, and the output current of each module is determined by ($R_{OUT}$ + parasitic resistance) of each module.

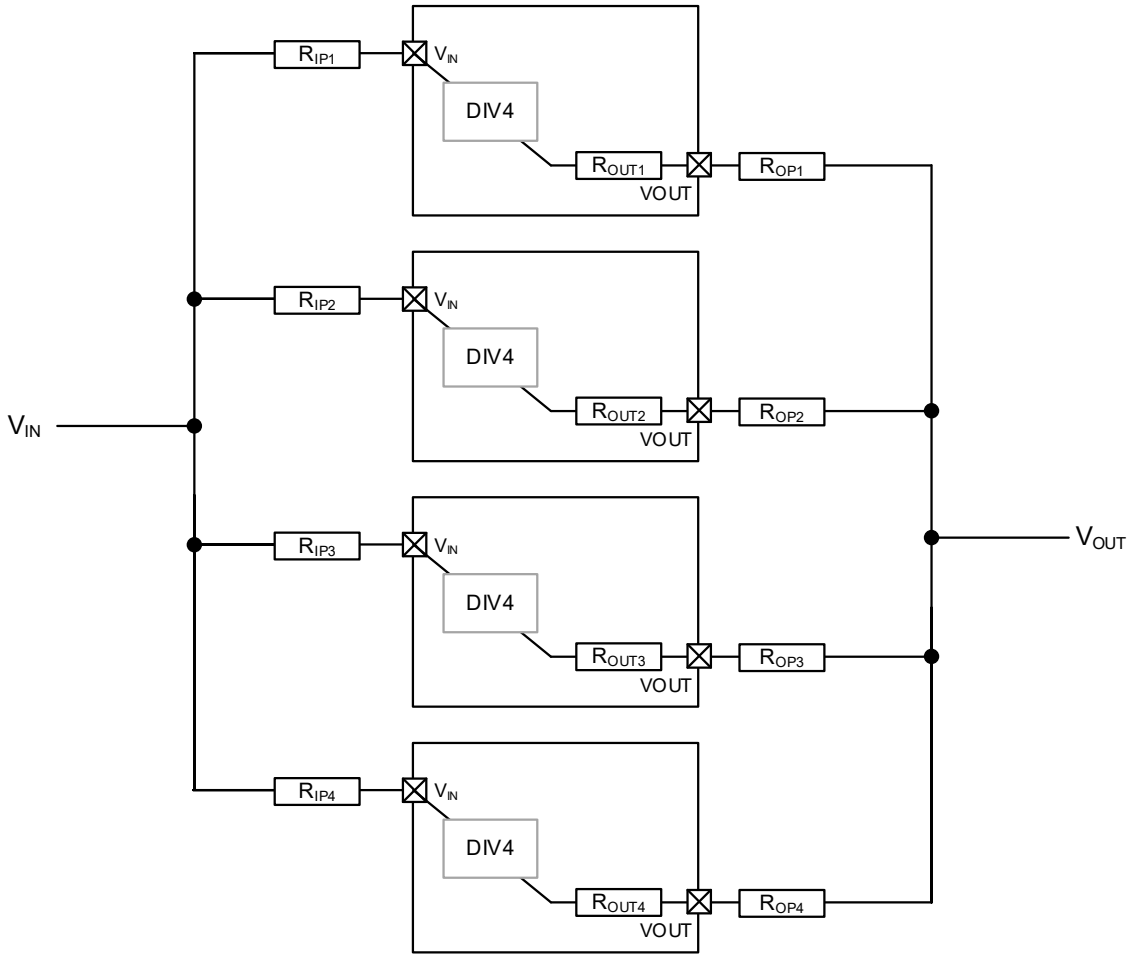
To properly distribute the load to each charge pump, care must be taken with the PCB layout to minimize parasitic resistance variations in the input and output lines.

The maximum output current for a single device in XM981A is 6A.

However, in parallel operation, the output current imbalance caused by parasitic impedances may cause one module to be current limited before another. This effect may limit the total power available in the system.

Power dissipation within the module results in an increase in junction temperature. This increase in junction temperature increases $R_{OUT}$, which helps maintain load sharing among the devices.

Therefore, each device must share the same thermal structure.



# ■OPERATIONAL EXPLANATION

Pin Connections for Parallel Operation

Pin connection limitation is slightly different from the single module operation.

(a) PG Pin

PG output must be pulled up together and combined in a wire OR configuration.

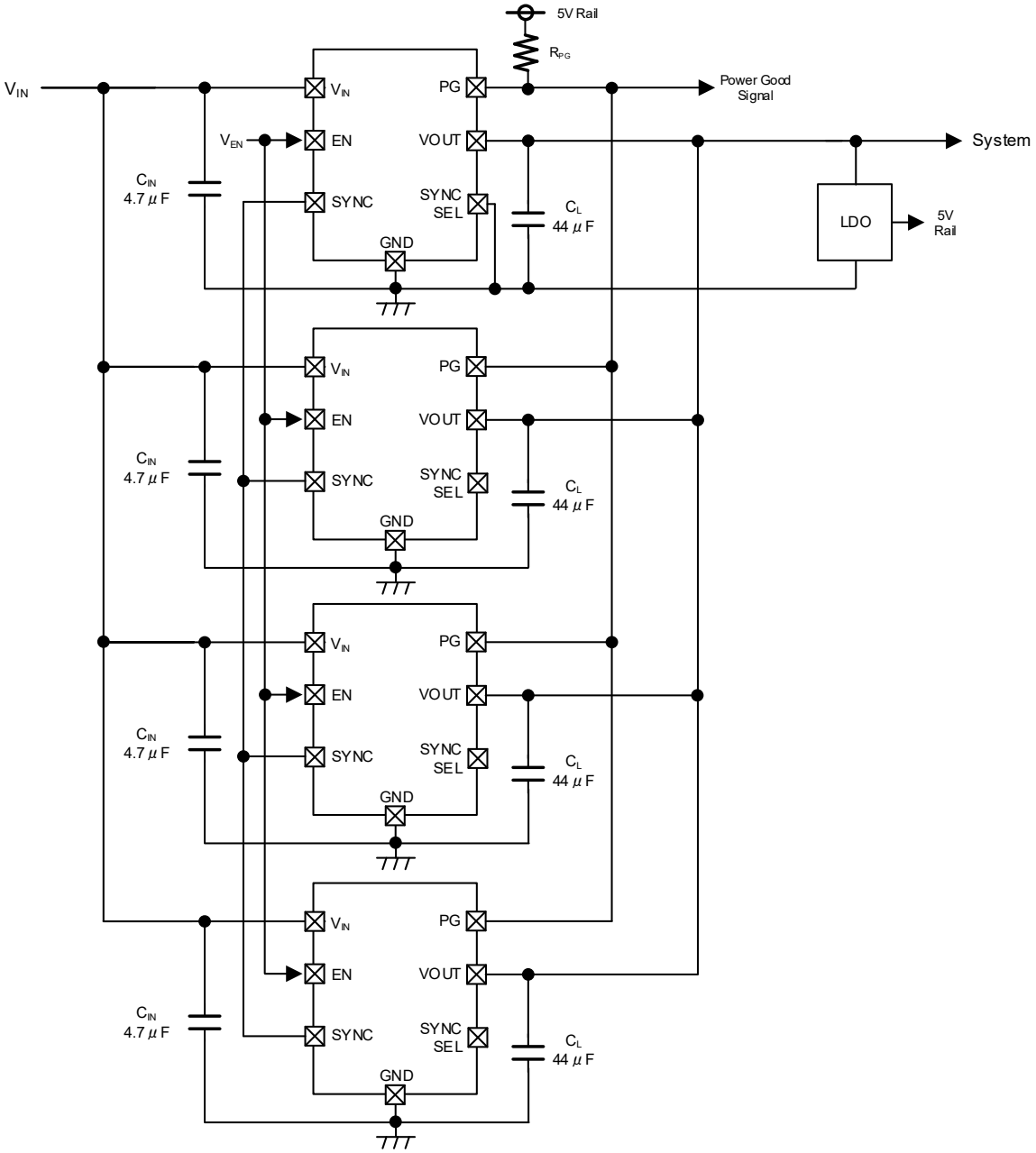
Do not operate load devices until PG of all modules goes “H”.

(b) SYNCSEL Pin

The SYNCSEL pin on one of the paralleled modules should be set SYNCSEL=GND to provide the clock for the others, the other paralleled modules should be set SYNCSEL=OPEN.

(c) SYNC Pin

Connect the SYNC pins of paralleled modules to the same node.



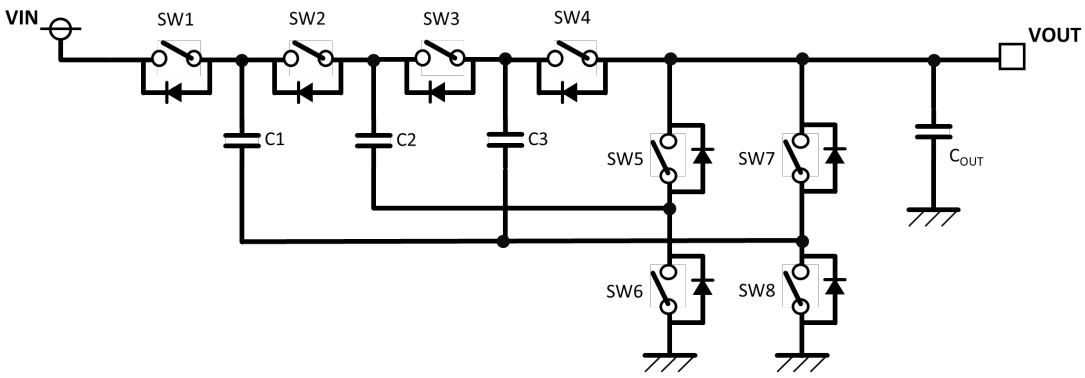
## ■OPERATIONAL EXPLANATION

**【Appendix】Charge Pump Operation**

Charge-pump based DC/DC converters are high-efficiency bus converters, but they do not have a regulation function. Due to its structure, it differs from conventional inductive buck converters in some respects.

Basis of Charge pump

A charge pump is a capacitive voltage converter that consists of multiple switches and capacitors.




Charge pump configuration

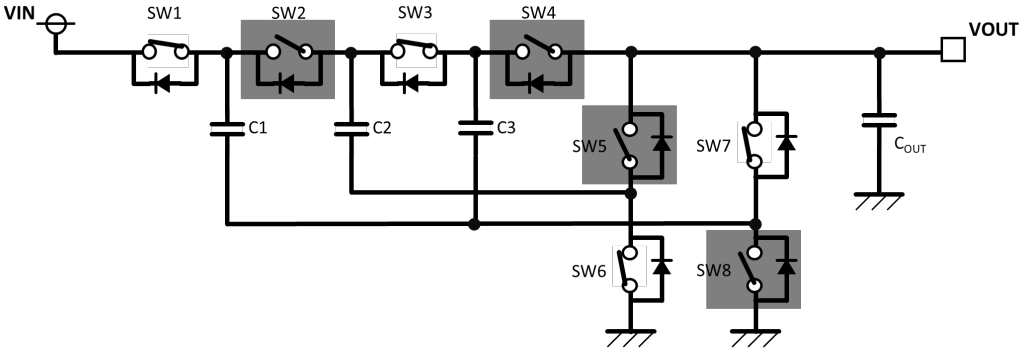
# ■OPERATIONAL EXPLANATION

**【Appendix】Charge Pump Operation (Continued)**

Charge pumps usually have two main switch states (phase 1, phase 2).
The connection of the flying capacitor in each state is shown below.

**Phase 1**

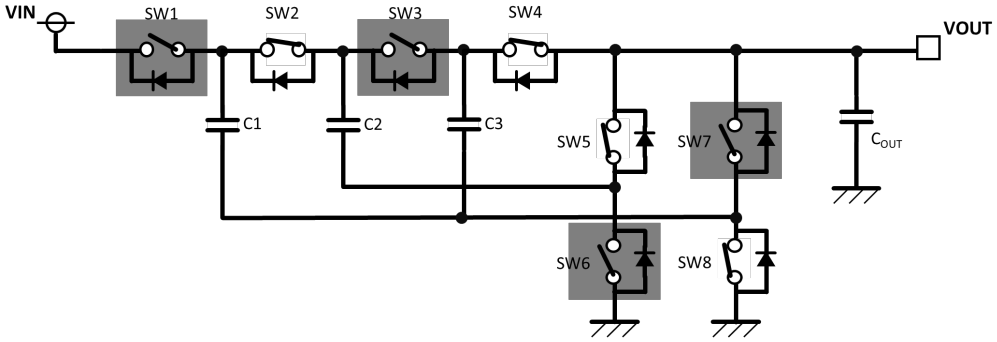
C1 : Connect between $V_{IN}$ and $V_{OUT}$.
C2 and C3 : Connect between $V_{OUT}$ and GND.




Charge Pump Main Switch Configuration: Phase 1

**Phase 2**

C1 and C2 : Connect between $V_{OUT}$ and GND.
C3 : Connect between $V_{OUT}$ and GND.

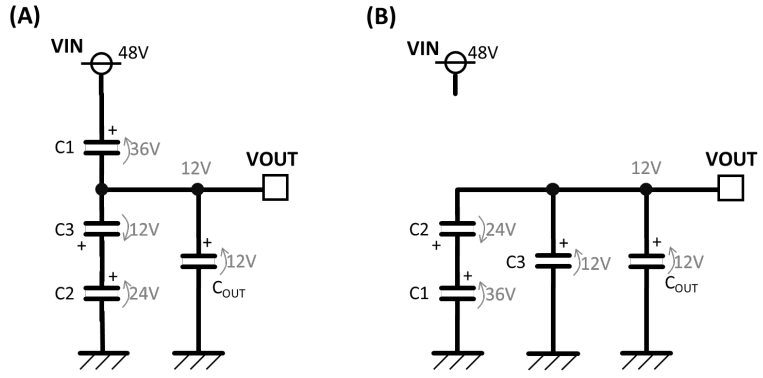



Charge Pump Main Switch Configuration: Phase 2

The following figure shows these two states of capacitor connection and charged voltage relationship. Once the charge pump finishes soft-start, each capacitor will have VIN/4, VIN*2/4 and VIN*3/4 voltage. This voltage will be maintained to keep switching between phase 1 and phase 2.

To improve the charge pump efficiency, increase of the flying capacitor capacitance works well. Also, minimize switch resistance and parasitic resistance works, too.

The XM981A is optimized in the module for flying capacitors, power switch resistors, and wiring parasitic resistors. Therefore, users wouldn't need to care about such a detail.




Flying capacitor connection

## ■NOTE ON USE

1) For the phenomenon of temporal and transitional voltage decrease or voltage increase, the Module may be damaged or deteriorated if Module is used beyond the absolute MAX. specifications. Also, if used under out of the recommended operating range, the IC may not operate normally or may cause deterioration.

2) Spike noise and ripple voltage arise in a switching regulator as with a DC/DC converter. These are greatly influenced by external component selection, such as the capacitance values, and board layout of external components. Once the design has been completed, verification with actual components should be done.

3) The DC/DC converter characteristics depend greatly on the externally connected components as well as on the characteristics of this Module, so refer to the specifications and standard circuit examples of each component when carefully considering which components to select. Especially for capacitor, it is recommended to use an appropriate ceramic capacitor according to the DC bias characteristics, ambient temperature characteristics, so that the effective capacitance value is equal to or higher than the recommended component under actual operating conditions.

4) The SYNC pin is high-impedance and may be affected by external noise.
Therefore, if the external clock output function is not used, leave the SYNCSEL pin to OPEN and connect the SYNC pin to GND through a resistor.

5) The current limit function of the XM981A operates by detecting the current flowing from $V_{IN}$. If the input voltage suddenly rises, a voltage difference occurs between the input voltage and the flying capacitor, causing an excessive inrush current. This excessive current may activate the current limit function, so please do not suddenly increase the input voltage when the XM981A is in full power mode.

6) The XM981A is a capacitive DC/DC converter with low inductance at the output for optimal efficiency. Due to the low output inductance, a hard short at the output can result in a much higher di/dt condition than a conventional inductive buck converter. Although the XM981A has output current protection, a very low impedance output short circuit can permanently damage the device. If such failures are a concern, consider adding primary protection external to the device to ensure adequate protection.

7) The parasitic diodes in the XM981A internal power switch are designed based on power flow from input to output. Therefore, reverse current flow from the output to the input side must be avoided.
When $V_{OUT}$ is greater than $V_{IN}$ /4, a reverse current may occur from the output to the input, so the condition "$V_{OUT} \leqq V_{IN}$ /4" must be satisfied. The IC should not start up when the condition " $V_{IN}$ /4 < $V_{OUT}$ " exists.
A condition for reverse current to occur is a sudden drop in the input voltage while the XM981A is active. This sudden drop in input voltage may lead to an unexpected shutdown. In full power mode, the input voltage should not drop at a rate of more than 8V/ms.
In addition, if the input voltage is reduced while EN = "L", and then the lower input voltage makes EN = "H" again, a reverse current may occur from the output capacitor to the input side.

8) Current-limited soft-start mode consumes more power than normal operation. Therefore, care must be taken to avoid temperature rise during soft-start.

9) Torex places an importance on improving our products and their reliability. We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems.

# ■NOTE ON USE (Continued)

10) Instructions of pattern layouts

Especially noted in the pattern layout are as follows.

Please refer to the reference pattern layout on the next page.

(a) Wire the large current line using thick, short connecting traces.

This makes it possible to reduce the wire impedance, which is expected to reduce noise and improve heat dissipation.

If the wire impedance of the large current line is large, it may cause noise or the IC to not operate normally.

(b) Place the input capacitance $C_{IN}$, output capacitance $C_L$ and IC which the large current flows on the same surface.

If they are placed on both sides, a large current will flow through Via, which has high impedance, it may cause noise and the IC may not operate normally.

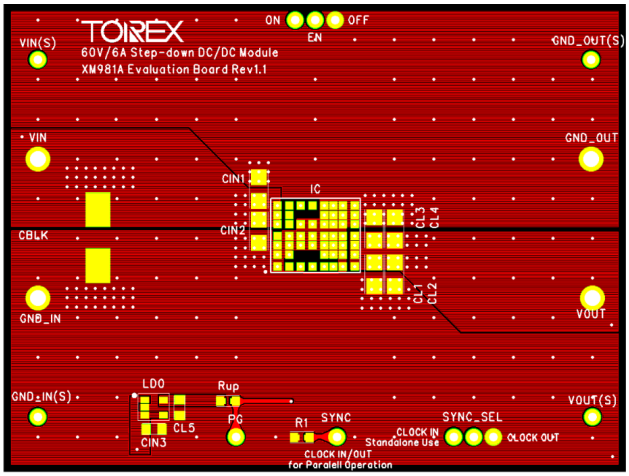
(c) Please mount each external component as close to the IC as possible.

Especially place the input capacitance $C_{IN}$ near the IC and connect it with as low impedance as possible.

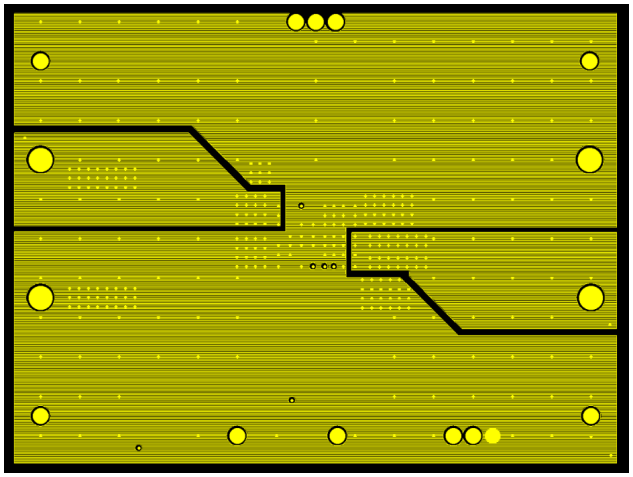
If the input capacity $C_{IN}$ and IC are too far apart, it may cause noise, or the IC may not operate normally.

＜Reference pattern layout＞

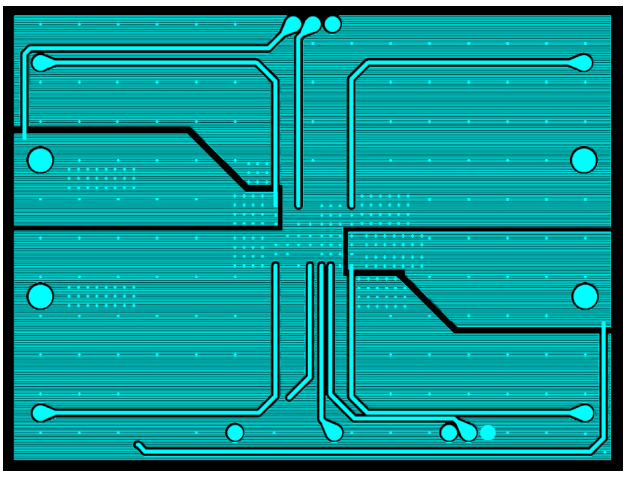
Layer 1



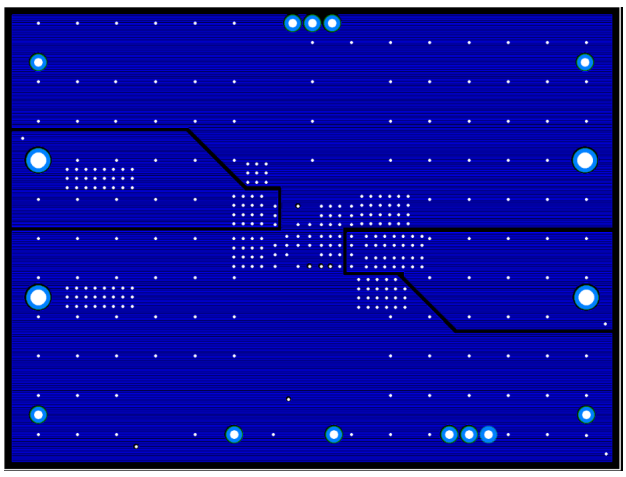

Layer 2



Layer 3



Layer 4



## ■Notes on handling of product

(1) Please solder the product with Rosin Flux, which contains chlorine 0.2wt% or less.
Please do NOT use acid flux or water-soluble flux, which could corrode metals and glass of the product.

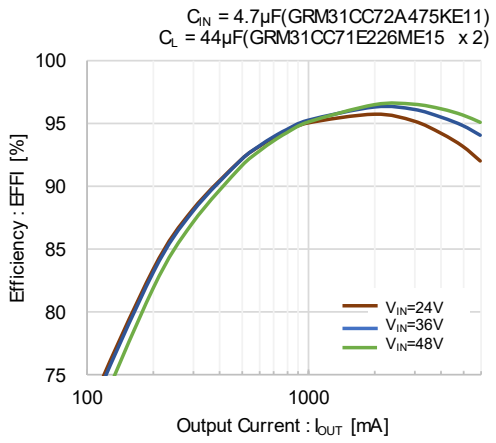
(2) Do not use this product in any of the following environments:
- Areas with dust accumulation;
- Locations exposed directly to sea breeze;
- Atmospheres containing corrosive gases such as $Cl_2$, $NH_3$, $SO_2$, or $NO_x$

(3) Please do not clean or wash the products.

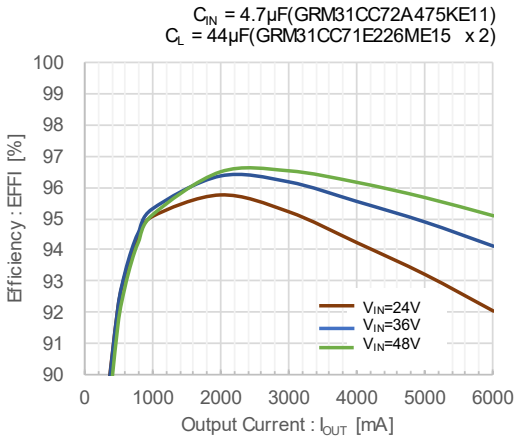
# ■TYPICAL PERFORMANCE CHARACTERISTICS

(1) Efficiency vs. Output Current

Log scale

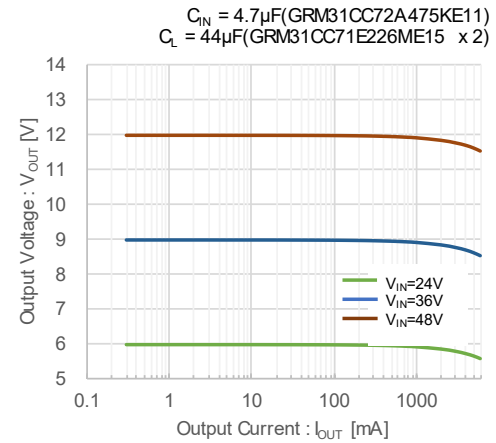



Linear scale

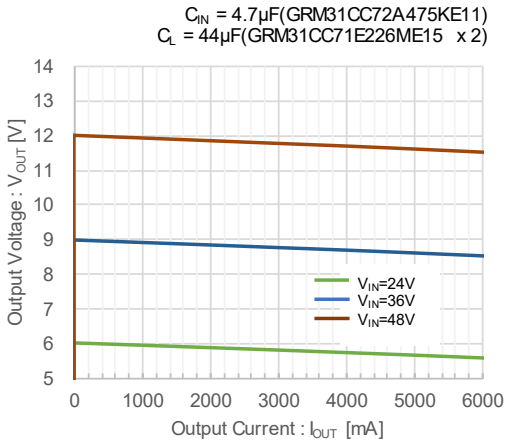



(2) Output Voltage vs. Output Current

Log scale

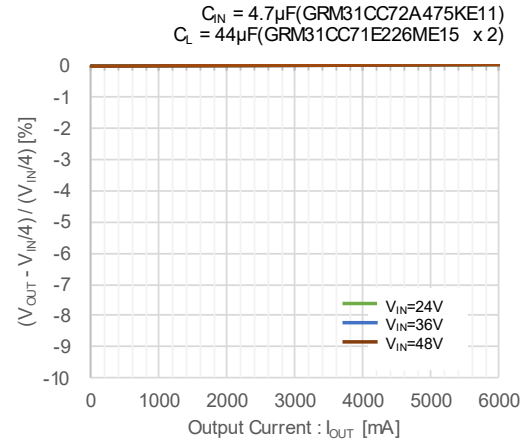



Linear scale



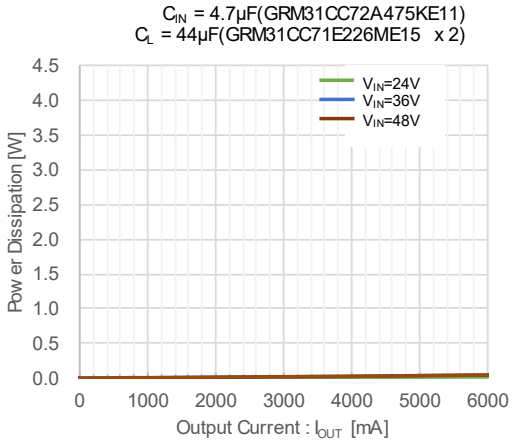

(3) Output Voltage Drop Ratio vs. Output Current

Linear scale




(4) Power Dissipation vs. Output Current

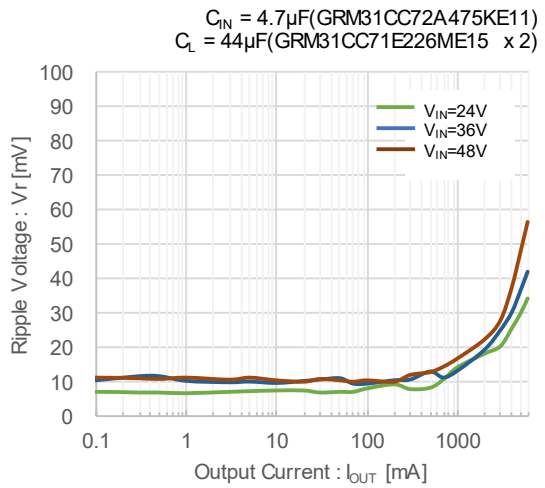
Linear scale



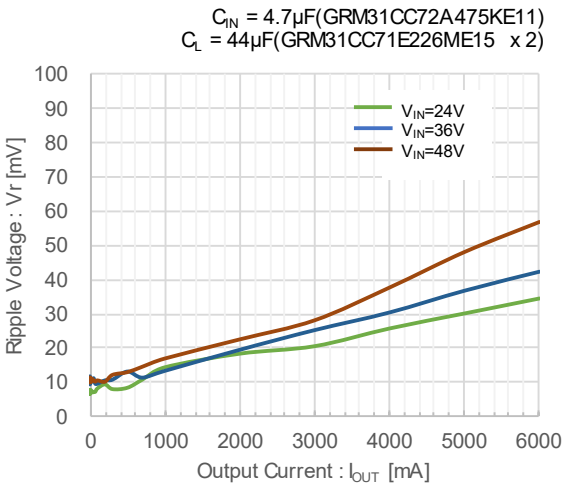
# ■TYPICAL PERFORMANCE CHARACTERISTICS

(5) Ripple Voltage vs. Output Current

Log scale

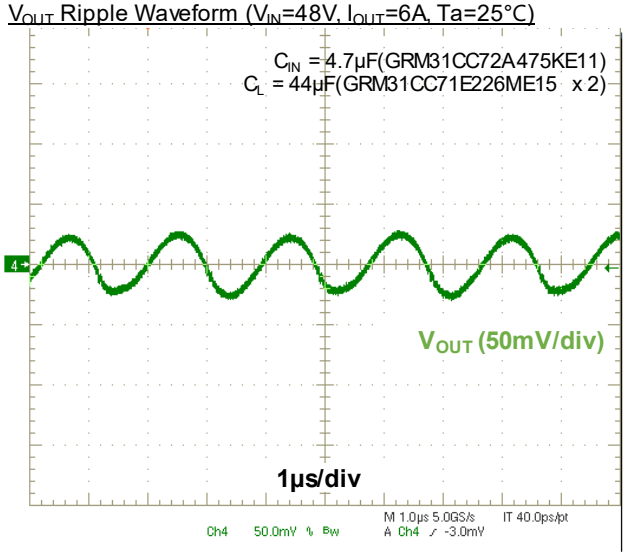



Linear scale

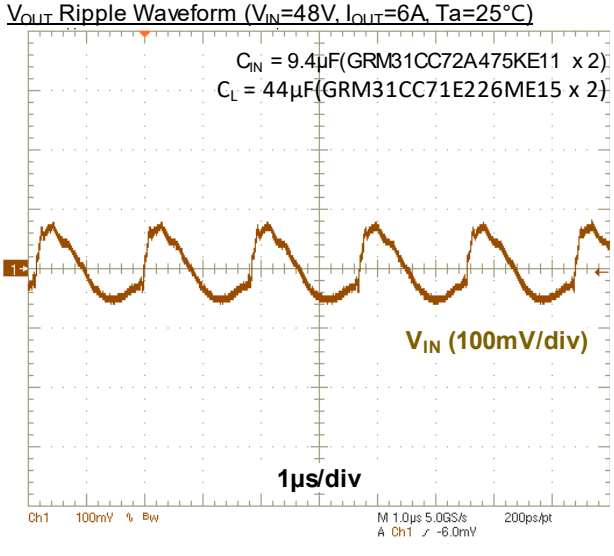



(6) Ripple Waveform

$V_{OUT}$ Ripple Waveform ($V_{IN}$=48V, $I_{OUT}$=6A, Ta=25°C)



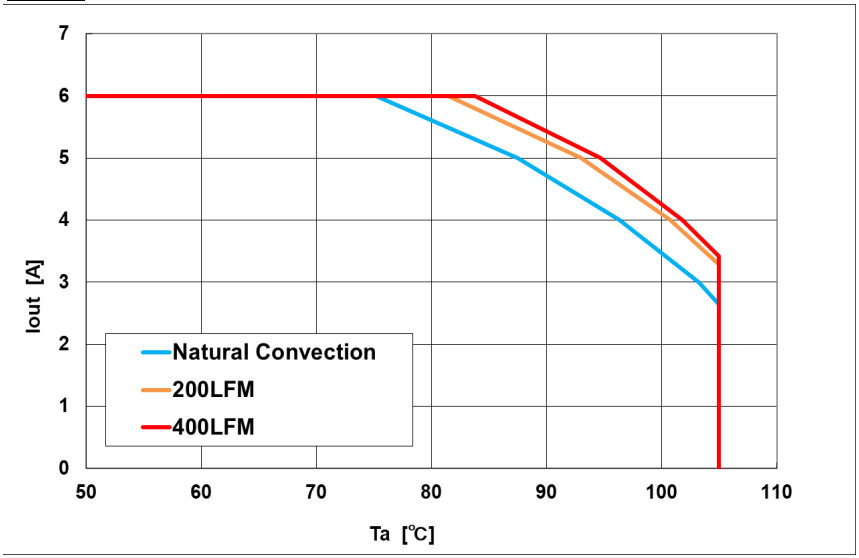

$V_{OUT}$ Ripple Waveform ($V_{IN}$=48V, $I_{OUT}$=6A, Ta=25°C)



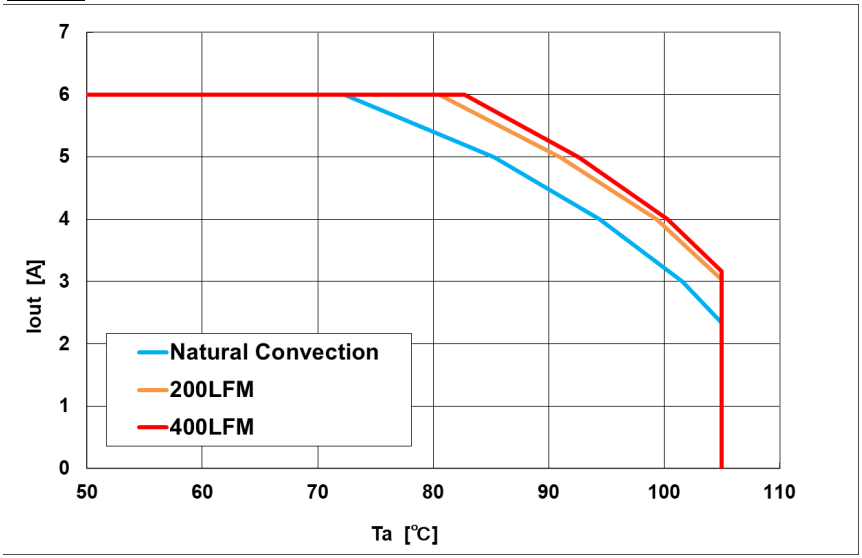
# ■TYPICAL PERFORMANCE CHARACTERISTICS

(7) Thermal Deratings

$V_{IN}$=48V




$V_{IN}$=54V



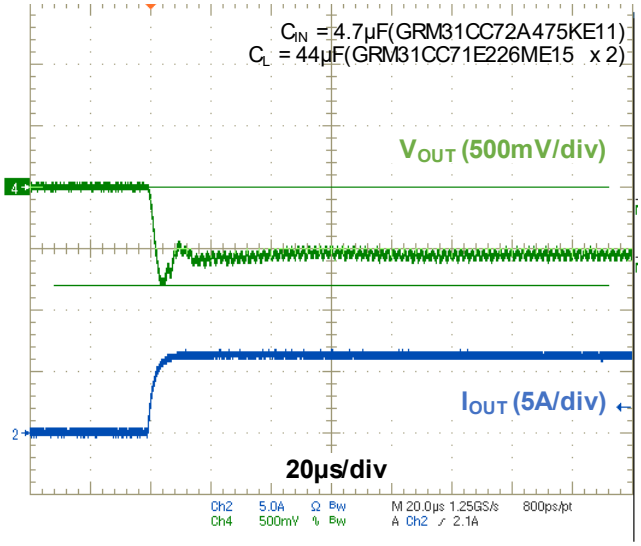

Condition

| | |
|---|---|
| Board Dimensions | : 114.5 x 101.5mm |
| Thickness | : 1.6mm |
| Material | : Glass Epoxy (FR-4) |
| Copper foil | : Layer1, 4: 70μm / Layer2, 3: 35μm |
| Surface temperature of the product | : 116°C (Max.) |

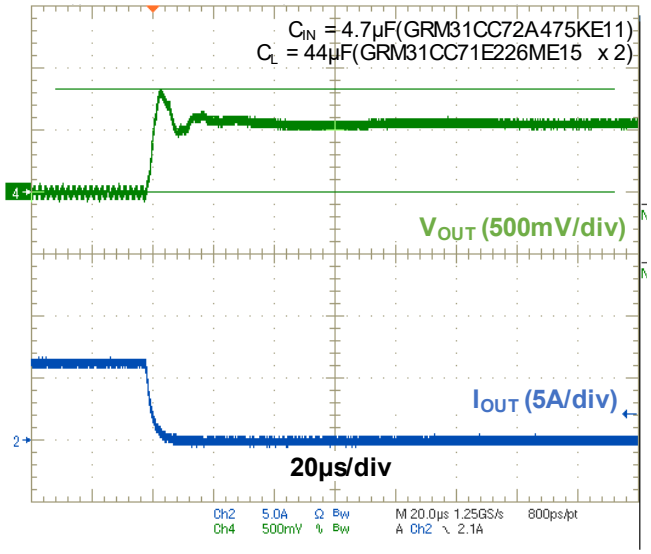
## ■TYPICAL PERFORMANCE CHARACTERISTICS

(8) Load Transient Response

Iout = 0A to 6A, Slew Rate=1A/μs, $V_{IN}$=48V, Ta=25°C

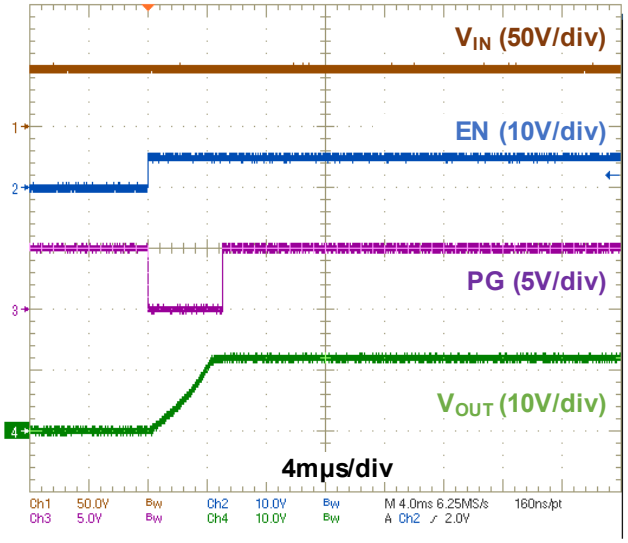



Iout = 6A to 0A, Slew Rate=1A/μs, $V_{IN}$=48V, Ta=25°C




(9) Start-up Waveform (EN Rising)

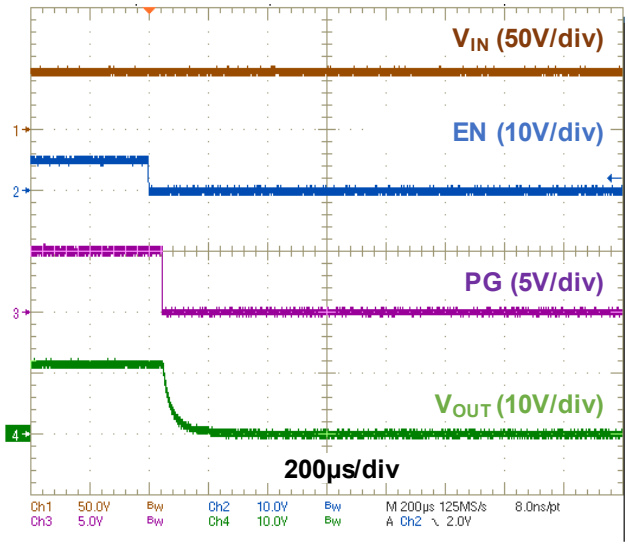
$V_{IN}$=48V, $I_{OUT}$=0A, Ta=25°C




CIN = 4.7μF(GRM31CC72A475KE11)
CL = 44μF(GRM31CC71E226ME15 x 2)

(10) Shutdown Waveform (EN Falling)

$V_{IN}$=48V, $I_{OUT}$=6A, Ta=25°C




CIN = 4.7μF(GRM31CC72A475KE11)
CL = 44μF(GRM31CC71E226ME15 x 2)

# ■PACKAGING INFORMATION

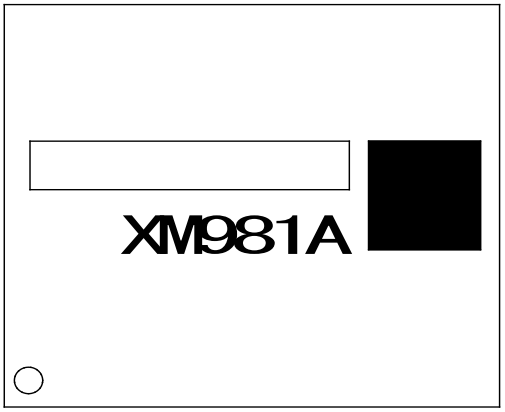
For the latest package information, please visit www.torex.co.jp/technical-support/packages/

| PACKAGE | OUTLINE / LAND PATTERN | THERMAL CHARACTERISTICS |
|---|---|---|
| LGA-52C01 | LGA-52C01 PKG | - |

## ■MARKING RULE

| CODES | DESCRIPTION |
|---|---|
| ○ | 1pin marking |
| XM981A | Product code |
| ▭ | Internal manufacturing code |
| ■ | QR code |

LGA-52C01



1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.

2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.

3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.

4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions. Do not use the product for the above use unless agreed by us in writing in advance.

5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.

6. Our products are not designed to be Radiation-resistant.

7. Please use the product listed in this datasheet within the specified ranges.

8. We assume no responsibility for damage or loss due to abnormal use.

9. 

TOREX SEMICONDUCTOR LTD.