XC9714 Series

ETR05096-000e

36V 2A Synchronous Step-Down DC/DC Converters

Preliminary

■GENERAL DESCRIPTION

The XC9714 series is 36V bootstrap synchronous step-down DC/DC converter with built-in Nch-Nch driver FETs.

The XC9714 series has operating voltage range of 4.5V~36V, the output voltage can be set from 2.5V to 18.0V. It can support 2.0A as an output current with high-efficiency and stable voltage.

The switching frequency is 800kHz, and the operation mode can be selected between PWM control and PWM/PFM control with the MODE pin. When PWM control is operated, the frequency is constant regardless of the load, so noise countermeasures are easy. PWM/PFM control can achieve high efficiency from light loads to heavy loads.

The same part number can be used for multiple power supply lines because the set value of the output voltage can be changed using an external resistor.

It is possible to externally adjust the soft-start time longer than the internal soft-start using an external resistor and capacitor connected to EN/SS pin.

In addition, the power good function monitors the state of the output voltage. The soft start external adjustment function and power good function make it easy to configure the power supply sequence.

Built-in protection functions include current limit, over voltage protection, thermal shutdown and Lx short protection for safety operation.

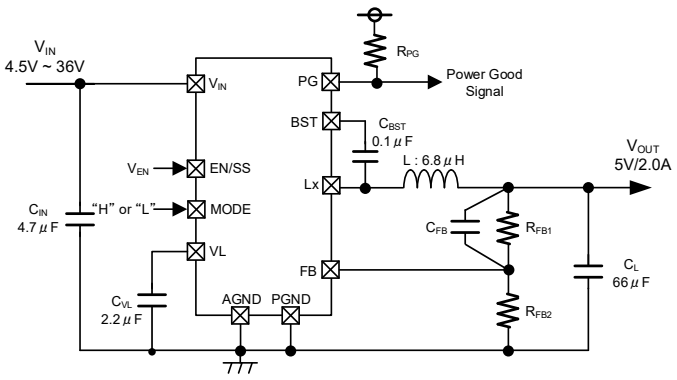
■APPLICATIONS

- 12V Battery Systems
- Industrial Automation
- Industrial Sensors
- Security Systems
- Home Appliances / Power Tools
- High-Voltage LDO Replacement
- General-Purpose Power-circuit / Point-of-load

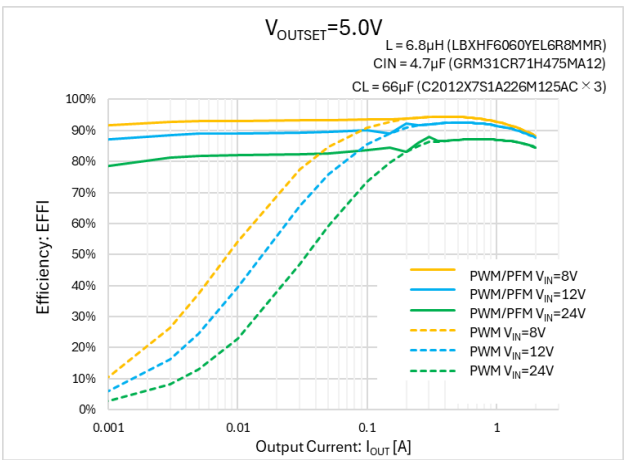
■FEATURES

Input Voltage Range	:	4.5V ~ 36.0V (Absolute Max 40.0V)
Output Voltage Range	:	2.5V ~ 18.0V
FB Voltage	:	0.75V±1.5%
Maximum Output Current	:	2.0A
Oscillation Frequency	:	800kHz
Control Methods	:	PWM control (MODE="H") PWM/PFM control (MODE="L")
Protection Functions	:	Current Limit (Foldback) Output Over Voltage Protection Thermal Shutdown Lx short protection
Functions	:	Power Good, UVLO Soft-start (external adjustment)
Output Capacitor	:	Ceramic Capacitor
Operating ambient temperature	:	-40 ~ 125℃/ Tjmax=150℃
Packages	:	DFN3030-12A(3.0x3.0x 0.75mm) HSOP-8N (6.2 x 5.2 x 1.7mm)
Environmentally Friendly	:	EU RoHS Compliant, Pb Free

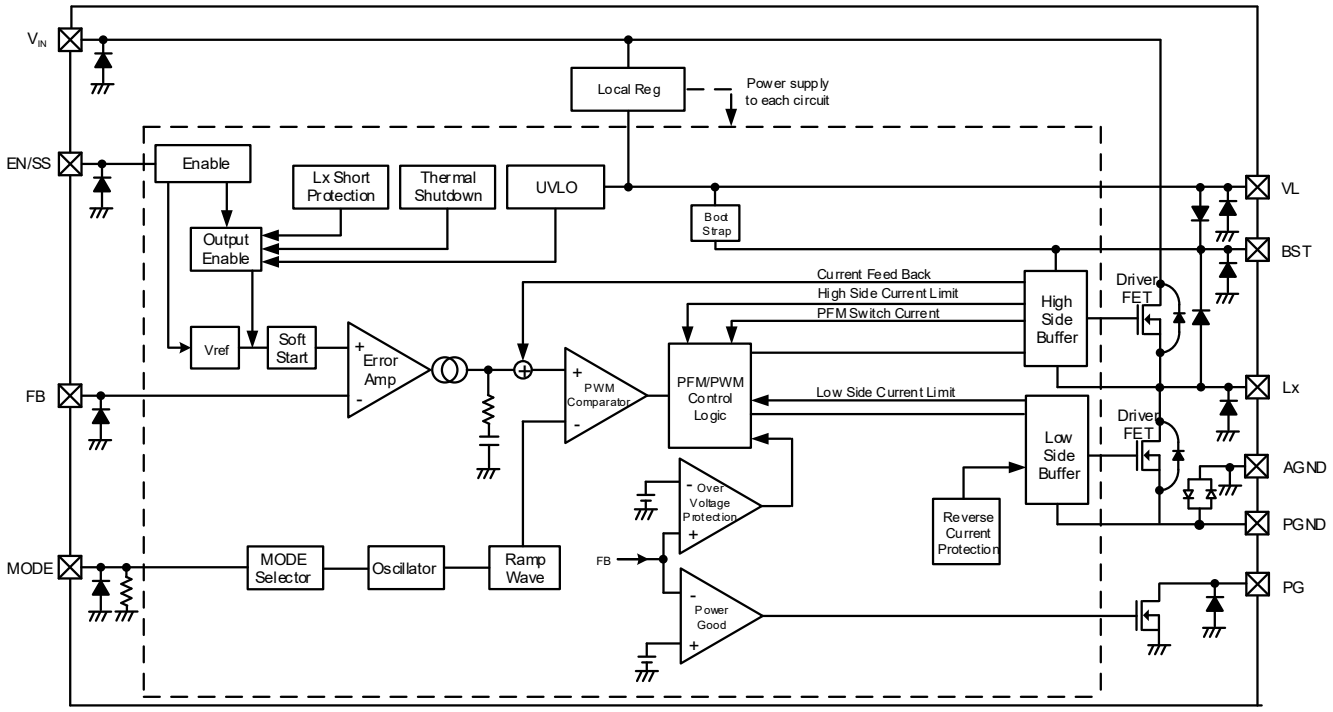
■TYPICAL APPLICATION CIRCUIT



■TYPICAL PERFORMANCE CHARACTERISTICS



■BLOCK DIAGRAM



* Diodes inside the circuit are ESD protection diodes and parasitic diode.

■PRODUCT CLASSIFICATION

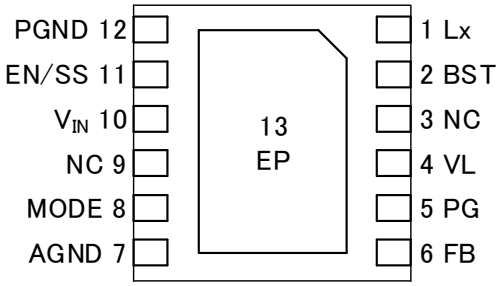
●Ordering Information

XC9714①②③④⑤⑥-⑦(*1)

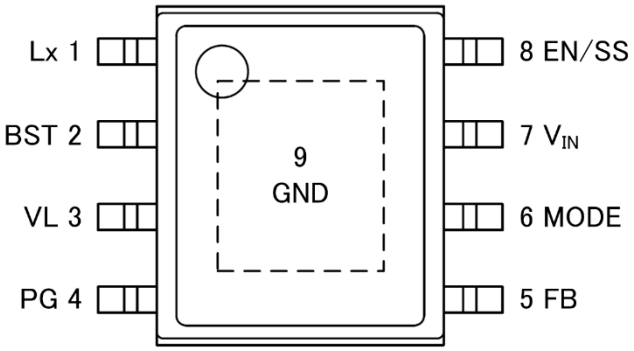
DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	A	-
②③	FB Voltage	75	0.75V
④	Oscillation Frequency	8	800kHz
⑤⑥-⑦(*1)	Packages (Order Unit)	6R-G	DFN3030-12A (3,000pcs/Reel)
		RR-G	HSOP-8N (1,000pcs/Reel)

(*1) The "-G" suffix indicates that the products are Halogen and Antimony free as well as being fully EU RoHS compliant.

■PIN CONFIGURATION



DFN3030-12A (BOTTOM View)



HSOP-8N (TOP View)

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTIONS
DFN3030-12A	HSOP-8N		
1	1	Lx	Switching
2	2	BST	Boot Strap
4	3	VL	Local Regulator
5	4	PG	Power Good Output
6	5	FB	Output Voltage Sense
7	-	AGND	Analog Ground
8	6	MODE	Operation Mode Select
10	7	V_{IN}	Power Input
11	8	EN/SS	Enable / Soft-Start
12	-	PGND	Power Ground
-	9	GND	Ground
3,9	-	NC	No Connection
13	-	EP	Exposed thermal pad. The Exposed pad must be connected to GND (Pin7,12)

■FUNCTION CHART

PIN NAME	SIGNAL	STATUS
EN/SS	H	Active
	L	Stand-by
	OPEN	Stand-by
MODE	H	PWM
	L	PWM/PFM Auto
	OPEN	PWM/PFM Auto

PIN NAME	CONDITION		SIGNAL
PG	EN/SS = H	$V_{FB} > V_{PGDET}$	H (High impedance)
		$V_{FB} \leqq V_{PGDET}$	L (Low impedance)
		Over Voltage Protection	H (High impedance)
		Thermal Shutdown	L (Low impedance)
		UVLO ($V_{IN} < V_{UVLOD}$)	Undefined State
	EN/SS = L	Stand-by	L (Low impedance)

■ABSOLUTE MAXIMUM RATINGS

Ta=25℃

PARAMETER		SYMBOL	RATINGS	UNITS
V_{IN} Pin Voltage		V_{IN}	-0.3 ~ 40.0	V
EN/SS Pin Voltage		$V_{EN/SS}$	-0.3 ~ 40.0	V
FB Pin Voltage		V_{FB}	-0.3 ~ 6.5	V
VL Pin Voltage		V_{VL}	-0.3 ~ V_{IN} + 0.3 or 6.5	V
VL Pin Current		I_{VL}	10	mA
MODE Pin Voltage		V_{MODE}	-0.3 ~ 6.5	V
PG Pin Voltage		V_{PG}	-0.3 ~ 6.5	V
PG Pin Current		I_{PG}	2	mA
BST Pin Voltage		V_{BST}	-0.3 ~ V_{LX} + 6.5	V
Lx Pin Voltage		V_{LX}	-0.3 ~ V_{IN} + 0.3 or 40.0 (*1)	V
Power Dissipation	DFN3030-12A	Pd	2050 (JESD51-7 board) (*2)	mW
	HSOP-8N		3125 (JESD51-7 board) (*2)	
Junction Temperature		Tj	-40 ~ 150	℃
Storage Temperature		Tstg	-55 ~ 150	℃

All voltages are described based on the GND (AGND, PGND) pin.

(*1) The maximum value should be either V_{IN}+0.3V or 40.0V in the lowest.

(*2) The power dissipation figure shown above is based upon PCB mounted and it is for reference only.
Please refer to PACKAGING INFORMATION for the mounting condition.

■RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNITS
Output Voltage Setting Range		V_{OUTSET}	2.5	-	18.0	V
Input Voltage		V_{IN}	4.5	-	36.0	V
Output Current		I_{OUT}	0	-	2000	mA
EN/SS Voltage		$V_{EN/SS}$	0.0	-	36.0	V
VL Pin Current		I_{VL}	Do not connect to external load.			-
MODE Pin Voltage		V_{MODE}	0.0	-	6.0	V
PG Pull-up Voltage		V_{PG}	0.0	-	6.0	V
PG Pull-up Resistor		R_{PG}	5	200	-	kΩ
Operating Ambient Temperature		Topr	-40	-	125	℃
Input Capacitor (Effective Value)		C_{IN}	1.2	-	1000 (*2)	μF
Output Capacitor (Effective Value)	2.5V≦V_{OUTSET}≦6.0V	C_L	21.0	-	1000 (*3)	μF
	6.0V＜V_{OUTSET}≦12.0V		13.0	-	1000 (*3)	
	12.0V＜V_{OUTSET}≦18.0V		9.0	-	1000 (*3)	
Local Regulator Capacitor (Effective Value)		C_{VL}	1.55	2.20	13	μF
Boot Strap Capacitor (Effective Value)		C_{BST}	0.075	0.100	0.125	μF

GND(AGND, PGND) are standard voltage for all the voltage.

(*1) Some ceramic capacitors have an effective capacitance that is significantly lower than the nominal value due to the applied DC bias and ambient temperature. For the input / output capacitance of this IC, use an appropriate ceramic capacitor according to the DC bias usage conditions (ambient temperature, input / output voltage) so that the effective capacitance value is equal to or higher than the recommended component.

(*2) If using a large-capacity capacitor such as an electrolytic capacitor or tantalum capacitor as the input capacitance, place a low ESR ceramic capacitor in parallel. If a ceramic capacitor is not placed, high-frequency voltage fluctuations will increase, and the IC may malfunction.

(*3) If using a large-capacity capacitor as the output capacitance, output stability may decrease and ripple voltage may increase. Even within the recommended capacitance range, output stability may be reduced depending on the type of capacitor such as ESR etc. used, so please verify this fully on the actual equipment before using.

■ELECTRICAL CHARACTERISTICS

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	CIRCUIT
Operating Input Voltage Range	V_{IN}			4.5	-	36.0	V	-
Setting Output Voltage Range	V_{OUTSET}			2.5	-	18.0	V	-
FB Voltage	V_{FB}	V_{FB}=0.768V→0.732V, V_{MODE}=5V V_{FB} when Lx pin oscillates		0.739	0.750	0.761	V	①
Local Regulator Output Voltage	V_{VL}	I_{VL}=0.1mA, V_{FB}=0.785V		4.75	5.00	5.25	V	②
UVLO Detect Voltage	V_{UVLOD}	V_{IN}=4.5V→3.3V, $V_{EN/SS}$=5V, V_{FB}=0.675V V_{IN} voltage when Lx pin holds “L” level		3.515	3.700	-	V	①
UVLO Release Voltage	V_{UVLOR}	V_{IN}=3.3V→4.5V, $V_{EN/SS}$=5V, V_{FB}=0.675V V_{IN} voltage when Lx pin changes from "L" to "H" level		-	4.000	4.200	V	①
Quiescent Current PFM	I_{q_PFM}	V_{FB}=0.785V, V_{LX}=0V, V_{MODE} =0V		-	9	25	μA	①
Quiescent Current PWM	I_{q_PWM}	V_{FB}=0.785V, V_{LX}=0V, V_{MODE}=5V		-	360	500	μA	①
Stand-by Current	I_{STB}	$V_{EN/SS}$=V_{FB}=V_{LX}=0V, V_{MODE}=0V		-	0.5	2.0	μA	①
Oscillation Frequency	f_{OSC}	V_{FB}=0.675V		720	800	880	kHz	①
Maximum Duty Cycle	D_{MAX}	V_{FB}=0.675V		85	90	-	%	①
Minimum Duty Cycle	D_{MIN}	V_{FB}=0.785V		-	-	0	%	①
Lx ”H” SW On Resistance	R_{LXH}	I_{LX}=150mA		-	200	300	mΩ	-
Lx ”L” SW On Resistance	R_{LXL}	I_{LX}=150mA		-	120	-	mΩ	-
PFM Switch Current	I_{PFM}	Connection to external components, I_{OUT}=1mA, V_{IN}=12V		-	450	-	mA	③
Low side Current Limit	I_{LIML}	V_{FB}=0.75V		2400(*1)	3000(*1)	3800(*1)	mA	-
Internal Soft-Start Time	t_{ss1}	V_{FB}=0.675V		1.0	2.5	5.5	ms	①
External Soft-Start Time	t_{ss2}	$V_{EN/SS}$=24V, V_{FB}=0.675V, R_{ss}=390kΩ, C_{ss}=0.47μF		-	8.8	-	ms	④
FB Voltage Temperature Characteristics	ΔV_{FB} / ΔT_{opr}* V_{FB})	-40≦T_{opr}≦125℃		-	±100	-	ppm/℃	①
Over Voltage Protection	V_{OVP}	V_{FB}=0.75V→0.9V, Lx pin voltage holding “L” level		0.796	0.829	0.862	V	-
PG Detect Voltage	V_{PGDET}	V_{FB}=0.75V→0.6V, R_{PG} =200kΩ pull-up to 5V V_{FB} when PG pin voltage changes from “H” level to “L” level.		0.630	0.667	0.704	V	⑤
PG Output Voltage	V_{PG}	V_{FB}=0.675V, I_{PG}=1mA		-	0.05	0.3	V	⑥
EN “H” Voltage	V_{ENH}	V_{FB}=0.675V, $V_{EN/SS}$ which Lx pin oscillates	Ta=25℃	2.5	-	36.0	V	①
			Ta=-40~125℃	2.5(*2)	-	36.0		
EN “L” Voltage	V_{ENL}	V_{FB}=0.785V, $V_{EN/SS}$ which Lx pin voltage holding “L” level	Ta=25℃	GND	-	0.4	V	①
			Ta=-40~125℃	GND	-	0.4(*2)		
EN “H” Current	I_{ENH}	V_{IN}=$V_{EN/SS}$=36V		-	-	1.1	μA	⑦
EN “L” Current	I_{ENL}	V_{IN}=36V, $V_{EN/SS}$=0V		-	0.0	0.1	μA	⑦
Thermal Shutdown Temperature	T_{TSD}	Junction Temperature		-	160	-	℃	-
Hysteresis Width	T_{HYS}	Junction Temperature		-	25	-	℃	-
MODE “H” Voltage	V_{MODEH}	Operation MODE “PWM/PFM Auto” to “PWM”	Ta=25℃	1.2	-	6.0	V	③
			Ta=-40~125℃	1.5(*2)	-	6.0		
MODE “L” Voltage	V_{MODEL}	Operation MODE “PWM” to “PWM/PFM Auto”	Ta=25℃	GND	-	0.45	V	③
			Ta=-40~125℃	GND	-	0.3(*2)		
MODE “H” Current	I_{MODEH}	V_{IN}=36V, $V_{EN/SS}$=5V, V_{MODE}=5V		-	2.5	5.5	μA	⑦
MODE “L” Current	I_{MODEL}	V_{IN}=36V, $V_{EN/SS}$=0V, V_{MODE}=0V		-	0.0	0.1	μA	⑦
FB “H” Current	I_{FBH}	V_{IN}=36V, $V_{EN/SS}$=5V, V_{FB}=1V		-	0.0	0.1	μA	⑦
FB “L” Current	I_{FBL}	V_{IN}=36V, $V_{EN/SS}$=0V, V_{FB}=0V		-	0.0	0.1	μA	⑦
Lx "H" Leakage Current	I_{LXH}	V_{IN}=36V, V_{LX}=0V, $V_{EN/SS}$=V_{FB}=0V		-	0.0	0.1	μA	⑧
Lx "L" Leakage Current	I_{LXL}	V_{IN}=36V, V_{LX}=36V, $V_{EN/SS}$=V_{FB}=0V		-	0.0	0.1	μA	⑧

Test Condition: Unless otherwise stated, V_{IN}=12V, $V_{EN/SS}$=12V

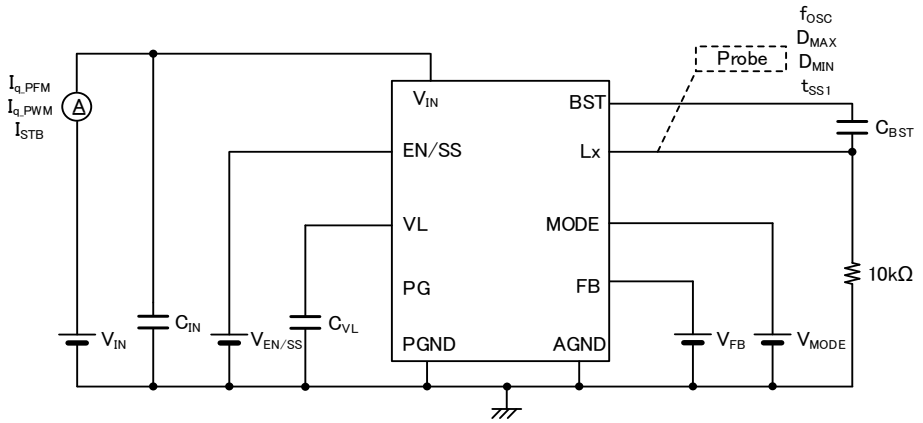
Connected to external components : L=6.8μH, R_{FB1}=680kΩ, R_{FB2}=120kΩ, C_{FB}=8pF, C_L=66μF, C_{IN}=4.7μF, C_{VL}=2.2μF, C_{BST}=0.1μF

*1: Current limit denotes the level of detection at bottom of coil current.

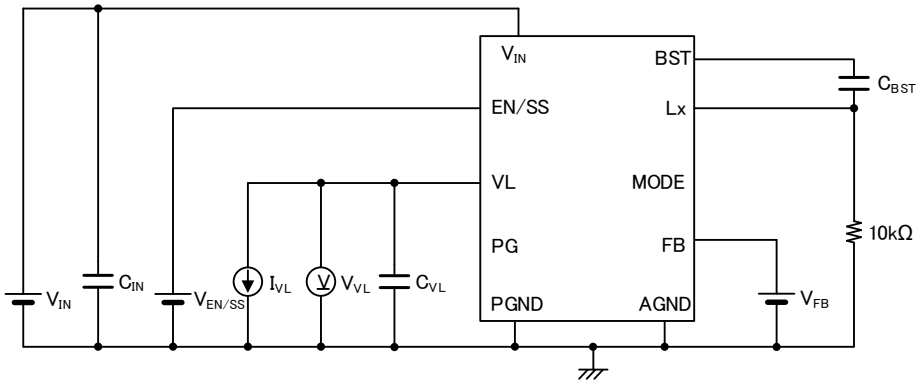
*2: Design value

■TEST CIRCUITS

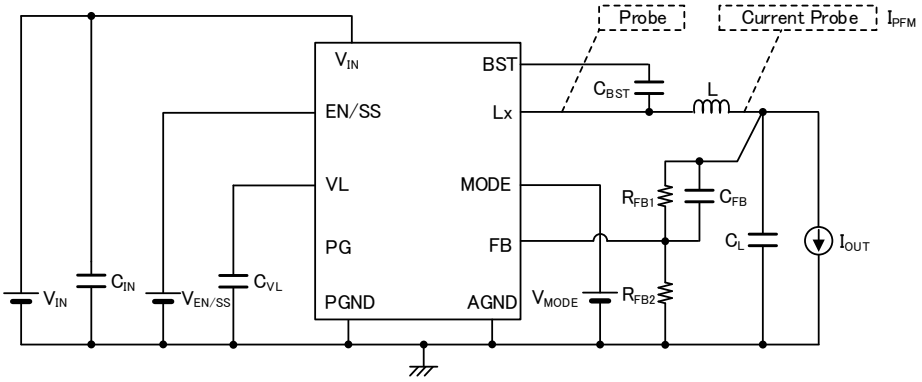
TEST CIRCUIT①



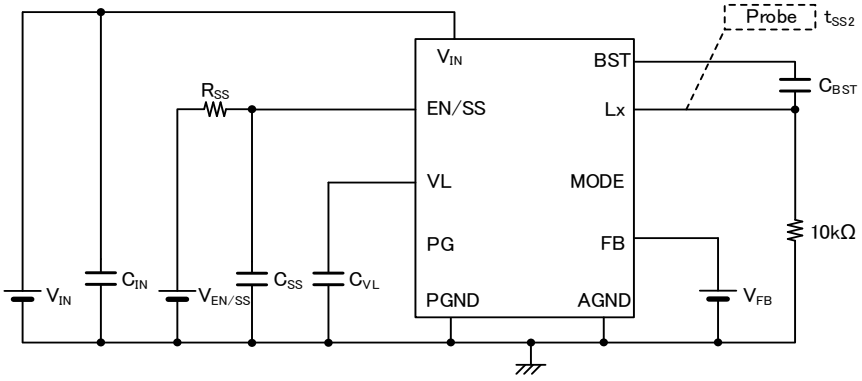
TEST CIRCUIT②



TEST CIRCUIT③

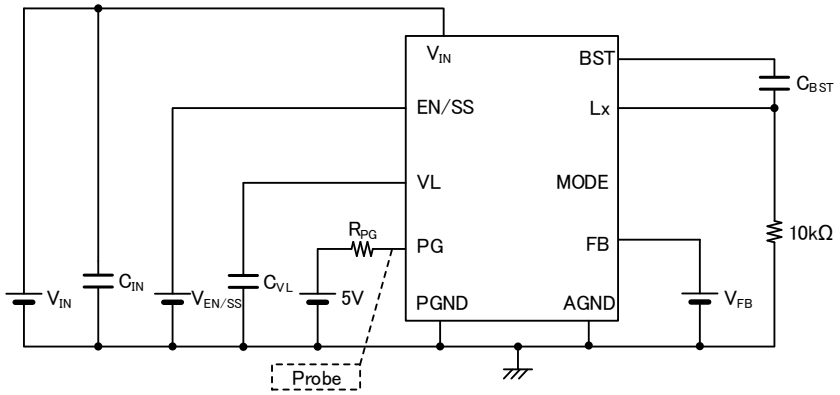


TEST CIRCUIT④

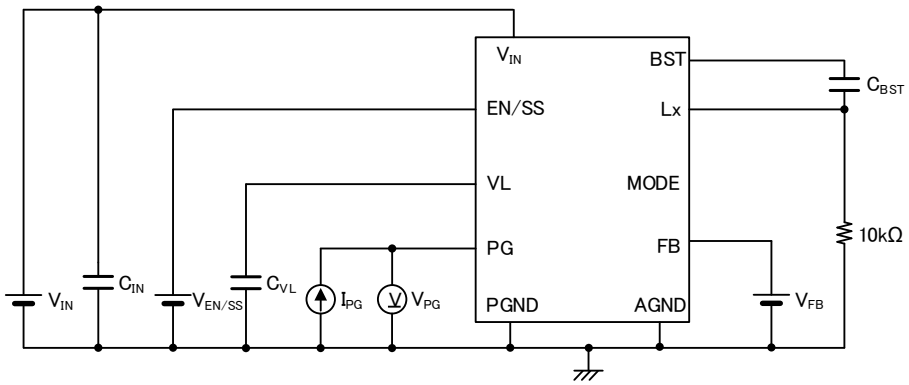


■TEST CIRCUITS

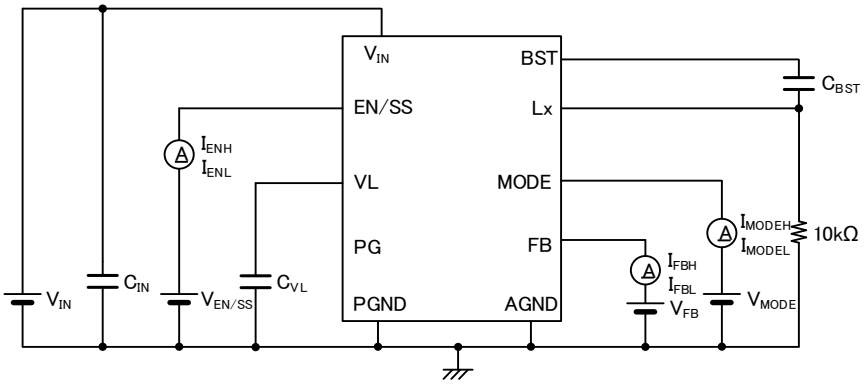
TEST CIRCUIT⑤



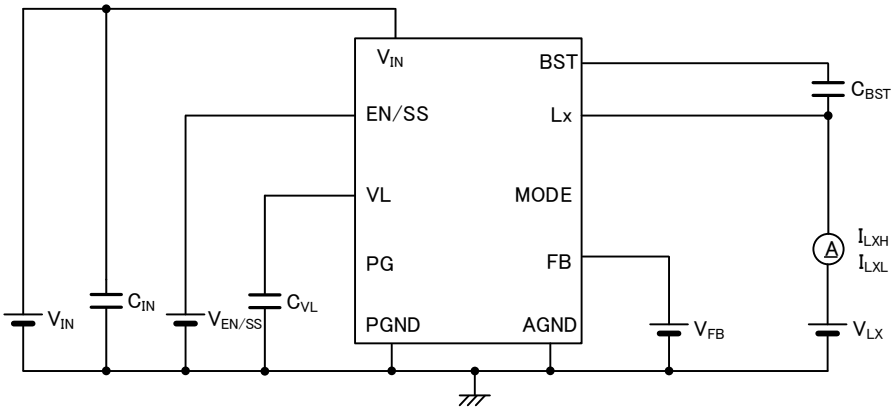
TEST CIRCUIT⑥



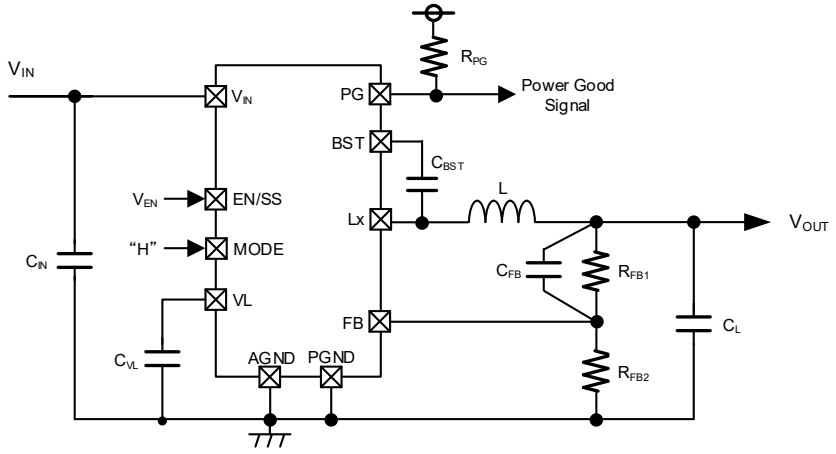
TEST CIRCUIT⑦



TEST CIRCUIT⑧



■TYPICAL APPLICATION CIRCUIT / PARTS SELECTION GUIDE



	CONDITIONS	MANUFACTURER	PRODUCT NUMBER	VALUE	SIZE(L×W×T)
L	VOUTSET≦6.0V	TAIYO YUDEN	LBXHF6060YEL6R8MMR	6.8μH	6.0×6.0×4.5mm
		Coilcraft	XGL4040-682MEC	6.8μH	4.0×4.0×4.1mm
	6.0V＜VOUTSET≦12.0V	TDK	VLS6045EX-150M-H	15μH	6.0×6.3×4.5mm
		TBD	TBD	TBD	TBD
	12.0V＜VOUTSET	TDK	SPM6545VT-220M-D	22μH	7.0×6.5×4.5mm
		TBD	TBD	TBD	TBD

	CONDITIONS	MANUFACTURER	PRODUCT NUMBER	VALUE	SIZE(L×W×T)
CIN	-	Murata	GRM31CR71H475MA12	4.7μF/50V	3.2×1.6×1.9mm
CL	VOUTSET≦6.0V	TDK	C2012X7S1A226M125AC	22μF/10V x 3	2.0×1.25×1.45mm
		TBD	TBD	TBD	TBD
	6.0V＜VOUTSET≦12.0V	TDK	C2012X7S1E106K125AC	10μF/25V x 3	2.0×1.25×1.50mm
		TBD	TBD	TBD	TBD
	12.0V＜VOUTSET	TDK	C3216X7R1H106K160AC	10μF/50V x 2	3.2×1.6×1.9mm
		TBD	TBD	TBD	TBD
CBST	-	TDK	C1005X7R1E104K050BB	0.1μF	1.0×0.5×0.55mm
		Murata	GCM155R71H104KE02D	0.1μF	1.0×0.5×0.55mm
CVL	-	TDK	C1608X7S1E225K080AB	2.2μF	1.6×0.8×1.0mm
		Murata	GRM188C71E225KE11D	2.2μF	1.6×0.8×1.0mm

(*1) Some ceramic capacitors have an effective capacitance that is significantly lower than the nominal value due to the applied DC bias and ambient temperature. For the input / output capacitance of this IC, use an appropriate ceramic capacitor according to the DC bias usage conditions (ambient temperature, input / output voltage) so that the effective capacitance value is equal to or higher than the recommended component.

(*2) If using a large-capacity capacitor such as an electrolytic capacitor or tantalum capacitor as the input capacitance, place a low ESR ceramic capacitor in parallel. If a ceramic capacitor is not placed, high-frequency voltage fluctuations will increase, and the IC may malfunction.

■TYPICAL APPLICATION CIRCUIT / PARTS SELECTION GUIDE

<Output voltage setting Value>

The output voltage can be set by adding an external dividing resistor.

The output voltage (V_{OUTSET}) is determined by the equation below based on the values of R_{FB1} and R_{FB2}.

$$V_{OUTSET} = V_{FB} \times (R_{FB1}+R_{FB2}) / R_{FB2}$$

However, $R_{FB2} \leqq 250k\Omega$ and $R_{FB1}+R_{FB2} \leqq 2M\Omega$

If the IC does not operate normally due to external noise, etc., noise resistance performance can be improved by using a combination of R_{FB1} and R_{FB2} smaller than the above conditional expression.

< C_{FB} setting>

The value of the speed-up capacitor C_{FB} is optimized by adjusting with the following equation.

The optimum value of f_{zfb} does not change regardless of the capacitance value of the output capacitor.

$$C_{\mathrm{FB}} = \frac{1}{2\pi \times f_{\mathrm{zfb}} \times R_{\mathrm{FB1}}}$$

$$f_{\mathrm{zfb}} = 30\mathrm{kHz}$$

【Calculation Example】

When the output voltage is set to 5.0V, R_{FB1}=680kΩ, R_{FB2}=120kΩ, V_{OUTSET}=0.75V×(680kΩ+120kΩ) / 120kΩ = 5.0V.

Since the target is f_{zfb}=30kHz, C_{FB}= 1/(2× π ×30kHz×680kΩ) =7.8pF from the above equation, which is 8pF for the E24 series.

PWM/PFM control(MODE="L" or OPEN) : Typical Examples

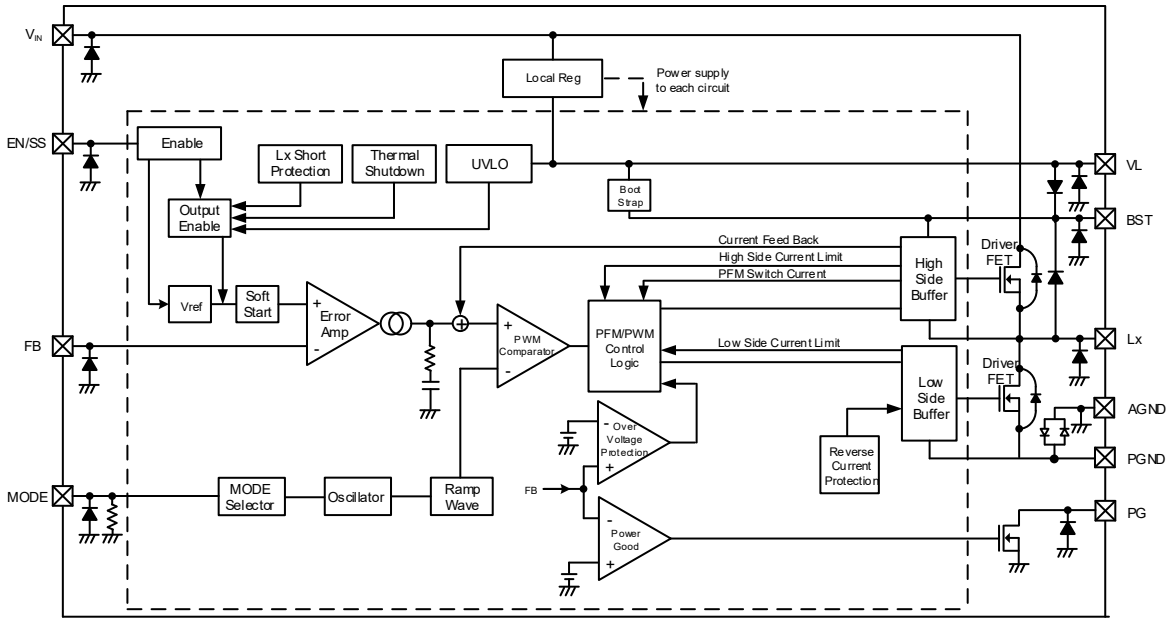
V_{OUTSET}	R_{FB1}	R_{FB2}	C_{FB}	f_{zfb}
2.5V	560kΩ	240kΩ	10pF	28.4kHz
3.3V	680kΩ	200kΩ	8pF	29.3kHz
5.0V	680kΩ	120kΩ	8pF	29.3kHz
6.0V	910kΩ	130kΩ	6pF	29.2kHz
12.0V	1800kΩ	120kΩ	3pF	29.5kHz
15.0V	820kΩ	43kΩ	7pF	27.7kHz
18.0V	620kΩ	27kΩ	9pF	28.5kHz

PWM control(MODE="H") : Typical Examples

V_{OUTSET}	R_{FB1}	R_{FB2}	C_{FB}	f_{zfb}
2.5V	56kΩ	24kΩ	100pF	28.4kHz
3.3V	68kΩ	20kΩ	82pF	28.6kHz
5.0V	68kΩ	12kΩ	82pF	28.6kHz
6.0V	91kΩ	13kΩ	56pF	31.2kHz
12.0V	180kΩ	12kΩ	27pF	32.8kHz
15.0V	82kΩ	4.3kΩ	68pF	28.6kHz
18.0V	62kΩ	2.7kΩ	91pF	28.2kHz

■OPERATIONAL EXPLANATION

The control method of this IC is a current mode control method compatible with low ESR ceramic capacitors.



<Internal power supply (Local Reg)>

This IC has a built-in regulator as an internal power supply for supplying voltage to the internal circuit.

The output of the regulator is output to the VL pin, and the VL pin voltage becomes V_{VL} (TYP. 5.0V). However, when the V_{IN} pin voltage becomes lower than V_{VL}, the regulator output voltage will drop.

Even when EN/SS="L", internal regulator operates and voltage is supplied to the internal circuit.

In addition to the internal circuit, the regulator supplies voltage to the BST pin via a backflow prevention switch.

The internal regulator has an output short circuit protection function.

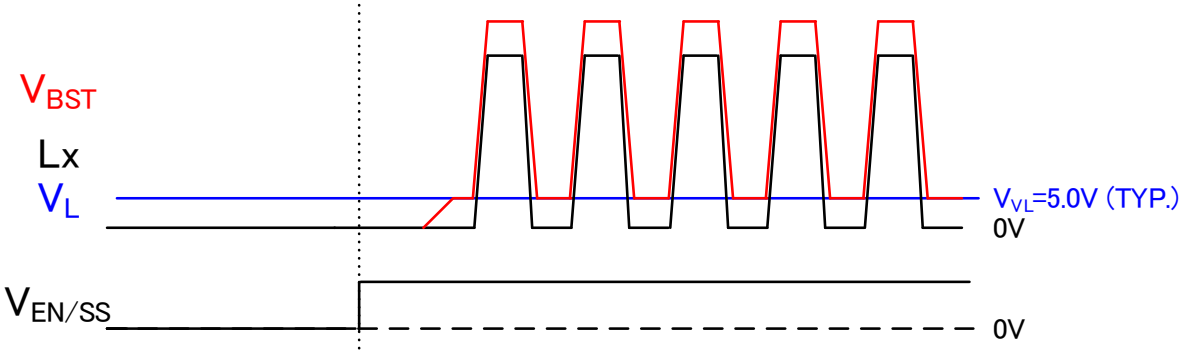
When the VL pin is shorted during regulator operation, or when the regulator is started with the VL pin already shorted, the output current of the regulator is controlled to prevent overcurrent from flowing. If the output short is released during regulator operation, it will automatically recover.

Note that using the VL pin voltage for purposes other than this IC is prohibited.

<Boot Strap>

This IC uses an Nch FET as the High side driver FET and has a built-in bootstrap circuit for generating its gate voltage.

During the on-time of the low-side driver FET (Lx≒0V), an external capacitor C_{BST} is charged by the internal power supply. The BST pin voltage is used as the power supply voltage for the high-side buffer circuit. Due to the external capacitor C_{BST}, the BST pin voltage is maintained at "Lx + V_{VL} (TYP. 5.0V)" even during the off-time of the low-side driver FET. It is possible to supply the gate voltage necessary for driving the high-side driver FET.



■OPERATIONAL EXPLANATION

<Normal operation>

The error amplifier compares the internal reference voltage Vref divided by resistance with FB pin voltage. And the control signal obtained by adding phase compensation to the output of the error amplifier is input to the PWM comparator to determine the switching ON time during PWM control.

The PWM comparator compares the above control signal with the ramp wave, and outputs a switching pulse with a controlled duty width from the Lx pin. The output voltage is stabilized by performing these controls continuously.

The current sense circuit monitors the current of the driver FET for each switching operation and modulates the output signal of the error amplifier as a multiple feedback signal (current feedback circuit). This enables a stable feedback control even using a low ESR capacitor such as a ceramic capacitor.

PWM control (MODE="H")

During MODE='H', the system operates in forced PWM mode.

Due to operating at a constant frequency f_{OSC} (TYP. 800kHz) regardless of the output current, it becomes easy to filter switching noise.

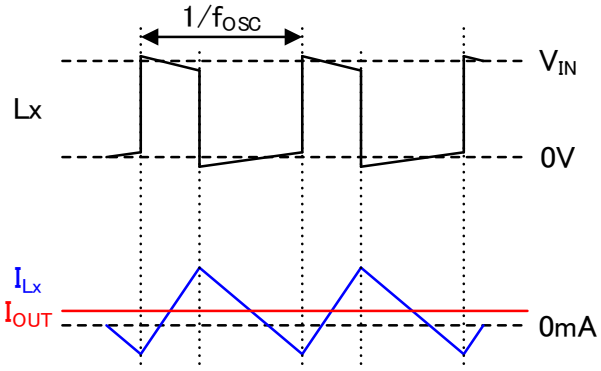
In addition, when the FB pin voltage keeps higher than V_{FB}, the switching operation stops (turns off the High-side/Low-side driver), and it stops until the FB pin voltage drops.

PWM/PFM automatic switching control (MODE="L" or "OPEN")

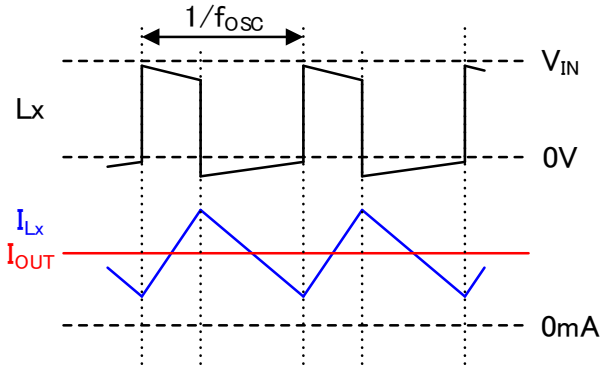
When MODE="L" or OPEN, it operates in PWM/PFM automatic switching mode.

PWM/PFM automatic switching control reduces the switching frequency at light load by turning on the High side driver FET until the coil current reaches the PFM current I_{PFM} (TYP. 450mA).

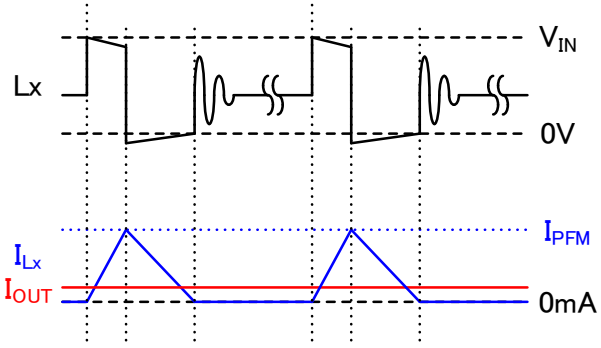
This operation reduces loss at light loads and achieves high efficiency from light loads to heavy loads. When the output current increases, the switching frequency increases in proportion to the output current. When the switching frequency reaches f_{OSC}, PFM control is switched to PWM control, and the switching frequency is fixed.



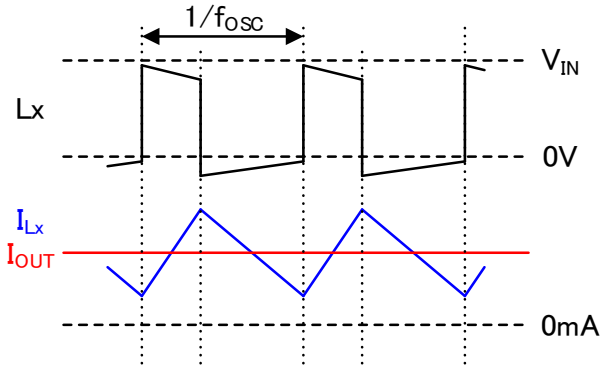
PWM control : operation example of light loads



PWM control : operation example of heavy loads



PWM/PFM control : operation example of light loads



PWM/PFM control : operation example of heavy loads

■OPERATIONAL EXPLANATION

<EN Function / Start Mode・Soft-start Function>

The state of the IC can be switched by applying voltage to the EN/SS pin.

PIN NAME	SIGNAL	STATUS
EN/SS	H	Active
	L	Stand-by
	OPEN	Stand-by

EN/SS="L" or "OPEN" : Stand-by mode

When the EN/SS pin voltage is "L" or "OPEN", the IC enters the stand-by mode, and the current consumption is reduced to the stand-by current I_{STB} (TYP. 0.5μA). In the stand-by mode, no signal is output to the Lx pin and the output voltage does not rise. In addition, various protection functions stop operating.

The internal regulator operates even in the stand-by state, but the output voltage of the regulator is lower than the active state voltage V_{VL} (TYP. 5.0V).

EN/SS="H" : Active mode

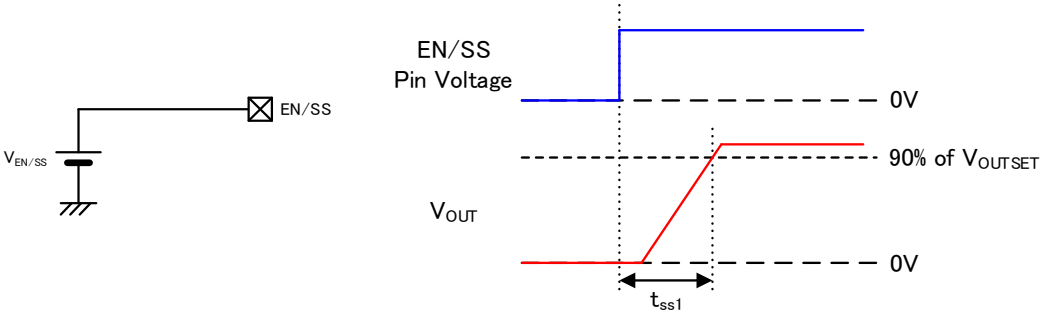
When the EN/SS pin voltage is "H", the IC becomes active. When the IC becomes active, it enters start-up mode and increases the output voltage to the set output voltage.

In start-up mode, a soft-start function is provided to gently raise the output voltage to suppress inrush current at start-up. The soft-start time can be adjusted by externally mounting a capacitor and resistor on the EN/SS pin.

During the start-up mode, the device operates in the same way as in normal operation, except that the reference voltage increases linearly.

(a) Internal soft-start time (no external RC)

When the EN/SS pin voltage rises steeply, the output voltage rises with an internally set soft-start time of t_{ss1} (TYP. 2.5ms) and shifts to normal mode.



■OPERATIONAL EXPLANATION

(b) Soft-start time external adjustment (with external RC)

The soft-start time can be adjusted by externally mounting a capacitor and resistor on the EN/SS pin.

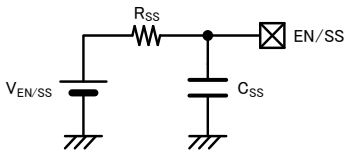
The externally set soft-start time (t_{SS2}) is determined by the following formula, depending on the EN/SS pin voltage ($V_{EN/SS}$), R_{SS}, and C_{SS} values.

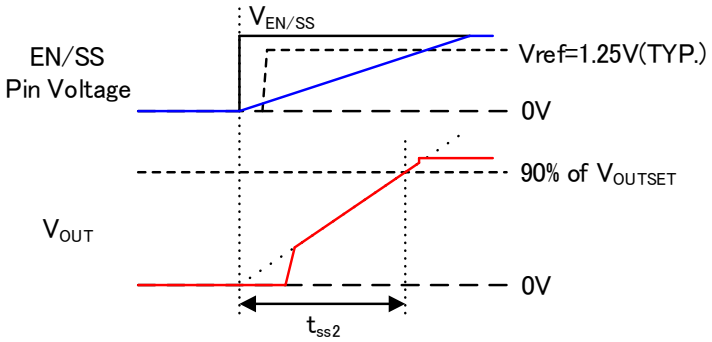
$$t_{ss2} = C_{ss} \times R_{ss} \times \ln \frac{V_{EN/SS}}{V_{EN/SS} - (1.25 \times 0.9)}$$

For example, When the soft-start time at C_{SS} = 0.47μF, R_{SS} = 390kΩ, $V_{EN/SS}$ = 24V, The result is as follows.

$$t_{ss2} = 0.47 \times 10^{-6} \times 390 \times 10^{3} \times \ln \frac{24}{24 - (1.25 \times 0.9)} = 8.8\text{ms}$$

However, it cannot start faster than the internally setting soft-start time t_{ss1}.





* Definition of soft-start time : Time from $V_{EN/SS}$ start-up until output voltage reaches 90% of set output voltage.

■OPERATIONAL EXPLANATION

<Current Limit>

The current limit circuit of this IC detects the current flowing through the driver FET connected to Lx and equivalently monitors the coil current. The current limit function operates when overcurrent is detected. The current limiting function includes a high side current limiting function and a low side current limiting function. The current limit state continues until the overcurrent state is released, and the output voltage automatically recovers when the overcurrent state is released.

A current fold-back circuit is used for the current limit function.

In a current fold-back circuit, the output voltage drops, and the current limit is hold down when the FB voltage drops. This operation results in a narrowing of the output current when the output voltage drops.

High side Current Limit

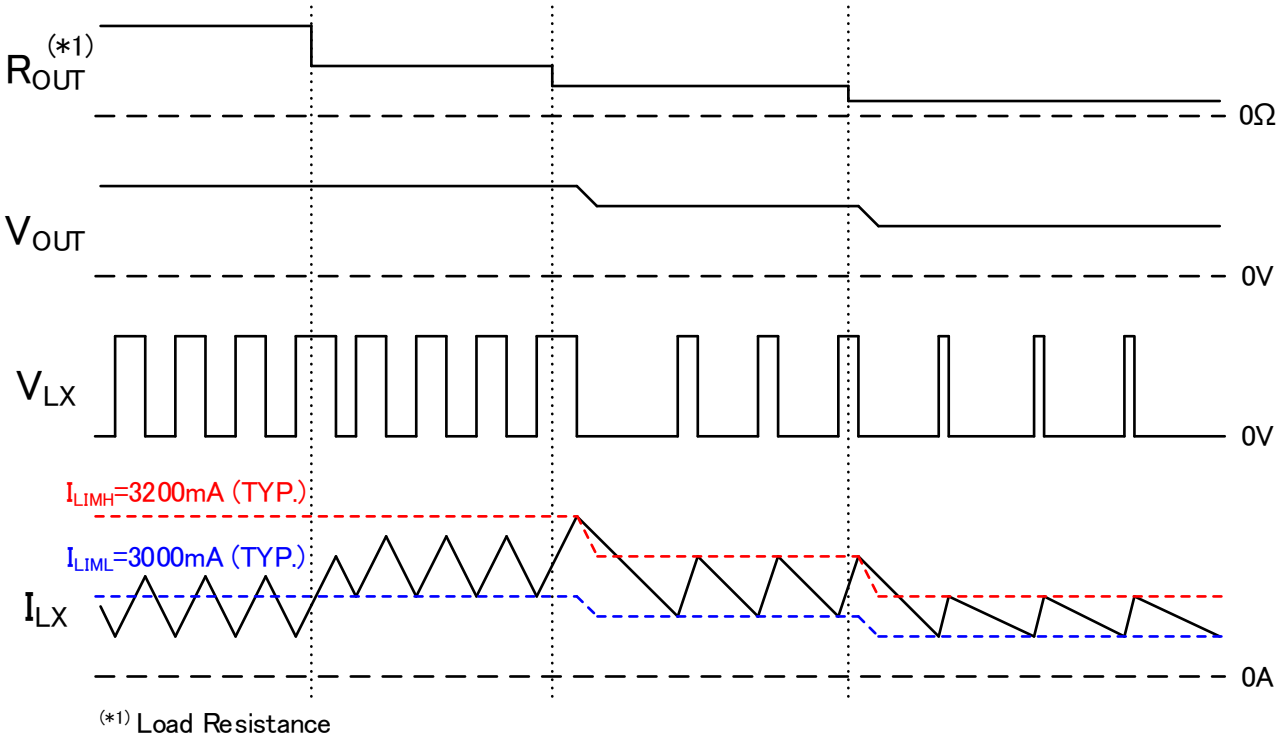
The High side current limit function detects when the coil current exceeds the High side current limit value I_{LIMH} (TYP. 3200mA) and turns off the High side driver FET. In other words, it controls the coil current peak so that it does not exceed I_{LIMH}. However, if the input voltage is high, the coil current peak value may exceed I_{LIMH} due to the operation delay of the internal circuit.

Low side Current Limit

The Low side current limit function turns on the Low side driver FET until the coil current becomes less than the Low side current limit value I_{LIML} (TYP. 3000mA). In other words, it controls the bottom of the coil current below I_{LIML}.

The current limit function also operates during start-up mode.

During start-up mode, the output voltage is lower than the set output voltage, the current limit value is reduced, which speeds up overcurrent detection. If an output capacitance with a higher effective capacitance value than the recommended component is used, the start-up will take place while the current limit function is operating, and the start-up time may be much longer than the soft-start time.



■OPERATIONAL EXPLANATION

<Thermal Shutdown>

The junction temperature is monitored to protect the IC from thermal destruction.

When the junction temperature reaches the thermal shutdown detection temperature T_{TSD} (TYP. 160°C), the thermal shutdown activated, the High side driver FET and Low side driver FET are turned off. When the junction temperature drops to the thermal shutdown release temperature T_{TSD}-T_{HYS} (TYP. 135°C) by stopping the current supply, the output voltage is turned on by the start-up mode, and then normal operation starts.

The internal regulator operates even during thermal shutdown, and the output voltage V_{VL} (TYP. 5.0V) is output to the VL pin.

<UVLO>

This function monitors the internal power supply of the IC and prevents false pulse output from the Lx pin due to unstable operation when the internal power supply is low. As the IC's internal power supply drops as the V_{IN} pin voltage drops, the UVLO function operates when the V_{IN} pin voltage drops.

When the V_{IN} pin voltage falls below V_{UVLOD} (TYP. 3.7V), the UVLO function operates, and forcibly turns off the driver FETs. When the V_{IN} pin voltage rises above V_{UVLOR} (TYP. 4.0V), the UVLO function is released, and the output voltage rises according to the start-up mode.

During UVLO operation, the internal regulator is still operating, and its output voltage approximately matches the V_{IN} pin voltage. However, if the V_{IN} pin voltage is so low that the regulator or the reference voltage Vref cannot operate, the regulator output voltage will be less than the V_{IN} pin voltage.

<Over Voltage Protection>

An output overvoltage protection function is built in to suppress output voltage overshoots after completion of start-up or transient response. When the FB pin voltage rises above V_{FB} x 1.105 (TYP.), the output overvoltage protection function operates and forcibly turns off the High side driver FET.

In forced PWM control (MODE="H"), the Low side driver FET is turned on immediately after the output overvoltage protection function operates and remains this state until the next cycle.

In PWM/PFM automatic switching control (MODE="L" or OPEN), the driver FET is turned off by the output overvoltage protection function. When the output voltage drops to the set value due to the output current, switching operation resumes.

<Lx Short Protection>

If the Lx pin is shorted to GND during normal operation, the Lx short protection function will operate.

The Lx short protection function turns off the driver FET to prevent IC breakdown due to overcurrent.

After the Lx short protection function operates, the output voltage rises in start-up mode, but if the Lx pin remains short to GND, the output voltage does not rise because the Lx short protection function is operated again during start-up mode.

If the IC is started up with the Lx pin short to GND, the Lx short protection function also operates and the output voltage does not rise.

■OPERATIONAL EXPLANATION

<Power Good>

Functions for monitoring the status of outputs and ICs.

CONDITIONS		SIGNAL
EN/SS=H	$V_{FB} > V_{PGDET}$	H (High impedance)
	$V_{FB} \leqq V_{PGDET}$	L (Low impedance)
	Over Voltage Protection	H (High impedance)
	Thermal Shutdown	L (Low impedance)
	UVLO ($V_{IN} < V_{UVLOD}$)	Undefined State
EN/SS=L or OPEN	Stand-by	L (Low impedance)

Since the PG pin is an Nch open-drain output, connect a pull-up resistor (approx. 200kΩ) to the PG pin.
When the power good function is not used, connect the PG pin to GND or leave it open.

A delay time of 600μs (TYP.) is provided from the moment, the FB pin voltage drops below V_{PGDET} to PG="L". If the FB pin voltage returns to a voltage higher than V_{PGDET} during the delay time, PG remains “H”. This prevents PG="L" due to output undershoot during transient response. In addition, there is no intentional delay for PG="L" due to the operation of the protection function or transition to the stand-by state.

<MODE switching function>

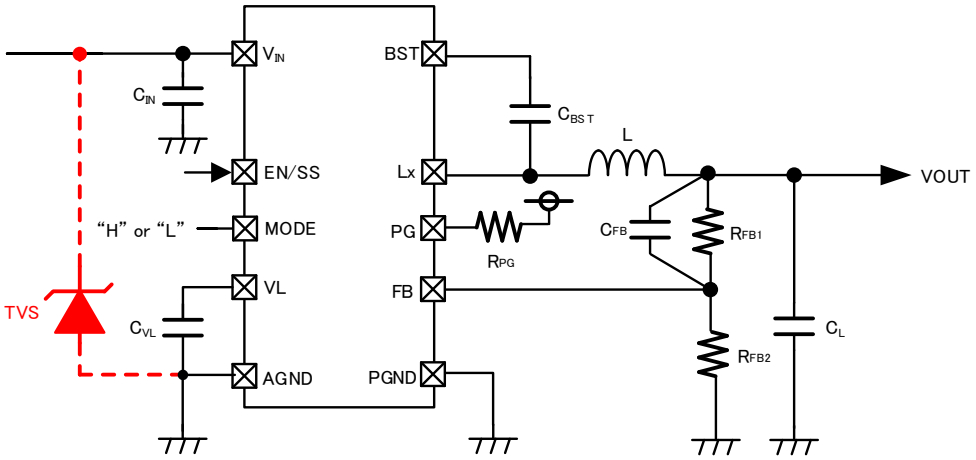
The operation mode can be selected from PWM and PWM/PFM control according to the voltage applied to the MODE pin.
It is also possible to switch the control mode by changing the MODE terminal voltage during normal operation.

PIN NAME	SIGNAL	STATUS
MODE	H	PWM
	L	PWM/PFM Auto
	OPEN	PWM/PFM Auto

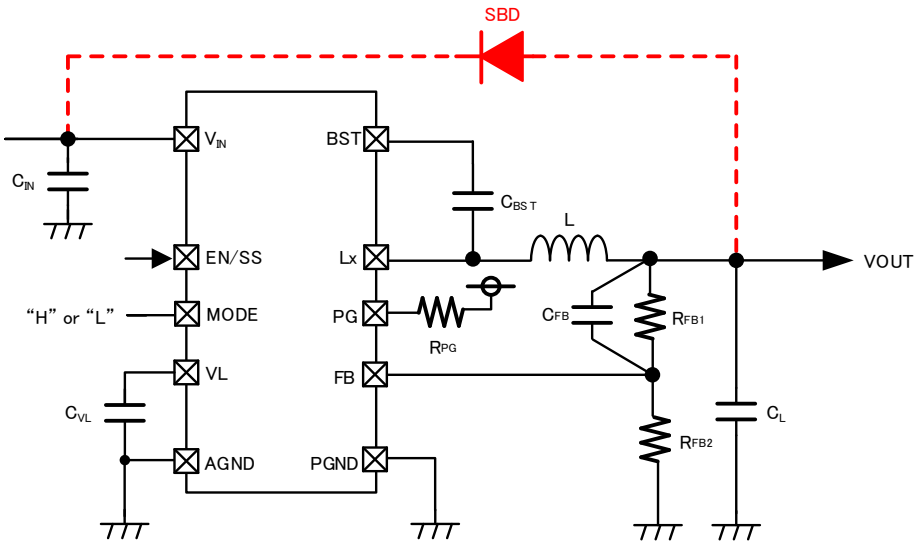
■NOTES ON USE

1) For the phenomenon of temporal and transitional voltage decrease or voltage increase, the IC may be damaged or deteriorated if IC is used beyond the absolute MAX. specifications. Also, if used under out of the recommended operating range, the IC may not operate normally or may cause deterioration.

If a voltage exceeding the absolute maximum voltage is applied to this IC due to chattering by mechanical switches or surge voltage from external sources, take measures using protective elements such as TVS and protective circuits.



Under conditions where the input voltage is lower than the output voltage, an overcurrent may flow through the parasitic diode inside the IC and exceed the absolute maximum rating of the Lx pin. If the impedance between V_{IN} and GND is low and current is drawn into the input side, take measures such as adding an SBD between V_{OUT} and V_{IN}.



2) Spike noise and ripple voltage arise in a switching regulator as with a DC/DC converter. These are greatly influenced by external component selection, such as the coil inductance, capacitance values, and board layout of external components. Once the design has been completed, verification with actual components should be done.

3) The DC/DC converter performance is greatly influenced by not only the ICs' characteristics, but also by those of the external components. Care must be taken when selecting the external components. Especially for capacitor, particular attention should be paid to DC bias characteristics, temperature characteristics, etc. to ensure that they have an effective capacitance equal to or greater than that of the recommended components under actual operating conditions.

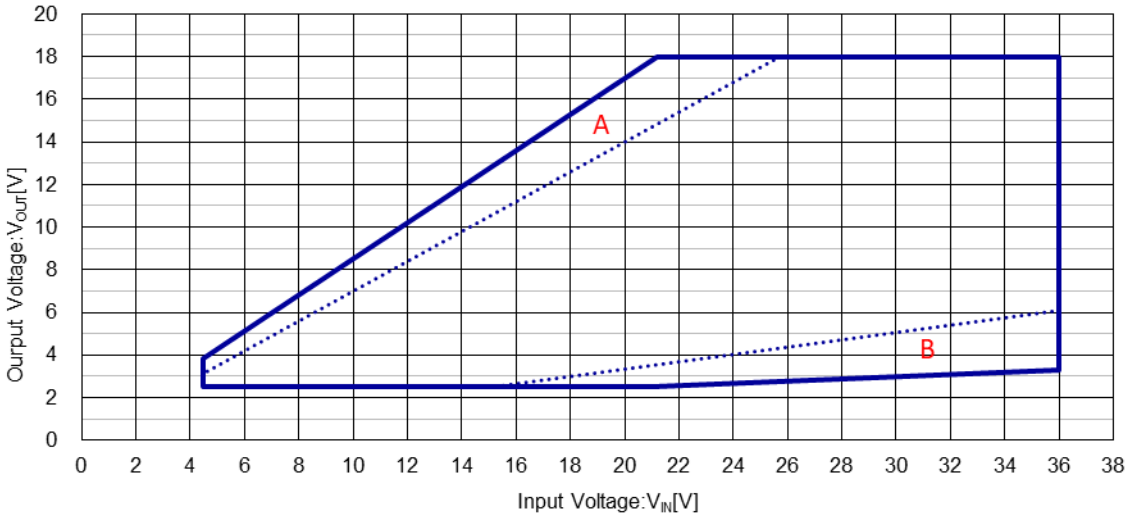
■NOTES ON USE

4) Stable Operating Range

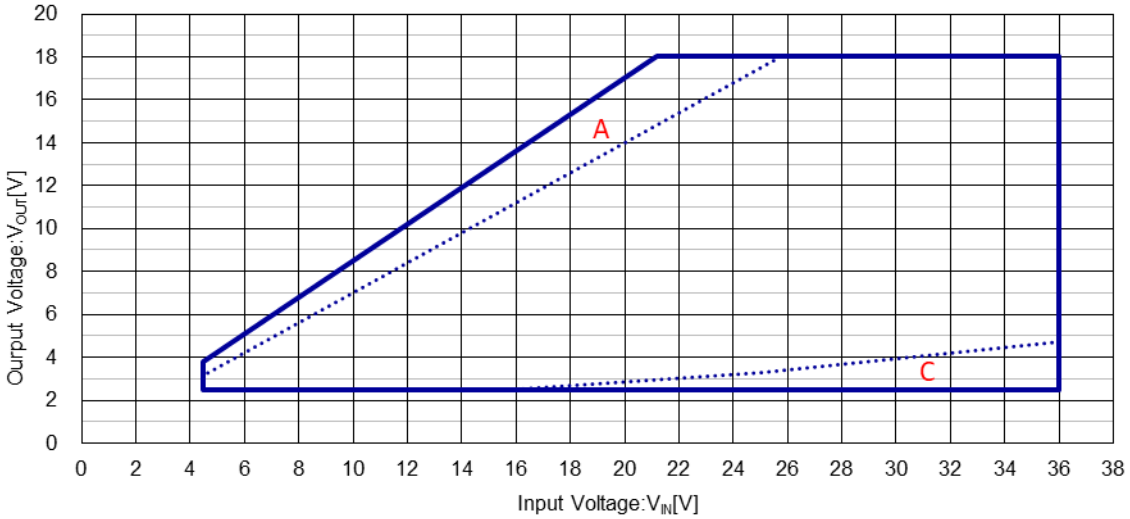
Please ensure that your power supply specifications are within the stable operating range before use.

V_{OUTSET}-V_{IN} Stable operating range

PWM Mode(MODE='H')



Automatic PWM/PFM Switching Mode(MODE='L')



[Within the Stable Operating Range]

When operating within the VOUTSET–VIN stable operating range and within areas A–C of the graph, please note the following:

(A) If used in the region where the duty cycle exceeds 70%, transient response may significantly deteriorate.

(B) If used in this range, stability may degrade in load regions where the inductor current flows in reverse (Iout ≈ 100 mA), and ripple voltage of up to 2% of the output voltage may occur.

(C) If used in this range, stability may degrade after switching to PWM operation, and large ripple voltage exceeding 10% of the output voltage may occur.

[Outside the Stable Operating Range]

If operated outside the VOUTSET–VIN stable operating range, the following behaviors may occur, and the IC may not operate properly:

(A) Under conditions with a high step-down ratio, abnormal sinusoidal oscillation may occur.

(B) Under conditions with a low step-down ratio, the device may operate at the maximum duty cycle, causing the output voltage to drop below the set output voltage.

■NOTES ON USE

5) After soft-start completion, if the input voltage (V_{IN}) is held below the internal power supply voltage (Local Reg): V_{VL} (TYP. 5.0V) and then increased with a slope of 1V/ms or more, the VL pin voltage may overshoot beyond its absolute maximum rating, potentially causing malfunction of the IC.

Under the operating conditions described above, to suppress fluctuations in the VL pin voltage, please use the following components or equivalent parts for CVL instead of the recommended components.

	MANUFACTURER	PRODUCT NUMBER	VALUE	SIZE(L×W×T)
C_{VL}	TDK	C2012X7S1E106KT	10μF/25V	2.0×1.25×1.50mm

6) Supply a stable input voltage to the V_{IN} pin with sufficiently reduced AC impedance due to the bypass capacitor to operate the IC normally. If the input voltage fluctuates momentarily, take countermeasures such as increasing the input capacitance.

7) The Lx short-circuit protection function may not operate if the short-circuit path includes wiring resistance or contact resistance. Even if the Lx short-circuit protection function does not operate, the IC is protected by the operation of the current limiting function and the thermal shutdown function.

8) Torex places an importance on improving our products and their reliability. We request that users incorporate fail safe designs and post aging protection treatment when using Torex products in their systems.

9) Instructions of pattern layouts.
Especially noted in the pattern layout are as follows.
Please refer to the reference pattern layout on the next page.

(a) Wire the large current line using thick, short connecting traces.
This makes it possible to reduce the wire impedance, which is expected to reduce noise and improve heat dissipation.
If the wire impedance of the large current line is large, it may cause noise, or the IC cannot operate normally.

(b) Place the input capacitance C_{IN}, output capacitance C_L, inductor L and IC which the large current flows on the same surface. If they are placed on both sides, a large current will flow through Via, which has high impedance, it may cause noise, and the IC may not operate normally.

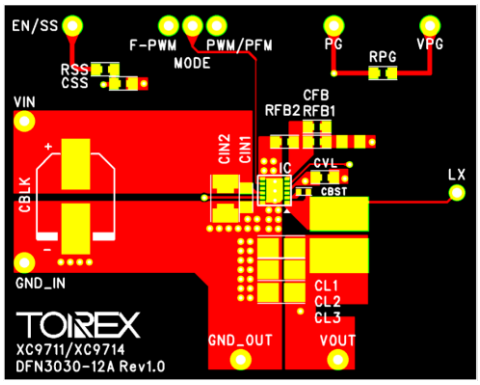
(c) Please mount each external component as close to the IC as possible.
Especially place the input capacitance C_{IN} near the IC and connect it with as low impedance as possible.
If C_{IN} is positioned too far from the IC, it may lead to increased noise or improper operation of the IC.

(d) Since the FB line connected to the FB pin is highly susceptible to noise, please keep the wiring as short as possible. If the FB line is long, the IC may not operate normally due to switching noise and external noise.
In addition, parasitic capacitance may increase due to copper planes or parallel traces located directly beneath the FB line.
This increase in parasitic capacitance can weaken the phase compensation effect provided by CFB, potentially leading to unstable output.
If the IC does not operate properly due to external noise, please consider revising the PCB layout or lowering the FB resistor value.
Note that reducing the FB resistor value may decrease efficiency during PFM operation, so be sure to verify thoroughly with actual equipment.

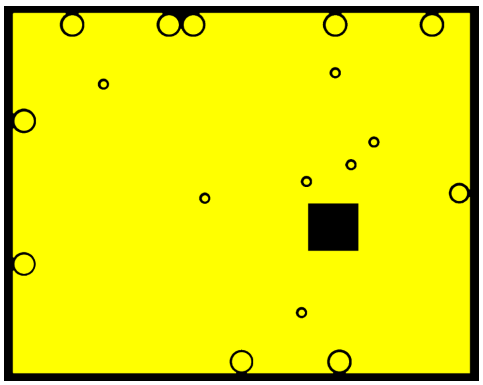
<Pattern layout>

DFN3030-12A

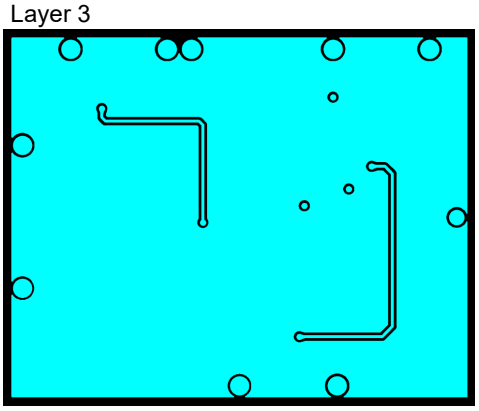
Layer 1



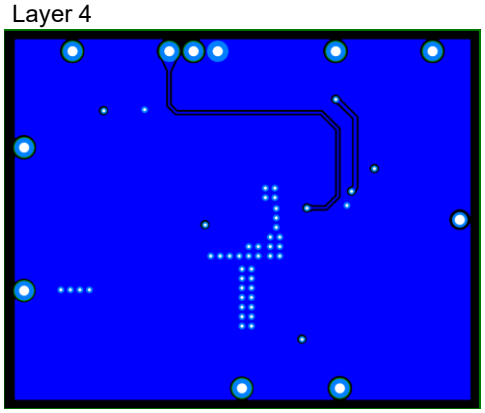
Layer 2



Layer 3

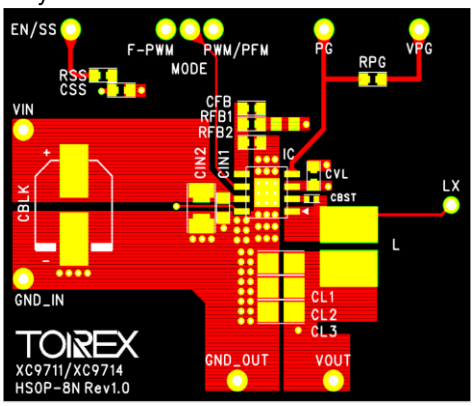


Layer 4

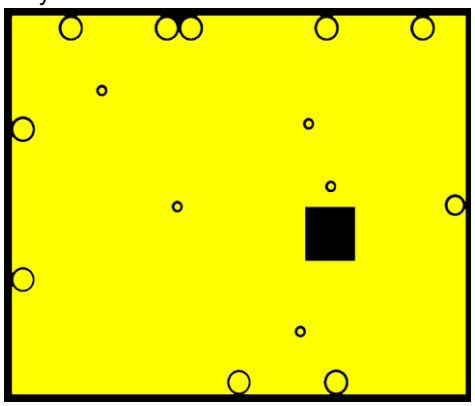


HSOP-8N

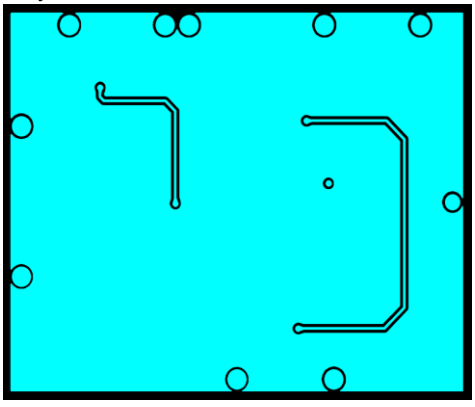
Layer 1



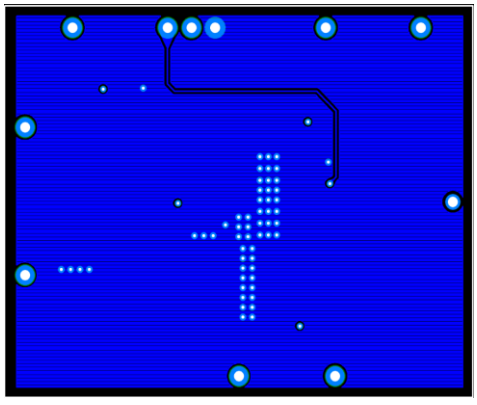
Layer 2



Layer 3



Layer 4



■PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS
DFN3030-12A	DFN3030-12A PKG	DFN3030-12A Power Dissipation
HSOP-8N	HSOP-8N PKG	HSOP-8N Power Dissipation

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.

2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.

3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.

4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions. Do not use the product for the above use unless agreed by us in writing in advance.

5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless, Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.

6. Our products are not designed to be Radiation-resistant.

7. Please use the product listed in this datasheet within the specified ranges.

8. We assume no responsibility for damage or loss due to abnormal use.

9.

TOREX SEMICONDUCTOR LTD.