MP27942

150Mbps, Six-Channel Digital Isolator with 4 Forward Channels and 2 Reverse Channels

DESCRIPTION

The MP27942 is a six-channel digital isolator that replaces a traditional optocoupler isolator in applications. It can support up to 150Mbps of data rate signal isolation.

The MP27942 employs capacitive isolation technology to provide up to $5kV_{RMS}$ of insulation voltage. The device offers a compact solution, with low power consumption and improved reliability compared to traditional optocoupler isolators.

A Schmitt trigger input and isolated encoding/decoding are provided for high immunity in noisy environments. The selectable high/low failsafe output supports a fixed output, even if the input signal power fails.

The MP27942 is available in an SOIC-16 wide-body (WB) package.

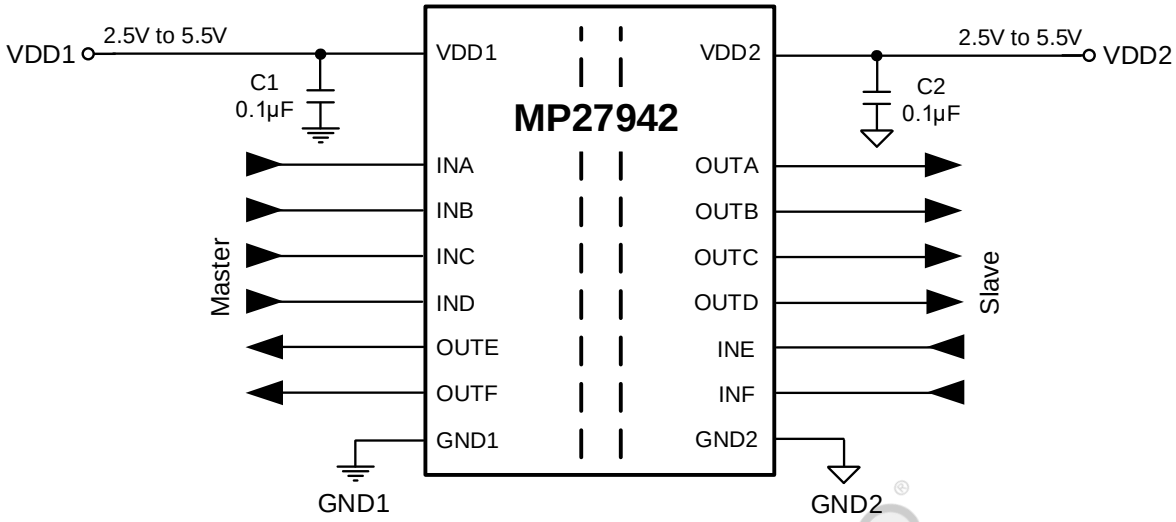
FEATURES

- Channel Direction: 4 Forward, 2 Reverse
- $5kV_{RMS}$ Isolation Voltage
- Supports 0Mbps (DC) to 150Mbps Data Rate
- 2.5V to 5.5V Operating Range
- >±100kV/μs Common-Mode Transient Immunity (CMTI)
- High System Level ESD, EFT, and Surge Immunity Performance
- 13ns Propagation Delay for 5V Operation
- Ultra-Low Power Supply Current
- Default Output Logic High (MP27942) and Low (MP27942-L) options
- 1.2kV Maximum Working Isolation Voltage (V_{IORM})
- Wide -40°C to +125°C Temperature Range
- Available in an SOIC-16 Wide-Body (WB) Package
- UL 1577 Fifth Edition Certified:
  - SOIC-16 WB: $5000V_{RMS}$ Isolation for 1 Minute
- CSA Component Notice 5A Approval:
  - SOIC-16 WB: $5000V_{RMS}$ Isolation for 1 Minute
- DIN EN IEC 60747-17 (VDE 0884-17): 2021-10 Certified:
  - SOIC-16 WB: $7071V_{PK}$ Isolation
- CQC Certification per GB 4943.1-2022
- CB Certification per IEC62368-1 Third Edition

APPLICATIONS

- Power Meters
- Programmable Logic Controllers (PLCs)
- Server Power
- Motor Controllers and Drivers
- Switches
- Solar Inverters
- Medical Equipment

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Output Default	Package	Top Marking	MSL Rating
MP27942GY	High	SOIC-16 WB	*See Below*	3
MP27942-LGY	Low			

* For Tape & Reel, add suffix -Z (e.g. MP27942GY-Z).

TOP MARKING (MP27942GY)

(SOIC-16 WB, Default High)

MPSYYWW
MP27942
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP27942: Part number
LLLLLLLLL: Lot number

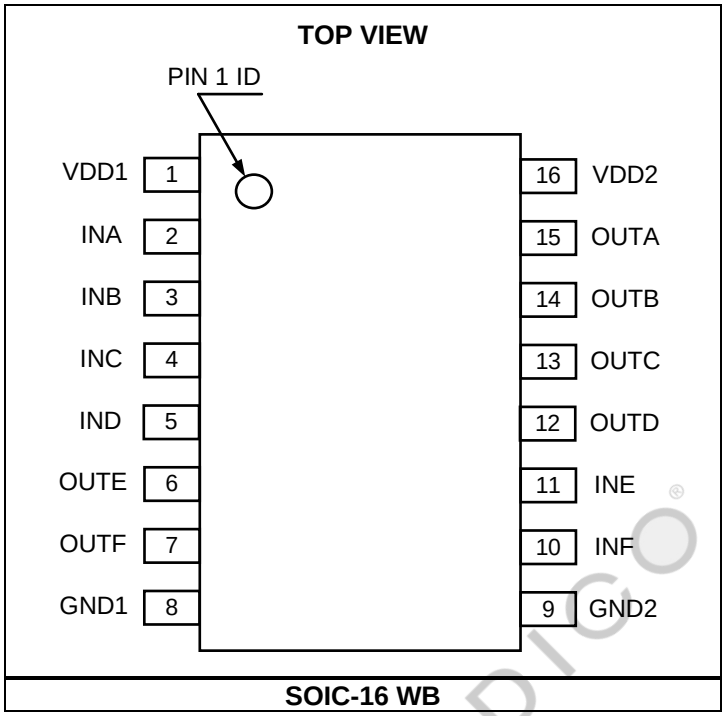
TOP MARKING (MP27942-LGY)

(SOIC-16 WB, Default Low)

MPS YYWW
MP27942-L
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP27942-L: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



SOIC-16 WB

PIN FUNCTIONS

Pin #	Name	Description
1	VDD1	**Side 1 power supply pin.** It is recommended to connect a 0.1μF decoupling capacitor between the VDD1 and GND1 pins.
2	INA	**Channel A input pin.**
3	INB	**Channel B input pin.**
4	INC	**Channel C input pin.**
5	IND	**Channel D input pin.**
6	OUTE	**Channel E output pin.**
7	OUTF	**Channel F output pin.**
8	GND1	**Side 1 ground pin.**
9	GND2	**Side 2 ground pin.**
10	INF	**Channel F input pin.**
11	INE	**Channel E input pin.**
12	OUTD	**Channel D output pin.**
13	OUTC	**Channel C output pin.**
14	OUTB	**Channel B output pin.**
15	OUTA	**Channel A output pin.**
16	VDD2	**Side 2 power supply pin.** It is recommended to connect a 0.1μF decoupling capacitor between the VDD2 and GND2 pins.

ABSOLUTE MAXIMUM RATINGS (1)

VDD1 to GND1, VDD2 to GND2……..
……...-0.3V to +6.5V
Side 1 other pins to GND1……..
……-0.3V to VDD1 + 0.3V (2)
Side 2 other pins to GND2……..
……..….-0.3V to VDD2 + 0.3V (2)
Average output current per pin .....
……...-10mA to +10mA
Common-mode transient immunity……
.....-100kV/μs to +100kV/μs
Continuous power dissipation (T_A = 25°C) (3) (5)
SOIC-16 WB 2.2W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM).....±6000V
Charged-device model (CDM).....±2000V
Isolation barrier withstand with HBM…….±8000V

Recommended Operating Conditions (4)

Supply voltage (V_{DD1}, V_{DD2}) .....2.5V to 5.5V
Maximum signal data rate……
……..0Mbps (DC) to 150Mbps
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

SOIC-16 WB		
EV27942-Y-00A (5)	56.8	21.3 °C/W
JESD51-7 (6)	75	48.7 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum voltage must not exceed 6.5V.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on the EV27942-Y-00A, a 2-layer PCB (51mmx51mm).
6) The θ_{JA} value given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{DD1} = V_{DD2} = 5V, T_J = -40°C to +125°C [7], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switching Timing Characteristics						
Minimum pulse width [8]	t_{MP}				5	ns
Propagation delay from low to high [11]	t_{PLH}			13	21	ns
Propagation delay from high to low [11]	t_{PHL}			13	21	ns
Pulse width distortion	PWD	$\|t_{PLH} - t_{PHL}\|$		1.5	5.5	ns
Propagation delay skew [9]	$t_{PSK(P-P)}$				4.5	ns
Channel-to-channel skew	t_{PS}	For both same and opposing directions		1	5	ns
Output rising time [11]	t_R	C_L = 15pF		2.5		ns
Output falling time [11]	t_F	C_L = 15pF		2.5		ns
Peak eye diagram jitter [10]	t_{JIT_PK}			1.5		ns
Input power failure to valid default output [11]	t_{SD}			500		ns
Start-up time [11]	t_{START}	From V_{DD1} or V_{DD2} on to valid output		80	105	µs
Common-mode transient immunity [10] [11]	CMTI	IN = 0V or V_{DD}, V_{CM} = 1.5kV	±100			kV/µs
Power Supply Range						
Supply voltage range	V_{DD1}		2.5		5.5	V
	V_{DD2}		2.5		5.5	V
Under-voltage lockout (UVLO) threshold	V_{UVLO1_R}	V_{DD1} rising	2.05	2.25	2.4	V
	V_{UVLO2_R}	V_{DD2} rising	2.05	2.25	2.4	V
UVLO threshold hysteresis	V_{UVLO_HYS1}	V_{DD1}		125		mV
	V_{UVLO_HYS2}	V_{DD2}		125		mV
Pin Input/Output Logic Threshold						
Input high voltage	V_{IH}	INx pins	2			V
Input low voltage	V_{IL}				0.8	V
Pin input current leakage	I_L	Connect INx to VDDx or GNDx			±15	µA
Output high voltage	V_{OUT_H}	OUTx pins, I_{OUT} = -4mA	V_{DDx} - 0.4	V_{DDx} - 0.2		V
Output low voltage	V_{OUT_L}	OUTx pins, I_{OUT} = 4mA		0.2	0.4	V
Output impedance [12]	Z_{OUT}	OUTx pins		50		Ω
Thermal Protection						
Thermal shutdown temperature [10]	T_{SD}			150		°C
Thermal shutdown hysteresis [10]	T_{HYS}			20		°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD1} = V_{DD2} = 5V, T_J = -40°C to +125°C [7], typical values are tested at T_J = 25°C, unless otherwise noted.

Part Number	Parameter	Condition	Min	Typ	Max	Units
Power Supply Current						
DC Supply Current (INA/B/C/D/E/F= 0V or V_{DD})						
MP27942	VDD1 current	INx = V_{DD}		5	7.5	mA
		INx = 0V		12.2	18.3	mA
	VDD2 current	INx = V_{DD}		7	10.5	mA
		INx = 0V		10.6	15.9	mA
MP27942-L	VDD1 current	INx = V_{DD}		12.2	18.3	mA
		INx = 0V		5	7.5	mA
	VDD2 current	INx = V_{DD}		10.6	15.9	mA
		INx = 0V		7	10.5	mA
1Mbps Supply Current (INA/B/C/D/E/F = 500kHz Square Wave, C_{LOAD} = 15pF on All Outputs)						
MP27942, MP27942-L	VDD1 current			6.6	13.1	mA
	VDD2 current			7.7	13.5	mA
10Mbps Supply Current (INA/B/C/D/E/F = 5MHz Square Wave, C_{LOAD} = 15 pF on All Outputs)						
MP27942, MP27942-L	VDD1 current			7.7	14.4	mA
	VDD2 current			10.2	16.2	mA
100Mbps Supply Current (INA/B/C/D/E/F = 50MHz Square Wave, C_{LOAD} = 15 pF on All Outputs)						
MP27942, MP27942-L	VDD1 current			19	27.9	mA
	VDD2 current			34.9	47.5	mA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD1} = V_{DD2} = 3.3V, T_J = -40°C to +125°C [7], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switching Timing Characteristics						
Minimum pulse width [8]					5	ns
Propagation delay from low to high [11]	t_{PLH}			14	22	ns
Propagation delay from high to low [11]	t_{PHL}			14	22	ns
Pulse width distortion	PWD	$\|t_{PLH} - t_{PHL}\|$		1.5	5.5	ns
Propagation delay skew [9]	$t_{PSK(P-P)}$				4.5	ns
Channel-to-channel skew	t_{PS}	For both same and opposing directions		1	5	ns
Output rising time [11]	t_R	C_L = 15pF		3.5		ns
Output falling time [11]	t_F	C_L = 15pF		3.5		ns
Peak eye diagram jitter [10]	t_{JIT_PK}			1.5		ns
Input power failure to valid default output [11]	t_{SD}			500		ns
Start-up time [11]	t_{START}	From V_{DD1} or V_{DD2} on to valid output		80	105	µs
Common-mode transient immunity [10] [11]	CMTI	IN = 0V or V_{DD}, V_{CM} = 1.5kV	±100			kV/µs
Power Supply Range						
Supply voltage range	V_{DD1}		2.5		5.5	V
	V_{DD2}		2.5		5.5	V
UVLO threshold	V_{UVLO1_R}	V_{DD1} rising	2.05	2.25	2.4	V
	V_{UVLO2_R}	V_{DD2} rising	2.05	2.25	2.4	V
UVLO threshold hysteresis	V_{UVLO_HYS1}	V_{DD1}		125		mV
	V_{UVLO_HYS2}	V_{DD2}		125		mV
Pin Input/Output Logic Threshold						
Input high voltage	V_{IH}	INx	2			V
Input low voltage	V_{IL}				0.8	V
Pin input current leakage	I_L	Connect INx to VDDx or GNDx			±15	µA
Output high voltage	V_{OUT_H}	OUTx pins, I_{OUT} = -4mA	V_{DDx} - 0.4	V_{DDx} - 0.2		V
Output low voltage	V_{OUT_L}	OUTx pins, I_{OUT} = 4mA		0.2	0.4	V
Output impedance [12]	Z_{OUT}	OUTx pins		50		Ω
Thermal Protection						
Thermal shutdown temperature [10]	T_{SD}			150		°C
Thermal shutdown hysteresis [10]	T_{HYS}			20		°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD1} = V_{DD2} = 3.3V, T_J = -40°C to +125°C [7], typical values are tested at T_J = 25°C, unless otherwise noted.

Part Number	Parameter	Condition	Min	Typ	Max	Units
Power Supply Current						
DC Supply Current (INA/B/C/D/E/F= 0V or V_{DD})						
MP27942	VDD1 current	INx = V_{DD}		5	7.5	mA
		INx = 0V		12.2	18.3	mA
	VDD2 current	INx = V_{DD}		7	10.5	mA
		INx = 0V		10.6	15.9	mA
MP27942-L	VDD1 current	INx = V_{DD}		12.2	18.3	mA
		INx = 0V		5	7.5	mA
	VDD2 current	INx = V_{DD}		10.6	15.9	mA
		INx = 0V		7	10.5	mA
1Mbps Supply Current (INA/B/C/D/E/F = 500kHz Square Wave, C_{LOAD} = 15pF on All Outputs)						
MP27942, MP27942-L	VDD1 current			6.5	13	mA
	VDD2 current			7.5	13.4	mA
10Mbps Supply Current (INA/B/C/D/E/F = 5MHz Square Wave, C_{LOAD} = 15pF on All Outputs)						
MP27942, MP27942-L	VDD1 current			7.2	14.1	mA
	VDD2 current			9.1	15.7	mA
100Mbps Supply Current (INA/B/C/D/E/F = 50MHz Square Wave, C_{LOAD} = 15pF on All Outputs)						
MP27942, MP27942-L	VDD1 current			15.1	25.2	mA
	VDD2 current			25.5	37.8	mA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD1} = V_{DD2} = 2.5V, T_J = -40°C to +125°C [7], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switching Timing Characteristics						
Minimum pulse width [8]	t_{MP}				5	ns
Propagation delay from low to high [11]	t_{PLH}			15	23	ns
Propagation delay from high to low [11]	t_{PHL}			15	23	ns
Pulse width distortion	PWD	$\|t_{PLH} - t_{PHL}\|$		1.5	5.5	ns
Propagation delay skew [9]	$t_{PSK(P-P)}$				4.5	ns
Channel-to-channel skew	t_{PS}	For both same and opposing directions		1	5	ns
Output rising time [11]	t_R	C_L = 15pF		4.5		ns
Output falling time [11]	t_F	C_L = 15pF		4.5		ns
Peak eye diagram jitter [10]	t_{JIT_PK}			1.5		ns
Input power failure to valid default output [11]	t_{SD}			500		ns
Start-up time [11]	t_{START}	From V_{DD1} or V_{DD2} on to valid output		80	105	µs
Common-mode transient immunity [10] [11]	CMTI	IN = 0V or V_{DD}, V_{CM} = 1.5kV	±100			kV/µs
Power Supply Range						
Supply voltage range	V_{DD1}		2.5		5.5	V
	V_{DD2}		2.5		5.5	V
UVLO threshold	V_{UVLO1_R}	V_{DD1} rising	2.05	2.25	2.4	V
	V_{UVLO2_R}	V_{DD2} rising	2.05	2.25	2.4	V
UVLO threshold hysteresis	V_{UVLO_HYS1}	V_{DD1}		125		mV
	V_{UVLO_HYS2}	V_{DD2}		125		mV
Pin Input/Output Logic Threshold						
Input high voltage	V_{IH}	INx	2			V
Input low voltage	V_{IL}				0.8	V
Pin input current leakage	I_L	Connect INx to VDDx or GNDx			±15	µA
Output high voltage	V_{OUT_H}	OUTx pins, I_{OUT} = -4mA	V_{DDx} - 0.4	V_{DDx} - 0.2		V
Output low voltage	V_{OUT_L}	OUTx pins, I_{OUT} = 4mA		0.2	0.4	V
Output impedance [12]	Z_{OUT}	OUTx pins		50		Ω
Thermal Protection						
Thermal shutdown temperature [10]	T_{SD}			150		°C
Thermal shutdown hysteresis [10]	T_{HYS}			20		°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD1} = V_{DD2} = 2.5V, T_J = -40°C to +125°C (7), typical values are tested at T_J = 25°C, unless otherwise noted.

Part Number	Parameter	Condition	Min	Typ	Max	Units
Power Supply Current						
DC Supply Current (INA/B/C/D/E/F= 0V or V_{DD})						
MP27942	VDD1 current	INx = V_{DD}		5	7.5	mA
		INx = 0V		12.2	18.3	mA
	VDD2 current	INx = V_{DD}		7	10.5	mA
		INx = 0V		10.6	15.9	mA
MP27942-L	VDD1 current	INx = V_{DD}		12.2	18.3	mA
		INx = 0V		5	7.5	mA
	VDD2 current	INx = V_{DD}		10.6	15.9	mA
		INx = 0V		7	10.5	mA
1Mbps Supply Current (INA/B/C/D/E/F = 500kHz Square Wave, C_{LOAD} = 15pF on All Outputs)						
MP27942, MP27942-L	VDD1 current			6.4	13	mA
	VDD2 current			7.4	13.4	mA
10Mbps Supply Current (INA/B/C/D/E/F = 5MHz Square Wave, C_{LOAD} = 15pF on All Outputs)						
MP27942, MP27942-L	VDD1 current			7.0	13.8	mA
	VDD2 current			8.6	15	mA
100Mbps Supply Current (INA/B/C/D/E/F = 50MHz Square Wave, C_{LOAD} = 15pF on All Outputs)						
MP27942, MP27942-L	VDD1 current			13.4	21.9	mA
	VDD2 current			19.3	31.2	mA

Notes:

7) Not tested in production. Derived by over-temperature correlation.
8) Derived by go/no-go test.
9) $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltage, load, and ambient temperature.
10) Derived by sample characterization. Not tested in production.
11) See Figure 4 and Figure 5 on page 20, and Figure 6 on page 21 for more details.
12) The nominal output impedance of an isolator driver channel is approximately 50Ω ±40%, which is a sum of the value of the on-chip series termination resistor and the output driver FET's channel resistance. When driving loads where transmission line effects may be a factor, ensure that the output pins are appropriately terminated with controlled-impedance PCB traces.

REGULATORY INFORMATION

UL	CSA	VDE (IEC)	CQC
Certified according to UL1577 Component Recognition Program	Certified according to CSA Component Acceptance Service Notice No.5A	Certified according to DIN EN IEC 60747-17 (VDE 0884-17): 2021-10; EN IEC 60747-17: 2020 + AC: 2021	Certified according to GB 4943.1-2022
SOIC-16 WB package: single protection, $5000V_{RMS}$ (13)	SOIC-16 WB package: single protection, $5000V_{RMS}$ (13)	Basic isolation: • Maximum transient isolation voltage: $7071V_{PK}$ • Maximum repetitive peak isolation voltage: 1200 V_{PK} • Maximum surge isolation voltage: $3077V_{PK}$	Altitude ≤ 5000m, tropical climate: • Reinforced insulation: $600V_{RMS}$ maximum working voltage • Basic insulation: $1000V_{RMS}$ maximum working voltage
File (E322138)	File (E322138)	File (40055422)	File (CQC22001348724)

Note:

13) The regulatory certification applies to $5000V_{RMS}$ rated devices that are production tested to $6000V_{RMS}$ for 1s.

INSULATION SPECIFICATIONS

Parameter	Symbol	Condition	SOIC-16 WB	Units
External clearance (14)	CLR	According to IEC 60664-1 (VDE 0110-1): shortest pin-to-pin distance through the air between the primary and secondary sides	>8	mm
External creepage (14)	CPG	According to IEC 60664-1 (VDE 0110-1): shortest pin-to-pin distance across the package surface between the primary and secondary sides	>8	mm
Minimum internal gap	DTI	Internal clearance	>20	µm
Tracking resistance (comparative tracking index)	CTI	According to IEC 60112	>600	V_{RMS}
Material group	-	According to IEC 60664-1	I	-
Over-voltage category per IEC 60664-1	-	Rated mains voltages ≤ $150V_{RMS}$	I-IV	-
		Rated mains voltages ≤ $300V_{RMS}$	I-IV	-
		Rated mains voltages ≤ $600V_{RMS}$	I-III	-

Note:

14) See the Package Information section on page 24 for more detailed dimensions. For isolated solutions, the recommended land pattern is used to maintain sufficient safety creepage and clearance distances on the PCB.

INSULATION CHARACTERISTICS

Parameter	Symbol	Condition	SOIC-16 WB	Units
UL 1577, Fifth Edition				
Isolation voltage rating	V_{ISO}	Refer to V_{RMS} Qualification test: V_{TEST} = V_{ISO}, t = 60s 100% production test: V_{TEST} = V_{ISO} x 1.2, t = 1s *(100% Production Test)*	5000	V
DIN EN IEC 60747-17 (VDE 0884-17): 2021-10 (17)				
Maximum working isolation voltage	V_{IORM}	Refer to V_{PEAK}	1200	V
Apparent charge (15)	Q_{PD}	Method B1 (routine test): 100% production test: $V_{PD(M)}$ = 1.875 x V_{IORM}, t_M = 1s	<5	pC
		Qualification test: Method A, after sample test and sub-group 1: $V_{PD(M)}$ = V_{IORM} x 1.3, t_M = 10s After type test sub-group 2/3: $V_{PD(M)}$ = V_{IORM} x 1.2, t_M = 10s	<5	pC
Transient over-voltage	V_{IOTM}	Refer to V_{PEAK} Qualification test: V_{TEST} = V_{IOTM} for t = 60s *(Qualification Test)* 100% production test: V_{TEST} = V_{IOTM} x 1.2 for t = 1s	7071	V
Maximum surge isolation voltage	V_{IOSM}	Refer to V_{PEAK} Qualification test, tested with surge waveform 1.2µs/50µs, V_{TEST} = V_{ISOM} x 1.3	3077	V
Barrier capacitance (16)	C_{IO}	Test frequency = 1MHz	2	pF
Insulation resistance (16)	R_{IO}	V_{IO} = 500V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	Ω
		V_{IO} = 500V, T_A = T_S = 150°C	$>10^{9}$	Ω
Pollution degree			2	
Climatic category			40/125/21	

Notes:

15) Electrical discharge caused by a partial discharge in the coupler.
16) The primary-side terminals, as well as the secondary-side terminals of the barrier, are connected together, forming a two-terminal device. Then C_{IO} and R_{IO} are measured between the two terminals of the coupler.
17) This coupler is suitable for basic electrical insulation only within the maximum operating ratings. Compliance with the safety ratings are ensured by means of suitable protective circuits.

SAFETY LIMITING VALUES (18)

Parameter	Symbol	Condition	SOIC-16 WB	Units
Maximum safety temperature (19)	T_S		150	°C
Safety input, output, or supply current	I_S	V_{DD} = 5.5V, T_J = 150°C, T_A = 25°C	400	mA
Safety input, output, or total power (20)	P_S	T_J = 150°C, T_A = 25°C	2200	mW

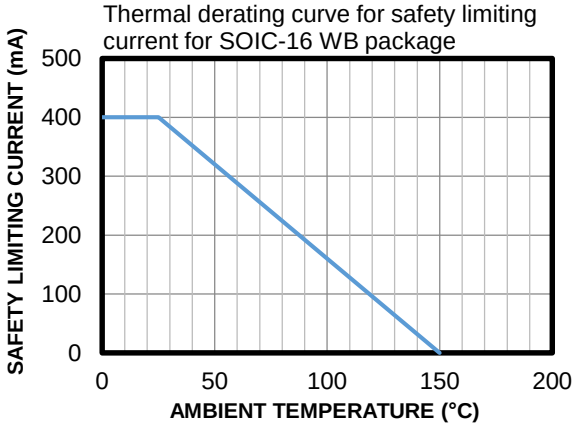
Notes:

18) These are the maximum values allowed in the event of a failure.
19) The maximum safety temperature (T_S) has the same value as the maximum junction temperature, T_J (MAX), specified in the Absolute Maximum Ratings section on page 6.
20) The safety power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A: T_S = T_J (MAX) = T_A + (θ_{JA} x P_S).

THERMAL DERATING CURVE FOR SAFETY LIMITING VALUES

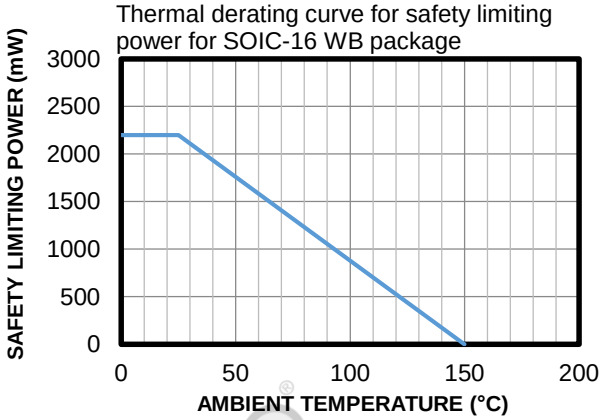
Safety Limiting Current vs. Ambient Temperature

Thermal derating curve for safety limiting current for SOIC-16 WB package



Safety Limiting Power vs. Ambient Temperature

Thermal derating curve for safety limiting power for SOIC-16 WB package

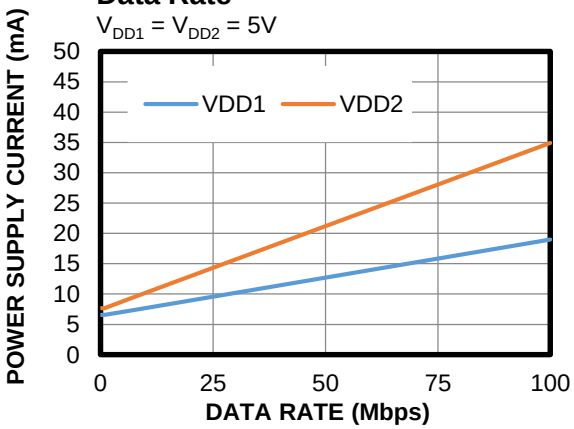


TYPICAL CHARACTERISTICS

V_{DD1} = V_{DD2} = 5V, INA, INB, INC, IND, INE and INF = 5MHz square waveform, T_A = 25°C, unless otherwise noted.

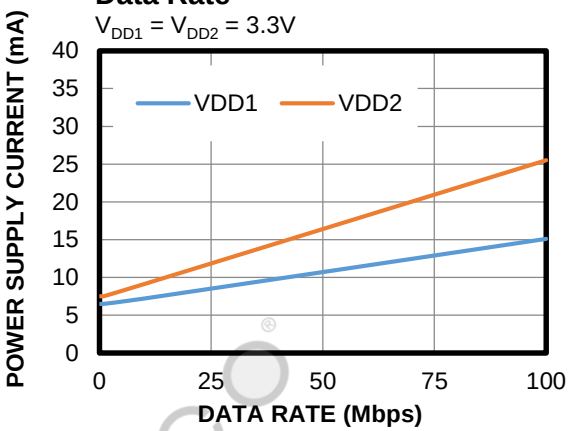
Power Supply Current vs. Data Rate

V_{DD1} = V_{DD2} = 5V



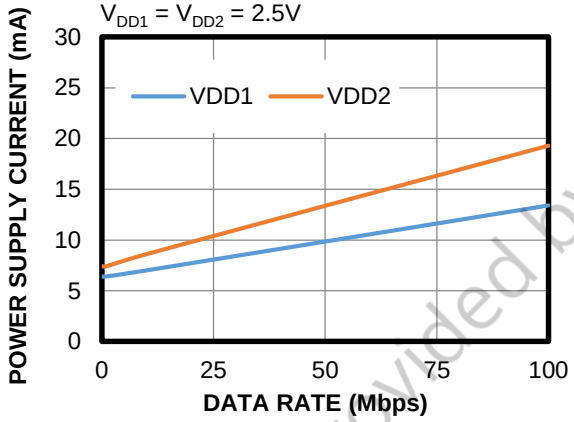
Power Supply Current vs. Data Rate

V_{DD1} = V_{DD2} = 3.3V



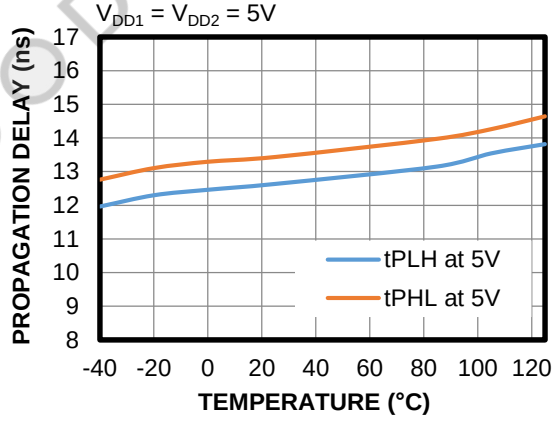
Power Supply Current vs. Data Rate

V_{DD1} = V_{DD2} = 2.5V



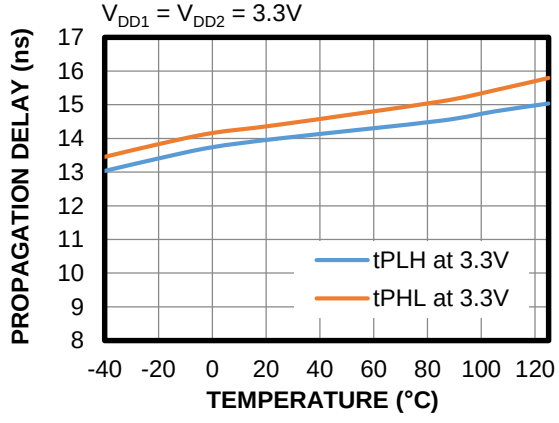
Propagation Delay vs. Temperature

V_{DD1} = V_{DD2} = 5V



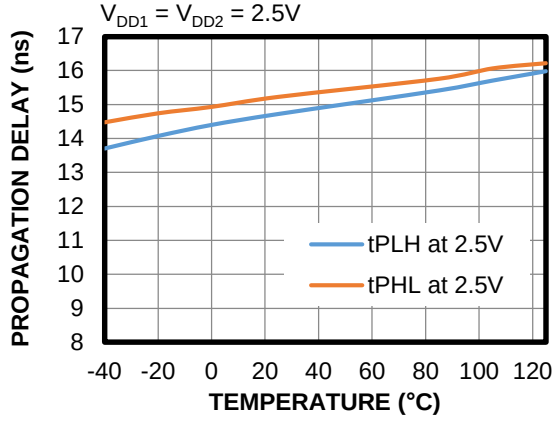
Propagation Delay vs. Temperature

V_{DD1} = V_{DD2} = 3.3V



Propagation Delay vs. Temperature

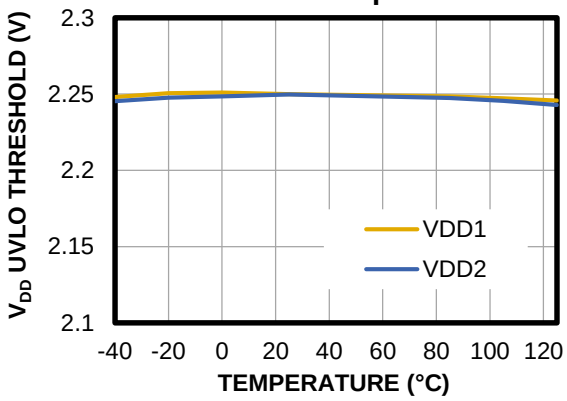
V_{DD1} = V_{DD2} = 2.5V



TYPICAL CHARACTERISTICS *(continued)*

V_{DD1} = V_{DD2} = 5V, INA, INB, INC, IND, INE and INF = 5MHz square waveform, T_A = 25°C, unless otherwise noted.

V_{DD} Under-Voltage Lockout Threshold vs. Temperature



FUNCTIONAL BLOCK DIAGRAM

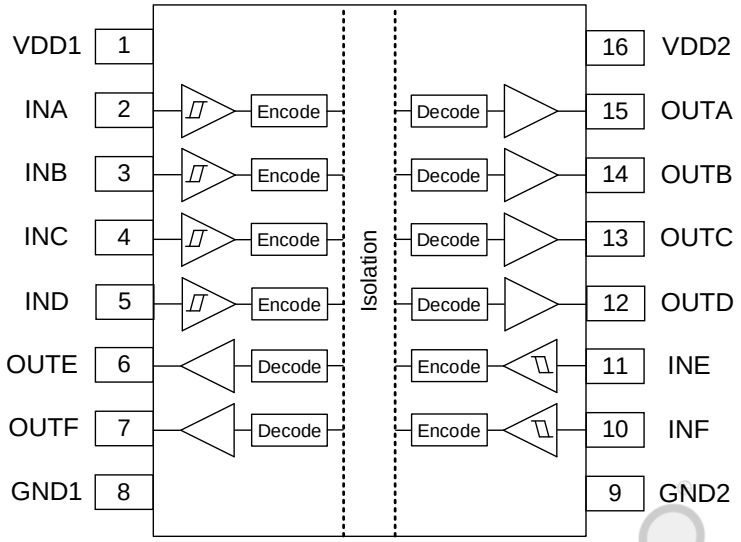


Figure 1: Functional Block Diagram

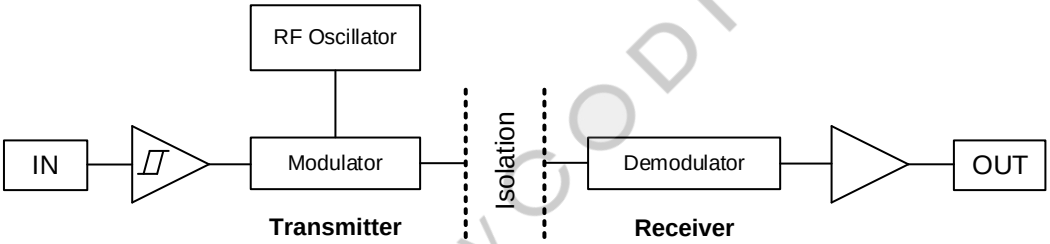


Figure 2: Isolated Signal Modulation Diagram

OUTPUT TRUTH TABLE

Table 1: Truth Table (21)

Input Side VDD	Output Side VDD	IN	OUT
Normal Working State			
Powered	Powered	High	High
Powered	Powered	Low	Low
Powered	Powered	Floating	High for MP27942, Low for MP27942-L
VDD Off State			
Not powered (22)	Powered	x	High for MP27942, Low for MP27942-L
x	Not powered (22)	x	I

Notes:

21) For this table, Hi-Z = high impedance; x = not applicable; floating = not connected; I = indeterminate; High = high-level voltage; Low = low-level voltage.
22) An I/O can power the die for a given side through an internal diode if its source has adequate current.

OPERATION

The MP27942 is a six-channel digital isolator that replaces a traditional optocoupler isolator in applications. It adopts capacitive isolation technology, and can support up to a 5kV$_{RMS}$ insulation voltage rating and 150Mbps of data rate signal isolation.

Signal Isolation Function

The MP27942 supports a 5kV$_{RMS}$ voltage isolation between two sides. The data signals applied on the INx pins are transmitted to the corresponding OUTx pin through the internal isolation barrier. Figure 1 on page 18 shows the IC diagram, and Figure 2 on page 18 shows the isolated signal transmission structures.

Each signal channel consists of an RF transmitter and RF receiver, separated by a semiconductor-based isolation barrier. On the input port, the transmitter modulates the signal through an RF oscillator. When the input signal is high, the RF oscillator stays off. When the input signal is low, the RF oscillator stays on. On the receiver's side, a demodulator decodes the input state according to its RF energy content, and then applies the result to the output pin. This signal modulation provides low power consumption and improved immunity for the magnetic fields. Figure 3 shows the modulation scheme.

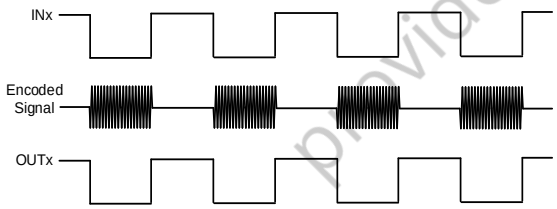


Figure 3: Signal Modulation Scheme

All channel signals have a Schmitt trigger input to enhance noise immunity. At the same time, all channels going in the same direction are optimized for propagation delay matching. This function can be used for serial peripheral interface (SPI) isolation, with an excellent channel-to-channel skew. Figure 4 shows the propagation delay time.

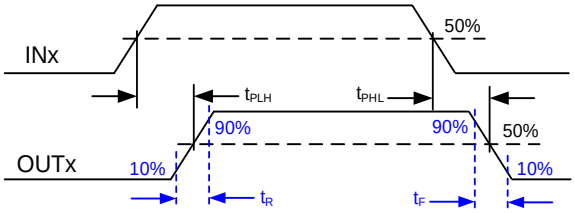


Figure 4: Propagation Delay Time

Fail-safe Operation

If an input power supply is not applied, then the MP27942's default output is high. If an input power supply is not applied, then the MP27942-L's default output is low.

By implementing a predetermined failsafe output, the device can ensure DC validity in the absence of input logic transitions. This means that the MP27942 can be used for SPI isolation, which prevents the slave device from being accidentally selected during a power failure status.

Power Supply

Both VDD1 and VDD2 have an under-voltage lockout (UVLO) function to prevent erroneous operation during device start-up and shutdown, or when the corresponding V_{DDx} is low.

The outputs stay at a high impedance during start-up until the corresponding V_{DDx} exceeds its UVLO threshold for the set time period (t_{START}). After this period, the outputs follow the state of the inputs. Figure 5 shows the UVLO delay function.

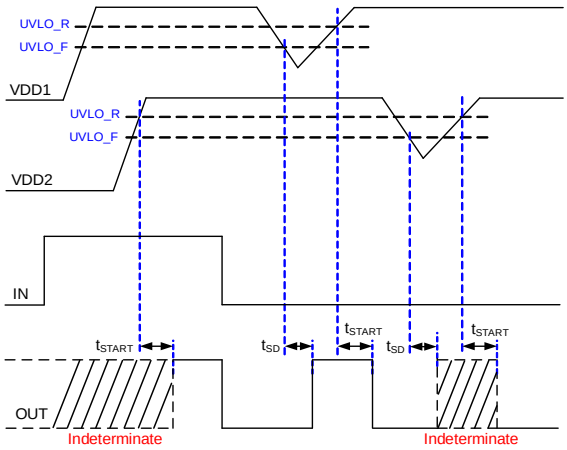


Figure 5: UVLO and Output Delay

Each side can enter or exit UVLO independently, even while the output states are different. For example, if VDD1 initiates UVLO, then the side 2 output stays high as long as VDD2 is on. If VDD2 initiates UVLO, the side 2 output enters a high impedance state, even if VDD1 is on. This feature can prevent outputs from incorrectly flipping during V_{DDx} start-up.

Output Short Protection

When the OUT pin outputs an overload or short to GND, an internal current-limit circuit prevents the current from running too high. In addition, if the die temperature rises too high due to the high current, the device triggers thermal protection.

Thermal Protection

The MP27942 has an over-temperature protection (OTP) function to protect the device from excessive power dissipation during fault conditions. The thermal protection circuit disables the driver outputs when a die temperature rises to 150°C. There is a hysteresis of about 20°C, meaning that the driver outputs are re-enabled and operate normally once the junction temperature drops to about 130°C.

Common-Mode Transient Immunity (CMTI)

Common-mode transient immunity (CMTI) is one of the key characteristics that determine an isolator's robustness. CMTI is especially important in high-voltage applications that utilize devices with a fast transient response.

When a power device is switching, the high slew rate dV/dt or dI/dt transient noise can corrupt the signal transmission across the isolation barrier (see Figure 6).

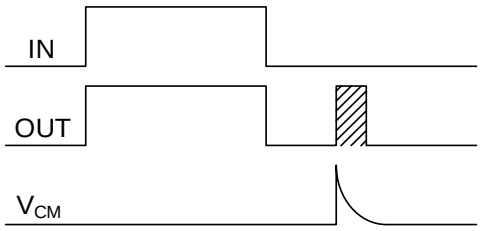


Figure 6: Common-Mode Transient Affects Transmission

CMTI is defined as the maximum tolerable rate of rising (or falling) for a common-mode voltage applied between two isolated circuits, most often in volts per second (V/ns or kV/µs). The isolator's output remains at the specified logic level and timing as long as the common-mode voltage remains below the maximum slew rate defined by CMTI.

Figure 7 shows the CMTI test set-up to measure the CMTI of a coupler under the specified common-mode pulse magnitude (V_{CM}), the specified slew rate for the common-mode pulse (dV_{CM}/dt), and other specified test or ambient conditions. The isolator's output should remain in the correct state as long as the pulse magnitude and the slew rate meet the relevant CMTI specifications.

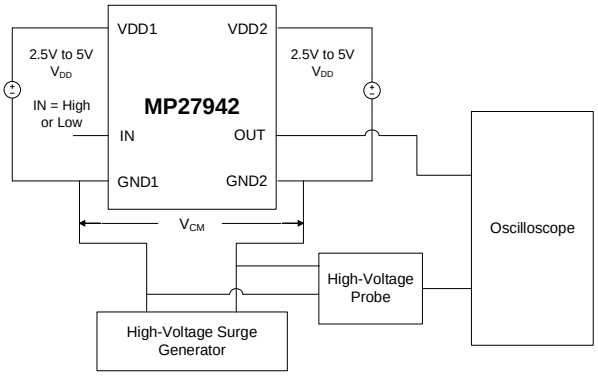


Figure 7: CMTI Test Circuit

APPLICATION INFORMATION

Bypass Capacitor

A 0.1µF capacitor is recommended to ensure reliable propagation. The bypass capacitor should be placed as close to power supply and ground pins as possible.

Design Example

Table 2 is a design example following the application guidelines for the specifications below.

Table 2: Design Example

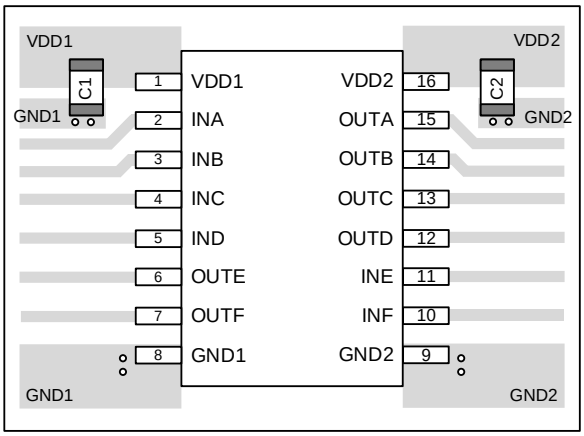
V_{DD1}	V_{DD2}
2.5V to 5.5V	2.5V to 5.5V

For the detailed application schematic, see Figure 9 on page 23. For more device applications, refer to the related evaluation board datasheet(s).

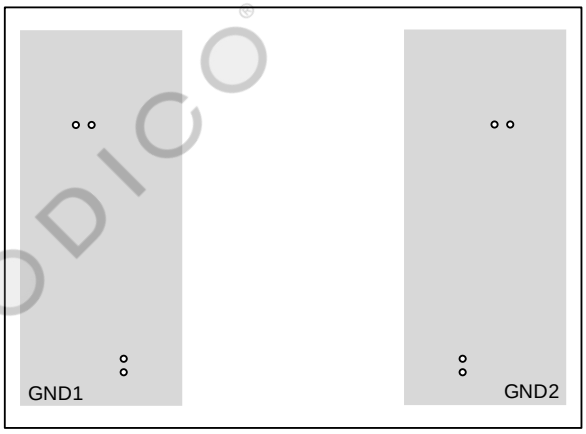
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 8 and follow the guidelines below:

1. The primary side and secondary side must be physically separated for safety reasons.
2. The creepage and clearance must meet the standards for the required application.
3. Minimize the loop area between signal traces and GND to avoid coupling noise in the system.
4. Route signal traces away from other high-speed traces or switching nodes, such as the transformer, power inductor, and MOSFET.
5. Place two ceramic input decoupling capacitors as close as possible to the VDD1 and GND1 pins, and VDD2 and GND2 pins.
6. Implement a 4-layer PCB for high-speed signals to improve EMI and signal propagation performance.
7. When stacking layers, stack in the following order: high-speed signal, solid GND plane, VDD plane, and low-frequency signal.



Top Layer



Bottom Layer

Figure 8: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

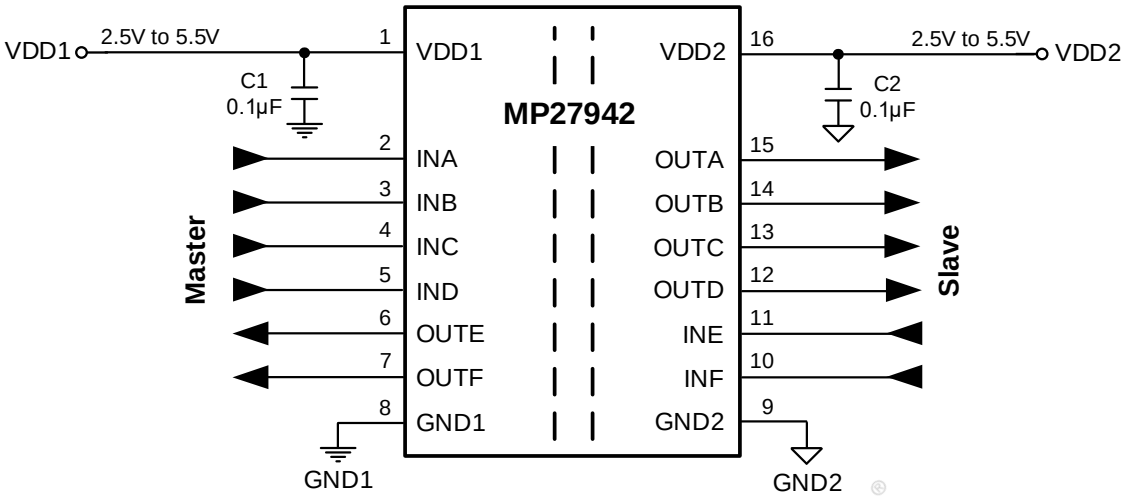
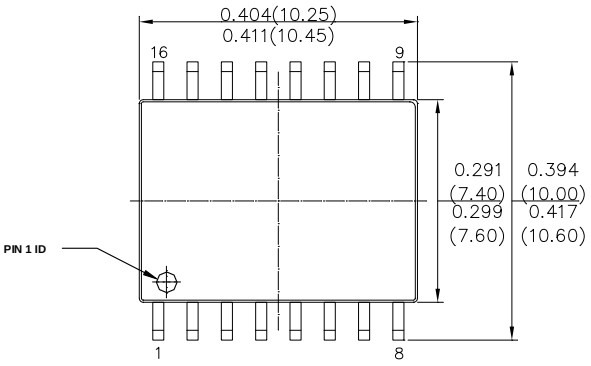


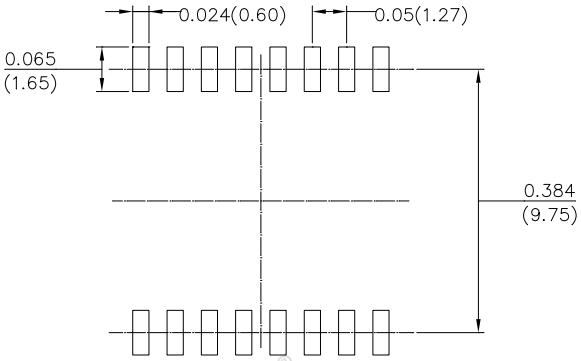
Figure 9: Typical Application Circuit (6 Channels, Channel Direction: 4 Forward and 2 Reverse, Isolated Interface)

PACKAGE INFORMATION

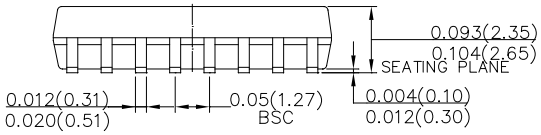
SOIC-16 WB (HV Isolation)



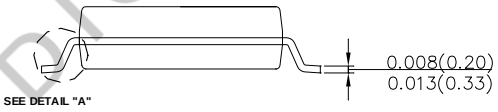
TOP VIEW



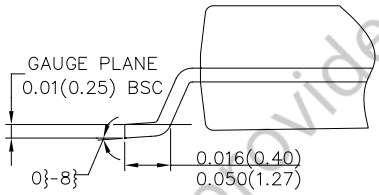
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

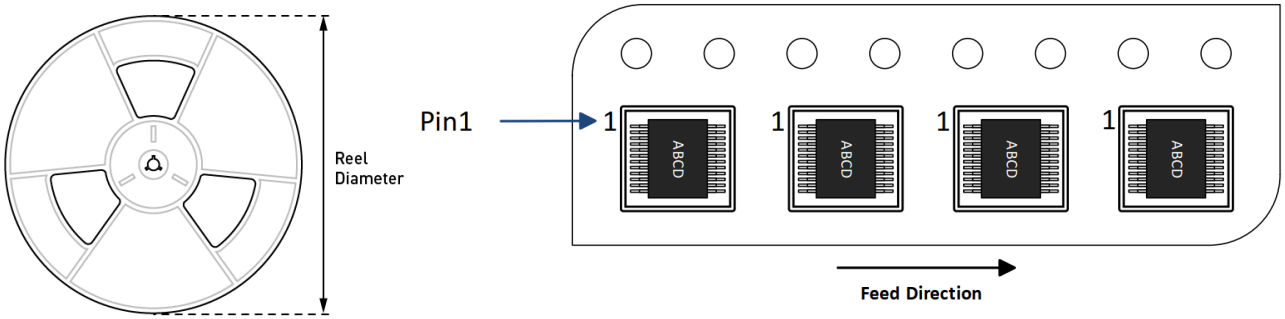


DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-013, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP27942GY-Z MP27942-LGY-Z	SOIC-16 WB	1000	N/A	N/A	13in	24mm	12mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/17/2023	Initial Release	-
1.01	10/3/2023	Updated Quantity/Tube to “N/A”	25