Datasheet

Nisshinbo Micro Devices Inc.

NL9620

Precision Low Power Instrumentation Amplifier

FEATURES

Gain Set with One External Resistor	
Gain Range	1 to 10,000
Low Input Offset Voltage	
T_a = 25°C	125μV max.
T_a = -40 to 85°C	185μV max.
Input Offset Voltage Drift	1μV/°C max.
Input Bias Current	2nA max.
Supply Current	0.9mA typ.
	1.3mA max.
Common-Mode Rejection Ratio	
(@G = 100)	110dB min.
Supply Voltage	±2.3V to ±18V
Integrated EMI filter	
Voltage Noise (f = 1kHz)	13nV/√Hz max.
-3dB Bandwidth (G = 100)	120kHz typ.
Slew Rate	0.75V/μs min.
Bipolar Architecture	
Operating Temperature (Specified)	-40°C to 85°C
Package	VSP-8-AF, EMP-8-AN

APPLICATIONS

Battery-powered Equipment
Sensor Interface
  Strain Gauge, Flow Meter, Pressure Sensor
Transducer Interface
Weigh Scales

GENERAL DESCRIPTION

The NL9620 is a high precision, low power instrumentation amplifier that requires only one external resistor to set gains of 1 to 10,000, and using bipolar process.

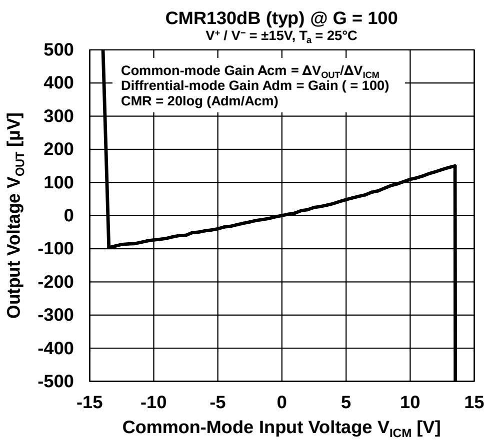
Characteristics such as low input offset voltage (125 μV max.), Low input offset voltage drift (1 μV/°C max.), High CMR (110 dB min. at G = 100), and low input bias current (2 nA max.) It is ideal for systems that required to sense signals from various sensors with high accuracy, such as transducer interfaces and weigh scales. It also has low supply current (1.3mA max.), which makes it ideal for battery-powered equipment applications.

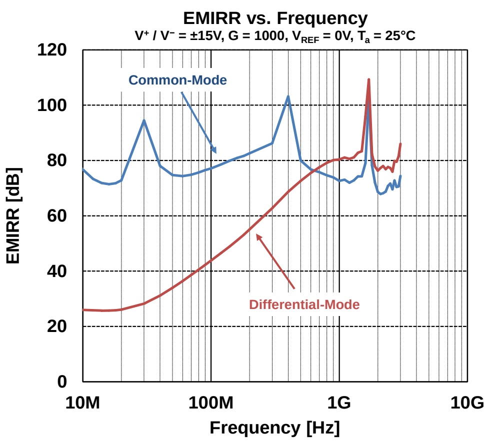
Since it has a built-in integrated EMI filter, it reduces malfunctions due to the influence of high frequencies such as mobile phones.

NL9620 is available in 8-pin VSP and EMP packages.

VSP-8-AF
2.9 x 4.0 x 1.1 (mm)

EMP-8-AN
5.0 x 6.0 x 1.5 (mm)





■ PRODUCT NAME INFORMATION

NL9620 aa A bb D

Description of configuration

Composition	Item	Description
aa	Package code	Indicates the package. AF: VSP-8-AF AN: EMP-8-AN
A	Version	Product version. A: Default
bb	Packing	E2: Insert Direction. Refer to the packing specifications.
D	Grade	Indicates the quality grade. D: Industrial

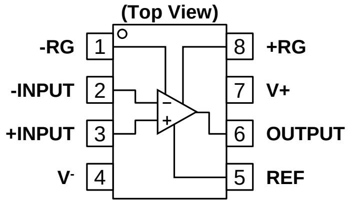
Grade

	Applications	Operating Temperature Range	Test Temperature
D	Industrial equipment and Social infrastructures	-40°C to 125°C	-40, 25°C, 85°C

■ ORDER INFORMATION

Product Name	Package	RoHS	Halogen-Free	Plating Composition	Weight (mg)	Quantity (pcs/reel)
NL9620AFAE2D	VSP-8-AF	✓	✓	Sn2Bi	21	2000
NL9620ANAE2D	EMP-8-AN	✓	✓	Sn2Bi	76	2000

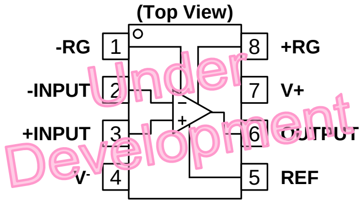
■ PIN DESCRIPTIONS (NL9620AF)



VSP-8-AF

Pin No.	Pin Name	I/O	Description
1	-RG	-	Gain setting pin. Place a gain resistor between pin 1 and pin 8.
2	−INPUT	I	Inverting input
3	+INPUT	I	Non-inverting input
4	V^-	-	Negative supply
5	REF	I	Reference input. This pin must be driven by low impedance.
6	OUTPUT	O	Output
7	V^+	-	Positive supply
8	+RG	-	Gain setting pin. Place a gain resistor between pin 1 and pin 8.

■ PIN DESCRIPTIONS (NL9620AN)



EMP-8-AN

Pin No.	Pin Name	I/O	Description
1	-RG	-	Gain setting pin. Place a gain resistor between pin 1 and pin 8.
2	−INPUT	I	Inverting input
3	+INPUT	I	Non-inverting input
4	V^-	-	Negative supply
5	REF	I	Reference input. This pin must be driven by low impedance.
6	OUTPUT	O	Output
7	V^+	-	Positive supply
8	+RG	-	Gain setting pin. Place a gain resistor between pin 1 and pin 8.

■ ABSOLUTE MAXIMUM RATINGS

	Symbol	Ratings	Unit
Supply Voltage	V^+ / V^-	±18	V
Input Voltage (+INPUT, −INPUT, REF) *1	V_{IN}	±18	V
Input Current *2	I_{IN}	±10	mA
Differential Input Voltage *3	V_{ID}	Gain ≤ 50 ; ±50/Gain *1 Gain > 50 ; ±1	V
Output Short-Circuit Duration *4		Continuous	
Storage Temperature	T_{stg}	-55 to 150	°C
Junction Temperature *5	T_j	150	°C

*1 For supply voltage less than ±18V, the absolute maximum rating is equal to the supply voltage.

*2 Input voltages outside the supply voltage will be clamped by ESD protection diodes. If the input voltage exceeds the supply voltage, the current must be limited 10 mA or less by µsing a restriction resistance. Input current inflow is positive and Input current outflow is negative.

*3 Differential voltage is the voltage difference between +INPUT and −INPUT.

*4 Power loss increases when output is short-circuited; do not exceed T_j.

*5 Calculate the power consumption of the IC from the operating conditions, and calculate the junction temperature with the thermal resistance.
Please refer to "Thermal characteristics" for the thermal resistance under our measurement board conditions.

ABSOLUTE MAXIMUM RATINGS
Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

■ THERMAL CHARACTERISTICS

Package	Measurement Result *1		Unit
	θja	ψjt	
VSP-8-AF	152	24	°C/W
EMP-8-AN	104	12	°C/W

θja: Junction-to-Ambient Thermal Resistance
ψjt: Junction-to-Top Thermal Characterization Parameter

*1 Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4), internal Cu area: 74.2 mm × 74.2 mm.

■ ELECTROSTATIC DISCHARGE (ESD) PROTECTION VOLTAGE

	Conditions	Protection Voltage
HBM	C = 100 pF, R = 1.5 kΩ	±2000V
CDM		±1000V

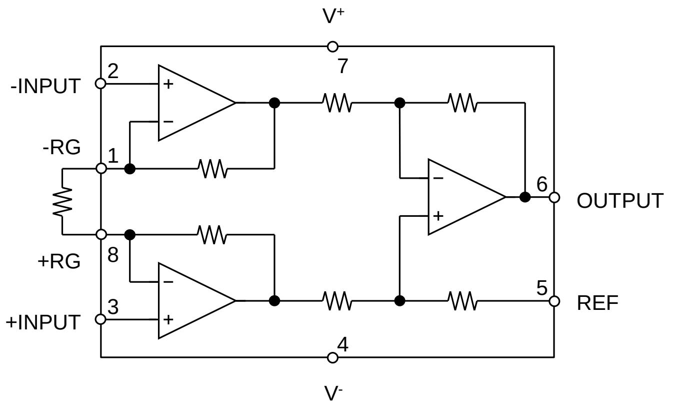
ELECTROSTATIC DISCHARGE RATINGS
The electrostatic discharge test is done based on JEDEC JS001 and JS002. In the HBM method, ESD is applied using the power supply pin and GND pin as reference pins.

■ RECOMMENDED OPERATING CONDITIONS

	Symbol	Ratings	Unit
Supply Voltage	V^+ / V^-	±2.3 to ±18	V
Operating Temperature Range	T_a	-40 to 85 (Specified) -40 to 125 (Operating)	°C

RECOMMENDED OPERATING CONDITIONS
All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

■ BLOCK DIAGRAM



■ ELECTRICAL CHARACTERISTICS

$V^+ / V^- = \pm15V$, $V_{REF}=0V$, $R_L = 5k\Omega$, $T_a = 25°C$, unless otherwise specified.

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Gain *1						
Gain Range			1	-	10,000	
Gain Error *2	G_{err}	$V_{OUT} = \pm10V$ G = 1 G = 10 G = 100 G = 1000	 - - - -	 0.03 0.15 0.15 0.40	 0.10 0.30 0.30 0.70	 % % % %
Nonlinearity	NL	V_{OUT} = -10 to 10V, $R_L = 10k\Omega$ G = 1-100 G = 1000 V_{OUT} = -10 to 10V, $R_L = 5k\Omega$ G = 1-100	 - - -	 10 40 10	 40 - 95	 ppm ppm ppm
Gain vs. Temperature	ΔG/ΔT	Ta = -40°C to 85°C G = 1 G > 1 *2	 - -	 - -	 10 50	 ppm/°C ppm/°C
Offset Voltage *3						
Input Offset Voltage	V_{OSI}	$V^+ / V^- = \pm5V$ to $\pm15V$ $V^+ / V^- = \pm5V$ to $\pm15V$, T_a = -40°C to 85°C	- -	30 -	125 185	µV µV
Input Offset Voltage Drift	$\Delta V_{OSI}/\Delta T$	$V^+ / V^- = \pm5V$ to $\pm15V$, T_a = -40°C to 85°C, VSP-8-AF $V^+ / V^- = \pm5V$ to $\pm15V$, T_a = -40°C to 85°C, EMP-8-AN	- -	0.3 0.3	1.3 1.0	µV/°C µV/°C
Output Offset Voltage	V_{OSO}	$V^+ / V^- = \pm15V$ $V^+ / V^- = \pm5V$ $V^+ / V^- = \pm5V$ to $\pm15V$, T_a = -40°C to 85°C	- - -	400 - -	1000 1500 2000	µV µV µV
Output Offset Voltage Drift	$\Delta V_{OSO}/\Delta T$	$V^+ / V^- = \pm5V$ to $\pm15V$, T_a = -40°C to 85°C	-	5	15	µV/°C
Supply Voltage Rejection Ratio	SVR	$V^+ / V^- = \pm2.3V$ to $\pm18V$ G = 1 G = 10 G = 100 G = 1000	 80 95 110 110	 100 120 140 140	 - - - -	 dB dB dB dB
Input Current						
Input Bias Current	I_B	T_a =25°C T_a = -40°C to 85°C	- -	0.5 -	2.0 2.5	nA nA
Input Bias Current Drift	$\Delta I_B/\Delta T$	T_a = -40°C to 85°C	-	3.0	-	pA/°C
Input Offset Current	I_{IO}	T_a =25°C T_a = -40°C to 85°C	- -	0.3 -	1.0 1.5	nA nA
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$	T_a = -40°C to 85°C	-	1.5	-	pA/°C

*1 $Gain = 1 + (49.4k\Omega/R_G)$

*2 Does not include effects of external resistor R_G.

*3 $Total\ RTI\ Error = V_{OSI} + V_{OSO}/G$

■ ELECTRICAL CHARACTERISTICS 2

$V^+ / V^- = \pm 15V$, V_{REF}=0V, R_L = 5kΩ, T_a = 25°C, unless otherwise specified.

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input						
Input Resistance	R_{IN}	Differential	-	60	-	GΩ
		Common-Mode	-	70	-	GΩ
Input Capacitance	C_{IN}	Differential	-	6	-	pF
		Common-Mode	-	2	-	pF
Input Voltage Range [*1]	V_{ICM}	$V^+ / V^- = \pm 2.3V$ to ±5V	V^- + 1.7	-	V^+ - 1.4	V
		$V^+ / V^- = \pm 2.3V$ to ±5V, T_a = -40°C to 85°C	V^- + 1.7	-	V^+ - 1.6	V
		$V^+ / V^- = \pm 5V$ to ±18V	V^- + 1.7	-	V^+ - 1.4	V
		$V^+ / V^- = \pm 5V$ to ±18V, T_a = -40°C to 85°C	V^- + 1.7	-	V^+ - 1.6	V
Common-Mode Rejection Ratio	CMR	DC with 1kΩ Source Imbalance, V_{CM} = 0V to ±10V				
		G = 1	73	90	-	dB
		G = 10	93	110	-	dB
		G = 100	110	130	-	dB
		G = 1000	110	130	-	dB
		f = 60Hz with 1kΩ Source Imbalance, V_{IN} = 20V_{PP}				
		G = 1	-	90	-	dB
		G = 10	-	110	-	dB
		G = 100	-	110	-	dB
		G = 1000	-	110	-	dB
Output						
High-level Output Voltage	V_{OH}	$V^+ / V^- = \pm 2.3V$ to ±5V, R_L = 10kΩ	-	-	V^+ - 1.2	V
		$V^+ / V^- = \pm 2.3V$ to ±5V, R_L = 10kΩ, T_a = -40°C to 85°C	-	-	V^+ - 1.3	V
		$V^+ / V^- = \pm 5V$ to ±18V, R_L = 10kΩ	-	-	V^+ - 1.4	V
		$V^+ / V^- = \pm 5V$ to ±18V, R_L = 10kΩ, T_a = -40°C to 85°C	-	-	V^+ - 1.5	V
Low-level Output Voltage	V_{OL}	$V^+ / V^- = \pm 2.3V$ to ±5V, R_L = 10kΩ	V^- + 1.1	-	-	V
		$V^+ / V^- = \pm 2.3V$ to ±5V, R_L = 10kΩ, T_a = -40°C to 85°C	V^- + 1.4	-	-	V
		$V^+ / V^- = \pm 5V$ to ±18V, R_L = 10kΩ	V^- + 1.2	-	-	V
		$V^+ / V^- = \pm 5V$ to ±18V, R_L = 10kΩ, T_a = -40°C to 85°C	V^- + 1.6	-	-	V
Output Short-Circuit Current	I_{SC}	Source	-	18	-	mA
		Sink	-	18	-	mA
Reference Input						
Input Resistance	$R_{IN (REF)}$		-	40	-	kΩ
Input Current	$I_{IN (REF)}$	G = 1, $V_{IN+} = V_{IN-} = V_{REF}$ = 0	-	30	50	µA
Input Voltage Range	$V_{ICM (REF)}$		V^- + 1.6	-	V^+ - 1.6	V
Gain	$G_{(REF)}$		-	1±0.0001	-	
Power Supply						
Supply Current	I_{SUPPLY}	$V^+ / V^- = \pm 2.3V$ to ±18V	-	0.9	1.3	mA
		$V^+ / V^- = \pm 2.3V$ to ±18V, T_a = -40°C to 85°C	-	1.1	1.6	mA

*1 One input grounded. G = 1.

■ ELECTRICAL CHARACTERISTICS 3

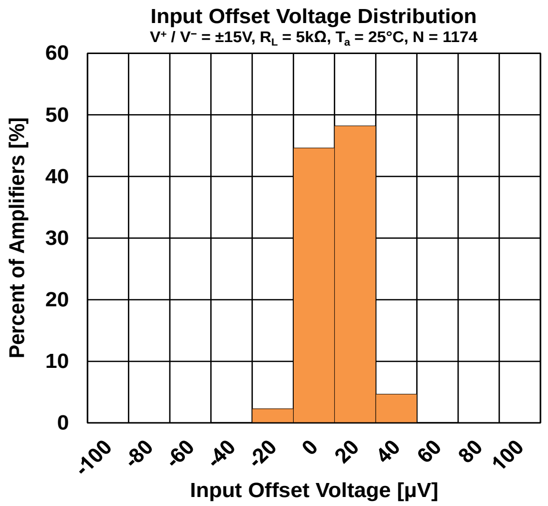
$V^+ / V^- = \pm15V$, V_{REF}=0V, R_L = 5kΩ, T_a = 25°C, unless otherwise specified.

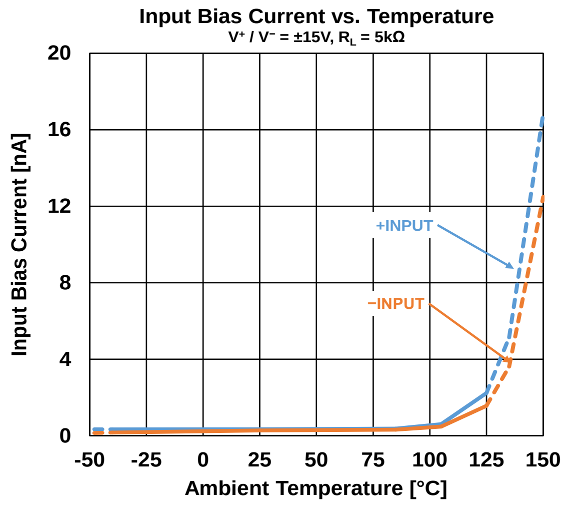
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency Response						
-3dB Bandwidth	BW_{-3dB}	G = 1	-	1000	-	kHz
		G = 10	-	800	-	kHz
		G = 100	-	120	-	kHz
		G = 1000	-	12	-	kHz
Slew Rate	SR	G = 1, V_{IN+} = 20V_{PP}, V_{IN-} = 0V	0.75	1.20	-	V/μs
Settling Time	t_S	0.01%, V_{OUT} = 10V_{PP}				
		G = 1-100	-	15	-	μs
		G = 1000	-	150	-	μs
Noise [*1]						
Input Noise Voltage	e_{ni}	f = 1kHz	-	9	13	nV/√Hz
Output Noise Voltage	e_{no}	f = 1kHz	-	72	100	nV/√Hz
Equivalent Input Noise Voltage	V_{NI}	f = 0.1Hz to 10Hz				
		G = 1	-	3.00	-	μV_{PP}
		G = 10	-	0.55	-	μV_{PP}
		G = 100-1000	-	0.28	-	μV_{PP}
Input Noise Current	i_n	f = 1kHz	-	285	-	fA/√Hz
	I_n	f = 0.1Hz to 10Hz	-	10	-	pApp

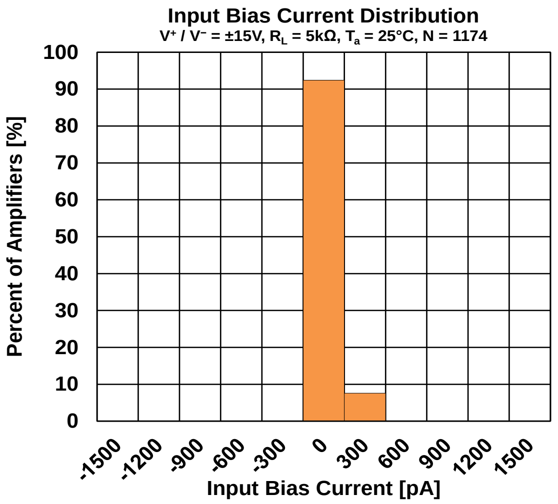
[*1] $Total\ RTI\ Noise = \sqrt{(e_{ni})^2 + (e_{no}/G)^2}$

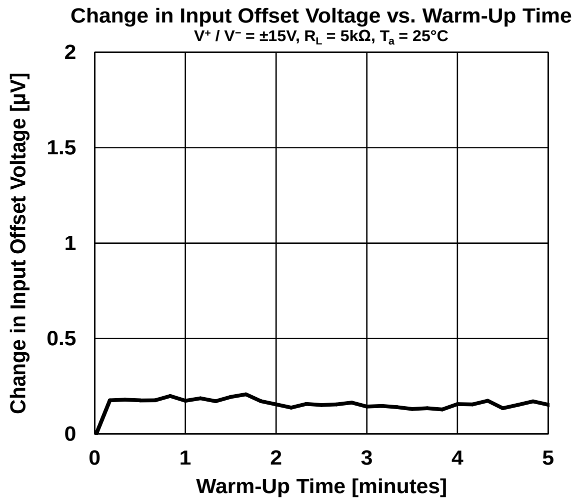
■ TYPICAL CHARACTERISTICS

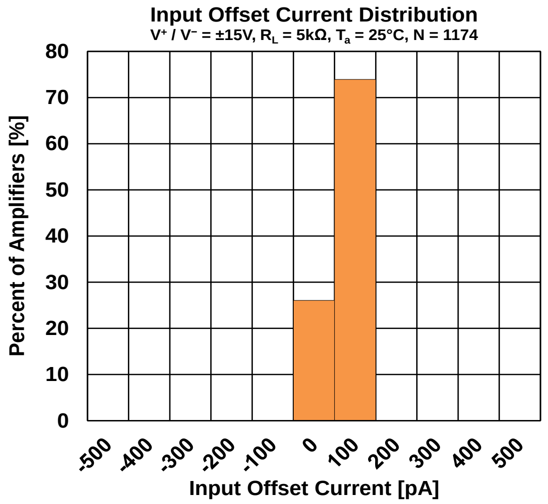
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

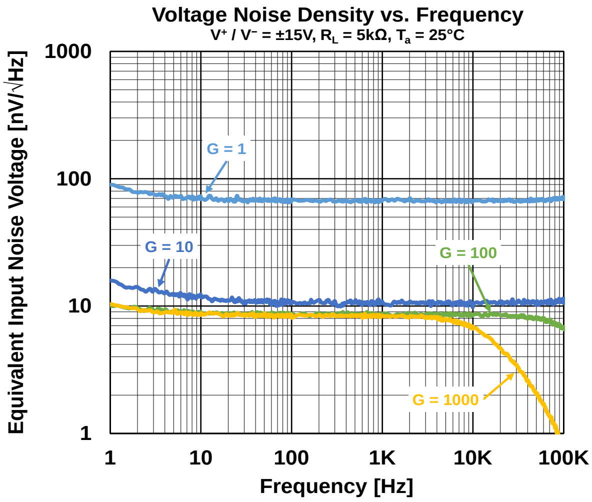












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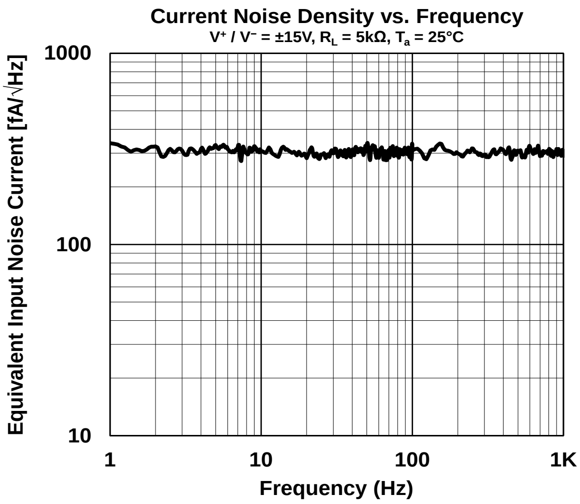
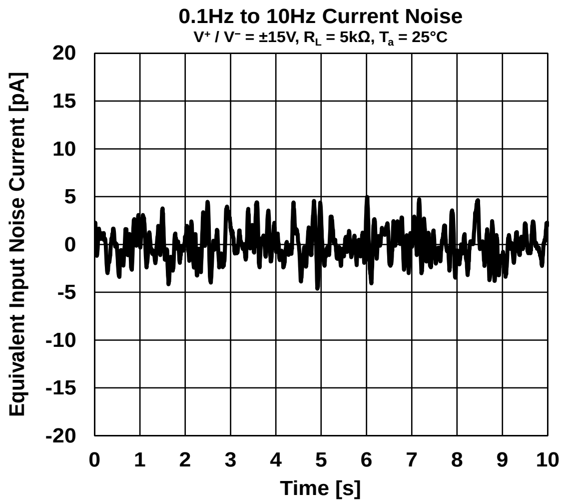
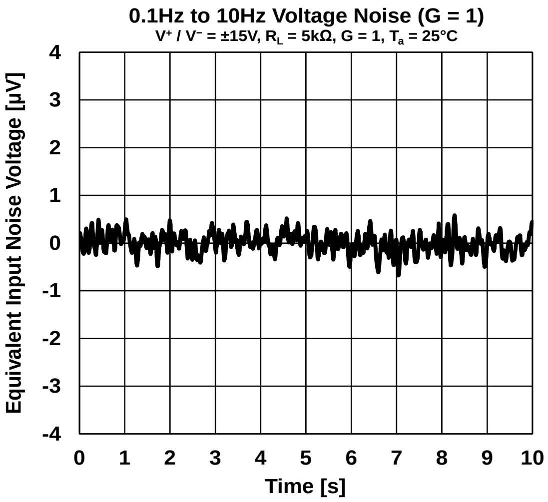
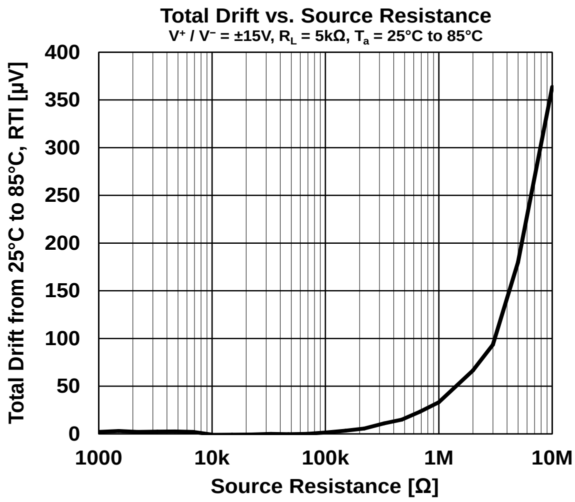
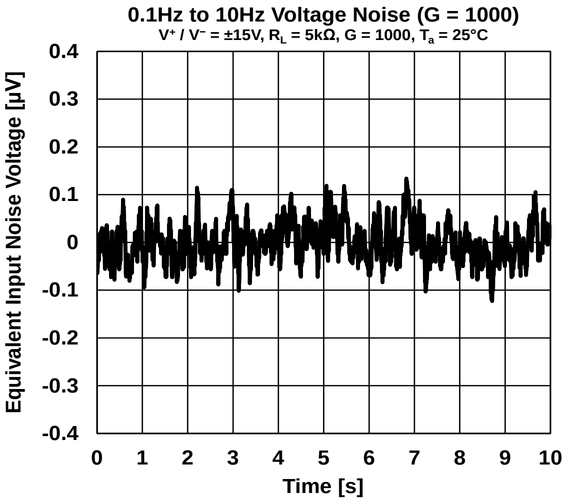
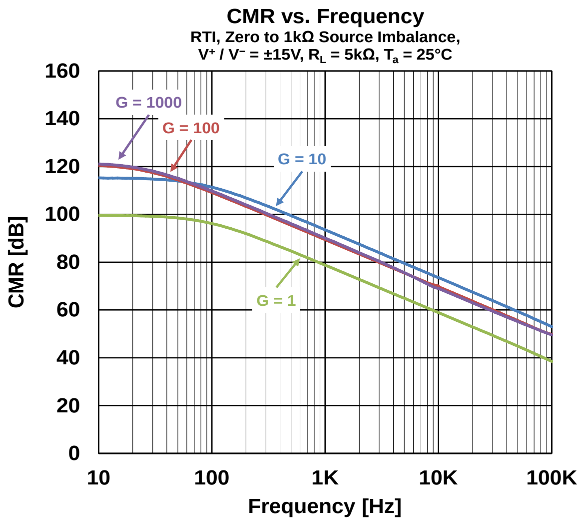








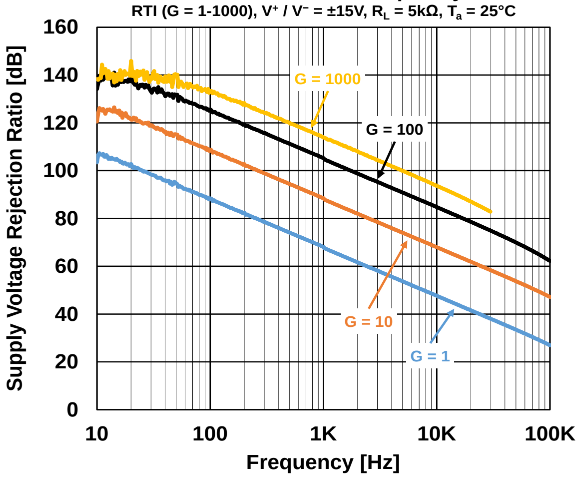




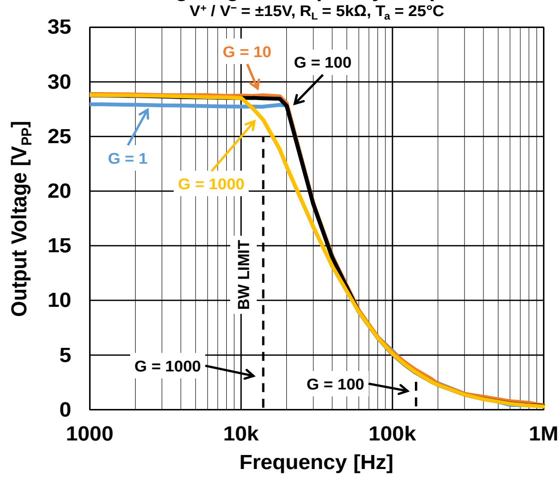
■ TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

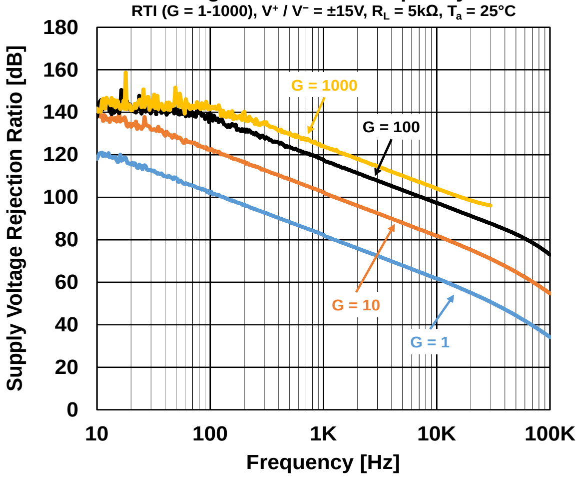
Positive SVR vs. Frequency
RTI (G = 1-1000), V+ / V− = ±15V, R_L = 5kΩ, T_a = 25°C



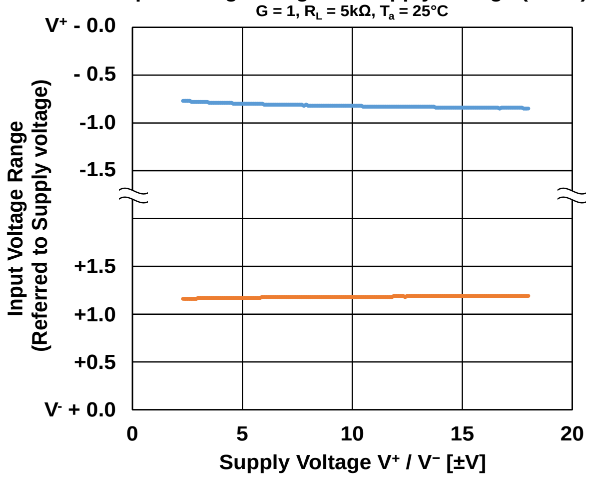
Large Signal Frequency Response
V+ / V− = ±15V, R_L = 5kΩ, T_a = 25°C



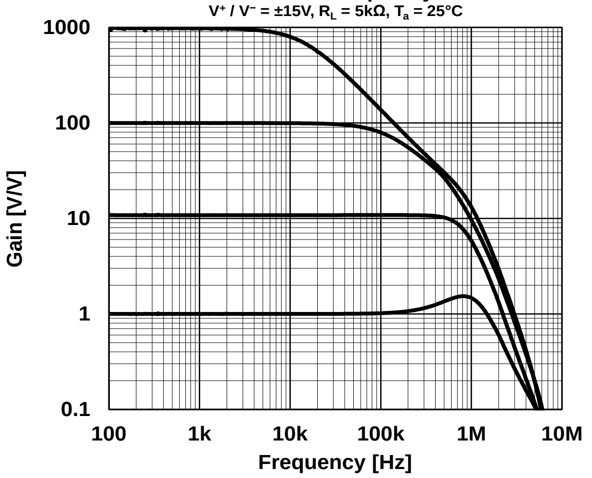
Negative SVR vs. Frequency
RTI (G = 1-1000), V+ / V− = ±15V, R_L = 5kΩ, T_a = 25°C



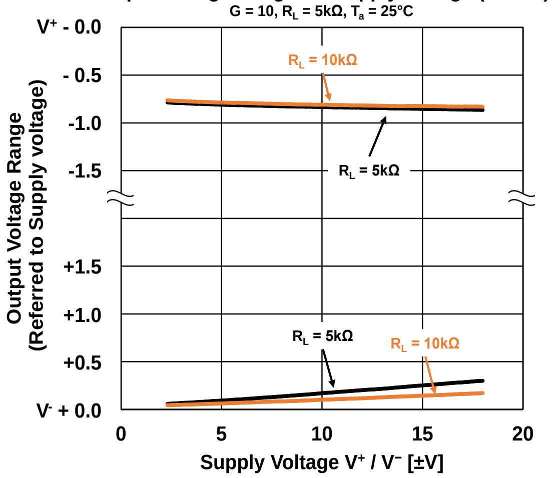
Input Voltage Range vs. Supply Voltage (G = 1)
G = 1, R_L = 5kΩ, T_a = 25°C



Gain vs. Frequency
V+ / V− = ±15V, R_L = 5kΩ, T_a = 25°C



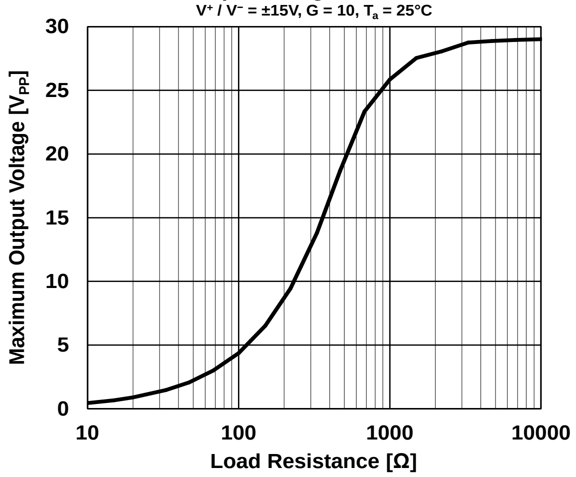
Output Voltage Range vs. Supply Voltage (G = 10)
G = 10, R_L = 5kΩ, T_a = 25°C



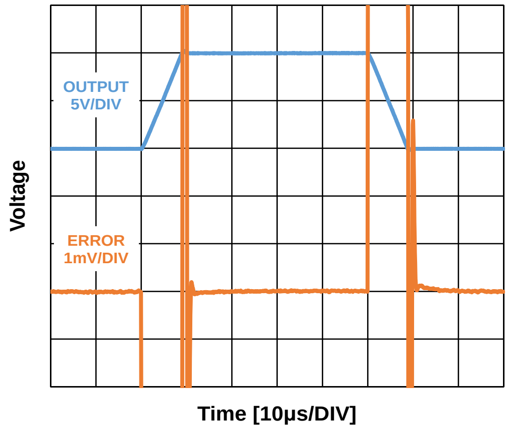
■ TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

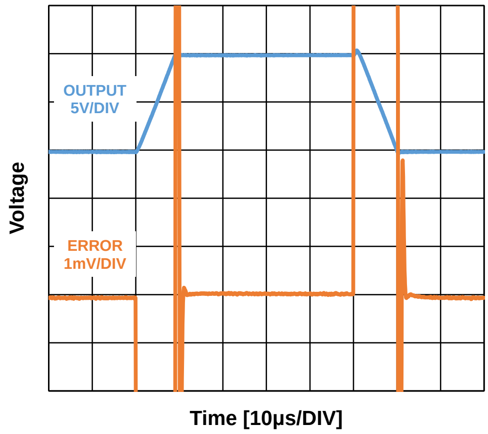
Maximum Output Voltage vs. Load Resistance
$V^+ / V^- = \pm15V$, G = 10, $T_a = 25°C$



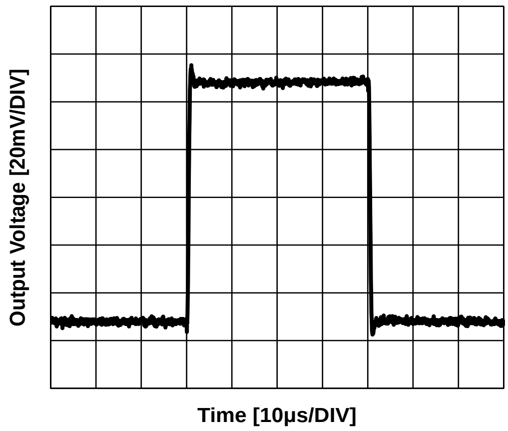
Large Signal Pulse Response and Settling Time
G = 10 (0.5 mV = 0.01%)
$V^+ / V^- = \pm15V$, $R_L = 5k\Omega$, $T_a = 25°C$



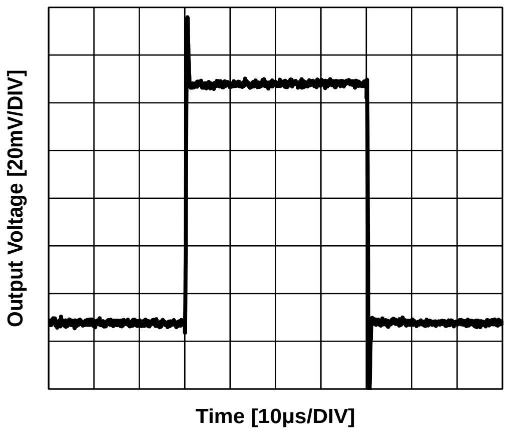
Large Signal Pulse Response and Settling Time
G = 1 (0.5 mV = 0.01%)
$V^+ / V^- = \pm15V$, $R_L = 5k\Omega$, $T_a = 25°C$



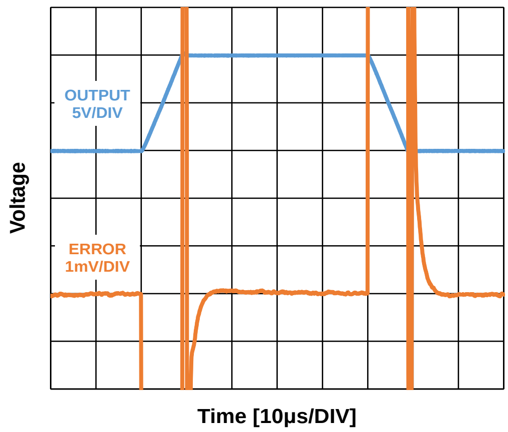
Small Signal Response
G = 10, $V^+ / V^- = \pm15V$, $R_L = 5 k\Omega$, $C_L = 100 pF$, $T_a = 25°C$



Small Signal Response
G = 1, $V^+ / V^- = \pm15V$, $R_L = 5 k\Omega$, $C_L = 100 pF$, $T_a = 25°C$

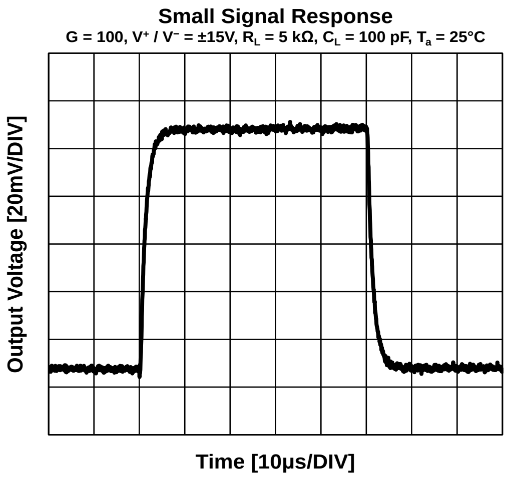


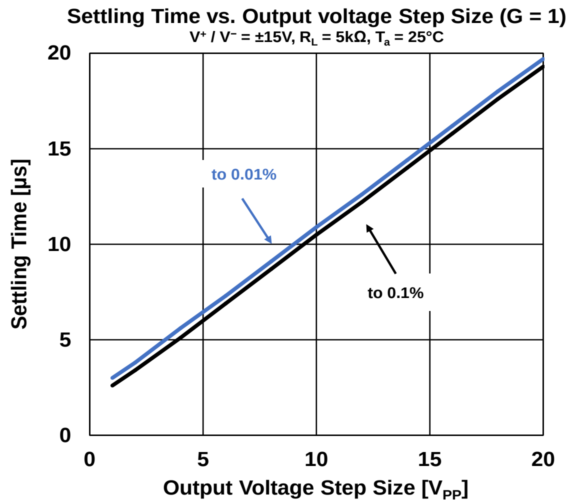
Large Signal Pulse Response and Settling Time
G = 100 (0.5 mV = 0.01%)
$V^+ / V^- = \pm15V$, $R_L = 5k\Omega$, $T_a = 25°C$

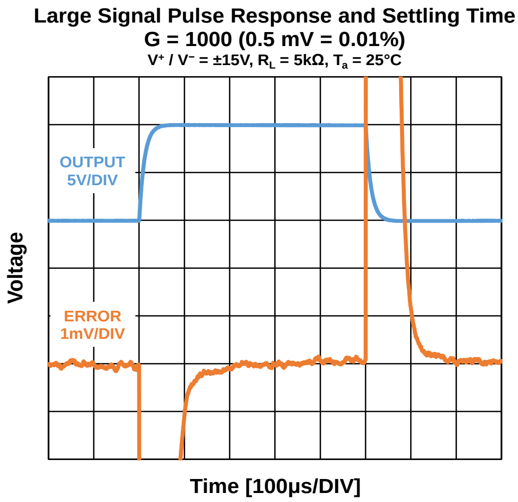


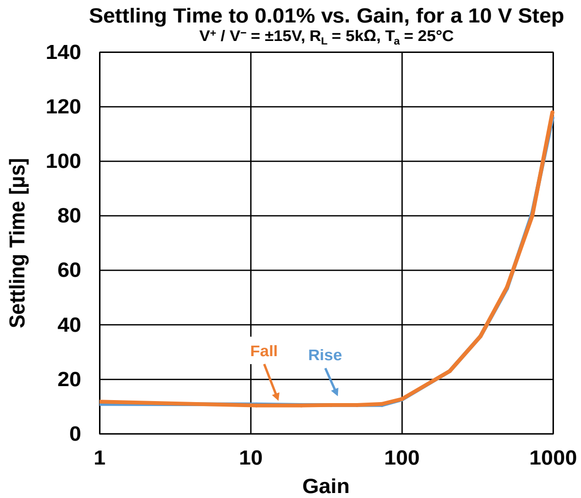
■ TYPICAL CHARACTERISTICS

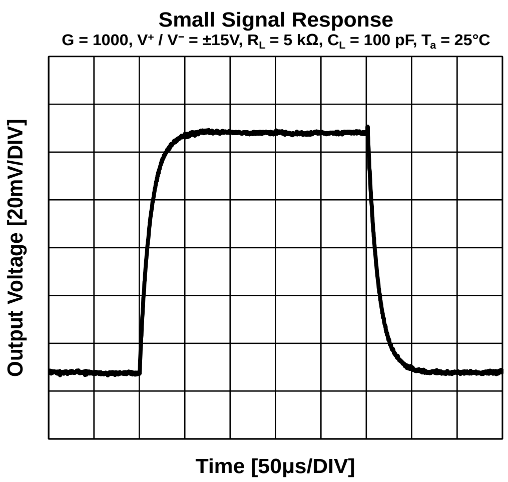
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

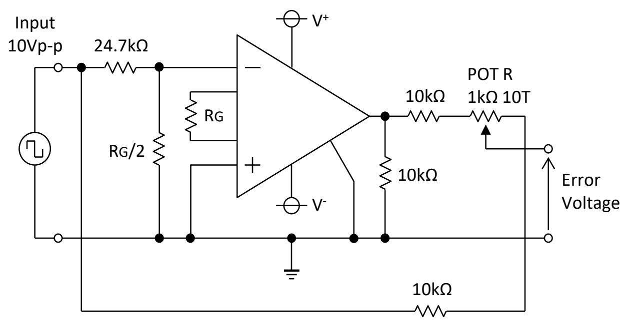








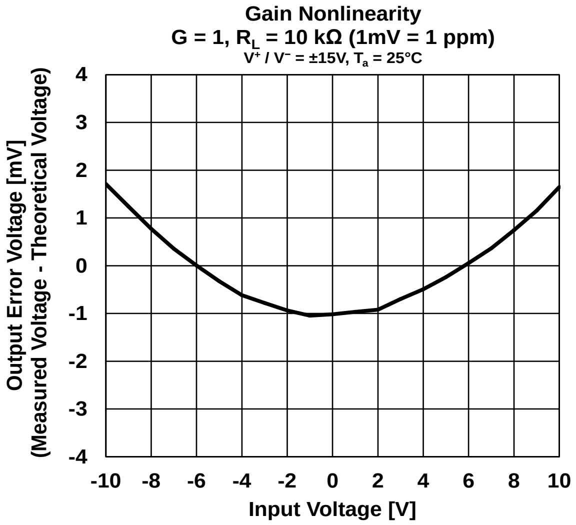


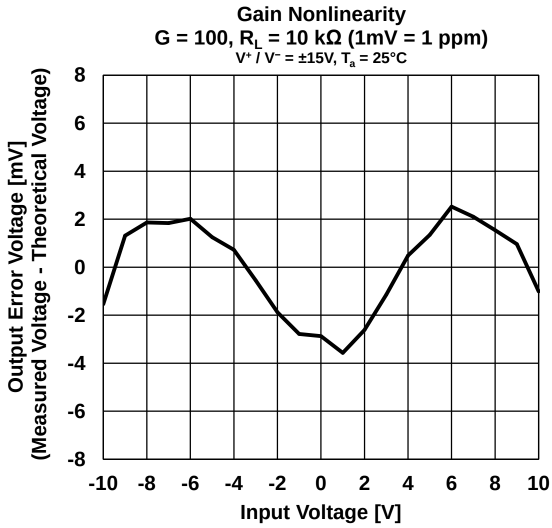


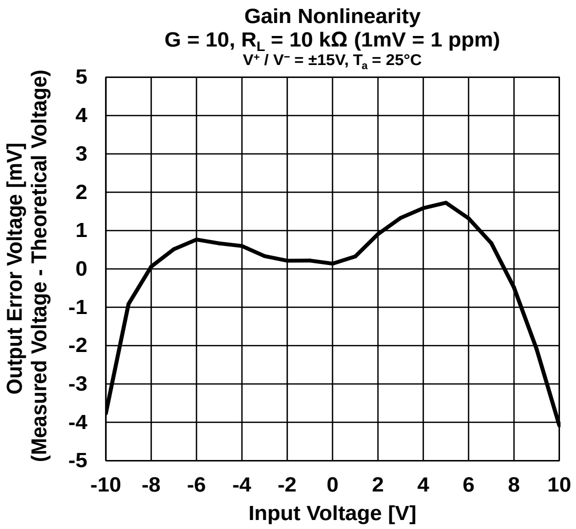
Settling Time Test Circuit

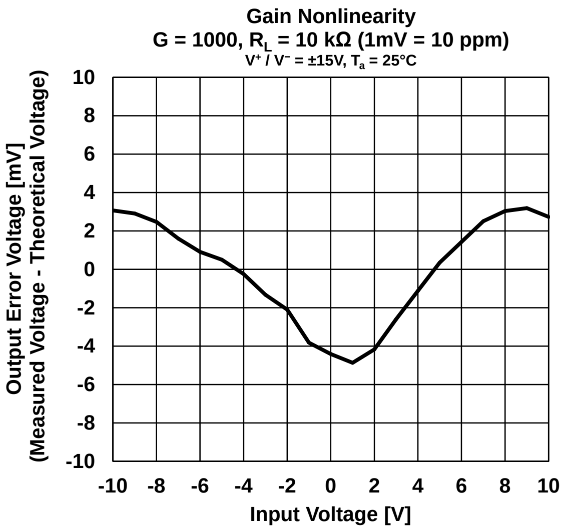
■ TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.









■ APPLICATION NOTES

Theory of Operation

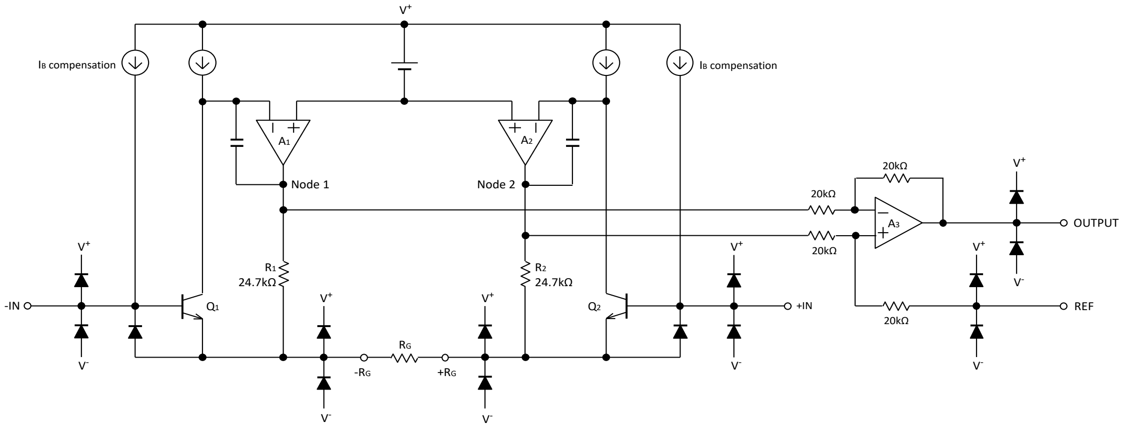


Fig.1. NL9620 Internal Block Diagram

The NL9620 is a general instrumentation amplifier consisting of three operational amplifiers. This instrumentation amplifier consists of two stages. The first stage consists of a differential amplifier circuit that amplifies differential signals, and the second stage consists of a subtraction circuit that removes common-mode signals. Fig.1 shows a Internal Block Diagram of the NL9620.

The operation of the first stage is described below. Amplifier A1 works to keep the collector of transistor Q1 at a constant voltage by the effect of a virtual short circuit. This is achieved by controlling the -RG pin to a voltage that is a diode voltage drop from the -IN pin voltage. Similarly, amplifier A2 controls the +RG pin to a voltage that is a diode voltage drop from the +IN pin voltage. As a result, a voltage equivalent to the differential input voltage is applied to both ends of the gain-setting resistor R_G. The current through resistor R_G is fed through resistors R1 and R2, producing an amplified differential signal between the outputs of amplifiers A1 and A2.

The second stage is a G = 1 subtraction circuit, consisting of amplifier A3 and four resistors. This stage removes the in-phase signal from the differential signal amplified in the first stage.

The transfer function of the NL9620 is expressed by the following equation

$$V_{OUT} = G \times (V_{IN+} - V_{IN-}) + V_{REF}$$

Here, the formula for the gain G is expressed by the following equation

$$G = 1 + \frac{49.4k\Omega}{R_G}$$

Gain Selection

Connecting a resistor between the R_G terminals sets the gain of the NL9620. The gain can be calculated by referring to Table 1 or using the following equation relating gain to resistor R_G.

$$R_G = \frac{49.4k\Omega}{G-1}$$

Table 1. gains set by resistors of the E96 series (tolerance ±1%)

Resistor R_G (1% std) [Ω]	Calculated Gain [V/V]
NC (open)	1.000
49.9k	1.990
12.4k	4.984
5.49k	10.00
2.61k	19.93
1.00k	50.40
499	100.0
249	199.4
100	495.0
49.9	991.0
24.9	1,985
9.76	5.063k
4.87	10.14k

To design for overall system gain accuracy, the resistance error and temperature drift of the resistor RGs should be considered in conjunction with the NL9620 gain specifications. When resistor R_G is not used (open), gain error and gain drift are minimised.

Supply Current of R_G

The NL9620 replicates the differential voltage between the input terminals to both ends of the resistor R_G. The size of resistor R_G must be selected to accommodate the power consumed by the resistor.

Input and Output Offset Voltage

There are two specifications related to the offset voltage of the instrumentation amplifier: the input offset voltage V_{OSI} and the output offset voltage V_{OSO}.
In the NL9620, each offset voltage is precisely adjusted by trimming.
The influence of these two offset voltages should be considered for each gain setting. At higher gain settings, the input offset voltage V_{OSI} dominates, and at lower gain settings, the output offset voltage V_{OSO} dominates.
The instrumentation amplifier input conversion offset voltage is calculated from the following equation using V_{OSI}, V_{OSO}, and gain G.

$$Total\ RTI\ Error = V_{OSI} + \frac{V_{OSO}}{G}$$

Input and Output Noise Voltage

Two types of noise voltage specifications are defined for instrumentation amplifiers: input noise voltage e_{ni} and output noise voltage e_{no}. The influence of these two types of noise voltage must be considered for each gain setting. At higher gain settings, the input noise voltage e_{ni} dominates, and at lower gain settings, the output noise voltage e_{no} dominates. The equivalent input noise voltage of the instrumentation amplifier is calculated from the following equation using e_{ni} and e_{no} and the gain G.

$$Total\ RTI\ Noise = \sqrt{(e_{ni})^2 + \left(\frac{e_{no}}{G}\right)^2}$$

Input Voltage Range

Fig. 2 through Fig. 4, shown as example characteristics, illustrate the common-mode input voltage that should be applied to obtain the required output voltage range at each supply voltage. In the NL9620's instrumentation amplifier structure, consisting of three operational amplifiers, the differential signal is amplified in the first amplifier stage before the common-mode signal is removed in a subtraction circuit consisting of a second-stage operational amplifier and four resistors. At the internal node between the first amplifier stage and the second-stage subtraction circuit (nodes 1 and 2 in Fig. 1), the amplified differential signal is combined with the common-mode signal and the voltage drop generated by the circuit operation. In an internal circuit where this combination signal is present, the internal node may be clipped at the supply voltage and cause the circuit to malfunction, even if the instrumentation amplifier is operated under conditions that meet the input and output voltage ranges of the instrumentation amplifier.

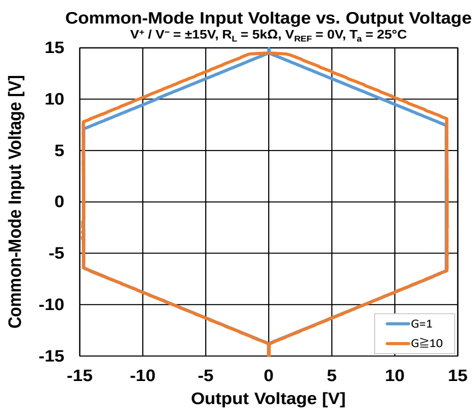


Fig.2. Input and Output Voltage range (V_S = ±15V)

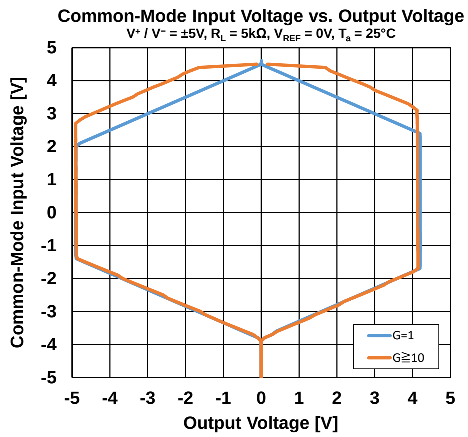


Fig.3. Input and Output Voltage range (VS = ±5V)

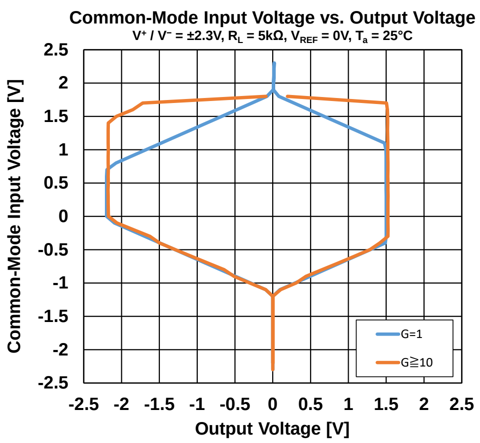


Fig.4. Input and Output Voltage range (VS = ±2.3V)

Reference Terminal

The output voltage of the NL9620 is generated with respect to the voltage applied to the REF pin. This function is useful to shift the output voltage of the instrumentation amplifier to a desired voltage level.
The impedance of the voltage source connected to the REF pin must be kept sufficiently lower than 1Ω to fully demonstrate the CMR performance of the NL9620. As shown in the simplified block diagram in fig.1, 20 kΩ is connected to the REF pin; the impedance of the voltage source connected to the REF pin adds to this 20 kΩ and affects the matching of the four resistors. This mismatch can cause gain errors and degradation of CMR and other parameters.
For example, a configuration like that shown in Fig.5 can be used to provide any voltage to the REF pin of the NL9620 with a low impedance.

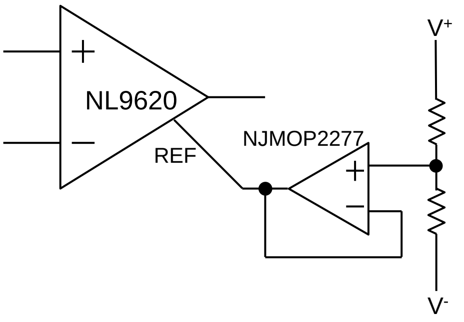


Fig.5. Example of a low impedance reference circuit.

CMR Performance over a Wide Bandwidth

In layouts where noise problems are not taken into account, some in-phase signals may be converted to differential signals before the signals reach the input terminals of the instrumentation amplifier. The cause of in-phase to differential conversion occurs when the frequency response of one input wiring differs from that of the other input wiring.
To maintain a high CMR over a wide bandwidth, the resistors and capacitors connected to the two input leads must be closely matched.
If resistors are placed in the input wiring, such as input protection resistors, they should be placed close to the input terminals of the instrumentation amplifier. This will minimise the influence of parasitic capacitance in the PCB wiring.
The parasitic capacitance of the gain setting pin also affects the frequency response of the CMR. If the PCB design includes switches, jumpers, etc. on the gain setting pins, these should be selected with the lowest possible parasitic capacitance.

Common-Mode Rejection

To obtain a high CMR over a wide bandwidth, the resistance and capacitance differences in the two input wires must be minimized. In environments where the influence of external noise is significant, shielded cables can be used in the transmission line. To compensate for the resistance and capacitance differences that occur at the + input and - input terminals, the lengths of the shielded cables should be matched as closely as possible.
Depending on the situation, common mode noise problems can be avoided by driving the shielded portion of the cable in phase with the signal, as shown in Fig.6 and Fig.7. Driving the shield section in phase with the signal ignores the capacitance between the signal line and the shield section, and thus works to reduce the capacitance difference between the + input terminal and the - input terminal.

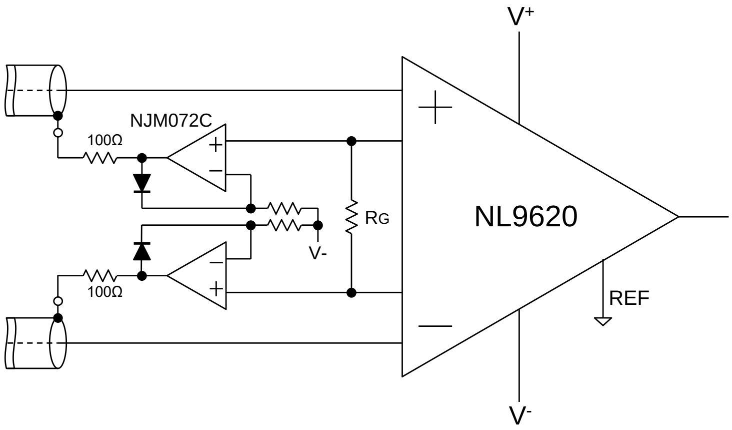


Fig.6. Differential Shield Driver

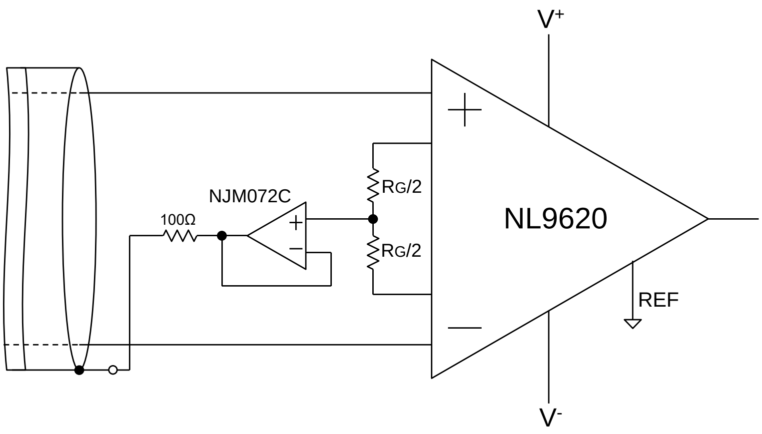


Fig.7. Common-Mode Shield Driver

Ground Returns for Input Bias Currents

The NL9620 generates a DC current that flows from or to the input terminals as an input bias current. (max. 2 nA)
A path (return path) must be provided for the DC input bias current flowing from the input terminals to return to ground. If there is no return path, the input voltage will transition to a voltage outside the operating range, resulting in circuit malfunction.
Design the return path for the input bias current with reference to the return path example shown in Fig. 8.

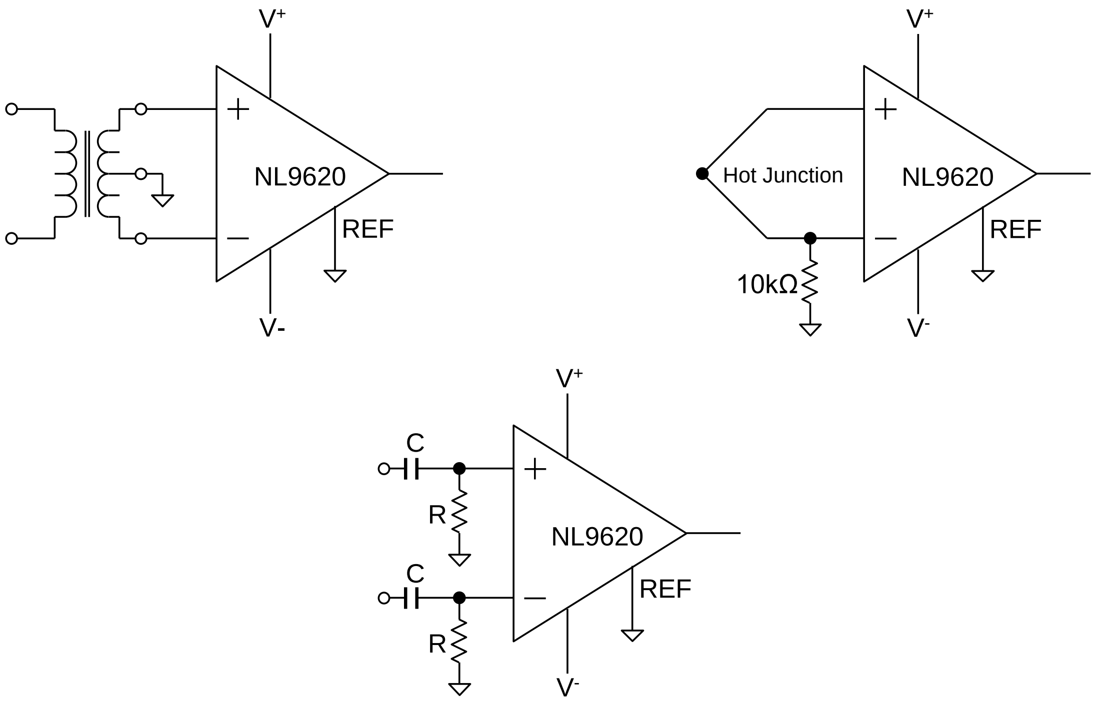


Fig.8. Examples of Ground Returns for Bias Currents

Input Protection

Input signals added to the NL9620 must operate within the input voltage range described in the Absolute Maximum Rated Voltage section.

Input voltages exceeding the supply voltage

If an input voltage in excess of the supply voltage is applied, an external resistor must be connected in series with each input terminal to limit the input current I_{IN} to within 10mA of the absolute maximum rating (Fig.9-1).
The input limiting resistor is calculated using the following formula

$$R_{PROTECT} \geq \frac{|V_{IN} - V_{SUPPLY}|}{I_{IN}}$$

Lower protection resistances may be required in applications where the effects of noise are significant: a clamp diode can be placed at the input of the NL9620 to prevent overcurrents flowing to its input terminals, resulting in a lower protection resistance value (Fig.9-2).

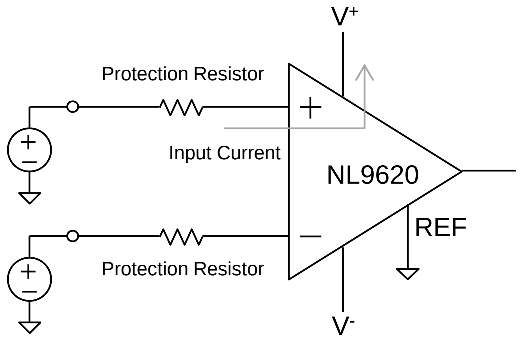


Fig.9-1. Simple Protection Circuit

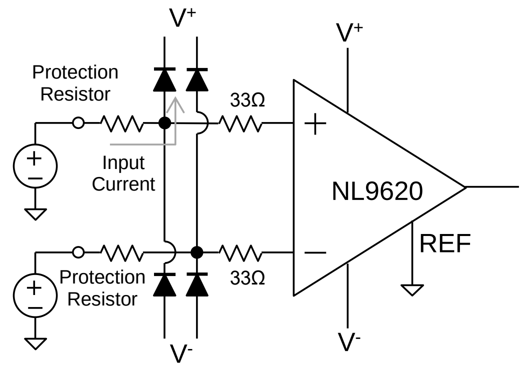


Fig.9-2. Low NOISE Protection Circuit Using Diodes

Fig.9. Example of protection circuit for Voltages Beyond Supply

Long-term Signal Input Close to the Supply Voltage

When G = 1, a maximum differential input voltage of 36V (±18V) is allowed. Note, however, that prolonged total time with 36V applied may affect reliability. For normal use, use within the input voltage range (V_{ICM}) shown in the electrical characteristics table.

large Differential Input Voltage at High Gain

When large differential signals exceeding the absolute maximum ratings are input, care should be taken to avoid overvoltage at the input terminals. The input terminals of the NL9620 can be protected by using clamp diodes between the input terminals of the NL9620 as shown in Fig. 10.

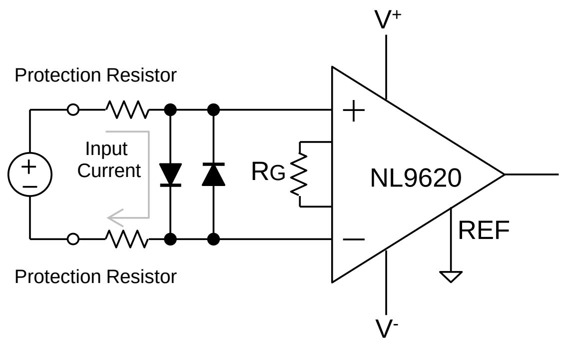


Fig.10. Protection Circuit for Large Differential Input.

EMIRR (EMI Rejection Ratio) Definition

The NL9620 has a built-in EMI rejection filter. As a result, it provides high-frequency noise immunity even when no external low-pass filter is connected to the input of the instrumentation amplifier. (Fig. 11 differential mode, Fig. 12 common mode)

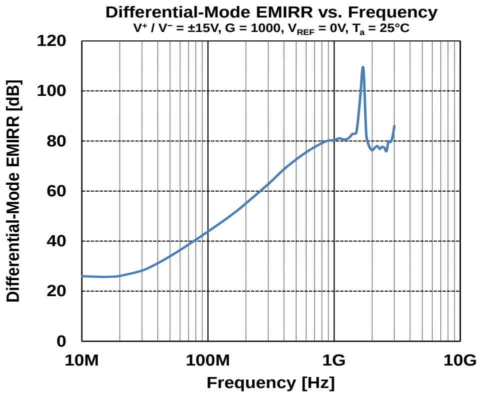


Fig.11. Differential-Mode EMIRR Characteristics

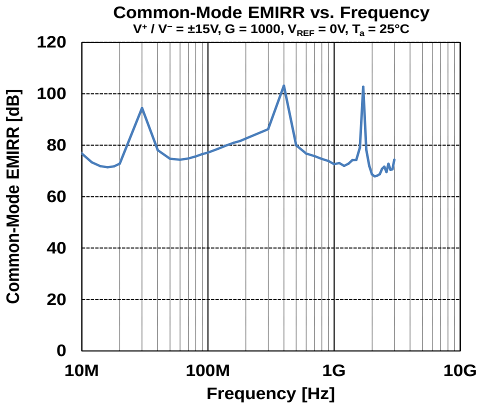


Fig.12. Common-Mode EMIRR characteristics

EMIRR is a parameter indicating the EMI robustness of an OpAmp. The definition of EMIRR is given by the following equation1.
The tolerance of the RF signal can be grasped by measuring an RF signal and offset voltage shift quantity. Offset voltage shift is small so that a value of EMIRR is big. And it understands that the tolerance for the RF signal is high. In addition, about the input offset voltage shift with the RF signal, there is the thinking that influence applied to the input terminal is dominant. Therefore, generally the EMIRR becomes value that applied an RF signal to +INPUT terminal.

$$\mathrm{EMIRR}=20\cdot\log\left(\frac{V_{\mathrm{RF\_PEAK}}}{|\Delta V_{\mathrm{IO}}|}\right) \qquad ---\ \mathrm{eq.1}$$

$V_{\mathrm{RF\_PEAK}}$: RF Signal Amplitude [VP]
ΔV_{IO}: Input offset voltage shift quantity [V]

*For details, refer to “Application Note for EMI Immunity" in our HP.

Design of External RC Filter Network

If the signal-to-noise ratio of the input signal needs to be improved by removing signals in unwanted frequency bands, it is also useful to place a filter network at the input. An example of a filter network is the RC low pass shown in Fig. 13.
It is recommended that an external RC low pass filter that achieves the desired cut-off frequency f_c be designed with a $C_D \geq 100$ pF. If the C_D is small, the desired cut-off frequency may not be achieved due to the influence of the EMIRR filter inside the IC. R, which generates thermal noise, should be as small as possible.
The capacitor C_C shown in Fig. 13 is used to remove common-mode noise.
For C_C to reduce common-mode noise, care should be taken to ensure that a mismatch does not occur between R x C_C on the + input terminal and R x C_C on the - input terminal. A mismatch converts part of the common-mode noise into differential noise and causes the signal-to-noise ratio of the signal to deteriorate.
Designing C_C using the $C_D \geq 10C_C$ relationship as a guide can reduce the effect of mismatch.

$$FilterFreq_{DIFF} = \frac{1}{2\pi R(2C_D+C_C)}$$
$$FilterFreq_{CM} = \frac{1}{2\pi R C_C}$$

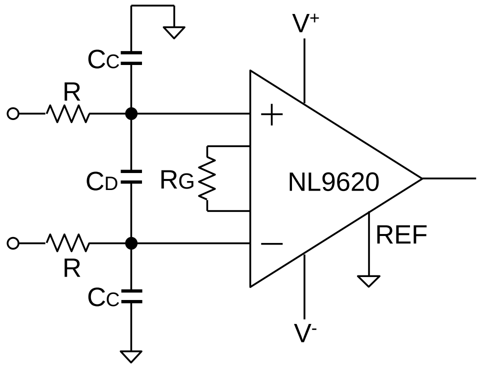


Fig.13. RC Low-Pass Filter to Improve the S/N Ratio of Input Signals

Precision V-I Converter

Fig. 14 shows an example application for a high accuracy current source using the NL9620 instrumentation amplifier. The input bias current of the operational amplifier gives an error in the output current, so an op amp with a low input bias current should be selected.
The output current value of a V-I converter is expressed by the following equation

$$I_L = \frac{V_X}{R1} = \frac{\{(V_{IN+}) - (V_{IN-})\}G}{R1}$$

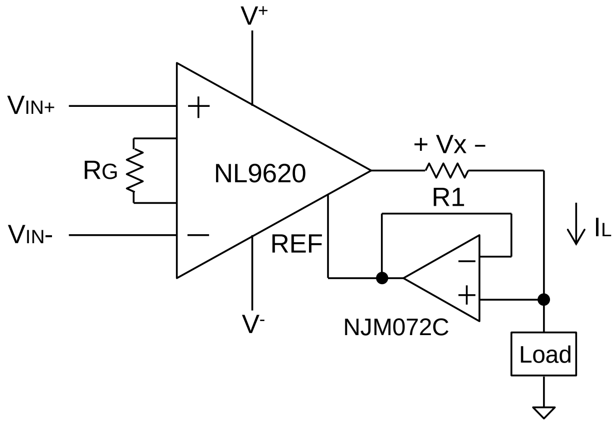
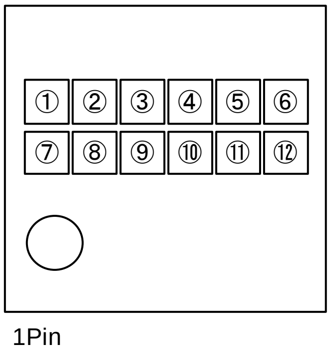


Fig.14. Precision V-I Converter Circuit Using Instrumentation Amplifier

■ MARKING SPECIFICATION (VSP-8-AF)

① to ⑦	Product Code	Refer to *Part Marking List*
⑧ to ⑫	Lot Number	Alphanumeric Serial Number



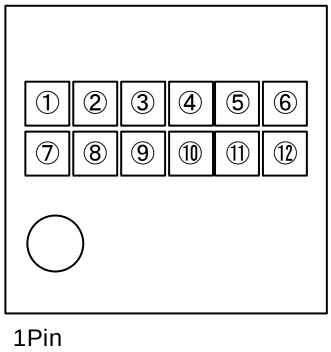
NOTICE
There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or distributor before attempting to use AOI.

Part Marking List

Product Name	①	②	③	④	⑤	⑥	⑦
NL9620AFAE1D	L	9	6	2	0	A	D

■ MARKING SPECIFICATION (EMP-8-AN)

① to ⑦	Product Code	Refer to *Part Marking List*
⑧ to ⑫	Lot Number	Alphanumeric Serial Number



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Part Marking List

Product Name	①	②	③	④	⑤	⑥	⑦
NL9620ANAE1D	L	9	6	2	0	A	D

Nisshinbo Micro Devices Inc.

VSP-8-AF

PI-VSP-8-AF-E-A

■ PACKAGE DIMENSIONS

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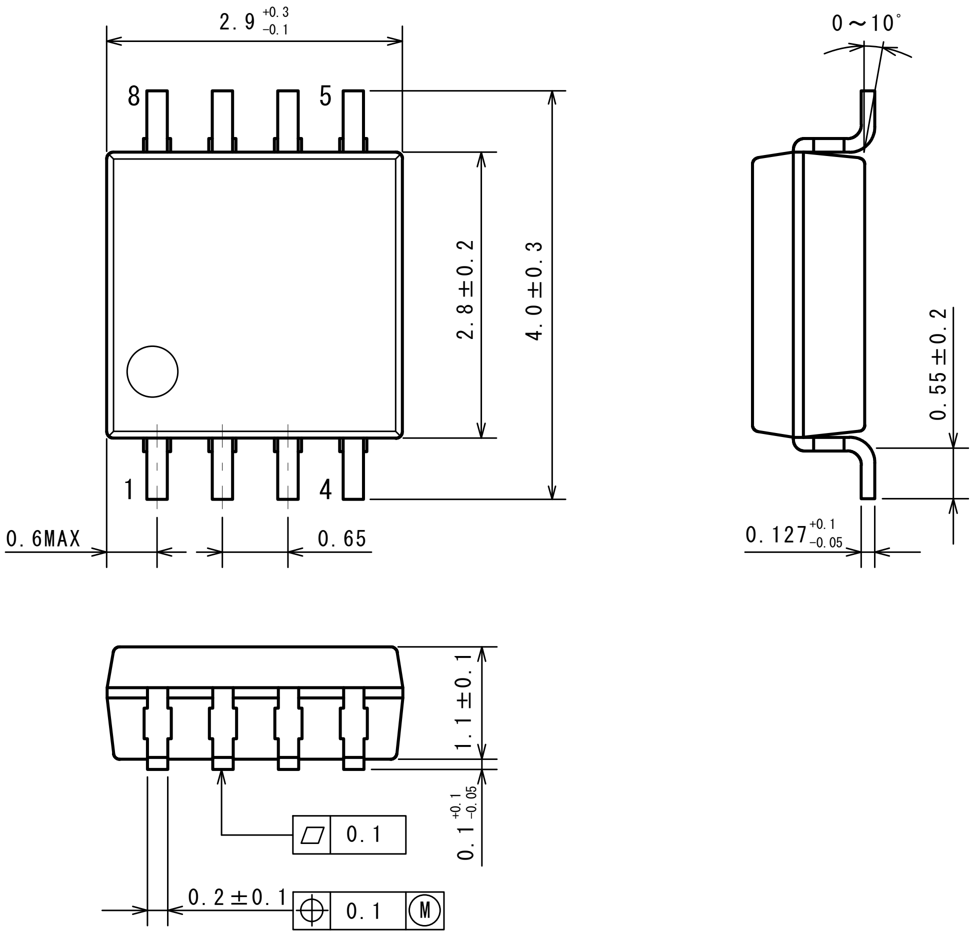

■ EXAMPLE OF SOLDER PADS DIMENSIONS

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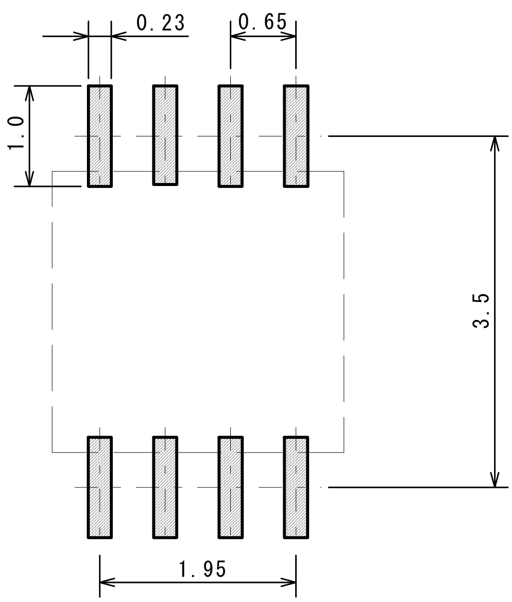

Nisshinbo Micro Devices Inc.

■ **PACKING SPEC**

UNIT: mm

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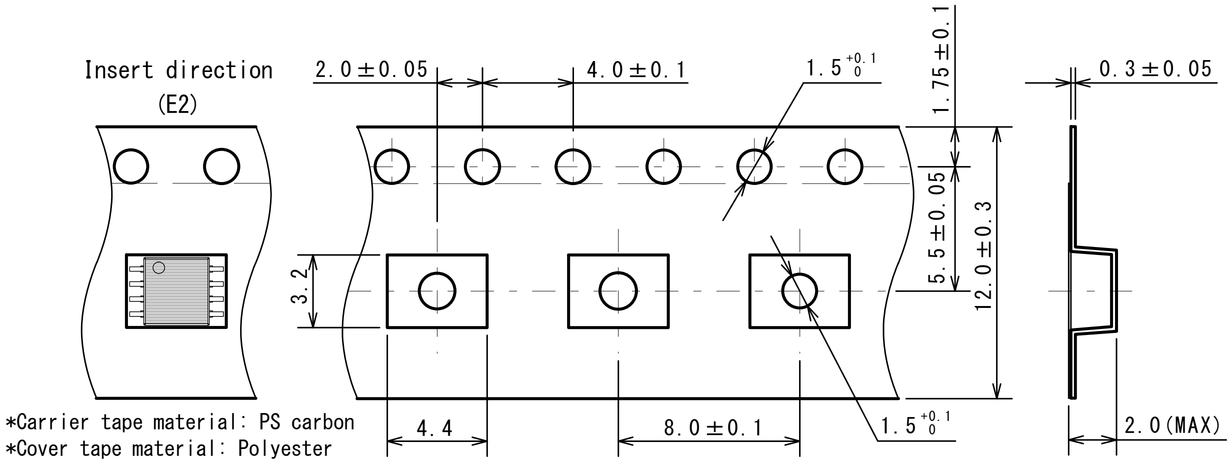
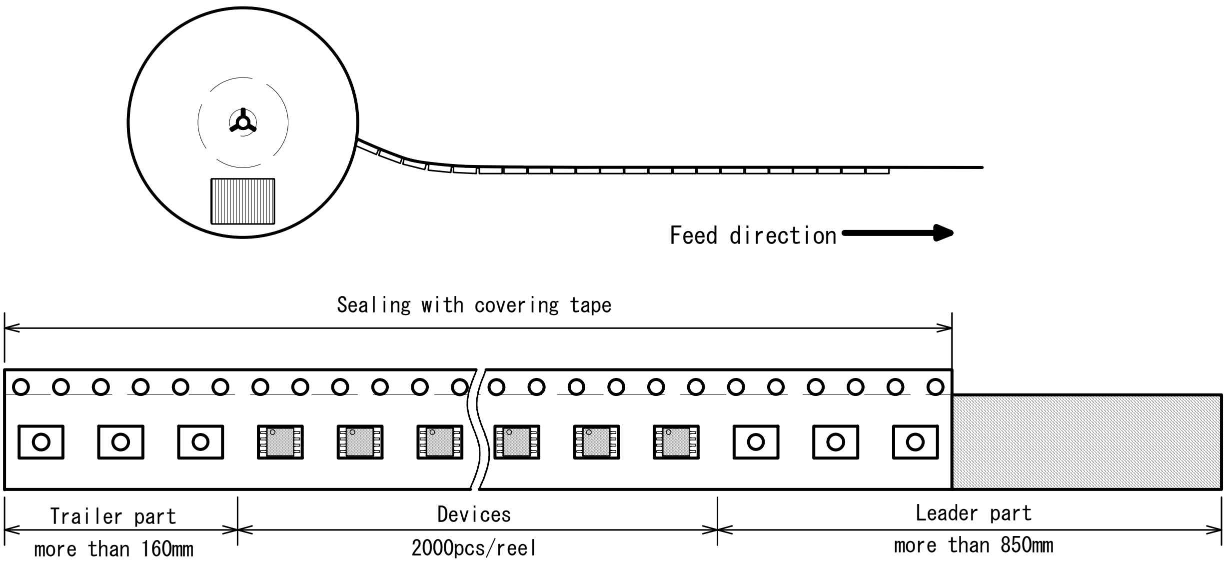
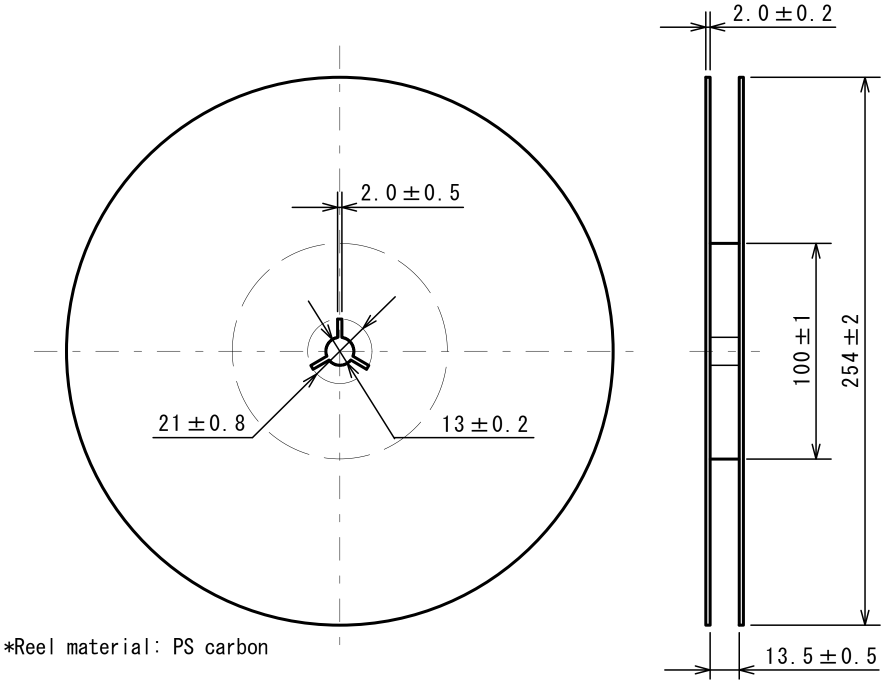


(2) Taping state

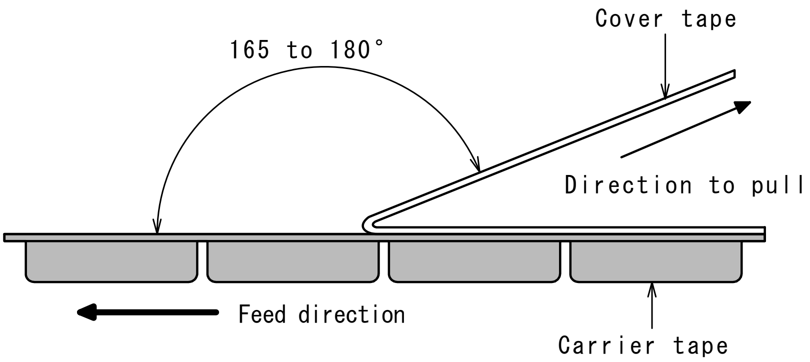


(3) Reel dimensions



(4) Peeling strength

Peeling strength of cover tape
- Peeling angle 165 to 180° degrees to the taped surface.
- Peeling speed 300mm/min
- Peeling strength 0.1 to 1.3N



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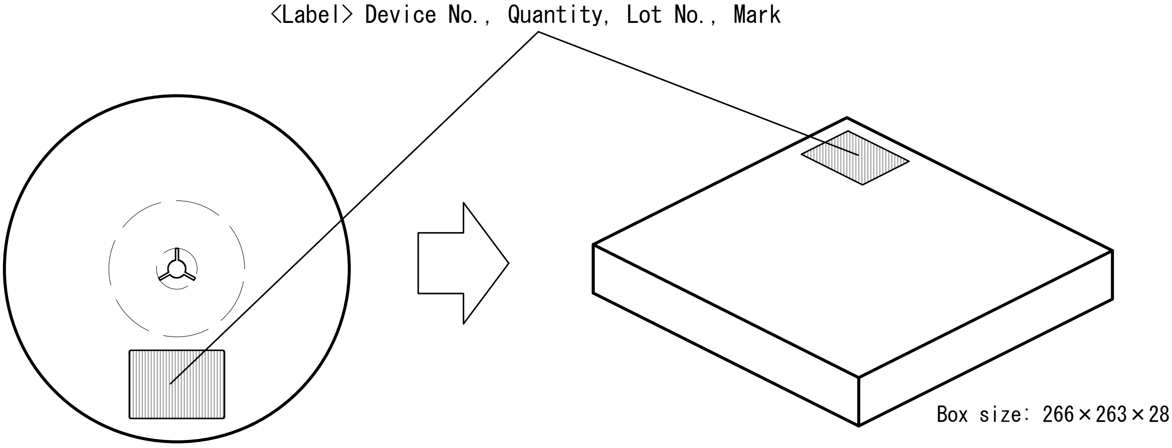
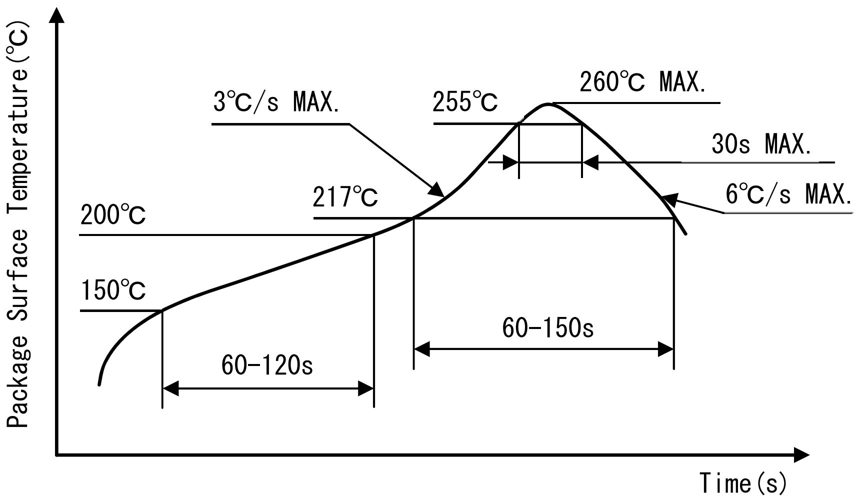


■ **HEAT-RESISTANCE PROFILES**



Reflow profile

■ **PACKAGE DIMENSIONS**

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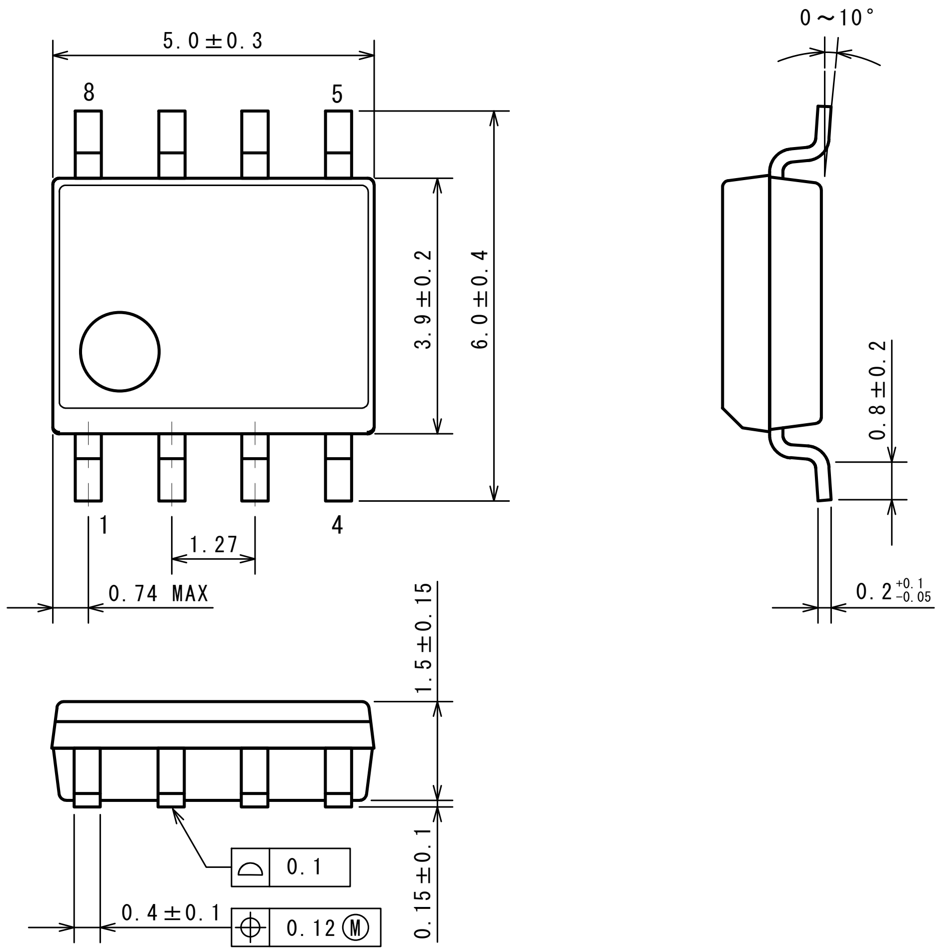
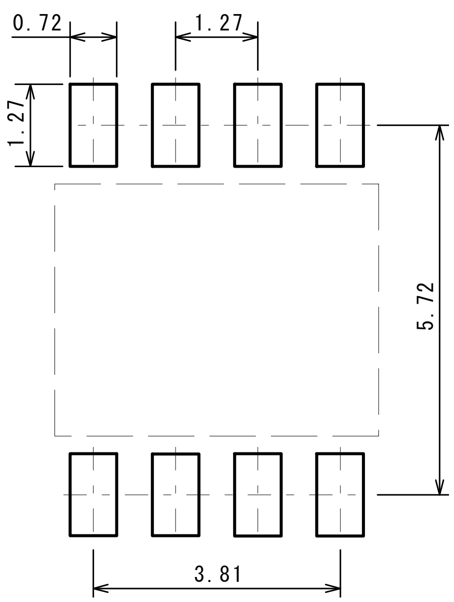


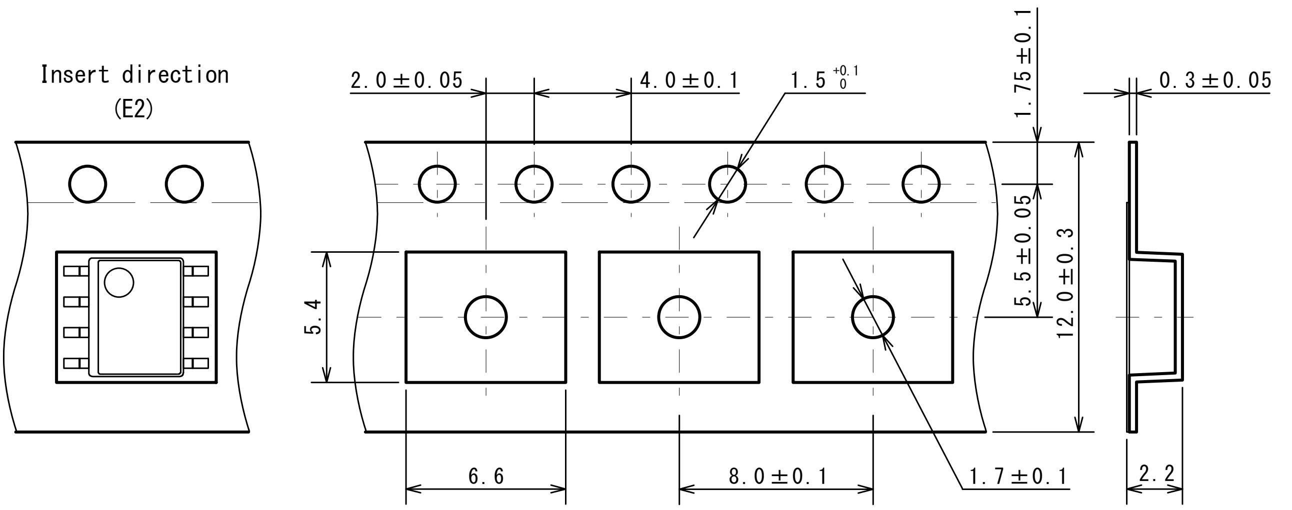
■ **EXAMPLE OF SOLDER PADS DIMENSIONS**



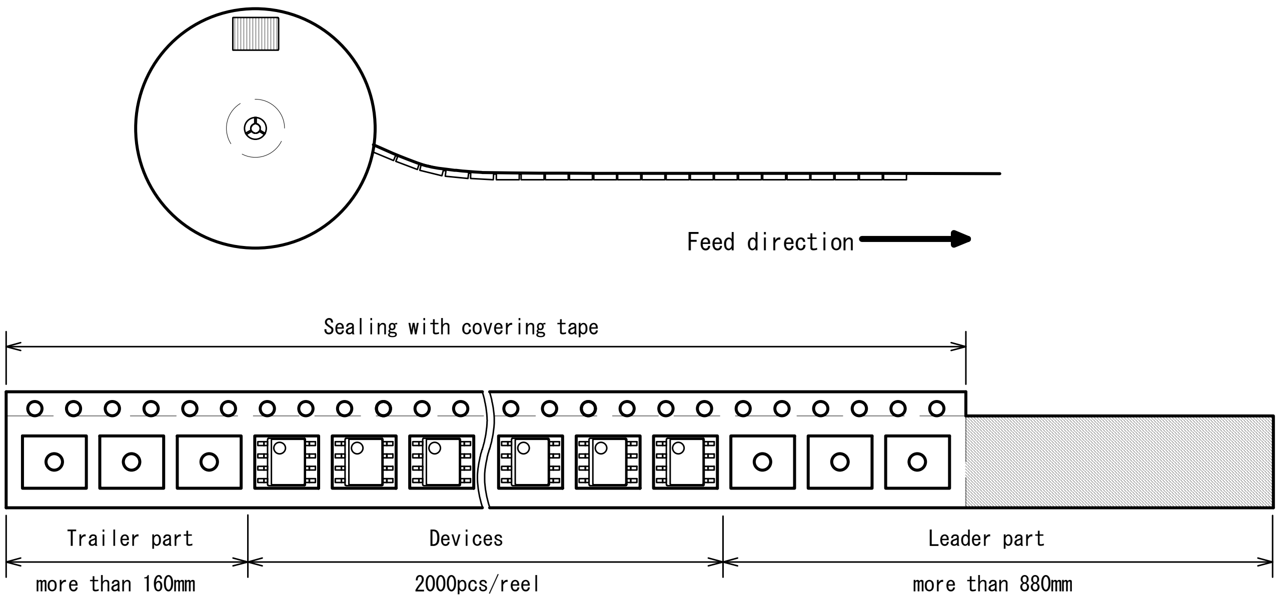
■ **PACKING SPEC**

UNIT: mm

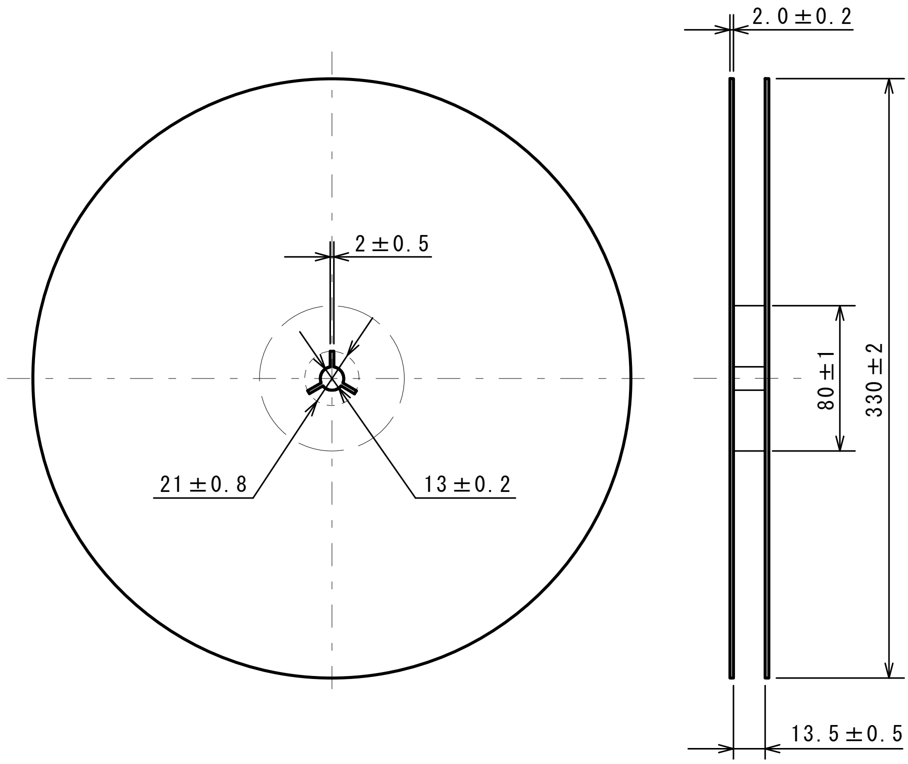
(1) Taping dimensions / Insert direction



(2) Taping state



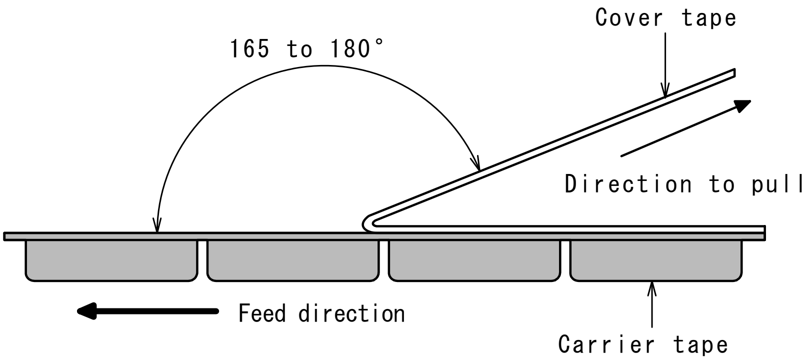
(3) Reel dimensions



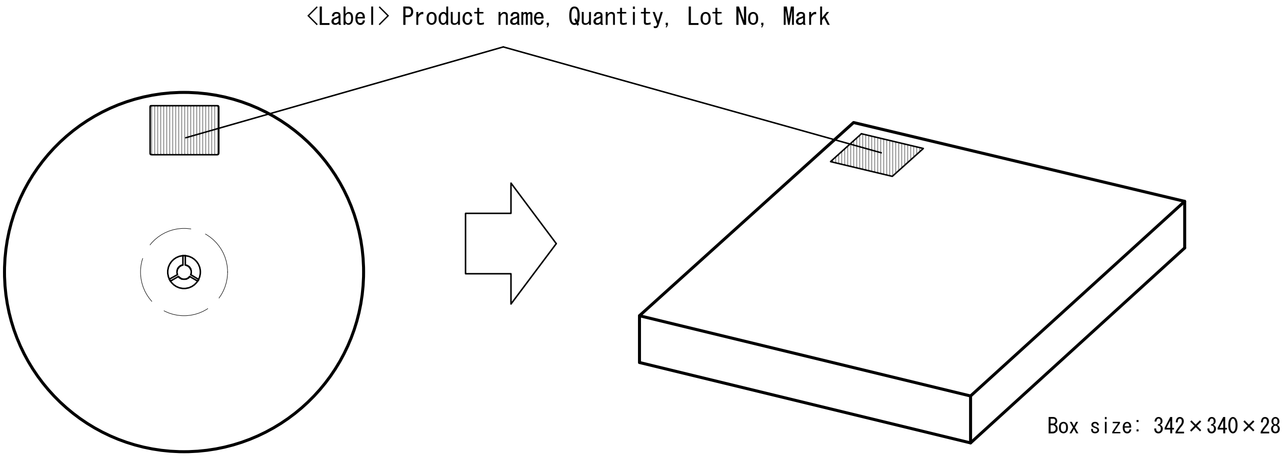
(4) Peeling strength

Peeling strength of cover tape

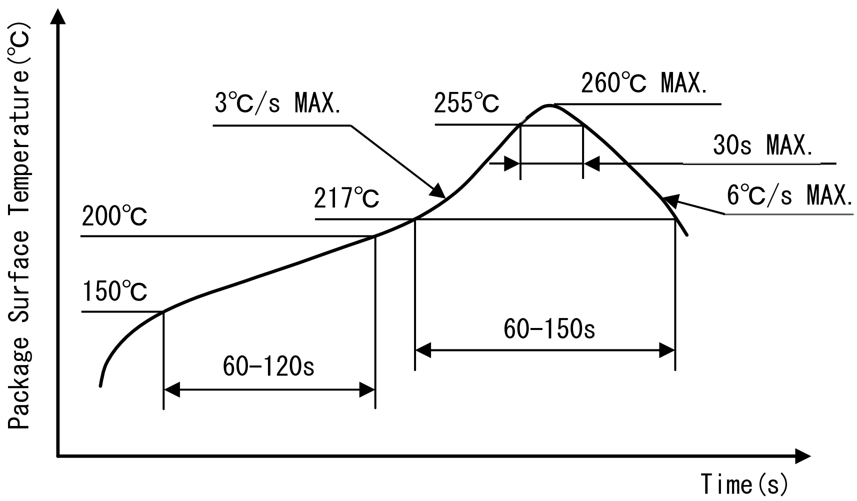
- ･Peeling angle 165 to 180° degrees to the taped surface.
- ･Peeling speed 300mm/min
- ･Peeling strength 0.1 to 1.3N



(5) Packing state



■ **HEAT-RESISTANCE PROFILES**



Reflow profile

■ **REVISION HISTORY**

Date	Revision	Contents of Changes
May 7, 2025	Ver.1.0	Initial Release

1. The products and the product specifications described in this document are subject to change or discontinuation of production without notice for reasons such as improvement. Therefore, before deciding to use the products, please refer to our sales representatives for the latest information thereon.
2. The materials in this document may not be copied or otherwise reproduced in whole or in part without the prior written consent of us.
3. This product and any technical information relating thereto are subject to complementary export controls (so-called KNOW controls) under the Foreign Exchange and Foreign Trade Law, and related politics ministerial ordinance of the law. (Note that the complementary export controls are inapplicable to any application-specific products, except rockets and pilotless aircraft, that are insusceptible to design or program changes.) Accordingly, when exporting or carrying abroad this product, follow the Foreign Exchange and Foreign Trade Control Law and its related regulations with respect to the complementary export controls.
4. The technical information described in this document shows typical characteristics and example application circuits for the products. The release of such information is not to be construed as a warranty of or a grant of license under our or any third party's intellectual property rights or any other rights.
5. The products listed in this document are intended and designed for use as general electronic components in standard applications (office equipment, telecommunication equipment, measuring instruments, consumer electronic products, amusement equipment etc.). Those customers intending to use a product in an application requiring extreme quality and reliability, for example, in a highly specific application where the failure or misoperation of the product could result in human injury or death should first contact us.
    - Aerospace Equipment
    - Equipment Used in the Deep Sea
    - Power Generator Control Equipment (nuclear, steam, hydraulic, etc.)
    - Life Maintenance Medical Equipment
    - Fire Alarms / Intruder Detectors
    - Vehicle Control Equipment (automotive, airplane, railroad, ship, etc.)
    - Various Safety Devices
    - Traffic control system
    - Combustion equipment

    In case your company desires to use this product for any applications other than general electronic equipment mentioned above, make sure to contact our company in advance. Note that the important requirements mentioned in this section are not applicable to cases where operation requirements such as application conditions are confirmed by our company in writing after consultation with your company.
6. We are making our continuous effort to improve the quality and reliability of our products, but semiconductor products are likely to fail with certain probability. In order to prevent any injury to persons or damages to property resulting from such failure, customers should be careful enough to incorporate safety measures in their design, such as redundancy feature, fire containment feature and fail-safe feature. We do not assume any liability or responsibility for any loss or damage arising from misuse or inappropriate use of the products.
7. The products have been designed and tested to function within controlled environmental conditions. Do not use products under conditions that deviate from methods or applications specified in this datasheet. Failure to employ the products in the proper applications can lead to deterioration, destruction or failure of the products. We shall not be responsible for any bodily injury, fires or accident, property damage or any consequential damages resulting from misuse or misapplication of the products.
8. Quality Warranty
    8-1. Quality Warranty Period
    In the case of a product purchased through an authorized distributor or directly from us, the warranty period for this product shall be one (1) year after delivery to your company. For defective products that occurred during this period, we will take the quality warranty measures described in section 8-2. However, if there is an agreement on the warranty period in the basic transaction agreement, quality assurance agreement, delivery specifications, etc., it shall be followed.
    8-2. Quality Warranty Remedies
    When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.
    Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.
    8-3. Remedies after Quality Warranty Period
    With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
9. Anti-radiation design is not implemented in the products described in this document.
10. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
11. WLCSP products should be used in light shielded environments. The light exposure can influence functions and characteristics of the products under operation or storage.
12. Warning for handling Gallium and Arsenic (GaAs) products (Applying to GaAs MMIC, Photo Reflector). These products use Gallium (Ga) and Arsenic (As) which are specified as poisonous chemicals by law. For the prevention of a hazard, do not burn, destroy, or process chemically to make them as gas or power. When the product is disposed of, please follow the related regulation and do not mix this with general industrial waste or household waste.
13. Please contact our sales representatives should you have any questions or comments concerning the products or the technical information.

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