CODICO

Specification for 4.2 inch EPD

Model NO. : DEPG0420BNU276F14

DKE's Confirmation:

Prepared by	Checked by	Approved by

Customer approval:

Customer	Approved by	Date

Revision History

Version	Content	Date	Producer
2.0	New release	2020/10/29	

CONTENTS

1. Over View

DEPG0420BNU276F14 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white and black full display capabilities. The 4.2 inch active area contains 300×400 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2. Features

- ◆300×400 pixels display
- ◆High contrast High reflectance
- ◆Ultra wide viewing angle Ultra low power consumption
- ◆Pure reflective mode
- ◆Bi-stable display
- ◆Commercial temperature range
- ◆Landscape portrait modes
- ◆Hard-coat antiglare display surface
- ◆Ultra Low current deep sleep mode
- ◆On chip display RAM
- ◆Waveform can stored in On-chip OTP or written by MCU
- ◆Serial peripheral interface available
- ◆On-chip oscillator
- ◆On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆I^2C signal master interface to read external temperature sensor
- ◆Support partial update mode
- ◆Built-in temperature sensor

3. Mechanical Specification

Parameter	Specifications	Unit	Remark
Screen Size	4.2	Inch	
Display Resolution	400(H)×300(V)	Pixel	DPI:120
Active Area	84.8×63.6	mm	
Pixel Pitch	0.212×0.212	mm	
Pixel Configuration	Rectangle		
Outline Dimension	91 (H)×77 (V) ×1.2(D)	mm	
Weight	16.1±0.3	g	

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
KS	Black State L* value		-	18	20		3-1
	Black Ghosting ΔL		-	1	-		3-1
WS	White State L* value		66	67	-		3-1
	White Ghosting ΔL		-	1	-		3-1
R	White Reflectivity	White	30	34	-	%	3-1
CR	Contrast Ratio	Indoor	15:1	20:1	-		3-1 3-2
GN	2Grey Level	-	-	-	-		
Life		Temp:23±3°C Humidity:55±10%RH		5years			3-3

Notes: 3-1. Luminance meter: Eye-One Pro Spectrophotometer.

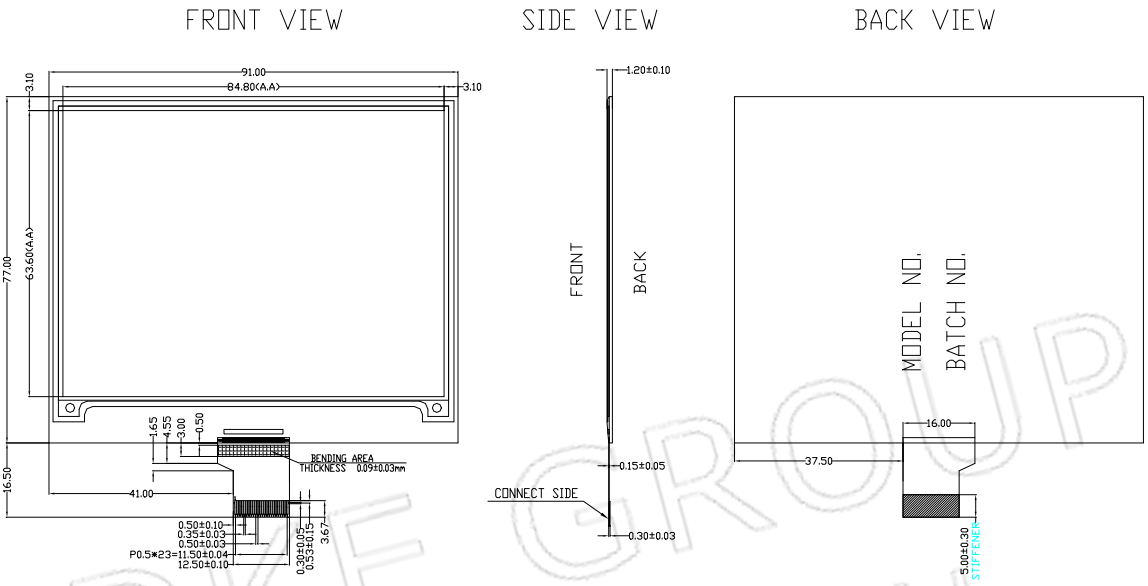
3-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

3-3. When the product is stored. The display screen should be kept white and face up.

4.Mechanical Drawing of EPD Module

Confirmation:

DATE	REV.	MODIFICATION
2020-02-26	A	FIRST ISSUE



NOTE

1 DISPLAY MODULE 4.2″ ARRAY FOR EPD
2 DRIVER IC:UC8276C
3 RESOLUTION:300gateX400source
4 PIXEL SIZE:0.212mmX0.212mm

TOLERANCES UNMARKED		TITLE:	PROJECT:			REV.:	DATE:	CUST. P/N:
ANGLES± 5°		EPD	DEPG0420_ _U276F14			A	20.02.26	
.X=± 0.4mm			DWN.	CHK.	APPR.	UNIT:	3RD ANGLE:	PAGE:
.XX=± 0.20mm	DKE	RoHS	XZ FAN	CC ZHENG	SY ZHAO	mm		1/1
.XXX=± 0.20mm								

5. Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage 2	
6	TSCL	O	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I2C Interface to digital temperature sensor Data pin	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	Keep Open
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin Low when -Outputting display waveform -Communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.3 to +6.0	V
Logic Input voltage	VIN	-0.3 to VCI +0.3	V
Operating Temp range	TOPR	0 to +50	ºC.
Storage Temp range	TSTG	-25 to+70	ºC.
Optimal Storage Temp	TSTGo	23±3	ºC.
Optimal Storage Humidity	HSTGo	55±10	%RH

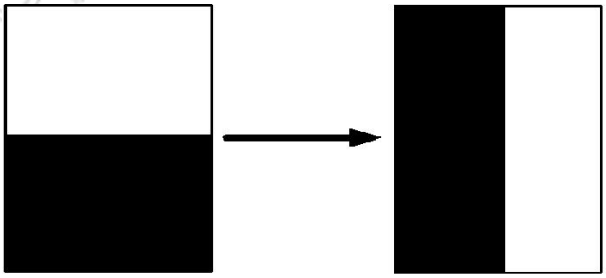
Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{CI}	-	VCI	2.3	3.0	3.6	V
Core logic voltage	V_{DD}		VDD	2.3	3.0	3.6	V
High level input voltage	V_{IH}	-	-	0.7 V_{CI}	-	V_{CI}	V
Low level input voltage	V_{IL}	-	-	0	-	0.3 V_{CI}	V
High level output voltage	V_{OH}	IOH =400uA	-	V_{CI} -0.4	-	-	V
Low level output voltage	V_{OL}	IOL = -400uA	-	0	-	0.4	V
Typical power	P_{TYP}	V_{CI} =3.0V	-	-	12.6	-	mW
Deep sleep mode	P_{STPY}	V_{CI} =3.0V	-	-	0.003	-	mW
Typical operating current	Iopr_VCI	V_{CI} =3.0V	-	-	4.2	- -	mA
Image update time	-	25 ºC	-	-	4	-	sec
Typical peak current	Iopr_VCI	2.3~3.6V			50	60	mA
Sleep mode current	Islp_V_{CI}	DC/DC off No clock No input load Ram data retain	-	-	20		uA
Deep sleep mode current	Idslp_V_{CI}	DC/DC off No clock No input load Ram data not retain	-	-	1	5	uA

Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3. The listed electrical characteristics are only guaranteed under the controller & waveform provided by DKE.

4. Electrical measurement： Tektronix oscilloscope - MDO3024，

Tektronix current probe – TCP0030A.

6.3 Panel AC Characteristics

6.3.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-3-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

Table 6-3-1: MCU interface assignment under different bus interface mode

6.3.2 MCU Serial Interface (4-wire SPI)

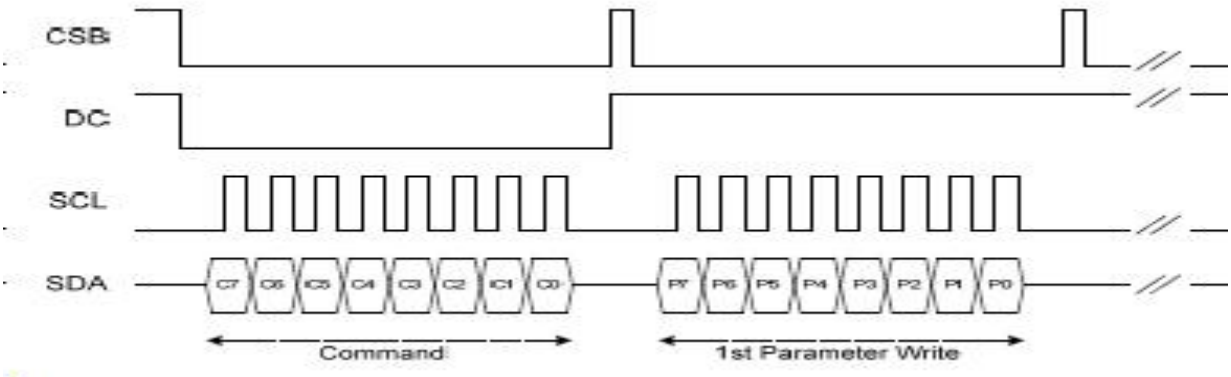
The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Table 6-3-2: Control pins of 4-wire Serial Peripheral interface

Note: ↑ stands for rising edge of signal

Figure 6-3-1: 4-wire SPI mode



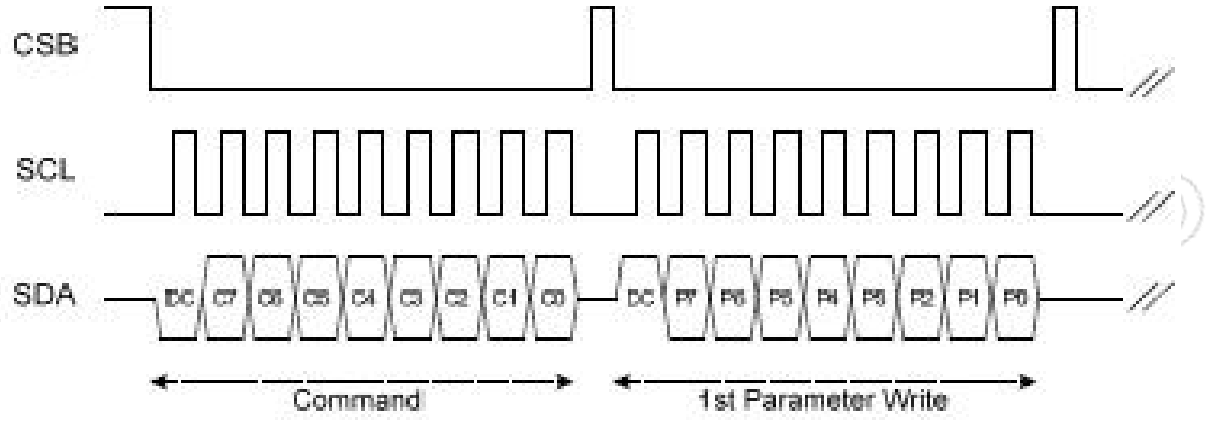
6.3.3 MCU Serial Interface (3-wire SPI)

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

Table 6-3-3: Control pins of 4-wire Serial Peripheral interface

Note：↑ stands for rising edge of signal

Figure 6-3-2: 3-wire SPI mode



6.3.4 Interface Timing

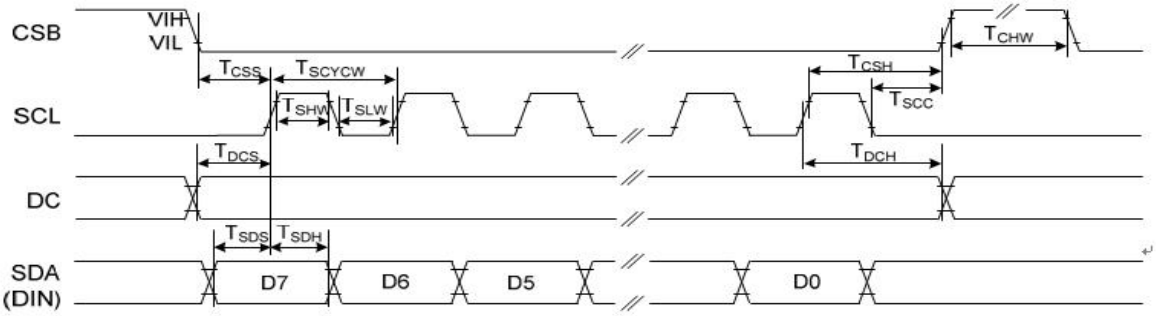


Figure: 4-wire Serial Interface Characteristics (Writemode)

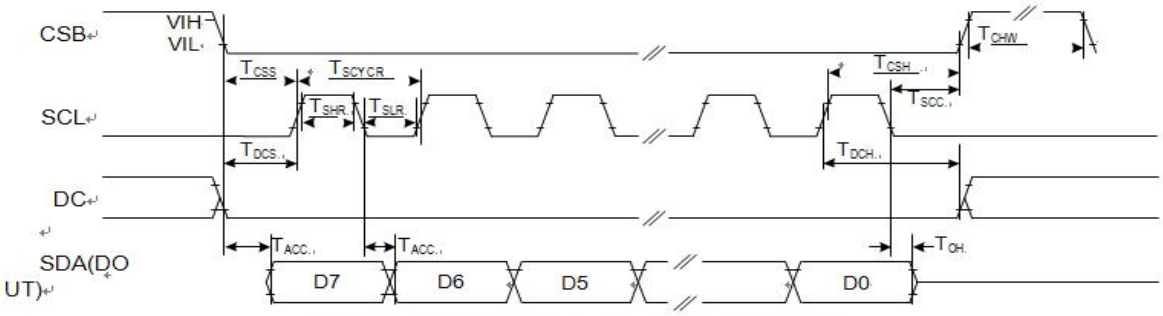


Figure: 4-wire Serial Interface Characteristics (Readmode)

Serial Interface Timing Characteristics

Symbol	Signal /Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle(Write)	100			ns
T_{SHW}		SCL “H” pulse width(Write)	35			ns
T_{SLW}		SCL “L” pulse width(Write)	35			ns
T_{SCYCR}		Serial clock cycle(Read)	150			ns
T_{SHR}		SCL “H” pulse width(Read)	60			ns
T_{SLR}		SCL “L” pulse width(Read)	60			ns
T_{DCS}	DC	DC setup time	30			ns
T_{DCH}		DC hold time	30			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			150	ns
T_{OH}		Output disable time	15			ns

7.Command Table

W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: –: Don't Care

1) PANEL SETTING(PSR) (REGISTER:R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting the panel	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
	0	1	RES1	RES0	REG	KW/R	UD	SHL	SHD_N	RST_N
	0	1	-	-	-	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ

RES[1:0]: Display Resolution setting(source x gate)

00b: 400x300 (Default) Active source channels: S0 ~ S399. Active gate channels: G0~G299..
01b:320x300 Active source channels: S0 ~ S319. Active gate channels: G0~G299.
10b:320x240 Active source channels: S0 ~ S319. Active gate channels: G0~G239..
11b:200x300 Active source channels: S0 ~ S199. Active gate channels: G0~G299.

REG: LUT selection

0: LUT from OTP.(Default)
1: LUT from register.

BWR: Black / White / Red

0: Pixel with Black/White/Red, KWR mode. (Default)
1: Pixel with Black/White, KW mode.

UD: Gate Scan Direction

0: Scan down. First line to Last line:Gn-1→ Gn-2→ Gn-3→ …→ G0
1: Scan up.(Default) First line to Last line:G0→ G1→ G2→ …….→ Gn-1

SHL: Source Shift Direction

0: Shift left. First data to Last data:Sn-1→ Sn-2→ Sn-3→ …→ S0
1: Shift right.(Default) First data to Last data:S0→ S1→ S2→ …….→ Sn-1

SHD_N: Booster Switch

0: Booster OFF
1: Booster ON (Default)

When SHD_N becomes LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF. And Source/Gate/Border/VCOM will be released to floating.

RST_N: Soft Reset

0: Reset. Booster OFF, Register data are set to their default values, all drivers will be reset, and all functions will be disabled. Source/Gate/Border/VCOM will be released to floating. After soft reset is transmitted, the internal operation needs at least 50uS to execute. During this period of time, the BUSY_N pin keeps low and any command will be ignored.1: No effect (Default).

1: No effect (Default).

VCMZ: VCOM function
0: No effect (Default).
1: VCOM is always floating.

TS_AUTO: Temperature sensor will be activated automatically one time.
0: No effect (Default).
1: Before enabling booster.Temperature sensor will be activated automatically one time.

TIEG: VGL state function
0: No effect (Default)
1 : After power off booster, VGL will be tied to GND.

NORG: VCOM state during refreshing display
0: No effect (Default)
1: Expect refreshing display, VCOM is tied to GND.

VC_LUTZ: VCOM state during refreshing display
0: No effect (Default)
1: After refreshing display, the output of VCOM is set to floating automatically.

Note: Priority of Vcom setting: VCMZ > EOPT > NORG > VC_LUTZ

2） POWER SETTING(PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Selecting Internal /External Power	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	0	1	-	-	-	BD_EN	-	-	VDS_E	VDG_EN
	0	1	-	-	-	VCOM_SLEW	VGHL_LV[3:0]			
	0	1	-	-	VSH[5:0]					
	0	1	-	-	VSL[5:0]					
	0	1	OPTEN	VDHR[6:0]						

BD_EN: Border l do enable control
0: Border LDO disable(Default)
Border level selection:00b:VCOM 01b:VSH 10b:VSL 11b:VDHR
1: Border LDO enable
Border level selection:00b:VCOM 01b:VBH(VCOM-VSL)10b:VSL 11b:VDHR

VDS_EN: Source power selection
0 : External source power from VDH/VDL/VDHR pins
1 : Internal DC/DC function for generating VDH/VDL/VDHR(Default)

VDG_EN: Gate power selection
0 : External gate power from VGH/VGL pins
1 : Internal DC/DC function for generating VGH/VGL(Default)

VCOM_HV: VCOM Voltage Level
0: VCOMH=VSH+VCOM_DC, VCOML=VSL+VCOM_DC.(Default)
1: VCOMH=VGH, VCOML=VGL

VGHL_LV[1:0]: VGH / VGL Voltage Level selection.

VGHL_LV	VGHL Voltage Level
0000(Default)	VGH=20V, VGL=-20V
0001	VGH=19V, VGL=-19V
0010	VGH=18V, VGL=-18V
0011	VGH=17V, VGL=-17V
0100	VGH=16V, VGL=-16V
0101	VGH=15V, VGL=-15V
0110	VGH=14V, VGL=-14V
0111	VGH=13V, VGL=-13V
1000	VGH=12V, VGL=-12V
1001	VGH=11V, VGL=-11V
1010	VGH=10V, VGL=-10V

VSH[5:0]: Internal VSH power selection for B/W pixel.(Default value: 11 1111b)

VSH	Voltage	VSH	Voltage	VSH	Voltage	VSH	Voltage
000000	2.4V	010000	5.6V	100000	8.8V	110000	12.0V
000001	2.6V	010001	5.8V	100001	9.0V	110001	12.2V
000010	2.8V	010010	6.0V	100010	9.2V	110010	12.4V
000011	3.0V	010011	6.2V	100011	9.4V	110011	12.6V
000100	3.2V	010100	6.4V	100100	9.6V	110100	12.8V
000101	3.4V	010101	6.6V	100101	9.8V	110101	13.0V

000110	3.6V	010110	6.8V	100110	10.0V	110110	13.2V
000111	3.8V	010111	7.0V	100111	10.2V	110111	13.4V
001000	4.4V	011000	7.2V	101000	10.4V	111000	13.6V
001001	4.2V	011001	7.4V	101001	10.6V	111001	13.8V
001010	4.4V	011010	7.6V	101010	10.8V	111010	14.0V
001011	4.6V	011011	7.8V	101011	11.0V	111011	14.2V
001100	4.8V	011100	8.0V	101100	11.2V	111100	14.4V
001101	5.0V	011101	8.2V	101101	11.4V	111101	14.6V
001110	5.2V	011110	8.4V	101110	11.6V	111110	14.8V
001111	5.4V	011111	8.6V	101111	11.8V	111111	15.0V

VSL[5:0]: Internal VSL power selection for B/W pixel. (Default value: 11 1111b)

VSL	Voltage	VSL	Voltage	VSL	Voltage	VSL	Voltage
000000	-2.4V	010000	-5.6V	100000	-8.8V	110000	-12.0V
000001	-2.6V	010001	-5.8V	100001	-9.0V	110001	-12.2V
000010	-2.8V	010010	-6.0V	100010	-9.2V	110010	-12.4V
000011	-3.0V	010011	-6.2V	100011	-9.4V	110011	-12.6V
000100	-3.2V	010100	-6.4V	100100	-9.6V	110100	-12.8V
000101	-3.4V	010101	-6.6V	100101	-9.8V	110101	-13.0V
000110	-3.6V	010110	-6.8V	100110	-10.0V	110110	-13.2V
000111	-3.8V	010111	-7.0V	100111	-10.2V	110111	-13.4V
001000	-4.4V	011000	-7.2V	101000	-10.4V	111000	-13.6V
001001	-4.2V	011001	-7.4V	101001	-10.6V	111001	-13.8V
001010	-4.4V	011010	-7.6V	101010	-10.8V	111010	-14.0V
001011	-4.6V	011011	-7.8V	101011	-11.0V	111011	-14.2V
001100	-4.8V	011100	-8.0V	101100	-11.2V	111100	-14.4V
001101	-5.0V	011101	-8.2V	101101	-11.4V	111101	-14.6V
001110	-5.2V	011110	-8.4V	101110	-11.6V	111110	-14.8V
001111	-5.4V	011111	-8.6V	101111	-11.8V	111111	-15.0V

VDHR[5:0]: Internal VDHR power selection for Red pixel. (Default value: 001101b)

VDHR	Voltage	VDHR	Voltage	VDHR	Voltage	VDHR	Voltage
000000	2.4V	010000	5.6V	100000	8.8V	110000	12.0V
000001	2.6V	010001	5.8V	100001	9.0V	110001	12.2V
000010	2.8V	010010	6.0V	100010	9.2V	110010	12.4V
000011	3.0V	010011	6.2V	100011	9.4V	110011	12.6V
000100	3.2V	010100	6.4V	100100	9.6V	110100	12.8V
000101	3.4V	010101	6.6V	100101	9.8V	110101	13.0V
000110	3.6V	010110	6.8V	100110	10.0V	110110	13.2V
000111	3.8V	010111	7.0V	100111	10.2V	110111	13.4V
001000	4.4V	011000	7.2V	101000	10.4V	111000	13.6V
001001	4.2V	011001	7.4V	101001	10.6V	111001	13.8V
001010	4.4V	011010	7.6V	101010	10.8V	111010	14.0V
001011	4.6V	011011	7.8V	101011	11.0V	111011	14.2V
001100	4.8V	011100	8.0V	101100	11.2V	111100	14.4V
001101	5.0V	011101	8.2V	101101	11.4V	111101	14.6V
001110	5.2V	011110	8.4V	101110	11.6V	111110	14.8V
001111	5.4V	011111	8.6V	101111	11.8V	111111	15.0V

OPTEN: 1 enable step-0.1V voltage selection.

VDHR	Voltage	VDHR	Voltage	VDHR	Voltage	VDHR	Voltage
1000 0000	2.4 V	1010 0000	5.6 V	1100 0000	8.8 V	1110 0000	12 V
1000 0001	2.5 V	1010 0001	5.7 V	1100 0001	8.9 V	1110 0001	12.1 V
1000 0010	2.6 V	1010 0010	5.8 V	1100 0010	9.0 V	1110 0010	12.2 V
1000 0011	2.7 V	1010 0011	5.9 V	1100 0011	9.1 V	1110 0011	12.3 V
1000 0100	2.8 V	1010 0100	6.0 V	1100 0100	9.2 V	1110 0100	12.4 V
1000 0101	2.9 V	1010 0101	6.1 V	1100 0101	9.3 V	1110 0101	12.5 V
1000 0110	3.0 V	1010 0110	6.2 V	1100 0110	9.4 V	1110 0110	12.6 V
1000 0111	3.1 V	1010 0111	6.3 V	1100 0111	9.5 V	1110 0111	12.7 V
1000 1000	3.2 V	1010 1000	6.4 V	1100 1000	9.6 V	1110 1000	12.8 V
1000 1001	3.3 V	10101001	6.5 V	1100 1001	9.7 V	1110 1001	12.9 V
1000 1010	3.4 V	1010 1010	6.6 V	1100 1010	9.8 V	1110 1010	13.0 V
1000 1011	3.5 V	1010 1011	6.7 V	1100 1011	9.9 V	1110 1011	13.1 V
1000 1100	3.6 V	1010 1100	6.8 V	1100 1100	10.0 V	1110 1100	13.2 V
1000 1101	3.7 V	1010 1101	6.9 V	1100 1101	10.1 V	1110 1101	13.3 V
1000 1110	3.8 V	1010 1110	7.0 V	1100 1110	10.2 V	1110 1110	13.4 V
1000 1111	3.9 V	1010 1111	7.1 V	1100 1111	10.3 V	1110 1111	13.5 V
1001 0000	4.0 V	1011 0000	7.2 V	1101 0000	10.4 V	1111 0000	13.6 V
1001 0001	4.1 V	1011 0001	7.3 V	1101 0001	10.5 V	1111 0001	13.7 V
1001 0010	4.2 V	1011 0010	7.4 V	1101 0010	10.6 V	1111 0010	13.8 V
1001 0011	4.3 V	1011 0011	7.5 V	1101 0011	10.7 V	1111 0011	13.9 V
1001 0100	4.4 V	1011 0100	7.6 V	1101 0100	10.8 V	1111 0100	14.0 V
1001 0101	4.5 V	1011 0101	7.7 V	1101 0101	10.9 V	1111 0101	14.1 V
1001 0110	4.6 V	1011 0110	7.8 V	1101 0110	11.0 V	1111 0110	14.2 V
1001 0111	4.7 V	1011 0111	7.9 V	1101 0111	11.1 V	1111 0111	14.3 V
1001 1000	4.8 V	1011 1000	8.0 V	1101 1000	11.2 V	1111 1000	14.4 V
1001 1001	4.9 V	1011 1001	8.1 V	1101 1001	11.3 V	1111 1001	14.5 V
1001 1010	5.0 V	1011 1010	8.2 V	1101 1010	11.4 V	1111 1010	14.6 V
1001 1011	5.1 V	1011 1011	8.3 V	1101 1011	11.5 V	1111 1011	14.7 V
1001 1100	5.2 V	1011 1100	8.4 V	11011100	11.6 V	1111 1100	14.8 V
1001 1101	5.3 V	1011 1101	8.5 V	1101 1101	11.7 V	1111 1101	14.9 V
1001 1110	5.4 V	1011 1110	8.6 V	1101 1110	11.8 V	1111 1110	15.0 V
1001 1111	5.5 V	1011 1111	8.7 V	1101 1111	11.9 V		

3）POWER OFF(POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

After the Power OFF command, the driver will be powered OFF. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode. Source/Gate/Border/VCOM will be released to floating

4）POWER OFF SEQUENCE SETTING(PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Power OFF sequence	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-

T_VDS_OFF[1:0]: Source to gate power off interval time.
00b: 1 frame(Default) 01b: 2frames 10b: 3frames 11b: 4frame

5）POWER ON(PON) (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the power	0	0	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**

After the Power ON command, the driver will be powered ON. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUSY_N signal will return to high.

6）POWER ON MEASURE(PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**

This command enables the internal bandgap, which will be cleared by the next POF.

7）BOOSTER SOFT START(BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**
	0	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0
	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0

BTPHA[7:6]: Soft start period of phase A.

00b:10mS 01b:20mS 10b:30mS 11b:40mS

BTPHA[5:3]: Driving strength of phase A

000b: strength1 001b: strength2 010b: strength3 011b: strength4

100b: strength5 101b: strength6 110b: strength7 111b: strength 8(strongest)

BTPHA[2:0]: Minimum OFF time setting of GDR in phase A

000b:0.27uS 001b:0.34uS 010b:0.40uS 011b:0.54uS

100b:0.80uS 101b:1.54uS 110b:3.34uS 111b:6.58uS

BTPHB[7:6]: Soft start period of phase B

00b:10mS 01b:20mS 10b:30mS 11b:40mS

BTPHB[5:3]: Driving strength of phase B

000b: strength1 001b: strength2 010b: strength3 011b: strength4

100b: strength5 101b: strength6 110b: strength7 111b: strength 8 (strongest)

BTPHB[2:0]: Minimum OFF time setting of GDR in phase B

000b:0.27uS 001b:0.34uS 010b:0.40uS 011b:0.54uS

100b:0.80uS 101b:1.54uS 110b:3.34uS 111b:6.58uS

BTPHC[5:3]: Driving strength of phase C

000b: strength1 001b: strength2 010b: strength3 011b: strength4

100b: strength5 101b: strength6 110b: strength7 111b: strength 8 (strongest)

BTPHC[2:0]: Minimum OFF time setting of GDR in phase C

000b:0.27uS 001b:0.34uS 010b:0.40uS 011b:0.54uS

100b:0.80uS 101b:1.54uS 110b:3.34uS 111b:6.58uS

8）DEEP SLEEP(DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep Sleep	0	0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**
	0	1	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

9）DATA START TRANSMISSION 1(DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	:	:	:	:	:	:	:	:
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes “OLD” data to SRAM.

In KWR mode, this command writes “B/W” data to SRAM.

In Program mode, this command writes “OTP” data to SRAM for programming.

10）DATA STOP(DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Stopping data transmission	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**1**
	1	1	data_flag	-	-	-	-	-	-	-

Check the completeness of data. If data is complete, start to refresh display.

Data_flag: Data flag of receiving user data.

0: Driver didn’t receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After “Data Start” (R10h) or “Data Stop” (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY_N signal will become “0”.

11) DISPLAY REFRESH(DRF) (R12H)

Action	W/R	C/D	D7	D5	D4	D3	D2	D1	D0
Refreshing the display	0	0	**0**	**0**	**1**	**0**	**0**	**1**	**0**

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY_N signal will become “0” and the refreshing of panel starts.

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**1**
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	:	:	:	:	:	:	:	:
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

The waiting interval from BUSY_N falling to the first FLG command must be larger than 200uS.

12) DATA START TRANSMISSION 2(DTM2) (R13H)

This command start transmitting data and write the min to SRAM.

In K/W mode, this command writes “NEW” data to SRAM.

In K/W/Red mode, this command writes “RED” data to SRAM.

13) VCOM LUT(LUTC) (R20H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-up Table for VCOM (57-byte command, structure of bytes2~8 Repeated 8 times)	0	0	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**
	0	1	Group Repeat Time [7:0]							
	0	1	Level Select 1-1[1:0]		Frame number 1-1 [5:0]					
	0	1	Level Select 1-2[1:0]		Frame number 1-2 [5:0]					
	0	1	Level Select 2-1[1:0]		Frame number 2-1 [5:0]					
	0	1	Level Select 2-2[1:0]		Frame number 2-2[5:0]					
	0	1	State 1 repeat times [7:0]							
	0	1	State 2 repeat times [7:0]							

This command stores VCOM Look-Up Table with 8 groups of data. This LUT includes 8 kinds of groups;Each group is of 7 bytes.Each group is divied to 2states and group repeat number.Each state made up 2 phases and each phase is combined with repeat time,level selection and frame number.

Bytes 2, 9,16,23,30...:

Group repeat times

0000 0000b: No repeat

0000 0000b~1111 1111b: Repeat 1~255times

Bytes 3~6,10~13,17~20,24~27,31~34...:

D[7:6]Level Selection

00b:VCOM_DC

01b: VSH+VCOM_DC(VCOMH)

10b: VSL-VCOM_DC(VCOML)

11b:Floating

D[5:0]Number of Frames (state 1&state 2)

00 0000b: 0 time

: :

: :

11 1111b: 63 times

Bytes 7~8, 14~15，21~22，28~29，35~36，...:

State 1&State 2 repeat times

0000 0000b: No repeat

0000 0000b~1111 1111b: 1~255times

If KW/R=0 (KWR mode), all 8 groups are used.

If KW/R=1(KW mode), only 6 groups are used.

14) W2W LUT(LUTWW) (R21H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build White Look-up Table for W2W (43-byte command, structure of bytes 2~8 repeated 6 times)	0	0	0	0	1	0	0	0	0	1
	0	1	Group Repeat Time [7:0]							
	0	1	Level Select 1-1[1:0]		Frame number 1-1 [5:0]					
	0	1	Level Select 1-2[1:0]		Frame number 1-2 [5:0]					
	0	1	Level Select 2-1[1:0]		Frame number 2-1 [5:0]					
	0	1	Level Select 2-2[1:0]		Frame number 2-2[5:0]					
	0	1	State 1 repeat times [7:0]							
	0	1	State 2 repeat times [7:0]							

This command stores LUTW2W Look-Up Table with 6 groups of data. This LUT includes 6 kinds of groups; each group is of 7 bytes. Each group is divied to 2states and group repeat number. Each state made up 2 phases and each phase is combined with repeat time, level selection and frame number.

Bytes 2, 9, 16, 23 , 30,… :

Group repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

Bytes 3~6, 10~13, 17~20, 24~27, 31~34……:

[D7:D6] Level selection

00b: 0V

01b: VSH

10b: VSL

11b: VDHR

[D5:D0] Number of Frames (state1 & state2)

00 0000b: 0 time

: :

: :

11 1111b: 63 times

Bytes 7~8, 14~15, 21~22, 28~29, 35~36,..:

State 1 & State 2 repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: 1 ~ 255times

If KW/R=0 (KWR mode), LUTWW is not used.

If KW/R=1 (KW mode), LUTWW is used.

15) K2W LUT(LUTKW/LUTR) (R22H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-up Table for K2W or Red (57-byte command, structure of bytes 2~8 repeated 8 times)	0	0	0	0	1	0	0	0	0	1
	0	1	Group Repeat Time [7:0]							
	0	1	Level Select 1-1[1:0]		Frame number 1-1 [5:0]					
	0	1	Level Select 1-2[1:0]		Frame number 1-2 [5:0]					
	0	1	Level Select 2-1[1:0]		Frame number 2-1 [5:0]					
	0	1	Level Select 2-2[1:0]		Frame number 2-2[5:0]					
	0	1	State 1 repeat times [7:0]							
	0	1	State 2 repeat times [7:0]							

This command stores LUTKW / LUTR Look-Up Table with 8 groups of data. This LUT includes 8 kinds of groups; each group is of 7 bytes. Each group is divied to 2states and group repeat number. Each state made up 2 phases and each phase is combined with repeat time, level selection and frame number.

Bytes 2, 9, 16, 23 , 30,… :

Group repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

Bytes 3~6, 10~13, 17~20, 24~27, 31~34……:

[D7:D6] Level selection

00b: 0V

01b: VSH

10b: VSL

11b: VDHR

[D5:D0] Number of Frames (state1 & state2)

00 0000b: 0 time

: :

11 1111b: 63 times

Bytes 7~8, 14~15, 21~22, 28~29, 35~36,..:

State 1 & State 2 repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: 1 ~ 255times

If KW/R=0 (KWR mode), all 8 groups are used.

If KW/R=1 (KW mode), only 6 groups are used.

16) W2K LUT (LUTWK / LUTW) (R23H)

This command builds Look-up Table for White-to-Black. Please refer to W2W LUT (LUTWW) for similar definition details.
Regardless of KW/R=0 or KW/R=1, LUTWK/LUTW is used

17) K2K LUT(LUTKK/LUTK) (R24H)

This command builds Look-up Table for Black-to-Black. Please refer to W2W LUT (LUTWW) for similar definition details. Regardless of KW/R=0 or KW/R=1, LUTKK/LUTK is used.
Note: All LUTs are independent of each other and could be deal with separately.If waveform time is different for each LUT , IC would elect longest LUT as refresh time and fill 0 (GND) to remaining refresh time for other LUT.

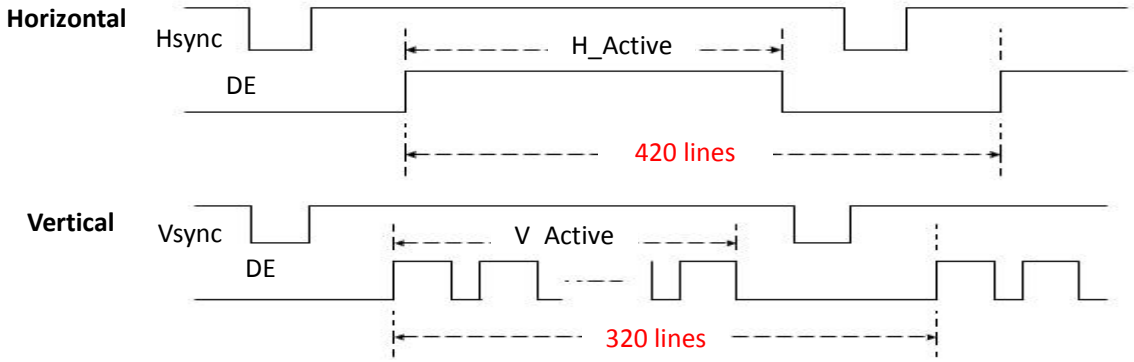
18) PLL CONTROL(PLL)(R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Controlling PLL	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**
	0	1	**-**	**-**	**-**	**FRS[4:0]**				

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

FRS	Frame rate
00000	5 Hz
00001	10 Hz
00010	15 Hz
00011	20 Hz
00100	25 Hz
00101	30 Hz
00110	35 Hz
00111	40 Hz
01000	45 Hz
01001	50 Hz
01010	55 Hz
01011	60 Hz
01100	65 Hz
01101	70 Hz
01110	75 Hz
01111	80 Hz

FRS	Frame rate
10000	85 Hz
10001	90 Hz
10010	95 Hz
10011	100 Hz
10100	105 Hz
10101	110 Hz
10110	115 Hz
10111	120 Hz
11000	130 Hz
11001	140 Hz
11010	150 Hz
11011	160 Hz
11100	170Hz
11101	180 Hz
11110	190 Hz
11111	200 Hz



19)TEMPERATURE SENSOR CALIBRATION(TSC) (R40H)

Action	W/	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	0	0	0	0	0	0
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6/TS3	D5/TS2	D4/TS1	D3/TS0
	1	1	D2	D1	D0	-	-	-	-	-

This command enables internal or external temperature sensor, and reads the result.

TS[7:0]:When TSE(R41h) is set to 0,this command reads internal temperature sensor value.

D[10:0]:When TSE(R41h) is set to 1,this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temperature(^oC)	TS[7:0]/D[10:3]	Temperature(^oC)	TS[7:0]/D[10:3]	Temperature(^oC)
1110_0111	-25	0000_0000	0	0001_1001	25
1110_1000	-24	0000_0001	1	0001_1010	26
1110_1001	-23	0000_0010	2	0001_1011	27
1110_1010	-22	0000_0011	3	0001_1100	28
1110_1011	-21	0000_0100	4	0001_1101	29
1110_1100	-20	0000_0101	5	0001_1110	30
1110_1101	-19	0000_0110	6	0001_1111	31
1110_1110	-18	0000_0111	7	0010_0000	32
1110_1111	-17	0000_1000	8	0010_0001	33
1111_0000	-16	0000_1001	9	0010_0010	34
1111_0001	-15	0000_1010	10	0010_0011	35
1111_0010	-14	0000_1011	11	0010_0100	36
1111_0011	-13	0000_1100	12	0010_0101	37
1111_0100	-12	0000_1101	13	0010_0110	38
1111_0101	-11	0000_1110	14	0010_0111	39
1111_0110	-10	0000_1111	15	0010_1000	40
1111_0111	-9	0001_0000	16	0010_1001	41
1111_1000	-8	0001_0001	17	0010_1010	42
1111_1001	-7	0001_0010	18	0010_1011	43
1111_1010	-6	0001_0011	19	0010_1100	44
1111_1011	-5	0001_0100	20	0010_1101	45
1111_1100	-4	0001_0101	21	0010_1110	46
1111_1101	-3	0001_0110	22	0010_1111	47
1111_1110	-2	0001_0111	23	0011_0000	48
1111_1111	-1	0001_1000	24	0011_0001	49

20) TEMPERATURE SENSOR ENABLE(TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enable Temperature Sensor /Offset	0	0	0	1	0	0	0	0	0	1
	0	1	TSE	-	-	-	TO[3:0]			

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable(default) 1: Disable; using external sensor.

TO[3:0]: Temperature offset.

TO[3:0]	Calculation
0000b	+0(Default)
0001	+1
0010	+2
0011	+3
0100	+4
0101	+5
0110	+6
0111	+7

TO[3:0]	Calculation
1000	-8
1001	-7
1010	-6
1011	-5
1100	-4
1101	-3
1110	-2
1111	-1

21) TEMPERATURE SENSOR WRITE(TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Write External Temperature Sensor	0	0	0	1	0	0	0	0	1	0
	0	1	WATTR[7:0]							
	0	1	WMSB[7:0]							
	0	1	WLSB[7:0]							

This command writes the temperature sensed by the temperature sensor.

WATTR[7:6]: I^2C Write Byte Number

00b : 1 byte (head byte only)

01b : 2 bytes (head byte +pointer)

10b : 3 bytes (head byte + pointer + 1st parameter)

11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

WATTR[5:3]: User-defined address bits (A2, A1,A0)

WATTR[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor

22)TEMPERATURE SENSOR READ(TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read External Temperature Sensor	0	0	0	1	0	0	0	0	1	1
	1	1	RMSB[7:0]							
	1	1	RLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.
RMSB[7:0]: MS Byte read data from external temperature sensor.
RLSB[7:0]: LS Byte read data from external temperature sensor.

23)VCOM AND DATA INTERVAL SETTING(CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval between VCOM and Data	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**
	0	1	VBD[1:0]		DDX[1:0]		CDI[3:0]			

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

VBD[1:0]: Border data selection

KWR mode (KW/R=0)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTK
1 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	Floating

KW mode (KW/R=1)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	Floating
1 (Default)	00	Floating
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	Floating

DDX[1:0]: Data polality.

Under KWR mode (KW/R=0):

DDX[1] is for RED data.
DDX[0] is for B/W data,

DDX[1:0]	Data {Red, B/W}	LUT
00	00	LUTW
	01	LUTK
	10	LUTR
	11	LUTR
01 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTR

DDX[1:0]	Data {Red, B/W}	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTK
11	00	LUTR
	01	LUTR
	10	LUTK
	11	LUTW

Under KW mode (KW/R=1):

DDX[1]=0 is for KW mode with NEW/OLD,
DDX[1]=1 is for KW mode without NEW/OLD.

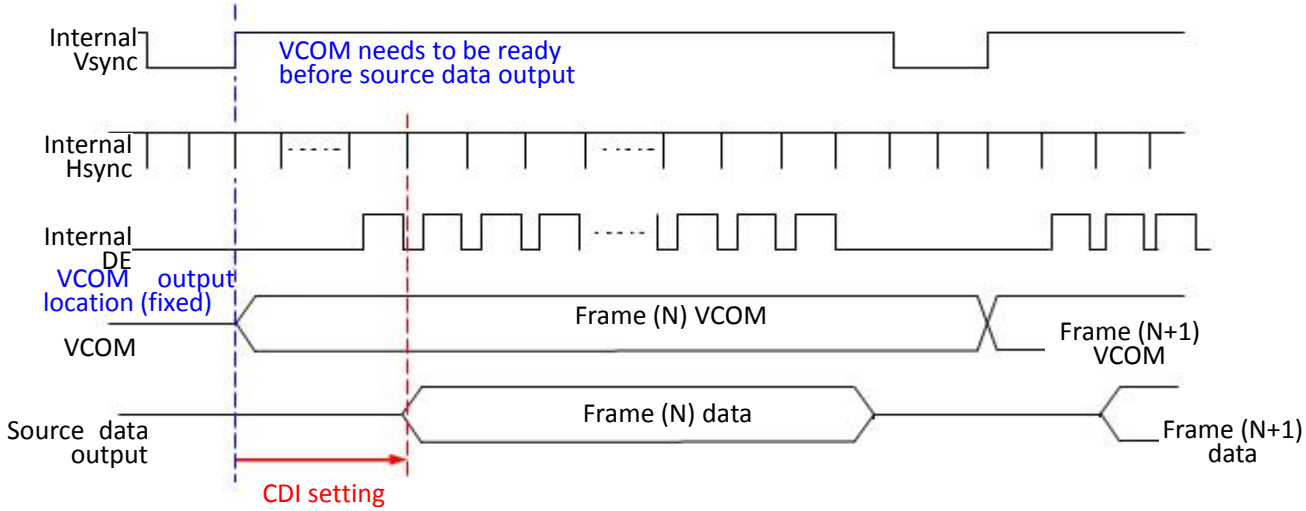
DDX[1:0]	Data {NEW, OLD}	LUT
00	00	LUTWW (0 → 0)
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (1 → 1)
01 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTWW (1 → 1)

DDX[1:0]	Data {NEW}	LUT
10	0	LUTKW (1 → 0)
	1	LUTWK (0 → 1)
11	0	LUTWK (1 → 0)
	1	LUTKW (0 → 1)

CDI[3:0]: VCOM and data interval

CDI[3:0]	VCOM and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	**10 (Default)**

CDI[3:0]	VCOM and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



24) Low Power Detection (LPD) (R51h)

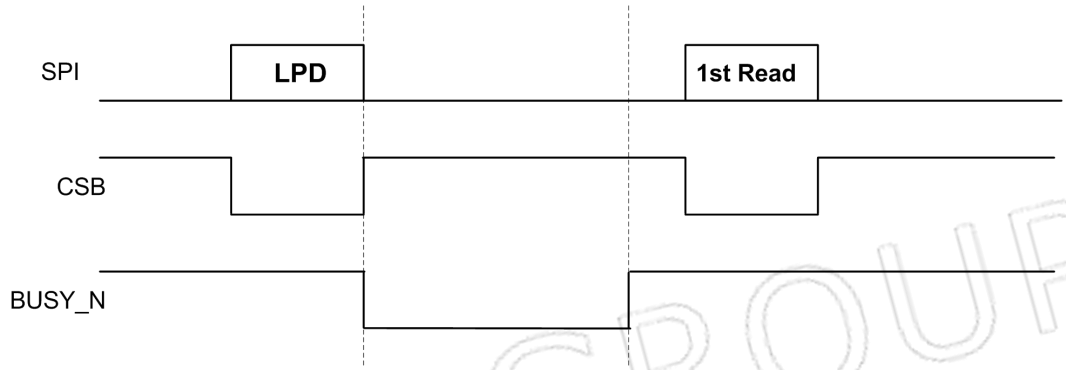
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Detect Low Power	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**
	1	1	-	-	-	-	-	-	-	LPD

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal Low Power Detection Flag

0: Low power input (V_{DD}<2.5V, selected by LVD_SEL[1:0] in command LVSEL)

1: Normal status (default)



25) TCON Setting (TCON) (R60h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Gate/Source Non-overlap Period	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**
	0	1	S2G[3:0]				G2S[3:0]			

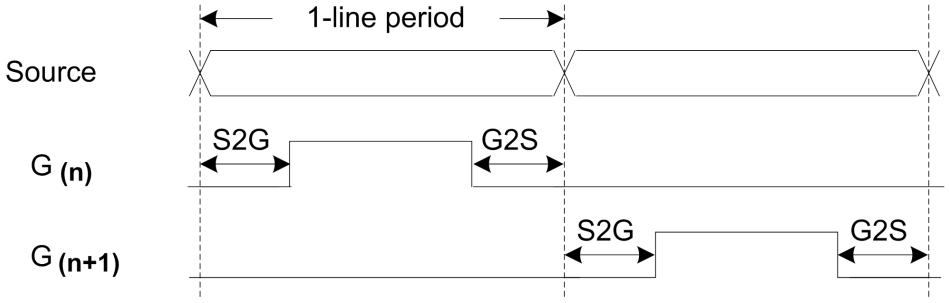
This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000 b	4
0001	8
0010	**12 (Default)**
0011	16
0100	20
0101	24
0110	28
0111	32

S2G[3:0] or G2S[3:0]	Period
1000 b	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	60
1111	64

Period Unit = 650 nS.



26) Resolution Setting (TRES) (R61h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Resolution	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**
	0	1	-	-	-	-	-	-	-	HRES[8]
	0	1	HRES[7:3]					**0**	**0**	**0**
	0	1	-	-	-	-	-	-	-	VRES[8]
	0	1	VRES[7:0]							

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[7:3]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Active channel calculation, assuming HST[7:0]=0, VST[8:0]=0:

Gate: First active gate = G0;
Last active gate = VRES[8:0] – 1

Source: First active source = S0;
Last active source = HRES[7:3]*8 - 1

Example: 128 (source) x 272 (gate), assuming HST[7:0]=0, VST[8:0]=0

Gate: First active gate = G0,
Last active gate = G271; (VRES[8:0] = 272, 272 - 1= 271)

Source: First active source = S0,
Last active source = S127; (HRES[7:3]=16, 16*8 – 1 = 127)

27) Revision (REV) (R70h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Chip Revision	0	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**
	1	1	RESERVED							
			CHIP_REV[7:0]							
	1	1	LUT_REV[7:0]							
	1	1	LUT_REV[15:8]							
	1	1	LUT_REV[23:16]							

The LUT_REV is read from OTP address = 0x001A~0x001C/0x0C1A~0x0C1C

CHIP_REV [3:0]: Chip Revision,fixed at 0x07h.

28) Auto Measure VCOM (AMV) (R80h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure VCOM	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE

This command controls automatic VCOM measurement mechanism.

AMVT[1:0]: Auto Measure VCOM Time

00b: 3s **01b: 5s (default)**
10b: 8s 11b: 10s

XON: All Gate ON of AMV

0: Gate normally scan during Auto Measure VCOM period. (default)
1: All Gate ON during Auto Measure VCOM period.

AMVS: Source output of AMV

0: Source output 0V during Auto Measure VCOM period. (default)
1: Source output VDHR during Auto Measure VCOM period.

AMV: Analog signal

0: Get VCOM value with the VV command (R81h) (default)
1: Get VCOM value in analog signal. (External analog to digital converter)

AMVE: Auto Measure VCOM Enable (/Disable)

0: No effect (default)
1: Trigger auto VCOM sensing.

29) VCOM Value (VV) (R81h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure VCOM	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	1	1	-	VV[6:0]						

This command gets the VCOM value.

VV[6:0]: VCOM Value Output

VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)
000 0000b	-0.1	010 1011b	-4.4	101 0110b	-8.7
000 0001b	-0.2	010 1100b	-4.5	101 0111b	-8.8
000 0010b	-0.3	010 1101b	-4.6	101 1000b	-8.9
000 0011b	-0.4	010 1110b	-4.7	101 1001b	-9.0
000 0100b	-0.5	010 1111b	-4.8	101 1010b	-9.1
000 0101b	-0.6	011 0000b	-4.9	101 1011b	-9.2
000 0110b	-0.7	011 0001b	-5	101 1100b	-9.3
000 0111b	-0.8	011 0010b	-5.1	101 1101b	-9.4
000 1000b	-0.9	011 0011b	-5.2	101 1110b	-9.5
000 1001b	-1	011 0100b	-5.3	101 1111b	-9.6
000 1010b	-1.1	011 0101b	-5.4	110 0000b	-9.7
000 1011b	-1.2	011 0110b	-5.5	110 0001b	-9.8
000 1100b	-1.3	011 0111b	-5.6	110 0010b	-9.9
000 1101b	-1.4	011 1000b	-5.7	110 0011b	-10
000 1110b	-1.5	011 1001b	-5.8	110 0100b	-10.1
000 1111b	-1.6	011 1010b	-5.9	110 0101b	-10.2
001 0000b	-1.7	011 1011b	-6	110 0110b	-10.3
001 0001b	-1.8	011 1100b	-6.1	110 0111b	-10.4
001 0010b	-1.9	011 1101b	-6.2	110 1000b	-10.5
001 0011b	-2	011 1110b	-6.3	110 1001b	-10.6
001 0100b	-2.1	011 1111b	-6.4	110 1010b	-10.7
001 0101b	-2.2	100 0000b	-6.5	110 1011b	-10.8
001 0110b	-2.3	100 0001b	-6.6	110 1100b	-10.9
001 0111b	-2.4	100 0010b	-6.7	110 1101b	-11
001 1000b	-2.5	100 0011b	-6.8	110 1110b	-11.1
001 1001b	-2.6	100 0100b	-6.9	110 1111b	-11.2
001 1010b	-2.7	100 0101b	-7.0	111 0000b	-11.3
001 1011b	-2.8	100 0110b	-7.1	111 0001b	-11.4
001 1100b	-2.9	100 0111b	-7.2	111 0010b	-11.5

001 1101b	-3.0	100 1000b	-7.3	111 0011b	-11.6
001 1110b	-3.1	100 1001b	-7.4	111 0100b	-11.7
001 1111b	-3.2	100 1010b	-7.5	111 0101b	-11.8
010 0000b	-3.3	100 1011b	-7.6	111 0110b	-11.9
010 0001b	-3.4	100 1100b	-7.7	111 0111b	-12
010 0010b	-3.5	100 1101b	-7.8	111 1000b	-12.1
010 0011b	-3.6	100 1110b	-7.9	111 1001b	-12.2
010 0100b	-3.7	100 1111b	-8.0	111 1010b	-12.3
010 0101b	-3.8	101 0000b	-8.1	111 1011b	-12.4
010 0110b	-3.9	101 0001b	-8.2	111 1100b	-12.5
010 0111b	-4	101 0010b	-8.3	111 1101b	-12.6
010 1000b	-4.1	101 0011b	-8.4	111 1110b	-12.7
010 1001b	-4.2	101 0100b	-8.5		
010 1010b	-4.3	101 0101b	-8.6		

30) VCOM_DC Setting (VDCS) (R82h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set VCOM_DC	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
	0	1	-	VDCS[5:0]						

This command sets VCOM_DC value

VDCS[6:0]: VCOM_DC Setting

VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)
000 0000b	-0.1	010 1011b	-4.4	101 0110b	-8.7
000 0001b	-0.2	010 1100b	-4.5	101 0111b	-8.8
000 0010b	-0.3	010 1101b	-4.6	101 1000b	-8.9
000 0011b	-0.4	010 1110b	-4.7	101 1001b	-9.0
000 0100b	-0.5	010 1111b	-4.8	101 1010b	-9.1
000 0101b	-0.6	011 0000b	-4.9	101 1011b	-9.2
000 0110b	-0.7	011 0001b	-5	101 1100b	-9.3
000 0111b	-0.8	011 0010b	-5.1	101 1101b	-9.4
000 1000b	-0.9	011 0011b	-5.2	101 1110b	-9.5
000 1001b	-1	011 0100b	-5.3	101 1111b	-9.6
000 1010b	-1.1	011 0101b	-5.4	110 0000b	-9.7
000 1011b	-1.2	011 0110b	-5.5	110 0001b	-9.8
000 1100b	-1.3	011 0111b	-5.6	110 0010b	-9.9
000 1101b	-1.4	011 1000b	-5.7	110 0011b	-10
000 1110b	-1.5	011 1001b	-5.8	110 0100b	-10.1
000 1111b	-1.6	011 1010b	-5.9	110 0101b	-10.2
001 0000b	-1.7	011 1011b	-6	110 0110b	-10.3
001 0001b	-1.8	011 1100b	-6.1	110 0111b	-10.4
001 0010b	-1.9	011 1101b	-6.2	110 1000b	-10.5
001 0011b	-2	011 1110b	-6.3	110 1001b	-10.6
001 0100b	-2.1	011 1111b	-6.4	110 1010b	-10.7
001 0101b	-2.2	100 0000b	-6.5	110 1011b	-10.8
001 0110b	-2.3	100 0001b	-6.6	110 1100b	-10.9
001 0111b	-2.4	100 0010b	-6.7	110 1101b	-11

001 1000b	-2.5	100 0011b	-6.8	110 1110b	-11.1
001 1001b	-2.6	100 0100b	-6.9	110 1111b	-11.2
001 1010b	-2.7	100 0101b	-7.0	111 0000b	-11.3
001 1011b	-2.8	100 0110b	-7.1	111 0001b	-11.4
001 1100b	-2.9	100 0111b	-7.2	111 0010b	-11.5
001 1101b	-3.0	100 1000b	-7.3	111 0011b	-11.6
001 1110b	-3.1	100 1001b	-7.4	111 0100b	-11.7
001 1111b	-3.2	100 1010b	-7.5	111 0101b	-11.8
010 0000b	-3.3	100 1011b	-7.6	111 0110b	-11.9
010 0001b	-3.4	100 1100b	-7.7	111 0111b	-12
010 0010b	-3.5	100 1101b	-7.8	111 1000b	-12.1
010 0011b	-3.6	100 1110b	-7.9	111 1001b	-12.2
010 0100b	-3.7	100 1111b	-8.0	111 1010b	-12.3
010 0101b	-3.8	101 0000b	-8.1	111 1011b	-12.4
010 0110b	-3.9	101 0001b	-8.2	111 1100b	-12.5
010 0111b	-4	101 0010b	-8.3	111 1101b	-12.6
010 1000b	-4.1	101 0011b	-8.4	111 1110b	-12.7
010 1001b	-4.2	101 0100b	-8.5		
010 1010b	-4.3	101 0101b	-8.6		

31) Program Mode (PGM) (RA0h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enter Program Mode	0	0	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**

After this command is issued, the chip would enter the program mode.

After the programming procedure completed, a hardware reset is necessary for leaving program mode.

32) Active Program (APG) (RA1h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Active Program OTP	0	0	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**1**

After this command is transmitted, the programming state machine would be activated.

The BUSY_N flag would fall to 0 until the programming is completed.

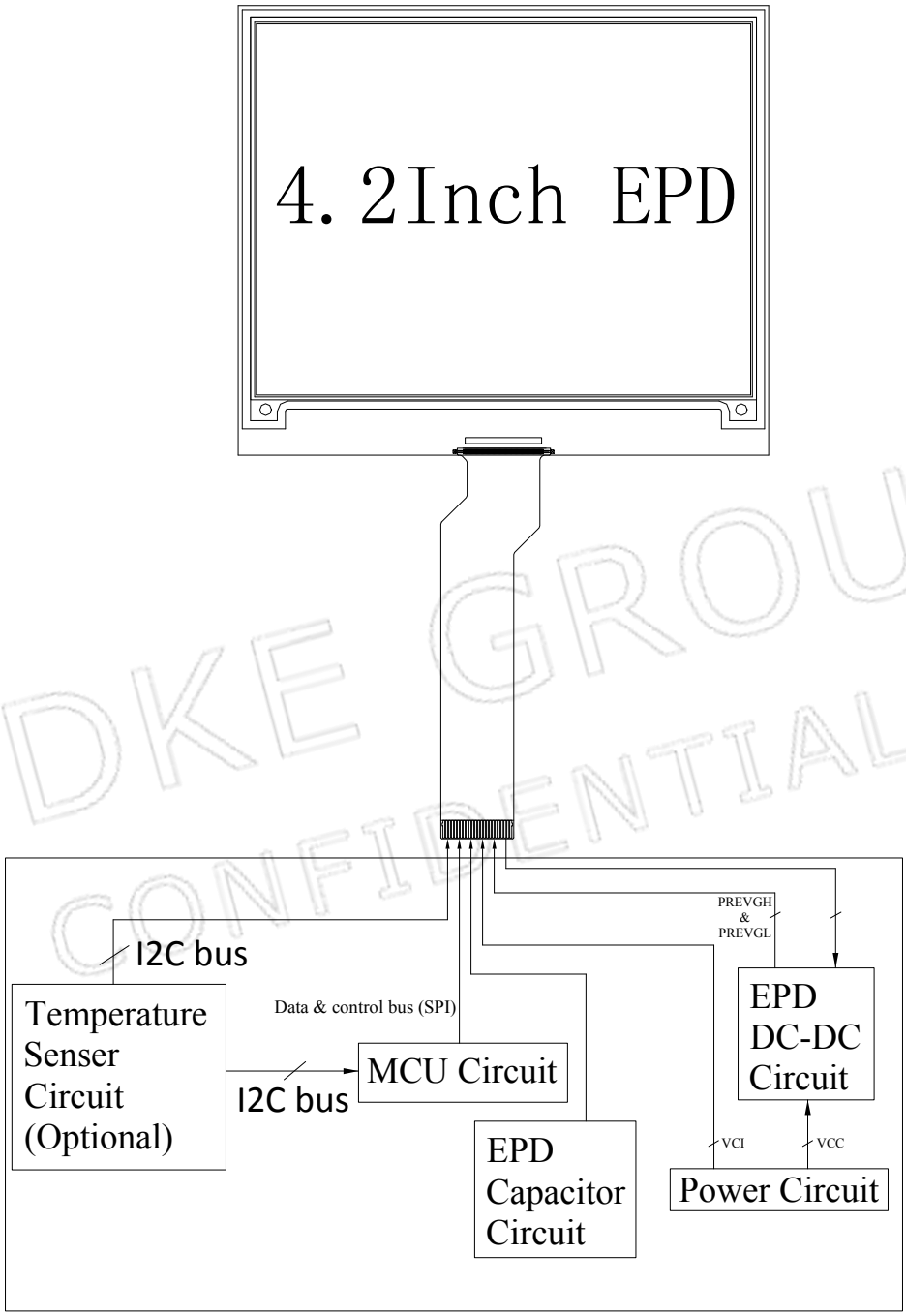
33) Read OTP Data (ROTP) (RA2h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read OTP data for check	0	0	**1**	**0**	**1**	**0**	**0**	**0**	**1**	**0**
	1	1	Dummy							
	1	1	The data of address 0x000 in the OTP							
	1	1	The data of address 0x001 in the OTP							
	1	1	:							
	1	1	The data of address (n-1) in the OTP							
	1	1	The data of address (n) in the OTP							

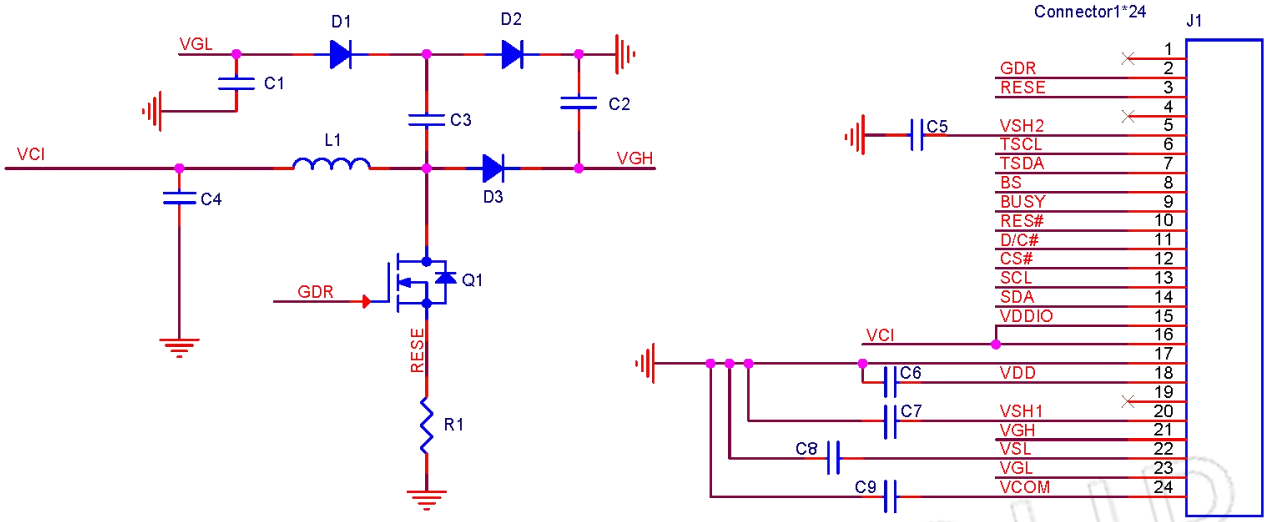
The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0xFFF.

8. Block Diagram



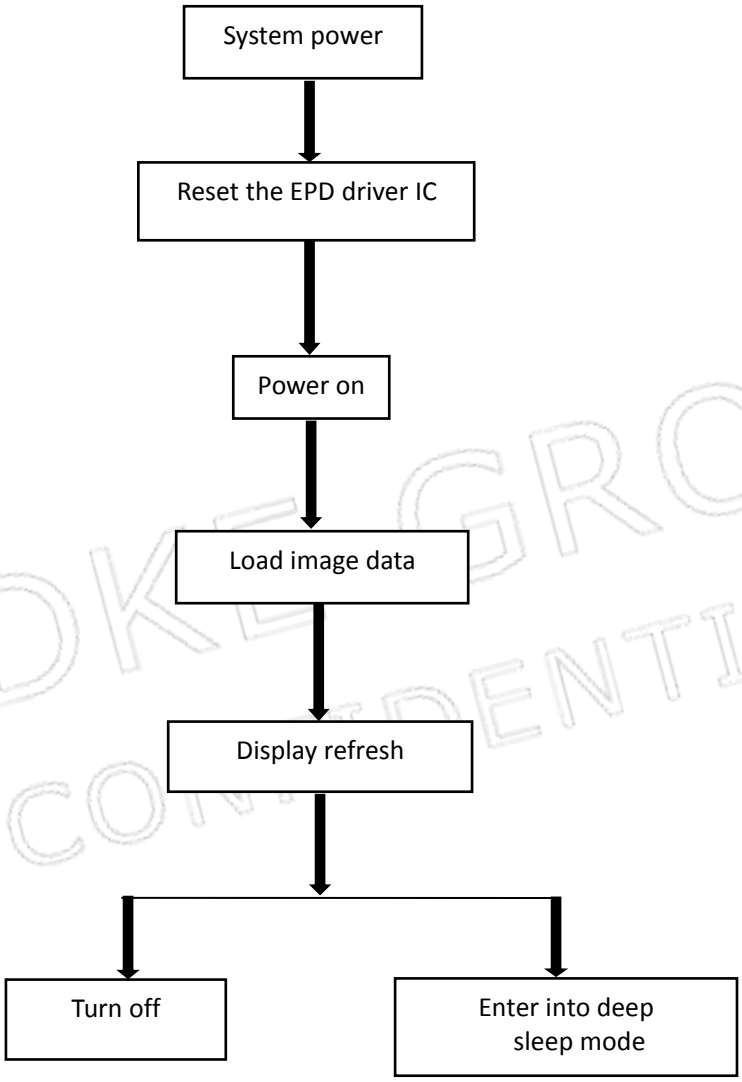
9.Typical Application Circuit with SPI Interface



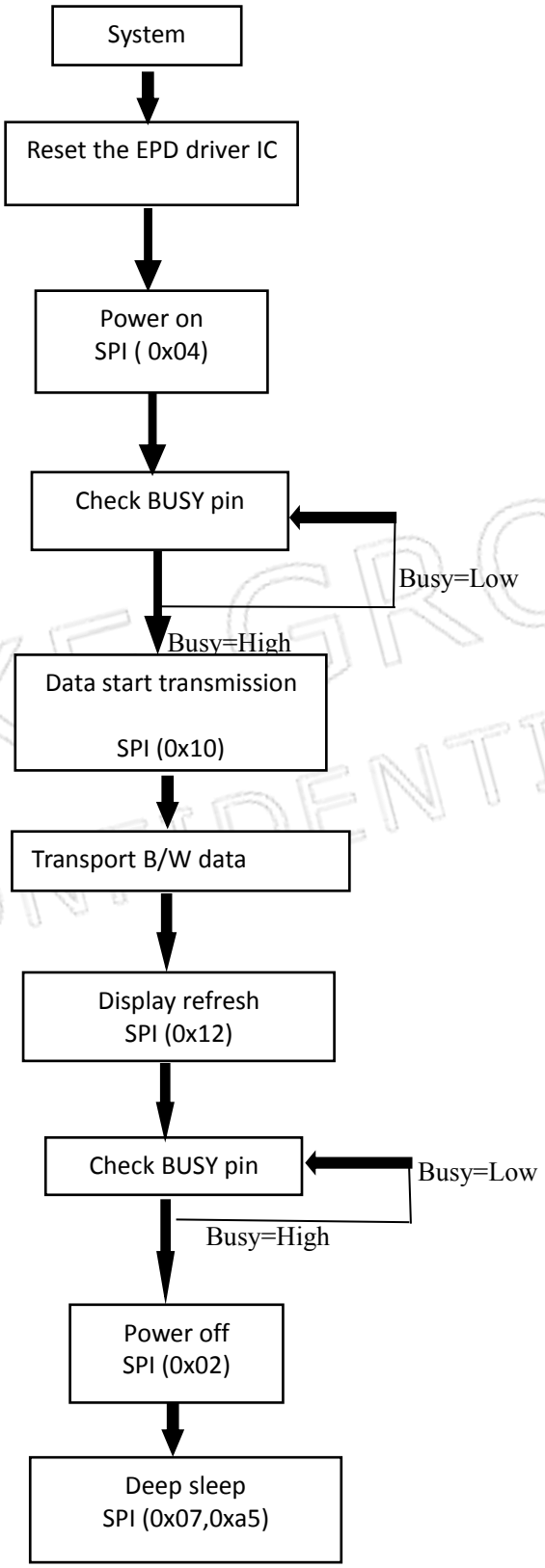
Part Name	Value	Reference Part	Requirements for spare part
C6	1uF	Voltage Rating:10v	
C4	4.7uF	Voltage Rating:10v	
C1 C9	1uF	Voltage Rating:25v	
C2 C3 C5 C7 C8	4.7uF	Voltage Rating:25v	
R1	0.47Ohm	No remark	
D4 D5 D6	Diode	MBR0530	V_R>25V,I_F>500mA,I_R<1mA@V_R=15V,Ta=100℃
Q1	NMOS	Si1308EDL	V_{DS}>25V,I_D>500mA,V_{GS}<1.5 C_{iss}<200pf,$R_{DS(ON)}$<400mΩ
L2	10uH	No remark	

10 Typical Operating Sequence

10.1 LUT from OTP Operation Flow



10.2 LUT from OTP Operation Reference Program Code



11. Reliability Test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=+70ºC，RH=40%，240h Test in white pattern
3	High-Temperature Operation	T=+50ºC，RH=30%，240h
4	Low-Temperature Operation	0ºC，240h
5	High-Temperature, High-Humidity Operation	T=40ºC，RH=90%，240h
6	High Temperature, High Humidity Storage	T=60ºC，RH=80%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min]→[+70 °C 30 min] : 100 cycles Test in white pattern
8	ESD Gun	Air+/-4KV;Contact+/-2KV (Naked EPD display, including IC and FPC area)

Note：1. Stay white pattern for storage and non-operstion test.
2. Operation is black→white pattern, the interval is 150s.

12.Quality Assurance

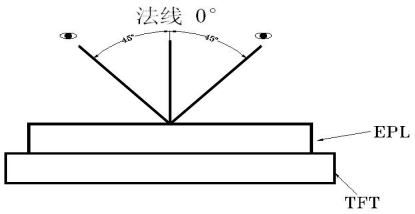
12.1 Environment

Temperature： 23±3℃
Humidity： 55±10%RH

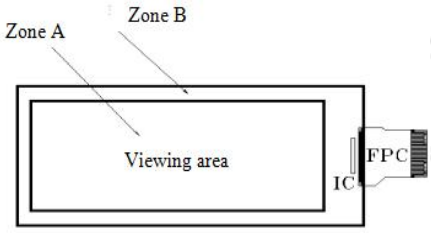
12.2 Illuminance

Brightness:1200～1500LUX;distance:20-30CM;Angle:Relate 45°surround.

12.3 Inspect method

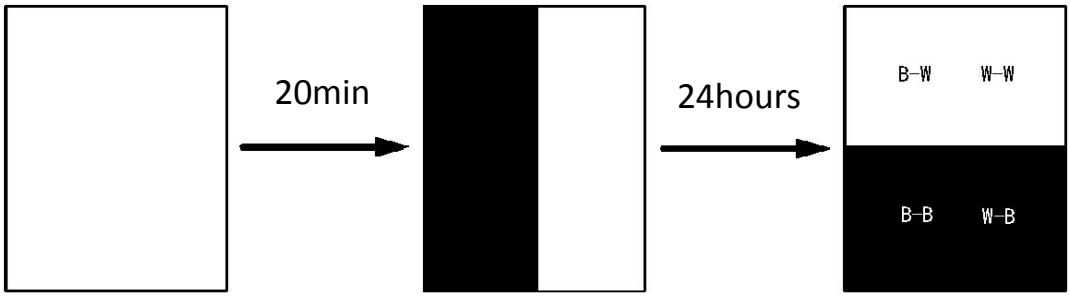


12.4 Display area



12.5 Ghosting test method

Two-color ghosting is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern. The listed optical characteristics are only guaranteed under the controller & waveform provided by DKE.



1）Measurement Instruments：X-rite i1Pro

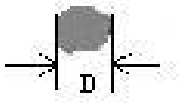
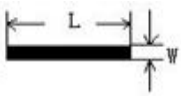
2）Ghosting formula:

W ghosting：△L= Max (Δ L(W-W, B-W)) - Min (Δ L(W-W B-W))

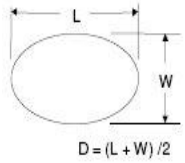
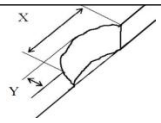
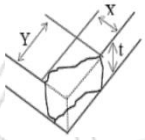
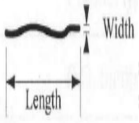
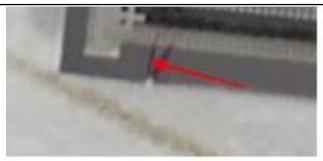
K ghosting：△L= Max (Δ L(W-B, B-B)) - Min(Δ L(W-B, B-B))

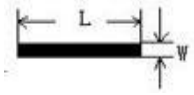
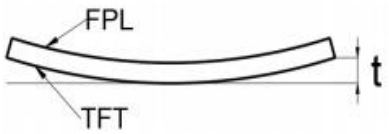
12.6 Inspection standard

12.6.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Clear display Display complete Display uniform	MA	Visual inspection	Zone A
2	Black/White spots	 D≤0.3mm，negligible 0.3mm ＜ D≤0.5mm, N ≤ 5 , Allowed 0.5mm＜D Not Allow	MI		
3	Black/White lines (No switch)	 L≤1.0mm,W≤0.15mm negligible 1.0mm＜L≤4.0mm 0.15mm＜W≤0.5mm N≤4 allowable L＞4.0mm ,W＞0.5mm is not allowed		Visual/ Inspection card	
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash dot / Multilateral	Flash points are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A Zone B
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment.	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Abnormal Display	Not Allow			

12.6.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 D≤0.3mm，Allowed 0.3mm＜D≤0.5mm，N≤5 D＞0.5mm，Not Allow	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	\Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 X≤3mm,Y≤0.5mm  2mm≤X or 2mm≤Y not Allow  W≤0.1mm,L≤5mm, n≤ 2 Edge crown：X≤0.3mm，Y≤3mm	MI	Visual / Microscope	Zone A Zone B
5	TFT Cracks	 Not Allow	MA	Visual / Microscope	Zone A Zone B
6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	Visual / Microscope	Zone A / Zone B
7	FPC broken/ FPC oxidation / scratch	  Not Allow	MA	Visual / Microscope	Zone B

8	B/W Line	 L≤1.0mm,W≤0.15mm negligible 1.0mm＜L≤4.0mm 0.15mm＜W≤0.5mm N≤4 allowable L＞4.0mm ,W＞0.5mm is not allowed	MI	Visual / Ruler	Zone B
9	TFT edge bulge /TFT chromatic aberration	TFT edge bulge： X≤3mm，Y≤0.3mm Allowed TFT chromatic aberration :Allowed	MI	Visual / Microscope	Zone A Zone B
10	Electrostatic point	D≤0.25mm, allow 0.25mm＜D≤0.4mm ,n≤4 allow D＞0.4mm is not allowed (n≤8 items are allowed within 5 mm in diameter)	MI	Visual / Microscope	Zone A
11	PCB damaged/ Poor welding/ Curl	PCB（Circuit area）damaged Not Allow PCB Poor welding Not Allow PCB Curl≤1%	MI	Visual / Ruler	Zone B
12	Edge glue height/ Edge glue bubble	Edge Adhesives H≤PS surface (Including protect film) Edge adhesives seep in≤1/2 Margin width Length excluding Edge adhesives bubble：bubble Width ≤1/2 Margin width；Length ≤5.0mm。n≤5	MI		
13	Protect film	Surface scratch but not effect protect function, Allow	MI	Visual Inspection	Zone B
14	Silicon glue	Thickness ≤ PS surface(With protect film): Full cover the IC; Shape: The width on the FPC≤0.5mm (Front) The width on the FPC≤1.0mm (Back) smooth surface, No obvious raised.	MI	Visual Inspection	
15	Warp degree (TFT substrate)	 t≤1.5mm	MI	Ruler	
16	Color difference in COM area (Silver point area)	Allowed		Visual Inspection	

13. Packaging

EPD PACKING INSTRUCTION

DKE-QS.D-010

DATE	
DESIGN	
CHECKED	
APPROVED	

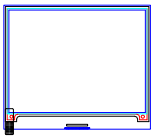
P/N	Customer Code	Ref.P/N
DEPG0420		

Type	PKG Method	Marking	Surface Marks	Pull Tape	
GLASS	Blister	BACK	None	YES	

Packing Materials List				
List	Model	Materials	Q'ty	Unit
Carton	7# 417*362*229 mm	corrugate	1	Piece
Inner Carton	7#(INNER)400*343 *95 mm	corrugate	2	Piece
Blister	DEPG0420A02 PET 1.0	PET	22	Piece
Thin foam	295.6*269.6*T1.8~2.0mm	EPE	20	Piece
Antistatic vacuum bag	450*590*0.075		2	Piece
Foam board	DKE2251-10	EPE	5	Piece
PULL TAPE	16*5*T0.05		180	Piece

9PCS/LAYER, 20LAYER/CTN, TOTAL 180PCS/CTN.

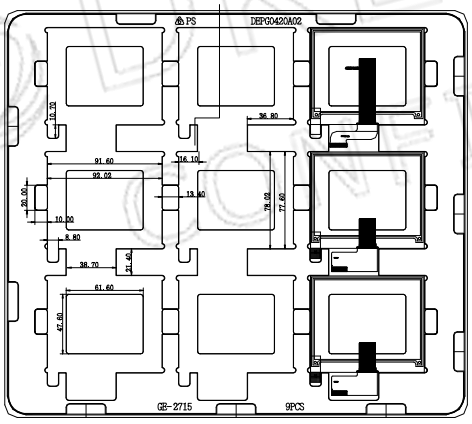
Pull tape:



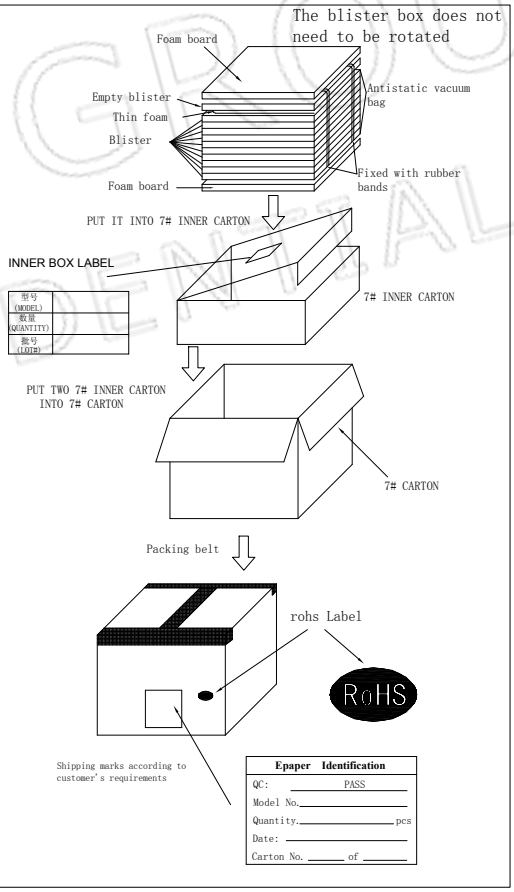
Detail:

Blister box:

Note: there are 20 layers of products, divided into 2 inner boxes, and an empty blister box is placed on the top of each inner box, so the number of blister boxes is 22



QUANTITY：9PCS



14. Handling, Safety, and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
Product Environmental certification	
ROHS	
REMARK	
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.	
Transport environment	
When the humidity of transportation environment is between 45%RH~70%RH, the product can be stored for 30 days, and the product can be stored for 10 days if it is lower or higher than this range	