GateMate FPGA Technology

GateMate™ FPGA

new

Suitable from university projects up to high volume applications

Supported by:
Federal Ministry for Economic Affairs and Energy
on the basis of a decision by the German Bundestag

Overview

The GateMate™ FPGA family of Cologne Chip™ AG addresses all application requirements of small to medium size FPGAs. Very low power and speed applications are feasible. Logic capacity, power consumption, package size and PCB compatibility are best in class. GateMate™ FPGAs combine these features with lowest cost in industry making the devices well suited from University projects to high volume applications. Because of the outstanding Circuit size/Cost ratio, even new applications now can use the benefits of FPGAs.

All this is based on a novel FPGA architecture combining a special logic element called Cologne Programmable Element (CPE) with a smart routing engine. Furthermore, arbitrary size Multipliers are usable. Memory aware applications can use block RAMs with bit widths of 1 to 80 bits. Even bit-wise enable is possible.

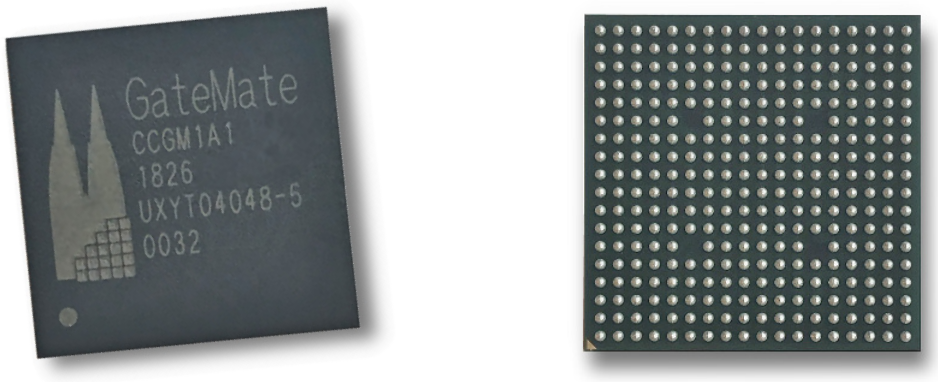
General Purpose IOs (GPIOs) can use different voltage levels from 1.2 to 2.5 Volt. GPIOs can be configured as single-ended or LVDS differential type. Furthermore a high speed SERDES interface is available.

GateMate™ FPGAs are supported by EasyConvert™, that enables the transfer of existing FPGA designs without new synthesis. Worldclass P&R-software maps and implements the design into GateMate™ FPGA.

A Static Timing Analysis (STA) is also performed and gives evidence about critical pathes and the overall performance of a design. The design can be easily simulated using Verilog netlist and SDF timing extraction.

The devices are manufactured using Global-foundries™ 28 nm SLP (Super Low Power) process. Due to manufacturing in Europe, there is no danger of trade restrictions or high taxation.

Pricing starts at USD 10



FBGA 320 ball 15x15 mm with 0.8 mm ball pitch package of **GateMate™ CCGM1A1**

Cologne Chip
GateMate FPGA

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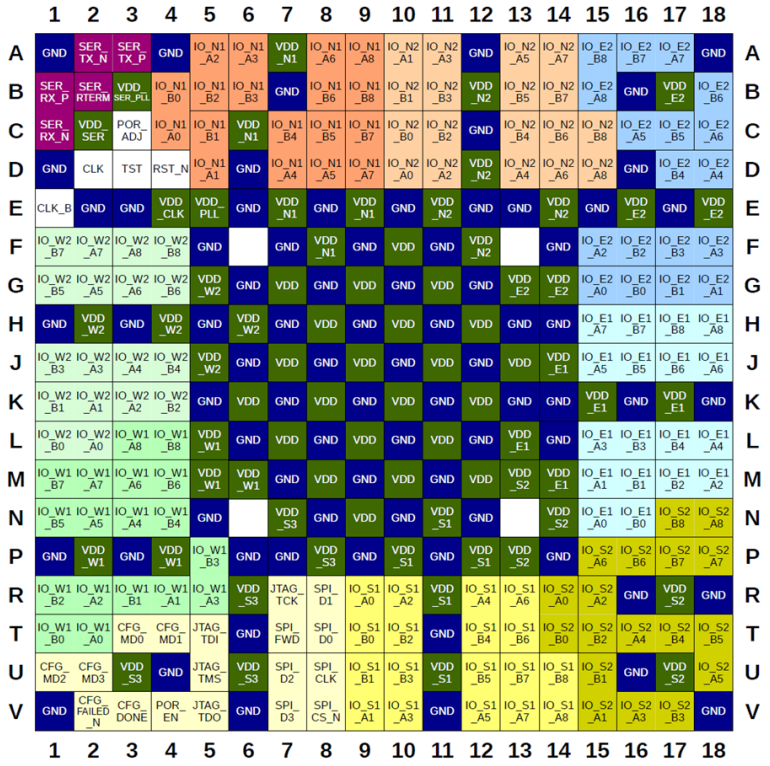
GateMate FPGA Technology

designed and manufactured in Germany

GateMate™ Features

- Logic capacity from 40.000 to more than a million LUT-4 equivalent cells
- Novel architecture with new programmable element (CPE)
- CPE consists of LUT tree with 8 inputs
- 3 operation areas: low power, economy, speed
- Pricing starts from $US 10 for **GateMate™ CCGM1A1** device in volume quantities
- FPGA in ball grid package for low size and high pin count
- Only 2 signal layers on PCB necessary
- Low configuration bit count
- Very fast configuration using 4 bit SPI interface up to 100 MHz
- No excessive start-up currents
- Only two supply voltages needed, that can be applied in any order
- Multiple clocking schemas
- Dual ported Block RAMs with 20-80 bit data width, also configurable as FIFO
- Multipliers with arbitrary factor width implementable
- SERDES 2.5 Gb/s
- General Purpose IOs (GPIO) configurable as single-ended or differential
- Pullup/Pulldown resistors configurable
- Support for ADC and DAC with additional IP cores
- Core voltage depending on application mode: 0.9 V, 1.0 V, 1.1 V
- Low Power 28 nm SLP Globalfoundries™ process technology
- Made in Europe
- EasyConvert™ software to migrate existing designs to GateMate™
- GateMate™ Place&Route with automatic clock Skew analysis and fixing
- Static Timing Analysis for performance evaluation
- Available in different size versions (see table)



Package Connections of **GateMate™ CCGM1A1** with ball positions and signal names

Pricing starts at USD 10

Device	Rel. size	Cologne Programmable Elements 1) 2)			Block RAM 3)		PLLs	SERDES	I/Os		Package	
		CPEs	8-Inp-LUT trees	FF/Latches	20Kb	40Kb			single-ended	differential	balls	size (mm)
CCGM1A1	1	20,480	20,480	40,960	64	32	4	1	162	81	320BGA	15x15
CCGM1A2	2	40,960	40,960	81,920	128	64	8	2	162	81	320BGA	15x15
CCGM1A4	4	81,920	81,920	163,840	256	128	16	4	162	81	320BGA	15x15
CCGM1A9	9	184,320	184,320	368,640	576	288	36	9	tbd	tbd	tbd	tbd
CCGM1A16	16	327,680	327,680	655,360	1,024	512	64	16	tbd	tbd	tbd	tbd
CCGM1A25	25	512,000	512,000	1,024,000	1,600	800	100	25	tbd	tbd	tbd	tbd

1) CPEs have 2x4 or 8 inputs connected to a LUT tree

2) Each CPE can be used as 2x2 Multiplier tile

3) Block RAM can have a max data width of 20 either 40 Bits

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