

# GateMate™ FPGA

new

Suitable from university projects up to high volume applications

Supported by:



on the basis of a decision  
by the German Bundestag

## Overview

The GateMate™ FPGA family of Cologne Chip™ AG addresses all application requirements of small to medium size FPGAs. Very low power and speed applications are feasible. Logic capacity, power consumption, package size and PCB compatibility are best in class. GateMate™ FPGAs combine these features with lowest cost in industry making the devices well suited from University projects to high volume applications. Because of the outstanding Circuit size/Cost ratio, even new applications now can use the benefits of FPGAs.

All this is based on a novel FPGA architecture combining a special logic element called Cologne Programmable Element (CPE) with a smart routing engine. Furthermore, arbitrary size Multipliers are usable. Memory aware applications can use block RAMs with bit widths of 1 to 80 bits. Even bit-wise enable is possible.

General Purpose IOs (GPIOs) can use different voltage levels from 1.2 to 2.5 Volt. GPIOs can be configured as single-ended or LVDS differential type. Furthermore a high speed SERDES interface is available.

GateMate™ FPGAs are supported by EasyConvert™, that enables the transfer of existing FPGA designs

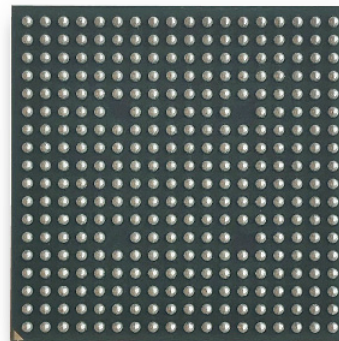
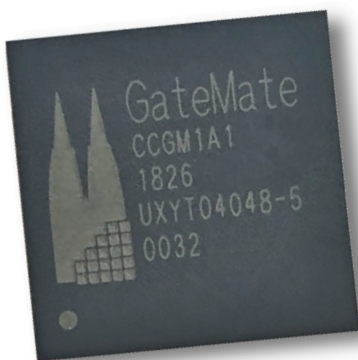


without new synthesis. Worldclass P&R-software maps and implements the design into GateMate™ FPGA.

A Static Timing Analysis (STA) is also performed and gives evidence about critical pathes and the overall performance of a design. The design can be easily simulated using Verilog netlist and SDF timing extraction.

The devices are manufactured using Global-foundries™ 28 nm SLP (Super Low Power) process. Due to manufacturing in Europe, there is no danger of trade restrictions or high taxation.

Pricing starts  
at USD 10



FBGA 320 ball 15x15 mm with 0.8 mm ball pitch package of GateMate™ CCGM1A1

**designed and  
manufactured  
in Germany**

## GateMate™ Features

- Logic capacity from 40.000 to more than a million LUT-4 equivalent cells
- Novel architecture with new programmable element (CPE)
- CPE consists of LUT tree with 8 inputs
- 3 operation areas: low power, economy, speed
- Pricing starts from \$US 10 for **GateMate™ CCGM1A1** device in volume quantities
- FPGA in ball grid package for low size and high pin count
- Only 2 signal layers on PCB necessary
- Low configuration bit count
- Very fast configuration using 4 bit SPI interface up to 100 MHz
- No excessive start-up currents
- Only two supply voltages needed, that can be applied in any order
- Multiple clocking schemas
- Dual ported Block RAMs with 20-80 bit data width, also configurable as FIFO
- Multipliers with arbitrary factor width implementable
- SERDES 2.5 Gb/s
- General Purpose IOs (GPIO) configurable as single-ended or differential
- Pullup/Pulldown resistors configurable

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	GND	SER_TX_N	SER_TX_P	GND	IO_N1_A2	IO_N1_A3	VDD_N1	IO_N1_A6	IO_N1_A8	IO_N2_A1	IO_N2_A3	GND	IO_N2_A5	IO_N2_A7	IO_E2_B8	IO_E2_B7	IO_E2_A7	GND	A
B	SER_RX_P	SER_RX_N	VDD_SER_PUL	IO_N1_B0	IO_N1_B2	IO_N1_B3	GND	IO_N1_B6	IO_N1_B8	IO_N2_B1	IO_N2_B3	VDD_N2	IO_N2_B5	IO_N2_B7	IO_E2_A8	GND	VDD_E2	IO_E2_B6	B
C	SER_RX_N	VDD_SER	POR_ADJ	IO_N1_A0	IO_N1_B1	VDD_N1	IO_N1_B4	IO_N1_B5	IO_N1_B7	IO_N2_B0	IO_N2_B2	GND	IO_N2_B4	IO_N2_B6	IO_N2_B8	IO_E2_A5	IO_E2_B5	IO_E2_A6	C
D	GND	CLK	TST	RST_N	IO_N1_A1	GND	IO_N1_A4	IO_N1_A5	IO_N1_A7	IO_N2_A0	IO_N2_A2	VDD_N2	IO_N2_A4	IO_N2_A6	IO_N2_A8	GND	IO_E2_B4	IO_E2_A4	D
E	CLK_B	GND	GND	VDD_CLK	VDD_PLL	GND	VDD_N1	GND	VDD_N2	GND	VDD_N2	GND	GND	VDD_N2	GND	VDD_E2	GND	VDD_E2	E
F	IO_W2_B7	IO_W2_A7	IO_W2_B8	IO_W2_A8	IO_W2_B8	GND	GND	VDD_N1	GND	VDD_N2	GND	VDD_N2	GND	GND	IO_E2_A2	IO_E2_B2	IO_E2_B3	IO_E2_A3	F
G	IO_W2_B5	IO_W2_A5	IO_W2_B6	IO_W2_A6	IO_W2_B6	VDD_W2	GND	VDD	GND	VDD	GND	VDD	GND	VDD	IO_E2_A0	IO_E2_B0	IO_E2_B1	IO_E2_A1	G
H	GND	VDD_W2	GND	VDD_W2	GND	VDD_W2	GND	VDD	GND	VDD	GND	VDD	GND	GND	IO_E1_A7	IO_E1_B7	IO_E1_B8	IO_E1_A8	H
J	IO_W2_B3	IO_W2_A3	IO_W2_B4	IO_W2_A4	IO_W2_B4	VDD_W2	GND	VDD	GND	VDD	GND	VDD	GND	VDD	IO_E1_A5	IO_E1_B5	IO_E1_B6	IO_E1_A6	J
K	IO_W2_B1	IO_W2_A1	IO_W2_B2	IO_W2_A2	IO_W2_B2	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD_E1	GND	VDD_E1	GND	K
L	IO_W2_B0	IO_W2_A0	IO_W1_B8	IO_W1_A8	IO_W1_B8	VDD_W1	GND	VDD	GND	VDD	GND	VDD	GND	VDD	IO_E1_A3	IO_E1_B3	IO_E1_B4	IO_E1_A4	L
M	IO_W1_B7	IO_W1_A7	IO_W1_B6	IO_W1_A6	IO_W1_B6	VDD_W1	GND	VDD	GND	VDD	GND	VDD	VDD_S2	VDD_E1	IO_E1_A1	IO_E1_B1	IO_E1_B2	IO_E1_A2	M
N	IO_W1_B5	IO_W1_A5	IO_W1_B4	IO_W1_A4	IO_W1_B4	GND	VDD_S3	GND	VDD	GND	VDD	GND	VDD_S2	VDD_S2	IO_E1_A0	IO_E1_B0	IO_S2_B8	IO_S2_A8	N
P	GND	VDD_W1	GND	VDD_W1	IO_W1_B3	GND	GND	VDD_S3	GND	VDD_S1	GND	VDD_S1	VDD_S2	GND	IO_S2_A6	IO_S2_B6	IO_S2_B7	IO_S2_A7	P
R	IO_W1_B2	IO_W1_A2	IO_W1_B1	IO_W1_A1	IO_W1_B1	VDD_S3	JTAG_TCK	SPL_D1	IO_S1_A0	IO_S1_A2	VDD_S1	IO_S1_A4	IO_S1_A6	IO_S2_A0	IO_S2_A2	GND	VDD_S2	GND	R
T	IO_W1_B0	IO_W1_A0	CFG_MD0	CFG_MD1	JTAG_TDI	GND	SPL_FWD	SPL_D0	IO_S1_B0	IO_S1_B2	GND	IO_S1_B4	IO_S1_B6	IO_S2_B0	IO_S2_B2	IO_S2_A4	IO_S2_B4	IO_S2_B5	T
U	CFG_MD2	CFG_MD3	VDD_S3	GND	JTAG_TMS	VDD_S3	SPL_D2	SPL_CLK	IO_S1_B1	IO_S1_B3	VDD_S1	IO_S1_B5	IO_S1_B7	IO_S1_B8	IO_S2_B1	GND	VDD_S2	IO_S2_A5	U
V	GND	CFG_FAILED_N	CFG_DONE	POR_EN	JTAG_TDO	GND	SPL_D3	SPL_CS_N	IO_S1_A1	IO_S1_A3	GND	IO_S1_A5	IO_S1_A7	IO_S1_A8	IO_S2_A1	IO_S2_A3	IO_S2_B3	GND	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

Package Connections of GateMate™ CCGM1A1 with ball positions and signal names

Pricing starts at USD 10

Device	Rel. size	Cologne Programmable Elements 1) 2)			Block RAM 3)		PLLs	SERDES	I/Os		Package	
		CPEs	8-Inp-LUT trees	FF/Latches	20Kb	40Kb			single-ended	differential	balls	size (mm)
CCGM1A1	1	20,480	20,480	40,960	64	32	4	1	162	81	320BGA	15x15
CCGM1A2	2	40,960	40,960	81,920	128	64	8	2	162	81	320BGA	15x15
CCGM1A4	4	81,920	81,920	163,840	256	128	16	4	162	81	320BGA	15x15
CCGM1A9	9	184,320	184,320	368,640	576	288	36	9	tbd	tbd	tbd	tbd
CCGM1A16	16	327,680	327,680	655,360	1,024	512	64	16	tbd	tbd	tbd	tbd
CCGM1A25	25	512,000	512,000	1,024,000	1,600	800	100	25	tbd	tbd	tbd	tbd

1) CPEs have 2x4 or 8 inputs connected to a LUT tree

2) Each CPE can be used as 2x2 Multiplier tile

3) Block RAM can have a max data width of 20 either 40 Bits