AX58200
EtherCAT Slave Controller SoC

Features

Document No: AX58200/V0.10/11/22/19

- **ARM® Cortex®-M4 processor, running up to 192 MHz**
  - Built-in Memory Protection Unit (MPU)
  - Built-in Nested Vectored Interrupt Controller (NVIC)
  - Hardware IEEE 754 compliant Floating-point Unit (FPU)
  - DSP extension with hardware divider and single-cycle 32-bit hardware multiplier
- **On-chip Memory**
  - Dual bank 512-KB Flash size (APROM) for Over-The-Air (OTA) upgrade
  - On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP)
  - On-chip 160 KB SRAM
  - 4 KB on-chip Flash for user-defined loader (LDROM)
  - 4 KB non-readble Security Protection ROM (SPROM)
- **Boot Loader**
  - Factory pre-loaded 32 KB mask ROM for secure boot procedure
  - Uses SHA-256 and AES-256 to validate data in on-chip Flash and external SPI Flash
  - ISP for firmware upgrade via UART and high speed USB device
- **Timers**
  - Supports four sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter
  - Supports twenty-four sets of 16-bit PWM counters
  - Supports 18-bit free running watchdog timer counter
  - Two Quadrature Encoder Interface (QEI) phase inputs (QEI_A, QEI_B) and one Index input (QEI_INDEX)
  - Supports one Enhanced Capture (ECAP) channels
- **Analog Interfaces**
  - One 12-bit, 16-ch 5 MSPS SAR ADC
  - Two 12-bit, 1 MSPS voltage type DAC
  - Two rail-to-rail Analog Comparators
  - Two Operational Amplifiers with 0~AV_{DD} input voltage range.
- **Communication Interfaces**
  - One USB 2.0 High Speed OTG with on-chip transceiver
  - One IEEE Std. 802.3 10/100Mbps Ethernet MAC with RMII
  - Up to 6 sets of UARTs
  - Three sets of ISO-7816-3
  - Three sets of I2C devices with Master/Slave mode
  - One SPI Master supports maximum 32 MB external SPI Flash memory
  - One set of Quad-SPI controller with Master/Slave mode
  - One set of I2S interface with Master/Slave mode
  - Two sets of USCI, configured as UART, SPI or I2C function
  - Two sets of CAN 2.0B controllers
  - Two sets of Secure Digital Host Controllers, compliant with SD Memory Card Specification Version 2.0.
- **Supports Hardware ECC, AES, DES, 3DES, SHA, HMAC accelerator cryptography engineers**
- **Supports Real-Time Clock**
- **Built-in Die Temperature Sensor (DTS) with 1℃ resolution**
- **EtherCAT Slave Controller (ESC) Sub-system**
  - 2 Integrated Fast Ethernet PHYs
  - 3rd Ethernet MII Port for flexible EtherCAT network configuration
  - 8 Fieldbus Memory Management Units (FMMUs)
  - 8 Sync Managers
  - 64-bit distributed clock support allows synchronization with other EtherCAT devices
  - 9K bytes RAM
  - Step & Direction Controller
  - Incremental and Hall Encoder Interface
  - SPI Master Controller
  - Emergency Stop Input
  - Configurable Watchdog for Outputs and Inputs Monitoring
- **Integrates On-chip Power-on Reset Circuit**
- **144-pin HSFBGA 10x10 mm, 0.8-mm pitch, RoHS Compliant Package**
- **Operating Temperature Range: -40 to +85°C, -40 to +105°C**

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PRELIMINARY

Target Applications

- Motion/Motor Control
- Digital I/O Control
- Robotics
- Sensors Data Acquisition
- EtherCAT to IO-Link Converter
- Communication Module
- Operator HMI Interfaces

Typical Applications Diagram

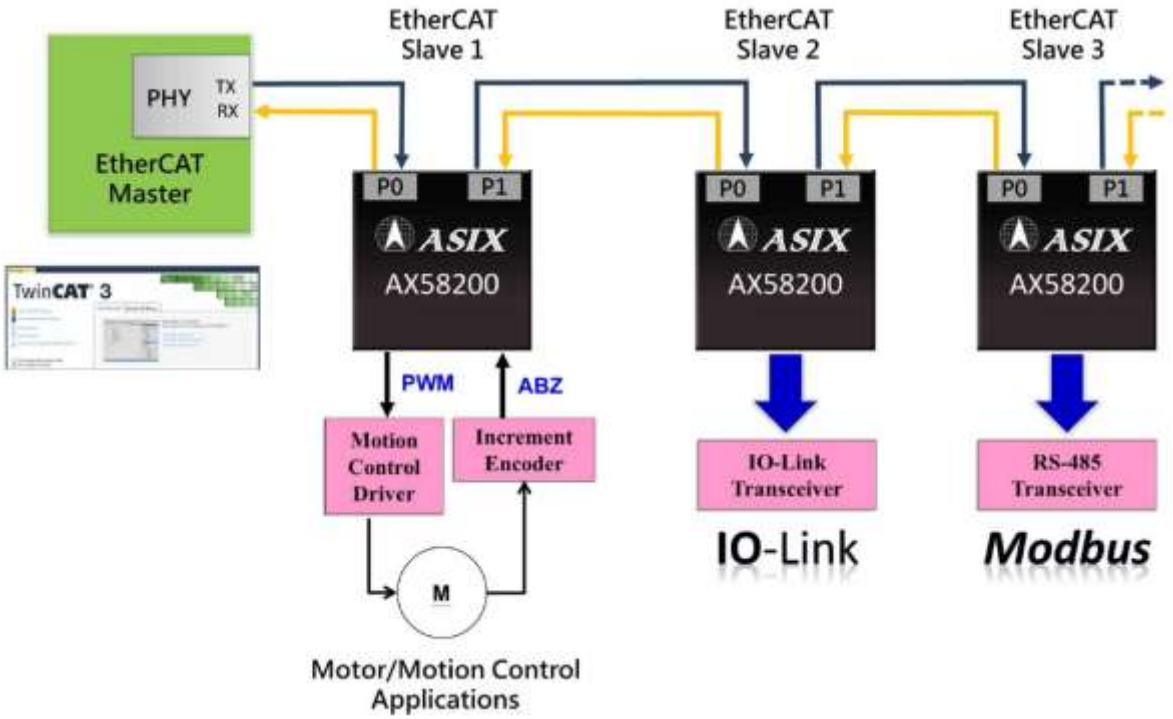

Figure 1.1-1: AX58200 Typical Applications Diagram

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1 Introduction

1.1 General Description

The AX58200 is a 2/3-port EtherCAT Slave Controller SoC equipped with Arm® Cortex®-M4F with DSP extension runs up to 192 MHz and EtherCAT Slave Controller (ESC) with two integrated Fast Ethernet PHYs which support 100Mbps full-duplex operation and HP Auto-MDIX. The AX58200 supports the CANopen (CoE), TFTP (FoE), Vender specific application (VoE), etc. standard EtherCAT protocols and provides a cost-effective solution for industrial automation, motion/motor control, robotics, digital I/O control, sensors data acquisition, etc. industrial fieldbus applications.

AX58200 embedded 512 KB Flash memory in dual-bank architecture supports Over-The-Air firmware upgrade. The 160 KB embedded SRAM includes 32 KB cache for speeding up code execution from the external SPI Flash. Built-in 4 KB Secure Protection ROM provides a safe space for saving confidential program or data.

The AX58200 is equipped with a large number of high speed digital peripherals, such as a USB 2.0 high speed interface with on-chip transceiver working in device/host/OTG mode, a USB 2.0 full speed interface with on-chip transceiver working in device/host mode, up to nine UART interfaces including three ISO-7816-3 interfaces, up to four composite SPI/I2S interfaces, a Quad-SPI interface, a SPI Flash interface supporting quad mode, three I2C interfaces, a 192 KHz/32-bit I2S interface, two SDIO interfaces, two CAN 2.0B interfaces, two QEI interfaces, a 10/100 Mbps Ethernet MAC supporting RMII and two Universal Serial Control Interfaces which can be configured as UART, SPI or I2C. The AX58200 also supports 16 channels peripheral DMA and up to 32 channels PWM running up to 192 MHz.

The AX58200 also provides high performance analog peripherals, such as a 12-bit 5MSPS SAR ADC with up to 16 channels, two 12-bit 1MSPS DAC, two analog comparators and two operational amplifiers, as well as a built-in hardware cryptography accelerator that supports ECC, AES, DES, triple DES, SHA, HMAC and a random number generator (RNG).

The AX58200's ESC circuit provides a three-channel PWM controller or a one-channel Step/Direction controller, and an increment/hall encode interface for closed-loop motor control, a SPI master controller for data acquisition and output, and an I/O watchdog for functional safety.

The AX58200, in 144-pin HSFBGA 10x10 mm, 0.8-mm pitch, supports the RoHS compliant package and industrial grade operating temperature range from -40 to 85°C or from -40 to 105°C.

1.2 Block Diagram

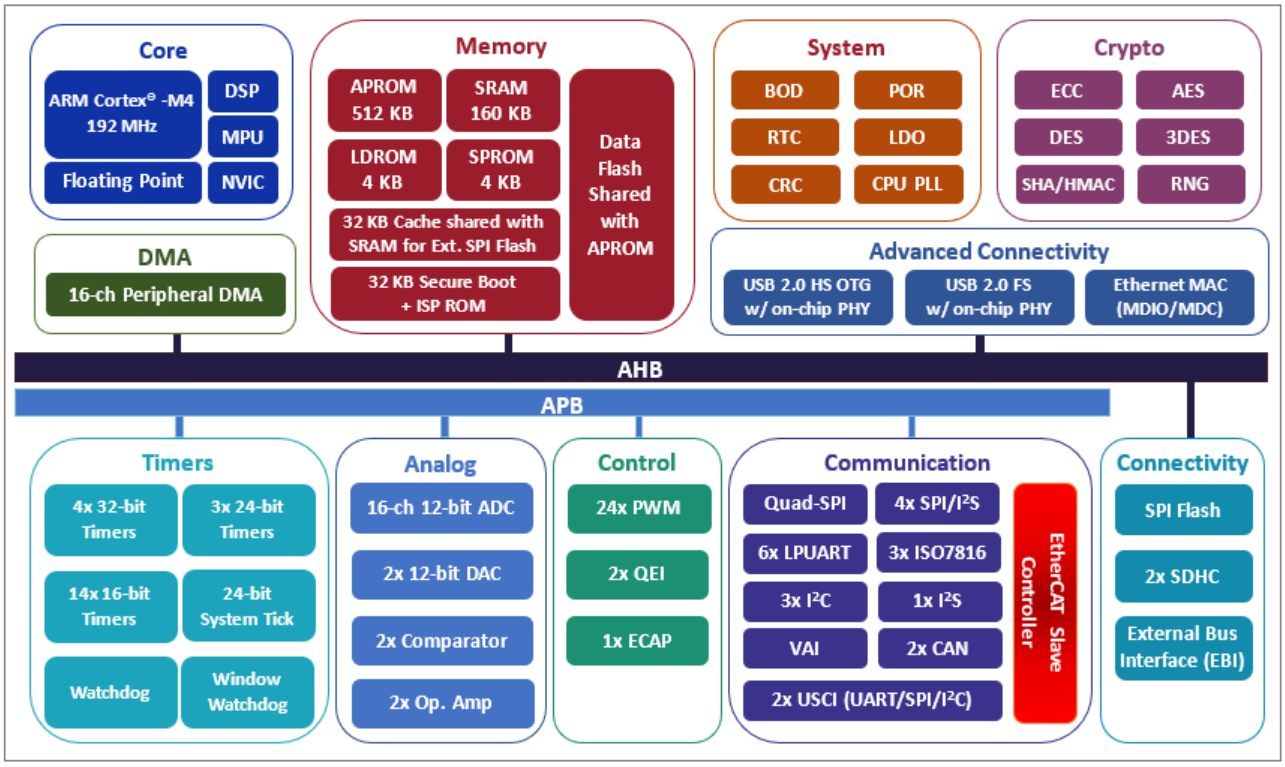


Figure 1.2-1: AX58200 Block Diagram

1.3 Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	
A	PB.7	PB.8	AV_{SS}	V_{REF}	AV_{DD}	PC.14	IO[23]	LDO_CAP	IO[21]	SCL	HSUSB_VDD12_CAP	HSUSB_D+	A
B	PB.6	PB.5	PB.10	IO[26]	IO[25]	IO[24]	IO[22]	PH.9	SDA	PDI_EMU	HSUSB_ID	HSUSB_D-	B
C	PB.4	PB.3	PB.9	PB.11	PB.14	V_{DD}	VCCK	PH.8	IO[4]	RSTn	HSUSB_VBUS	HSUSB_VRES	C
D	PB.2	PB.1	PB.13	PB.15	PB.12	V_{DD}	VCCK	OE_EXT	TEST	PE.0	HSUSB_VSS	HSUSB_VDD33	D
E	PB.0	SYNC_LATCH[1]	SYNC_LATCH[0]	SOF	OUTVLD	V_{DD}	VCCK	VCC12A_PLL	RSTO	PE.7	PE.1	PE.2	E
F	PA.10	PA.11	IO[2]	EOF	GND	GND	GND	GND	NC	PE.6	PE.4	PE.3	F
G	PF.4	PA.9	PA.8	WD_TRIG	GND	GND	GND	GND	IO[1]	IO[17]	IO[19]	PE.5	G
H	PF.5	PF.6	IO[27]	LAT_IN	RSET_BG	VCC3IO	VCC3IO	VCC3IO	IO[20]	IO[0]	IO[18]	V_{DDIO}	H
J	PF.2	IO[28]	IO[29]	PE.13	PC.8	PA.7	PA.5	PA.2	PA.0	P0_ACT	P1_ACT	IO[16]	J
K	PF.3	EEP_DONE	IO[30]	PC.7	PC.6	PA.6	PA.4	PA.3	PA.1	nRESET	PC.1	PC.0	K
L	LED_RUN	LED_ERR	P1_TXON	P1_RXIN	P1_SD	P0_TXON	P0_RXIN	P0_SD	XSCI	PF.1	PC.3	PC.2	L
M	IO[31]	VCC33A	P1_TXOP	P1_RXIP	VCC33A	P0_TXOP	P0_RXIP	VCC33A	XSCO	PF.0	PC.5	PC.4	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 1.3-1: AX58200 Pinout Diagram

1.4 Signal Description

Following abbreviations are used in "Type" column of below pin description tables. Note that some I/O pins with multiple signal definitions on the same pin may have different attributes in "Type" column for different signal definition.

A	Analog
B5	Bi-directional I/O, 3.3V with 5V tolerant
I5	Input, 3.3V with 5V tolerant
O5	Output, 3.3V with 5V tolerant
B3	Bi-directional I/O, 3.3V
I3	Input, 3.3V
O3	Output, 3.3V
PU	Internal Pull-Up
PD	Internal Pull-Down
P	Power/Ground pin
S	Schmitt Trigger
T	Tri-state
4m	4mA driving strength
8m	8mA driving strength

1.4.1 Main System Pin Description

Pin No	Pin Name	Type	MFP	Description
K10	nRESET	I3/S	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
J9	PA.0	B5	MFP0	General purpose digital I/O pin.
	SPIM_MOSI	I/O	MFP2	SPIM MOSI (Master Out, Slave In) pin.
	QSPI0_MOSI0	I/O	MFP3	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	SD1_DAT0	I/O	MFP5	SD/SDIO1 data line bit 0.
	SC0_CLK	O	MFP6	Smart Card 0 clock pin.
	UART0_RXD	I	MFP7	UART0 data receiver input pin.
	UART1_nRTS	O	MFP8	UART1 request to Send output pin.
	I2C2_SDA	I/O	MFP9	I2C2 data input/output pin.
	BPWM0_CH0	I/O	MFP12	BPWM0 channel 0 output/capture input.
	EPWM0_CH5	I/O	MFP13	EPWM0 channel 5 output/capture input.
	DAC0_ST	I	MFP15	DAC0 external trigger input.
K9	PA.1	B5	MFP0	General purpose digital I/O pin.
	SPIM_MISO	I/O	MFP2	SPIM MISO (Master In, Slave Out) pin.
	QSPI0_MISO0	I/O	MFP3	Quad SPI0 MISO0 (Master In, Slave Out) pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	SD1_DAT1	I/O	MFP5	SD/SDIO1 data line bit 1.
	SC0_DAT	I/O	MFP6	Smart Card 0 data pin.
	UART0_TXD	O	MFP7	UART0 data transmitter output pin.
	UART1_nCTS	I	MFP8	UART1 clear to Send input pin.
	I2C2_SCL	I/O	MFP9	I2C2 clock pin.
	BPWM0_CH1	I/O	MFP12	BPWM0 channel 1 output/capture input.
	EPWM0_CH4	I/O	MFP13	EPWM0 channel 4 output/capture input.
	DAC1_ST	I	MFP15	DAC1 external trigger input.
J8	PA.2	B5	MFP0	General purpose digital I/O pin.
	SPIM_CLK	I/O	MFP2	SPIM serial clock pin.
	QSPI0_CLK	I/O	MFP3	Quad SPI0 serial clock pin.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	SD1_DAT2	I/O	MFP5	SD/SDIO1 data line bit 2.
	SC0_RST	O	MFP6	Smart Card 0 reset pin.
	UART4_RXD	I	MFP7	UART4 data receiver input pin.

Pin No	Pin Name	Type	MFP	Description
	UART1_RXD	I	MFP8	UART1 data receiver input pin.
	I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
	BPWM0_CH2	I/O	MFP12	BPWM0 channel 2 output/capture input.
	EPWM0_CH3	I/O	MFP13	EPWM0 channel 3 output/capture input.
K8	PA.3	B5	MFP0	General purpose digital I/O pin.
	SPIM_SS	I/O	MFP2	SPIM slave select pin.
	QSPI0_SS	I/O	MFP3	Quad SPI0 slave select pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	SD1_DAT3	I/O	MFP5	SD/SDIO1 data line bit 3.
	SC0_PWR	O	MFP6	Smart Card 0 power pin.
	UART4_TXD	O	MFP7	UART4 data transmitter output pin.
	UART1_TXD	O	MFP8	UART1 data transmitter output pin.
	I2C1_SCL	I/O	MFP9	I2C1 clock pin.
	BPWM0_CH3	I/O	MFP12	BPWM0 channel 3 output/capture input.
	EPWM0_CH2	I/O	MFP13	EPWM0 channel 2 output/capture input.
	QEI0_B	I	MFP14	Quadrature encoder 0 phase B input
K7	PA.4	B5	MFP0	General purpose digital I/O pin.
	SPIM_D3	I/O	MFP2	SPIM data 3 pin for Quad Mode I/O.
	QSPI0_MOSI1	I/O	MFP3	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
	SPI0_I2SMCLK	I/O	MFP4	SPI0 I2S master clock output pin
	SD1_CLK	O	MFP5	SD/SDIO1 clock output pin
	SC0_nCD	I	MFP6	Smart Card 0 card detect pin.
	UART0_nRTS	O	MFP7	UART0 request to Send output pin.
	UART5_RXD	I	MFP8	UART5 data receiver input pin.
	I2C0_SDA	I/O	MFP9	I2C0 data input/output pin.
	CAN0_RXD	I	MFP10	CAN0 bus receiver input.
	BPWM0_CH4	I/O	MFP12	BPWM0 channel 4 output/capture input.
	EPWM0_CH1	I/O	MFP13	EPWM0 channel 1 output/capture input.
	QEI0_A	I	MFP14	Quadrature encoder 0 phase A input
J7	PA.5	B5	MFP0	General purpose digital I/O pin.
	SPIM_D2	I/O	MFP2	SPIM data 2 pin for Quad Mode I/O.
	QSPI0_MISO1	I/O	MFP3	Quad SPI0 MISO1 (Master In, Slave Out) pin.
	SPI1_I2SMCLK	I/O	MFP4	SPI1 I2S master clock output pin
	SD1_CMD	I/O	MFP5	SD/SDIO1 command/response pin
	SC2_nCD	I	MFP6	Smart Card 2 card detect pin.
	UART0_nCTS	I	MFP7	UART0 clear to Send input pin.
	UART5_TXD	O	MFP8	UART5 data transmitter output pin.
	I2C0_SCL	I/O	MFP9	I2C0 clock pin.
	CAN0_TXD	O	MFP10	CAN0 bus transmitter output.
	BPWM0_CH5	I/O	MFP12	BPWM0 channel 5 output/capture input.
	EPWM0_CH0	I/O	MFP13	EPWM0 channel 0 output/capture input.
	QEI0_INDEX	I	MFP14	Quadrature encoder 0 index input
K6	PA.6	B5	MFP0	General purpose digital I/O pin.
	EBI_AD6	I/O	MFP2	EBI address/data bus bit 6.
	EMAC_RMII_RXERR	I	MFP3	EMAC RMII Receive Data Error input pin.
	SPI1_SS	I/O	MFP4	SPI1 slave select pin.
	SD1_nCD	I	MFP5	SD/SDIO1 card detect input pin
	SC2_CLK	O	MFP6	Smart Card 2 clock pin.
	UART0_RXD	I	MFP7	UART0 data receiver input pin.
	I2C1_SDA	I/O	MFP8	I2C1 data input/output pin.

Pin No	Pin Name	Type	MFP	Description
	EPWM1_CH5	I/O	MFP11	EPWM1 channel 5 output/capture input.
	BPWM1_CH3	I/O	MFP12	BPWM1 channel 3 output/capture input.
	ACMP1_WLAT	I	MFP13	Analog comparator 1 window latch input pin
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT0	I	MFP15	External interrupt 0 input pin.
J6	PA.7	B5	MFP0	General purpose digital I/O pin.
	EBI_AD7	I/O	MFP2	EBI address/data bus bit 7.
	EMAC_RMII_CRSDV	I	MFP3	EMAC RMII Carrier Sense/Receive Data input pin.
	SPI1_CLK	I/O	MFP4	SPI1 serial clock pin.
	SC2_DAT	I/O	MFP6	Smart Card 2 data pin.
	UART0_TXD	O	MFP7	UART0 data transmitter output pin.
	I2C1_SCL	I/O	MFP8	I2C1 clock pin.
	EPWM1_CH4	I/O	MFP11	EPWM1 channel 4 output/capture input.
	BPWM1_CH2	I/O	MFP12	BPWM1 channel 2 output/capture input.
	ACMP0_WLAT	I	MFP13	Analog comparator 0 window latch input pin
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
G3	PA.8	B3	MFP0	General purpose digital I/O pin.
	OPA1_P	A	MFP1	Operational amplifier 1 positive input pin.
	EBI_ALE	O	MFP2	EBI address latch enable output pin.
	SC2_CLK	O	MFP3	Smart Card 2 clock pin.
	SPI2_MOSI	I/O	MFP4	SPI2 MOSI (Master Out, Slave In) pin.
	SD1_DAT0	I/O	MFP5	SD/SDIO1 data line bit 0.
	USCI0_CTL1	I/O	MFP6	USCI0 control 1 pin.
	UART1_RXD	I	MFP7	UART1 data receiver input pin.
	BPWM0_CH3	I/O	MFP9	BPWM0 channel 3 output/capture input.
	QEI1_B	I	MFP10	Quadrature encoder 1 phase B input
	ECAP0_IC2	I	MFP11	Enhanced capture unit 0 input 2 pin.
	TM3_EXT	I/O	MFP13	Timer3 external capture input/toggle output pin.
	INT4	I	MFP15	External interrupt 4 input pin.
G2	PA.9	B3	MFP0	General purpose digital I/O pin.
	OPA1_N	A	MFP1	Operational amplifier 1 negative input pin.
	EBI_MCLK	O	MFP2	EBI external clock output pin.
	SC2_DAT	I/O	MFP3	Smart Card 2 data pin.
	SPI2_MISO	I/O	MFP4	SPI2 MISO (Master In, Slave Out) pin.
	SD1_DAT1	I/O	MFP5	SD/SDIO1 data line bit 1.
	USCI0_DAT1	I/O	MFP6	USCI0 data 1 pin.
	UART1_TXD	O	MFP7	UART1 data transmitter output pin.
	BPWM0_CH2	I/O	MFP9	BPWM0 channel 2 output/capture input.
	QEI1_A	I	MFP10	Quadrature encoder 1 phase A input
	ECAP0_IC1	I	MFP11	Enhanced capture unit 0 input 1 pin.
	TM2_EXT	I/O	MFP13	Timer2 external capture input/toggle output pin.
F1	PA.10	B3	MFP0	General purpose digital I/O pin.
	ACMP1_P0	A	MFP1	Analog comparator 1 positive input 0 pin.
	OPA1_O	A	MFP1	Operational amplifier 1 output pin.
	EBI_nWR	O	MFP2	EBI write enable output pin.
	SC2_RST	O	MFP3	Smart Card 2 reset pin.
	SPI2_CLK	I/O	MFP4	SPI2 serial clock pin.
	SD1_DAT2	I/O	MFP5	SD/SDIO1 data line bit 2.

Pin No	Pin Name	Type	MFP	Description
	USCI0_DAT0	I/O	MFP6	USCI0 data 0 pin.
	I2C2_SDA	I/O	MFP7	I2C2 data input/output pin.
	BPWM0_CH1	I/O	MFP9	BPWM0 channel 1 output/capture input.
	QEI1_INDEX	I	MFP10	Quadrature encoder 1 index input
	ECAP0_IC0	I	MFP11	Enhanced capture unit 0 input 0 pin.
	TM1_EXT	I/O	MFP13	Timer1 external capture input/toggle output pin.
	DAC0_ST	I	MFP14	DAC0 external trigger input.
F2	PA.11	B3	MFP0	General purpose digital I/O pin.
	ACMP0_P0	A	MFP1	Analog comparator 0 positive input 0 pin.
	EBI_nRD	O	MFP2	EBI read enable output pin.
	SC2_PWR	O	MFP3	Smart Card 2 power pin.
	SPI2_SS	I/O	MFP4	SPI2 slave select pin.
	SD1_DAT3	I/O	MFP5	SD/SDIO1 data line bit 3.
	USCI0_CLK	I/O	MFP6	USCI0 clock pin.
	I2C2_SCL	I/O	MFP7	I2C2 clock pin.
	BPWM0_CH0	I/O	MFP9	BPWM0 channel 0 output/capture input.
	EPWM0_SYNC_OUT	O	MFP10	EPWM0 counter synchronous trigger output pin.
	TM0_EXT	I/O	MFP13	Timer0 external capture input/toggle output pin.
	DAC1_ST	I	MFP14	DAC1 external trigger input.
E1	PB.0	B3	MFP0	General purpose digital I/O pin.
	EADC0_CH0	A	MFP1	EADC0 channel 0 analog input.
	OPA0_P	A	MFP1	Operational amplifier 0 positive input pin.
	EBI_ADR9	O	MFP2	EBI address bus bit 9.
	SD0_CMD	I/O	MFP3	SD/SDIO0 command/response pin
	UART2_RXD	I	MFP7	UART2 data receiver input pin.
	SPI0_I2SMCLK	I/O	MFP8	SPI0 I2S master clock output pin
	I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
	EPWM0_CH5	I/O	MFP11	EPWM0 channel 5 output/capture input.
	EPWM1_CH5	I/O	MFP12	EPWM1 channel 5 output/capture input.
	EPWM0_BRAKE1	I	MFP13	EPWM0 Brake 1 input pin.
D2	PB.1	B3	MFP0	General purpose digital I/O pin.
	EADC0_CH1	A	MFP1	EADC0 channel 1 analog input.
	OPA0_N	A	MFP1	Operational amplifier 0 negative input pin.
	EBI_ADR8	O	MFP2	EBI address bus bit 8.
	SD0_CLK	O	MFP3	SD/SDIO0 clock output pin
	EMAC_RMII_RXERR	I	MFP4	EMAC RMII Receive Data Error input pin.
	SPI1_I2SMCLK	I/O	MFP5	SPI1 I2S master clock output pin
	SPI3_I2SMCLK	I/O	MFP6	SPI3 I2S master clock output pin
	UART2_TXD	O	MFP7	UART2 data transmitter output pin.
	USCI1_CLK	I/O	MFP8	USCI1 clock pin.
	I2C1_SCL	I/O	MFP9	I2C1 clock pin.
	I2S0_LRCK	O	MFP10	I2S0 left right channel clock output pin.
	EPWM0_CH4	I/O	MFP11	EPWM0 channel 4 output/capture input.
	EPWM1_CH4	I/O	MFP12	EPWM1 channel 4 output/capture input.
	EPWM0_BRAKE0	I	MFP13	EPWM0 Brake 0 input pin.
D1	PB.2	B3	MFP0	General purpose digital I/O pin.
	EADC0_CH2	A	MFP1	EADC0 channel 2 analog input.
	ACMP0_P1	A	MFP1	Analog comparator 0 positive input 1 pin.
	OPA0_O	A	MFP1	Operational amplifier 0 output pin.
	EBI_ADR3	O	MFP2	EBI address bus bit 3.

Pin No	Pin Name	Type	MFP	Description
	SD0_DAT0	I/O	MFP3	SD/SDIO0 data line bit 0.
	EMAC_RMII_CRSDV	I	MFP4	EMAC RMII Carrier Sense/Receive Data input pin.
	SPI1_SS	I/O	MFP5	SPI1 slave select pin.
	UART1_RXD	I	MFP6	UART1 data receiver input pin.
	UART5_nCTS	I	MFP7	UART5 clear to Send input pin.
	USCI1_DAT0	I/O	MFP8	USCI1 data 0 pin.
	SC0_PWR	O	MFP9	Smart Card 0 power pin.
	I2S0_DO	O	MFP10	I2S0 data output pin.
	EPWM0_CH3	I/O	MFP11	EPWM0 channel 3 output/capture input.
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT3	I	MFP15	External interrupt 3 input pin.
C2	PB.3	B3	MFP0	General purpose digital I/O pin.
	EADC0_CH3	A	MFP1	EADC0 channel 3 analog input.
	ACMP0_N	A	MFP1	Analog comparator 0 negative input pin.
	EBI_ADR2	O	MFP2	EBI address bus bit 2.
	SD0_DAT1	I/O	MFP3	SD/SDIO0 data line bit 1.
	EMAC_RMII_RXD1	I	MFP4	EMAC RMII Receive Data bus bit 1.
	SPI1_CLK	I/O	MFP5	SPI1 serial clock pin.
	UART1_TXD	O	MFP6	UART1 data transmitter output pin.
	UART5_nRTS	O	MFP7	UART5 request to Send output pin.
	USCI1_DAT1	I/O	MFP8	USCI1 data 1 pin.
	SC0_RST	O	MFP9	Smart Card 0 reset pin.
	I2S0_DI	I	MFP10	I2S0 data input pin.
	EPWM0_CH2	I/O	MFP11	EPWM0 channel 2 output/capture input.
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
	INT2	I	MFP15	External interrupt 2 input pin.
C1	PB.4	B3	MFP0	General purpose digital I/O pin.
	EADC0_CH4	A	MFP1	EADC0 channel 4 analog input.
	ACMP1_P1	A	MFP1	Analog comparator 1 positive input 1 pin.
	EBI_ADR1	O	MFP2	EBI address bus bit 1.
	SD0_DAT2	I/O	MFP3	SD/SDIO0 data line bit 2.
	EMAC_RMII_RXD0	I	MFP4	EMAC RMII Receive Data bus bit 0.
	SPI1_MOSI	I/O	MFP5	SPI1 MOSI (Master Out, Slave In) pin.
	I2C0_SDA	I/O	MFP6	I2C0 data input/output pin.
	UART5_RXD	I	MFP7	UART5 data receiver input pin.
	USCI1_CTL1	I/O	MFP8	USCI1 control 1 pin.
	SC0_DAT	I/O	MFP9	Smart Card 0 data pin.
	I2S0_MCLK	O	MFP10	I2S0 master clock output pin.
	EPWM0_CH1	I/O	MFP11	EPWM0 channel 1 output/capture input.
	TM1	I/O	MFP14	Timer1 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
B2	PB.5	B3	MFP0	General purpose digital I/O pin.
	EADC0_CH5	A	MFP1	EADC0 channel 5 analog input.
	ACMP1_N	A	MFP1	Analog comparator 1 negative input pin.
	EBI_ADR0	O	MFP2	EBI address bus bit 0.
	SD0_DAT3	I/O	MFP3	SD/SDIO0 data line bit 3.
	EMAC_RMII_REFCLK	I	MFP4	EMAC RMII reference clock input pin.
	SPI1_MISO	I/O	MFP5	SPI1 MISO (Master In, Slave Out) pin.

Pin No	Pin Name	Type	MFP	Description
	I2C0_SCL	I/O	MFP6	I2C0 clock pin.
	UART5_TXD	O	MFP7	UART5 data transmitter output pin.
	USCI1_CTL0	I/O	MFP8	USCI1 control 0 pin.
	SC0_CLK	O	MFP9	Smart Card 0 clock pin.
	I2S0_BCLK	O	MFP10	I2S0 bit clock output pin.
	EPWM0_CH0	I/O	MFP11	EPWM0 channel 0 output/capture input.
	TM0	I/O	MFP14	Timer0 event counter input/toggle output pin.
	INT0	I	MFP15	External interrupt 0 input pin.
B1	PB.6	B3	MFP0	General purpose digital I/O pin.
	EADC0_CH6	A	MFP1	EADC0 channel 6 analog input.
	EBI_nWRH	O	MFP2	EBI high byte write enable output pin
	EMAC_PPS	O	MFP3	EMAC Pulse Per Second output pin.
	USCI1_DAT1	I/O	MFP4	USCI1 data 1 pin.
	CAN1_RXD	I	MFP5	CAN1 bus receiver input.
	UART1_RXD	I	MFP6	UART1 data receiver input pin.
	SD1_CLK	O	MFP7	SD/SDIO1 clock output pin
	EBI_nCS1	O	MFP8	EBI chip select 1 output pin.
	BPWM1_CH5	I/O	MFP10	BPWM1 channel 5 output/capture input.
	EPWM1_BRAKE1	I	MFP11	EPWM1 Brake 1 input pin.
	EPWM1_CH5	I/O	MFP12	EPWM1 channel 5 output/capture input.
	INT4	I	MFP13	External interrupt 4 input pin.
	USB_VBUS_EN	O	MFP14	USB external VBUS regulator enable pin.
	ACMP1_O	O	MFP15	Analog comparator 1 output pin.
A1	PB.7	B3	MFP0	General purpose digital I/O pin.
	EADC0_CH7	A	MFP1	EADC0 channel 7 analog input.
	EBI_nWRL	O	MFP2	EBI low byte write enable output pin.
	EMAC_RMII_TXEN	O	MFP3	EMAC RMII Transmit Enable output pin.
	USCI1_DAT0	I/O	MFP4	USCI1 data 0 pin.
	CAN1_TXD	O	MFP5	CAN1 bus transmitter output.
	UART1_TXD	O	MFP6	UART1 data transmitter output pin.
	SD1_CMD	I/O	MFP7	SD/SDIO1 command/response pin
	EBI_nCS0	O	MFP8	EBI chip select 0 output pin.
	BPWM1_CH4	I/O	MFP10	BPWM1 channel 4 output/capture input.
	EPWM1_BRAKE0	I	MFP11	EPWM1 Brake 0 input pin.
	EPWM1_CH4	I/O	MFP12	EPWM1 channel 4 output/capture input.
	INT5	I	MFP13	External interrupt 5 input pin.
	USB_VBUS_ST	I	MFP14	USB external VBUS regulator status pin.
	ACMP0_O	O	MFP15	Analog comparator 0 output pin.
A2	PB.8	B3	MFP0	General purpose digital I/O pin.
	EADC0_CH8	A	MFP1	EADC0 channel 8 analog input.
	EBI_ADR19	O	MFP2	EBI address bus bit 19.
	EMAC_RMII_TXD1	O	MFP3	EMAC RMII Transmit Data bus bit 1.
	USCI1_CLK	I/O	MFP4	USCI1 clock pin.
	UART0_RXD	I	MFP5	UART0 data receiver input pin.
	UART1_nRTS	O	MFP6	UART1 request to Send output pin.
	I2C1_SMBSUS	O	MFP7	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
	BPWM1_CH3	I/O	MFP10	BPWM1 channel 3 output/capture input.
	SPI3_MOSI	I/O	MFP11	SPI3 MOSI (Master Out, Slave In) pin.
	INT6	I	MFP13	External interrupt 6 input pin.

Pin No	Pin Name	Type	MFP	Description
C3	PB.9	B3	MFP0	General purpose digital I/O pin.
	EADC0_CH9	A	MFP1	EADC0 channel 9 analog input.
	EBI_ADR18	O	MFP2	EBI address bus bit 18.
	EMAC_RMII_TXD0	O	MFP3	EMAC RMII Transmit Data bus bit 0.
	USCI1_CTL1	I/O	MFP4	USCI1 control 1 pin.
	UART0_TXD	O	MFP5	UART0 data transmitter output pin.
	UART1_nCTS	I	MFP6	UART1 clear to Send input pin.
	I2C1_SMBAL	O	MFP7	I2C1 SMBus SMBALTER pin
	BPWM1_CH2	I/O	MFP10	BPWM1 channel 2 output/capture input.
	SPI3_MISO	I/O	MFP11	SPI3 MISO (Master In, Slave Out) pin.
	INT7	I	MFP13	External interrupt 7 input pin.
B3	PB.10	B3	MFP0	General purpose digital I/O pin.
	EADC0_CH10	A	MFP1	EADC0 channel 10 analog input.
	EBI_ADR17	O	MFP2	EBI address bus bit 17.
	EMAC_RMII_MDIO	I/O	MFP3	EMAC RMII PHY Management Data pin.
	USCI1_CTL0	I/O	MFP4	USCI1 control 0 pin.
	UART0_nRTS	O	MFP5	UART0 request to Send output pin.
	UART4_RXD	I	MFP6	UART4 data receiver input pin.
	I2C1_SDA	I/O	MFP7	I2C1 data input/output pin.
	CAN0_RXD	I	MFP8	CAN0 bus receiver input.
	BPWM1_CH1	I/O	MFP10	BPWM1 channel 1 output/capture input.
	SPI3_SS	I/O	MFP11	SPI3 slave select pin.
	HSUSB_VBUS_EN	O	MFP14	HSUSB external VBUS regulator enable pin.
C4	PB.11	B3	MFP0	General purpose digital I/O pin.
	EADC0_CH11	A	MFP1	EADC0 channel 11 analog input.
	EBI_ADR16	O	MFP2	EBI address bus bit 16.
	EMAC_RMII_MDC	O	MFP3	EMAC RMII PHY Management Clock output pin.
	UART0_nCTS	I	MFP5	UART0 clear to Send input pin.
	UART4_TXD	O	MFP6	UART4 data transmitter output pin.
	I2C1_SCL	I/O	MFP7	I2C1 clock pin.
	CAN0_TXD	O	MFP8	CAN0 bus transmitter output.
	SPI0_I2SMCLK	I/O	MFP9	SPI0 I2S master clock output pin
	BPWM1_CH0	I/O	MFP10	BPWM1 channel 0 output/capture input.
	SPI3_CLK	I/O	MFP11	SPI3 serial clock pin.
	HSUSB_VBUS_ST	I	MFP14	HSUSB external VBUS regulator status pin.
D5	PB.12	B3	MFP0	General purpose digital I/O pin.
	EADC0_CH12	A	MFP1	EADC0 channel 12 analog input.
	DAC0_OUT	A	MFP1	DAC0 channel analog output.
	ACMP0_P2	A	MFP1	Analog comparator 0 positive input 2 pin.
	ACMP1_P2	A	MFP1	Analog comparator 1 positive input 2 pin.
	EBI_AD15	I/O	MFP2	EBI address/data bus bit 15.
	SC1_CLK	O	MFP3	Smart Card 1 clock pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	USCI0_CLK	I/O	MFP5	USCI0 clock pin.
	UART0_RXD	I	MFP6	UART0 data receiver input pin.
	UART3_nCTS	I	MFP7	UART3 clear to Send input pin.
	I2C2_SDA	I/O	MFP8	I2C2 data input/output pin.
	SD0_nCD	I	MFP9	SD/SDIO0 card detect input pin
	EPWM1_CH3	I/O	MFP11	EPWM1 channel 3 output/capture input.
	TM3_EXT	I/O	MFP13	Timer3 external capture input/toggle output pin.

Pin No	Pin Name	Type	MFP	Description
D3	PB.13	B3	MFP0	General purpose digital I/O pin.
	EADC0_CH13	A	MFP1	EADC0 channel 13 analog input.
	DAC1_OUT	A	MFP1	DAC1 channel analog output.
	ACMP0_P3	A	MFP1	Analog comparator 0 positive input 3 pin.
	ACMP1_P3	A	MFP1	Analog comparator 1 positive input 3 pin.
	EBI_AD14	I/O	MFP2	EBI address/data bus bit 14.
	SC1_DAT	I/O	MFP3	Smart Card 1 data pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	USCI0_DAT0	I/O	MFP5	USCI0 data 0 pin.
	UART0_TXD	O	MFP6	UART0 data transmitter output pin.
	UART3_nRTS	O	MFP7	UART3 request to Send output pin.
	I2C2_SCL	I/O	MFP8	I2C2 clock pin.
	EPWM1_CH2	I/O	MFP11	EPWM1 channel 2 output/capture input.
	TM2_EXT	I/O	MFP13	Timer2 external capture input/toggle output pin.
C5	PB.14	B3	MFP0	General purpose digital I/O pin.
	EADC0_CH14	A	MFP1	EADC0 channel 14 analog input.
	EBI_AD13	I/O	MFP2	EBI address/data bus bit 13.
	SC1_RST	O	MFP3	Smart Card 1 reset pin.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	USCI0_DAT1	I/O	MFP5	USCI0 data 1 pin.
	UART0_nRTS	O	MFP6	UART0 request to Send output pin.
	UART3_RXD	I	MFP7	UART3 data receiver input pin.
	I2C2_SMBSUS	O	MFP8	I2C2 SMBus SMBSUS pin (PMBus CONTROL pin)
	EPWM1_CH1	I/O	MFP11	EPWM1 channel 1 output/capture input.
	TM1_EXT	I/O	MFP13	Timer1 external capture input/toggle output pin.
	CLKO	O	MFP14	Clock Out
D4	PB.15	B3	MFP0	General purpose digital I/O pin.
	EADC0_CH15	A	MFP1	EADC0 channel 15 analog input.
	EBI_AD12	I/O	MFP2	EBI address/data bus bit 12.
	SC1_PWR	O	MFP3	Smart Card 1 power pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	USCI0_CTL1	I/O	MFP5	USCI0 control 1 pin.
	UART0_nCTS	I	MFP6	UART0 clear to Send input pin.
	UART3_TXD	O	MFP7	UART3 data transmitter output pin.
	I2C2_SMBAL	O	MFP8	I2C2 SMBus SMBALTER pin
	EPWM1_CH0	I/O	MFP11	EPWM1 channel 0 output/capture input.
	TM0_EXT	I/O	MFP13	Timer0 external capture input/toggle output pin.
	USB_VBUS_EN	O	MFP14	USB external VBUS regulator enable pin.
	HSUSB_VBUS_EN	O	MFP15	HSUSB external VBUS regulator enable pin.
K12	PC.0	B5	MFP0	General purpose digital I/O pin.
	EBI_AD0	I/O	MFP2	EBI address/data bus bit 0.
	SPIM_MOSI	I/O	MFP3	SPIM MOSI (Master Out, Slave In) pin.
	QSPI0_MOSI0	I/O	MFP4	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
	SC1_CLK	O	MFP5	Smart Card 1 clock pin.
	I2S0_LRCK	O	MFP6	I2S0 left right channel clock output pin.
	SPI1_SS	I/O	MFP7	SPI1 slave select pin.
	UART2_RXD	I	MFP8	UART2 data receiver input pin.
	I2C0_SDA	I/O	MFP9	I2C0 data input/output pin.
	EPWM1_CH5	I/O	MFP12	EPWM1 channel 5 output/capture input.

Pin No	Pin Name	Type	MFP	Description
	ACMP1_O	O	MFP14	Analog comparator 1 output pin.
K11	PC.1	B5	MFP0	General purpose digital I/O pin.
	EBI_AD1	I/O	MFP2	EBI address/data bus bit 1.
	SPIM_MISO	I/O	MFP3	SPIM MISO (Master In, Slave Out) pin.
	QSPI0_MISO0	I/O	MFP4	Quad SPI0 MISO0 (Master In, Slave Out) pin.
	SC1_DAT	I/O	MFP5	Smart Card 1 data pin.
	I2S0_DO	O	MFP6	I2S0 data output pin.
	SPI1_CLK	I/O	MFP7	SPI1 serial clock pin.
	UART2_TXD	O	MFP8	UART2 data transmitter output pin.
	I2C0_SCL	I/O	MFP9	I2C0 clock pin.
	EPWM1_CH4	I/O	MFP12	EPWM1 channel 4 output/capture input.
	ACMP0_O	O	MFP14	Analog comparator 0 output pin.
L12	PC.2	B5	MFP0	General purpose digital I/O pin.
	EBI_AD2	I/O	MFP2	EBI address/data bus bit 2.
	SPIM_CLK	I/O	MFP3	SPIM serial clock pin.
	QSPI0_CLK	I/O	MFP4	Quad SPI0 serial clock pin.
	SC1_RST	O	MFP5	Smart Card 1 reset pin.
	I2S0_DI	I	MFP6	I2S0 data input pin.
	SPI1_MOSI	I/O	MFP7	SPI1 MOSI (Master Out, Slave In) pin.
	UART2_nCTS	I	MFP8	UART2 clear to Send input pin.
	I2C0_SMBSUS	O	MFP9	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
	CAN1_RXD	I	MFP10	CAN1 bus receiver input.
	UART3_RXD	I	MFP11	UART3 data receiver input pin.
	EPWM1_CH3	I/O	MFP12	EPWM1 channel 3 output/capture input.
L11	PC.3	B5	MFP0	General purpose digital I/O pin.
	EBI_AD3	I/O	MFP2	EBI address/data bus bit 3.
	SPIM_SS	I/O	MFP3	SPIM slave select pin.
	QSPI0_SS	I/O	MFP4	Quad SPI0 slave select pin.
	SC1_PWR	O	MFP5	Smart Card 1 power pin.
	I2S0_MCLK	O	MFP6	I2S0 master clock output pin.
	SPI1_MISO	I/O	MFP7	SPI1 MISO (Master In, Slave Out) pin.
	UART2_nRTS	O	MFP8	UART2 request to Send output pin.
	I2C0_SMBAL	O	MFP9	I2C0 SMBus SMBALTER pin
	CAN1_TXD	O	MFP10	CAN1 bus transmitter output.
	UART3_TXD	O	MFP11	UART3 data transmitter output pin.
	EPWM1_CH2	I/O	MFP12	EPWM1 channel 2 output/capture input.
M12	PC.4	B5	MFP0	General purpose digital I/O pin.
	EBI_AD4	I/O	MFP2	EBI address/data bus bit 4.
	SPIM_D3	I/O	MFP3	SPIM data 3 pin for Quad Mode I/O.
	QSPI0_MOSI1	I/O	MFP4	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
	SC1_nCD	I	MFP5	Smart Card 1 card detect pin.
	I2S0_BCLK	O	MFP6	I2S0 bit clock output pin.
	SPI1_I2SMCLK	I/O	MFP7	SPI1 I2S master clock output pin
	UART2_RXD	I	MFP8	UART2 data receiver input pin.
	I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
	CAN0_RXD	I	MFP10	CAN0 bus receiver input.
	UART4_RXD	I	MFP11	UART4 data receiver input pin.
	EPWM1_CH1	I/O	MFP12	EPWM1 channel 1 output/capture input.
M11	PC.5	B5	MFP0	General purpose digital I/O pin.

Pin No	Pin Name	Type	MFP	Description
	EBI_AD5	I/O	MFP2	EBI address/data bus bit 5.
	SPIM_D2	I/O	MFP3	SPIM data 2 pin for Quad Mode I/O.
	QSPI0_MISO1	I/O	MFP4	Quad SPI0 MISO1 (Master In, Slave Out) pin.
	UART2_TXD	O	MFP8	UART2 data transmitter output pin.
	I2C1_SCL	I/O	MFP9	I2C1 clock pin.
	CAN0_TXD	O	MFP10	CAN0 bus transmitter output.
	UART4_TXD	O	MFP11	UART4 data transmitter output pin.
	EPWM1_CH0	I/O	MFP12	EPWM1 channel 0 output/capture input.
K5	PC.6	B5	MFP0	General purpose digital I/O pin.
	EBI_AD8	I/O	MFP2	EBI address/data bus bit 8.
	EMAC_RMII_RXD1	I	MFP3	EMAC RMII Receive Data bus bit 1.
	SPI1_MOSI	I/O	MFP4	SPI1 MOSI (Master Out, Slave In) pin.
	UART4_RXD	I	MFP5	UART4 data receiver input pin.
	SC2_RST	O	MFP6	Smart Card 2 reset pin.
	UART0_nRTS	O	MFP7	UART0 request to Send output pin.
	I2C1_SMBSUS	O	MFP8	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
	EPWM1_CH3	I/O	MFP11	EPWM1 channel 3 output/capture input.
	BPWM1_CH1	I/O	MFP12	BPWM1 channel 1 output/capture input.
	TM1	I/O	MFP14	Timer1 event counter input/toggle output pin.
	INT2	I	MFP15	External interrupt 2 input pin.
K4	PC.7	B5	MFP0	General purpose digital I/O pin.
	EBI_AD9	I/O	MFP2	EBI address/data bus bit 9.
	EMAC_RMII_RXD0	I	MFP3	EMAC RMII Receive Data bus bit 0.
	SPI1_MISO	I/O	MFP4	SPI1 MISO (Master In, Slave Out) pin.
	UART4_TXD	O	MFP5	UART4 data transmitter output pin.
	SC2_PWR	O	MFP6	Smart Card 2 power pin.
	UART0_nCTS	I	MFP7	UART0 clear to Send input pin.
	I2C1_SMBAL	O	MFP8	I2C1 SMBus SMBALTER pin
	EPWM1_CH2	I/O	MFP11	EPWM1 channel 2 output/capture input.
	BPWM1_CH0	I/O	MFP12	BPWM1 channel 0 output/capture input.
	TM0	I/O	MFP14	Timer0 event counter input/toggle output pin.
	INT3	I	MFP15	External interrupt 3 input pin.
J5	PC.8	B5	MFP0	General purpose digital I/O pin.
	EBI_ADR16	O	MFP2	EBI address bus bit 16.
	EMAC_RMII_REFCLK	I	MFP3	EMAC RMII reference clock input pin.
	I2C0_SDA	I/O	MFP4	I2C0 data input/output pin.
	UART4_nCTS	I	MFP5	UART4 clear to Send input pin.
	UART1_RXD	I	MFP8	UART1 data receiver input pin.
	EPWM1_CH1	I/O	MFP11	EPWM1 channel 1 output/capture input.
	BPWM1_CH4	I/O	MFP12	BPWM1 channel 4 output/capture input.
A6	PC.14	B5	MFP0	General purpose digital I/O pin.
	EBI_AD11	I/O	MFP2	EBI address/data bus bit 11.
	SC1_nCD	I	MFP3	Smart Card 1 card detect pin.
	SPI0_I2SMCLK	I/O	MFP4	SPI0 I2S master clock output pin
	USCI0_CTL0	I/O	MFP5	USCI0 control 0 pin.
	QSPI0_CLK	I/O	MFP6	Quad SPI0 serial clock pin.
	EPWM0_SYNC_IN	I	MFP11	EPWM0 counter synchronous trigger input pin.
	TM1	I/O	MFP13	Timer1 event counter input/toggle output pin.

Pin No	Pin Name	Type	MFP	Description
	USB_VBUS_ST	I	MFP14	USB external VBUS regulator status pin.
	HSUSB_VBUS_ST	I	MFP15	HSUSB external VBUS regulator status pin.
D10	PE.0	B5	MFP0	General purpose digital I/O pin.
	EBI_AD11	I/O	MFP2	EBI address/data bus bit 11.
	QSPI0_MOSI0	I/O	MFP3	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
	SC2_CLK	O	MFP4	Smart Card 2 clock pin.
	I2S0_MCLK	O	MFP5	I2S0 master clock output pin.
	SPI1_MOSI	I/O	MFP6	SPI1 MOSI (Master Out, Slave In) pin.
	UART3_RXD	I	MFP7	UART3 data receiver input pin.
	I2C1_SDA	I/O	MFP8	I2C1 data input/output pin.
	UART4_nRTS	O	MFP9	UART4 request to Send output pin.
E11	PE.1	B5	MFP0	General purpose digital I/O pin.
	EBI_AD10	I/O	MFP2	EBI address/data bus bit 10.
	QSPI0_MISO0	I/O	MFP3	Quad SPI0 MISO0 (Master In, Slave Out) pin.
	SC2_DAT	I/O	MFP4	Smart Card 2 data pin.
	I2S0_BCLK	O	MFP5	I2S0 bit clock output pin.
	SPI1_MISO	I/O	MFP6	SPI1 MISO (Master In, Slave Out) pin.
	UART3_TXD	O	MFP7	UART3 data transmitter output pin.
	I2C1_SCL	I/O	MFP8	I2C1 clock pin.
	UART4_nCTS	I	MFP9	UART4 clear to Send input pin.
E12	PE.2	B5	MFP0	General purpose digital I/O pin.
	EBI_ALE	O	MFP2	EBI address latch enable output pin.
	SD0_DAT0	I/O	MFP3	SD/SDIO0 data line bit 0.
	SPIM_MOSI	I/O	MFP4	SPIM MOSI (Master Out, Slave In) pin.
	SPI3_MOSI	I/O	MFP5	SPI3 MOSI (Master Out, Slave In) pin.
	SC0_CLK	O	MFP6	Smart Card 0 clock pin.
	USCI0_CLK	I/O	MFP7	USCI0 clock pin.
	QEI0_B	I	MFP11	Quadrature encoder 0 phase B input
	EPWM0_CH5	I/O	MFP12	EPWM0 channel 5 output/capture input.
	BPWM0_CH0	I/O	MFP13	BPWM0 channel 0 output/capture input.
F12	PE.3	B5	MFP0	General purpose digital I/O pin.
	EBI_MCLK	O	MFP2	EBI external clock output pin.
	SD0_DAT1	I/O	MFP3	SD/SDIO0 data line bit 1.
	SPIM_MISO	I/O	MFP4	SPIM MISO (Master In, Slave Out) pin.
	SPI3_MISO	I/O	MFP5	SPI3 MISO (Master In, Slave Out) pin.
	SC0_DAT	I/O	MFP6	Smart Card 0 data pin.
	USCI0_DAT0	I/O	MFP7	USCI0 data 0 pin.
	QEI0_A	I	MFP11	Quadrature encoder 0 phase A input
	EPWM0_CH4	I/O	MFP12	EPWM0 channel 4 output/capture input.
	BPWM0_CH1	I/O	MFP13	BPWM0 channel 1 output/capture input.
F11	PE.4	B5	MFP0	General purpose digital I/O pin.
	EBI_nWR	O	MFP2	EBI write enable output pin.
	SD0_DAT2	I/O	MFP3	SD/SDIO0 data line bit 2.
	SPIM_CLK	I/O	MFP4	SPIM serial clock pin.
	SPI3_CLK	I/O	MFP5	SPI3 serial clock pin.
	SC0_RST	O	MFP6	Smart Card 0 reset pin.
	USCI0_DAT1	I/O	MFP7	USCI0 data 1 pin.
	QEI0_INDEX	I	MFP11	Quadrature encoder 0 index input
	EPWM0_CH3	I/O	MFP12	EPWM0 channel 3 output/capture input.
	BPWM0_CH2	I/O	MFP13	BPWM0 channel 2 output/capture input.

Pin No	Pin Name	Type	MFP	Description
G12	PE.5	B5	MFP0	General purpose digital I/O pin.
	EBI_nRD	O	MFP2	EBI read enable output pin.
	SD0_DAT3	I/O	MFP3	SD/SDIO0 data line bit 3.
	SPIM_SS	I/O	MFP4	SPIM slave select pin.
	SPI3_SS	I/O	MFP5	SPI3 slave select pin.
	SC0_PWR	O	MFP6	Smart Card 0 power pin.
	USCI0_CTL1	I/O	MFP7	USCI0 control 1 pin.
	QEI1_B	I	MFP11	Quadrature encoder 1 phase B input
	EPWM0_CH2	I/O	MFP12	EPWM0 channel 2 output/capture input.
	BPWM0_CH3	I/O	MFP13	BPWM0 channel 3 output/capture input.
F10	PE.6	B5	MFP0	General purpose digital I/O pin.
	SD0_CLK	O	MFP3	SD/SDIO0 clock output pin
	SPIM_D3	I/O	MFP4	SPIM data 3 pin for Quad Mode I/O.
	SPI3_I2SMCLK	I/O	MFP5	SPI3 I2S master clock output pin
	SC0_nCD	I	MFP6	Smart Card 0 card detect pin.
	USCI0_CTL0	I/O	MFP7	USCI0 control 0 pin.
	UART5_RXD	I	MFP8	UART5 data receiver input pin.
	CAN1_RXD	I	MFP9	CAN1 bus receiver input.
	QEI1_A	I	MFP11	Quadrature encoder 1 phase A input
	EPWM0_CH1	I/O	MFP12	EPWM0 channel 1 output/capture input.
	BPWM0_CH4	I/O	MFP13	BPWM0 channel 4 output/capture input.
E10	PE.7	B5	MFP0	General purpose digital I/O pin.
	SD0_CMD	I/O	MFP3	SD/SDIO0 command/response pin
	SPIM_D2	I/O	MFP4	SPIM data 2 pin for Quad Mode I/O.
	UART5_TXD	O	MFP8	UART5 data transmitter output pin.
	CAN1_TXD	O	MFP9	CAN1 bus transmitter output.
	QEI1_INDEX	I	MFP11	Quadrature encoder 1 index input
	EPWM0_CH0	I/O	MFP12	EPWM0 channel 0 output/capture input.
	BPWM0_CH5	I/O	MFP13	BPWM0 channel 5 output/capture input.
J4	PE.13	B5	MFP0	General purpose digital I/O pin.
	EBI_ADR15	O	MFP2	EBI address bus bit 15.
	EMAC_PPS	O	MFP3	EMAC Pulse Per Second output pin.
	I2C0_SCL	I/O	MFP4	I2C0 clock pin.
	UART4_nRTS	O	MFP5	UART4 request to Send output pin.
	UART1_TXD	O	MFP8	UART1 data transmitter output pin.
	EPWM0_CH5	I/O	MFP10	EPWM0 channel 5 output/capture input.
	EPWM1_CH0	I/O	MFP11	EPWM1 channel 0 output/capture input.
	BPWM1_CH5	I/O	MFP12	BPWM1 channel 5 output/capture input.
	ECAP1_IC0	I	MFP13	Enhanced capture unit 1 input 0 pin.
M10	PF.0	B5	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MFP2	UART1 data transmitter output pin.
	I2C1_SCL	I/O	MFP3	I2C1 clock pin.
	BPWM1_CH0	I/O	MFP12	BPWM1 channel 0 output/capture input.
	ICE_DAT	O	MFP14	Serial wired debugger data pin.
L10	PF.1	B5	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MFP2	UART1 data receiver input pin.
	I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
	BPWM1_CH1	I/O	MFP12	BPWM1 channel 1 output/capture input.
	ICE_CLK	I	MFP14	Serial wired debugger clock pin.
J1	PF.2	B3	MFP0	General purpose digital I/O pin.

Pin No	Pin Name	Type	MFP	Description
	EBI_nCS1	O	MFP2	EBI chip select 1 output pin.
	UART0_RXD	I	MFP3	UART0 data receiver input pin.
	I2C0_SDA	I/O	MFP4	I2C0 data input/output pin.
	QSPI0_CLK	I/O	MFP5	Quad SPI0 serial clock pin.
	XT1_OUT	O	MFP10	External 4~24 MHz (high speed) crystal output pin.
	BPWM1_CH1	I/O	MFP11	BPWM1 channel 1 output/capture input.
K1	PF.3	B3	MFP0	General purpose digital I/O pin.
	EBI_nCS0	O	MFP2	EBI chip select 0 output pin.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.
	I2C0_SCL	I/O	MFP4	I2C0 clock pin.
	XT1_IN	I	MFP10	External 4~24 MHz (high speed) crystal input pin.
	BPWM1_CH0	I/O	MFP11	BPWM1 channel 0 output/capture input.
G1	PF.4	B3	MFP0	General purpose digital I/O pin.
	UART2_TXD	O	MFP2	UART2 data transmitter output pin.
	UART2_nRTS	O	MFP4	UART2 request to Send output pin.
	BPWM0_CH5	I/O	MFP8	BPWM0 channel 5 output/capture input.
	X32_OUT	O	MFP10	External 32.768 KHz crystal output pin.
H1	PF.5	B3	MFP0	General purpose digital I/O pin.
	UART2_RXD	I	MFP2	UART2 data receiver input pin.
	UART2_nCTS	I	MFP4	UART2 clear to Send input pin.
	BPWM0_CH4	I/O	MFP8	BPWM0 channel 4 output/capture input.
	EPWM0_SYNC_OUT	O	MFP9	EPWM0 counter synchronous trigger output pin.
	X32_IN	I	MFP10	External 32.768 KHz crystal input pin.
	EADC0_ST	I	MFP11	EADC0 external trigger input.
H2	PF.6	B5	MFP0	General purpose digital I/O pin.
	EBI_ADR19	O	MFP2	EBI address bus bit 19.
	SC0_CLK	O	MFP3	Smart Card 0 clock pin.
	I2S0_LRCK	O	MFP4	I2S0 left right channel clock output pin.
	SPI0_MOSI	I/O	MFP5	SPI0 MOSI (Master Out, Slave In) pin.
	UART4_RXD	I	MFP6	UART4 data receiver input pin.
	EBI_nCS0	O	MFP7	EBI chip select 0 output pin.
	TAMPER0	I/O	MFP10	TAMPER detector loop pin 0.
C8	PH.8	B5	MFP0	General purpose digital I/O pin.
	EBI_AD12	I/O	MFP2	EBI address/data bus bit 12.
	QSPI0_CLK	I/O	MFP3	Quad SPI0 serial clock pin.
	SC2_PWR	O	MFP4	Smart Card 2 power pin.
	I2S0_DI	I	MFP5	I2S0 data input pin.
	SPI1_CLK	I/O	MFP6	SPI1 serial clock pin.
	UART3_nRTS	O	MFP7	UART3 request to Send output pin.
	I2C1_SMBAL	O	MFP8	I2C1 SMBus SMBALTER pin
	I2C2_SCL	I/O	MFP9	I2C2 clock pin.
	UART1_TXD	O	MFP10	UART1 data transmitter output pin.
B8	PH.9	B5	MFP0	General purpose digital I/O pin.
	EBI_AD13	I/O	MFP2	EBI address/data bus bit 13.
	QSPI0_SS	I/O	MFP3	Quad SPI0 slave select pin.
	SC2_RST	O	MFP4	Smart Card 2 reset pin.
	I2S0_DO	O	MFP5	I2S0 data output pin.
	SPI1_SS	I/O	MFP6	SPI1 slave select pin.
	UART3_nCTS	I	MFP7	UART3 clear to Send input pin.

Pin No	Pin Name	Type	MFP	Description
	I2C1_SMBSUS	O	MFP8	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
	I2C2_SDA	I/O	MFP9	I2C2 data input/output pin.
	UART1_RXD	I	MFP10	UART1 data receiver input pin.
A11	HSUSB_VDD12_CAP	A	MFP0	HSUSB Internal power regulator output 1.2V decoupling pin. Note: This pin needs to be connected with a 1uF capacitor.
A12	HSUSB_D+	A	MFP0	HSUSB differential signal D+.
B11	HSUSB_ID	I	MFP0	HSUSB identification.
B12	HSUSB_D-	A	MFP0	HSUSB differential signal D-.
C11	HSUSB_VBUS	P	MFP0	HSUSB Power supply from USB host or HUB.
C12	HSUSB_VRES	A	MFP0	HSUSB module reference resister
D11	HSUSB_VSS	P	MFP0	Ground pin for HSUSB.
D12	HSUSB_VDD33	P	MFP0	Power supply for HSUSB VDD33

1.4.2 ESC Sub-system Pin Description

The multi-function pin settings are configured by the I^2C Hardware Configuration EEPROM (HWCFGEE). Please refer to Section 2.43.4.2 for details.

Pin No	Pin Name	Type	MFP	Description
D9	TEST	I5/PD/S		Test mode enable For normal operation, please always tie to logic low or NC.
C10	RSTn	I5/PU/S		Reset Input, active low RST_N is the hardware reset input used to reset this chip. This input is AND with internal Power-On-Reset (POR) circuit, which generates the main system reset for this chip.
E9	RSTO\ RSTO_POL	O5/8m		Reset Output This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the RSTO polarity, please refer to Section 2.43.4.1.
F9	NC	I3		Reserved. Please connect to GND.
L1	LED_RUN\ EEP_SIZE	B5/4m		RUN LED This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the EEPROM size configuration, please refer to Section 2.43.4.1.
L2	LED_ERR\ 3PORT_MODE	B5/4m		Error LED This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the Port 2 MII enable configuration, please refer to Section 2.43.4.1.
J10	P0_ACT\ P0_FIBER	B5/4m		PHY 0 Link/Activity LED This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the PHY 0 media mode, please refer to Section 2.43.4.1.
J11	P1_ACT\ P1_FIBER	B5/4m		PHY 1 Link/Activity LED This pin is input direction during chip reset stage

Pin No	Pin Name	Type	MFP	Description
				used to bootstrap the mode setting to decide the PHY 1 media mode, please refer to Section 2.43.4.1.
E2	SYNC_LATCH[1]	B5/8m		Distributed Clocks SyncSignal output or LatchSignal input 1
E3	SYNC_LATCH[0]	B5/8m		Distributed Clocks SyncSignal output or LatchSignal input 0
K2	EEP_DONE	O5/8m		EEPROM is loaded, PDI is active.
B10	PDI_EMU	I5		PDI Emulation enable
D8	OE_EXT	I5		Output Enable
	LRDn	I5		Local bus Read
	SCLK	I5		SPI Clock
E4	SOF	O5/8m		Start-of-Frame
	LECSn	I5		Local bus ESC Chip Select
	SCS_ESC	I5		SPI Chip Select for ESC
E5	OUTVLD	O5/8m		Output data Valid/Output event
	LWRn	I5		Local bus Write
	MOSI	I5		SPI data MOSI
F4	EOF	O5/8m		End-of-Frame
	LFCSn	I5		Local bus Function Chip Select
	SCS_FUNC	I5		SPI Chip Select for Function
G4	WD_TRIG	O5/8m		Watchdog Trigger
	LINT	O5/T		Local bus Interrupt
	SINT	O5/T		SPI Interrupt
A10	SCL	O5/T/4m /S		I2C Serial Clock line for I2C master controller SCL is a tri-stateable output, which requires an external pull-up resistor.
B9	SDA	B5/T/4m /S		I2C Serial Data line for I2C master controller. SDA is a tri-stateable output, which requires an external pull-up resistor.
H4	LAT_IN	I5		external data Latch
	LRDY	O5/T		Local bus Ready
	MISO	O5		SPI data MISO
H10	IO[0]	B5/8m		Digital /General Purpose I/O[7:0]
	LDA[0]	B5		Local bus Data bus [7:0]
	MSCLK	O5		SPI Master SCLK
G9	IO[1]	B5/8m		Digital /General Purpose I/O[7:0]
	LDA[1]	B5		Local bus Data bus [7:0]
	MMOSI	O5		SPI Master MOSI
F3	IO[2]	B5/8m		Digital /General Purpose I/O[7:0]
	LDA[2]	B5		Local bus Data bus [7:0]
	MMISO	I5		SPI Master MISO
C9	IO[4]	B5/8m		Digital /General Purpose I/O[7:0]
	LDA[4]	B5		Local bus Data bus [7:0]
	MSS[0]	O5		SPI Master Slave Select
J12	IO[16]	B5/8m		Digital /General Purpose I/O[23:16]
	LA[8]	I5		Local bus Address bus
	LINK	I5		LINK Provided by the PHY if a 100 Mbps (Full Duplex) link is established.
G10	IO[17]	B5/8m		Digital /General Purpose I/O[23:16]
	LA[9]	I5		Local bus Address bus

Pin No	Pin Name	Type	MFP	Description
	PULAB	O5		Pulse AB, toggle when programmable point A and B
	MDIO	B5		PHY Management Interface data
H11	IO[18]	B5/8m		Digital /General Purpose I/O[23:16]
	LA[10]	I5		Local bus Address bus
	PULC	O5		Pulse C, PWM period central point
	MDC	O5		PHY Management Interface clock
G11	IO[19]	B5/8m		Digital /General Purpose I/O[23:16]
	LA[11]	I5		Local bus Address bus
	PULZ	O5		Pulse Z, PWM period start point
	TXD[0] \ LINK_POL	O5		Transmit data [0] These pins are input direction during chip reset use to bootstrap the mode setting to decide external PHY's LINK polarity, please refer to Section 3.1.
H9	IO[20]	B5/8m		Digital /General Purpose I/O[23:16]
	LA[12]	I5		Local bus Address bus
	PULB	O5		Pulse B, programmable point B
	TXD[1] TXD[2:1]\ TX_SH[1:0]	O5		Transmit data [2:1] This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the external PHY's TXD phase shift, please refer to Section 2.43.4.1.
A9	IO[21]	B5/8m		Digital /General Purpose I/O[23:16]
	LA[13]	I5		Local bus Address bus
	PULA	O5		Pulse A, programmable point A
	TXD[2] TXD[2:1]\ TX_SH[1:0]	O5		Transmit data [2:1] This pin is input direction during chip reset stage used to bootstrap the mode setting to decide the external PHY's TXD phase shift, please refer to Section 2.43.4.1.
B7	IO[22]	B5/8m		Digital /General Purpose I/O[23:16]
	LBHE	I5		Local bus Byte High Enable (16-bit width only)
	PWM3H	O5/T		PWM 3 High pin
	TXD[3]	O5		Transmit data [3]
A7	IO[23]	B5/8m		Digital /General Purpose I/O[23:16]
	PWM3L	O5/T		PWM 3 Low pin
	TX_EN	O5		Transmit enable
B6	IO[24]	B5/8m		Digital/General Purpose I/O[31:24]
	LDA[8]	B5		Local bus Data bus [15:8]
	PWM2H	O5/T		PWM 2 High pin
	RXD[0]	I5		Receive data
B5	IO[25]	B5/8m		Digital/General Purpose I/O[31:24]
	LDA[9]	B5		Local bus Data bus [15:8]
	PWM2L	O5/T		PWM 2 Low pin
	RXD[1]	I5		Receive data
B4	IO[26]	B5/8m		Digital/General Purpose I/O[31:24]
	LDA[10]	B5		Local bus Data bus [15:8]
	PWM1H	O5/T		PWM 1 High pin or DIR pin
	RXD[2]	I5		Receive data
H3	IO[27]	B5/8m		Digital/General Purpose I/O[31:24]
	LDA[11]	B5		Local bus Data bus [15:8]
	PWM1L	O5/T		PWM 1 Low pin or STEP pin

Pin No	Pin Name	Type	MFP	Description
	RXD[3]	I5		Receive data
J2	IO[28]	B5/8m		Digital/General Purpose I/O[31:24]
	LDA[12]	B5		Local bus Data bus [15:8]
	EMn	I5		Emergency input, active low
	RX_ER	I5		Receive error
J3	IO[29]	B5/8m		Digital/General Purpose I/O[31:24]
	LDA[13]	B5		Local bus Data bus [15:8]
	ENCA	I5		ENC input A, Sin., CW, CLK, or HALL A
	RX_DV	I5		Receive data valid
K3	IO[30]	B5/8m		Digital/General Purpose I/O[31:24]
	LDA[14]	B5		Local bus Data bus [15:8]
	ENCB	I5		ENC input B, Cos., CCW, DIR, or HALL B
	RX_CLK	I5		Receive Clock
M1	IO[31]	B5/8m		Digital/General Purpose I/O[31:24]
	LDA[15]	B5		Local bus Data bus [15:8]
	ENCZ	I5		ENC input Z, Zero point or HALL C
	MCLK	O5		MII Clock 25 MHz clock source for Ethernet PHYs
L3	P1_TXON	A		PHY 1 differential Transmitted Negative signal
L4	P1_RXIN	A		PHY 1 differential Received Negative signal
L5	P1_SD	A		PHY 1 fiber mode Signal Detect Same P0_SD description
L6	P0_TXON	A		PHY 0 differential Transmitted Negative signal
L7	P0_RXIN	A		PHY 0 differential Received Negative signal
L8	P0_SD	A		PHY 0 fiber mode Signal Detect SD < 0.2V, Copper mode- 1.0V < SD < 1.8V, Fiber mode without detected signal. Generate far-end fault SD > 2.4V, Fiber mode with detected signal
L9	XSCI	A		Crystal 25MHz Input
M9	XSCO	A		Crystal 25MHz Output
M3	P1_TXOP	A		PHY 1 differential Transmitted Positive signal Same as PHY0 TXOP/ON description
M4	P1_RXIP	A		PHY 1 differential Received Positive signal Same as PHY0 RXIP/IN description
M6	P0_TXOP	A		PHY 0 differential Transmitted Positive signal In the copper mode, the differential data is transmitted to the media on the TXOP/TXON signal pair in the MDI mode. In the fiber mode, the signal pair should be connected to the TX+/TX- pin of the fiber transceiver.
M7	P0_RXIP	A		PHY 0 differential Received Positive signal In the copper mode, the differential data from the media is received on the RXIP/RXIN signal pair in the MDI mode. In the fiber mode, the signal pair should be connected to the RX+/RX- pin of the fiber transceiver.
H5	RSET_BG	A		PHY off-chip Bias Resistor Connects an external resistor of 12 KΩ ± 1% to the PCB analog ground.

1.4.3 Power/Ground Pin Description

Pin No	Pin Name	Type	MFP	Description
A3	AV_{SS}	P	MFP0	Ground pin for ADC analog circuit.
A4	V_{REF}	A	MFP0	ADC reference voltage input. Note: This pin needs to be connected with a 1uF capacitor.
A5	AV_{DD}	P	MFP0	Power supply for internal ADC analog circuit.
C6, D6, E6	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
A8	LDO_CAP	A	MFP0	LDO output pin.
H12	V_{DDIO}	P	MFP0	Power supply for PA.0~PA.5.
F5, F6, F7, F8, G5,G6, G7, G8	GND (V_{SS})	P		Ground for all Analog and Digital Power.
C7, D7, E7	VCCK	P		Digital Power for core, 1.2V Please add a 0.1uF bypass capacitor between each VCCK and GND.
E8	VCC12A_PLL	P		Analog Power for PLL, 1.2V. Please add a 0.1uF bypass capacitor between VCC12A_PLL and GND.
H6, H7, H8	VCC3IO	P		Digital Power for I/O pins, 3.3V Please add a 0.1uF bypass capacitor between each VCC3IO and GND.
M2, M5, M8	VCC33A	P		Analog Power for Ethernet PHY, 3.3V Please add a 0.1uF bypass capacitor between VCC33A and GND.

2 Function Description

2.1 ARM® Cortex® -M4 Core

The Cortex®-M4 processor, a configurable, multistage, 32-bit RISC processor, has three AMBA AHB- Lite interfaces for best parallel performance and includes an NVIC component. The processor with optional hardware debug functionality can execute Thumb code and is compatible with other Cortex-M profile processors. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. The Cortex®-M4F is a processor with the same capability as the Cortex®-M4 processor and includes floating point arithmetic functionality. The AX58200 is embedded with Cortex®-M4F processor. Throughout this document, the name Cortex®-M4 refers to both Cortex®-M4 and Cortex®-M4F processors. Figure 2.1-1 shows the functional controller of the processor.

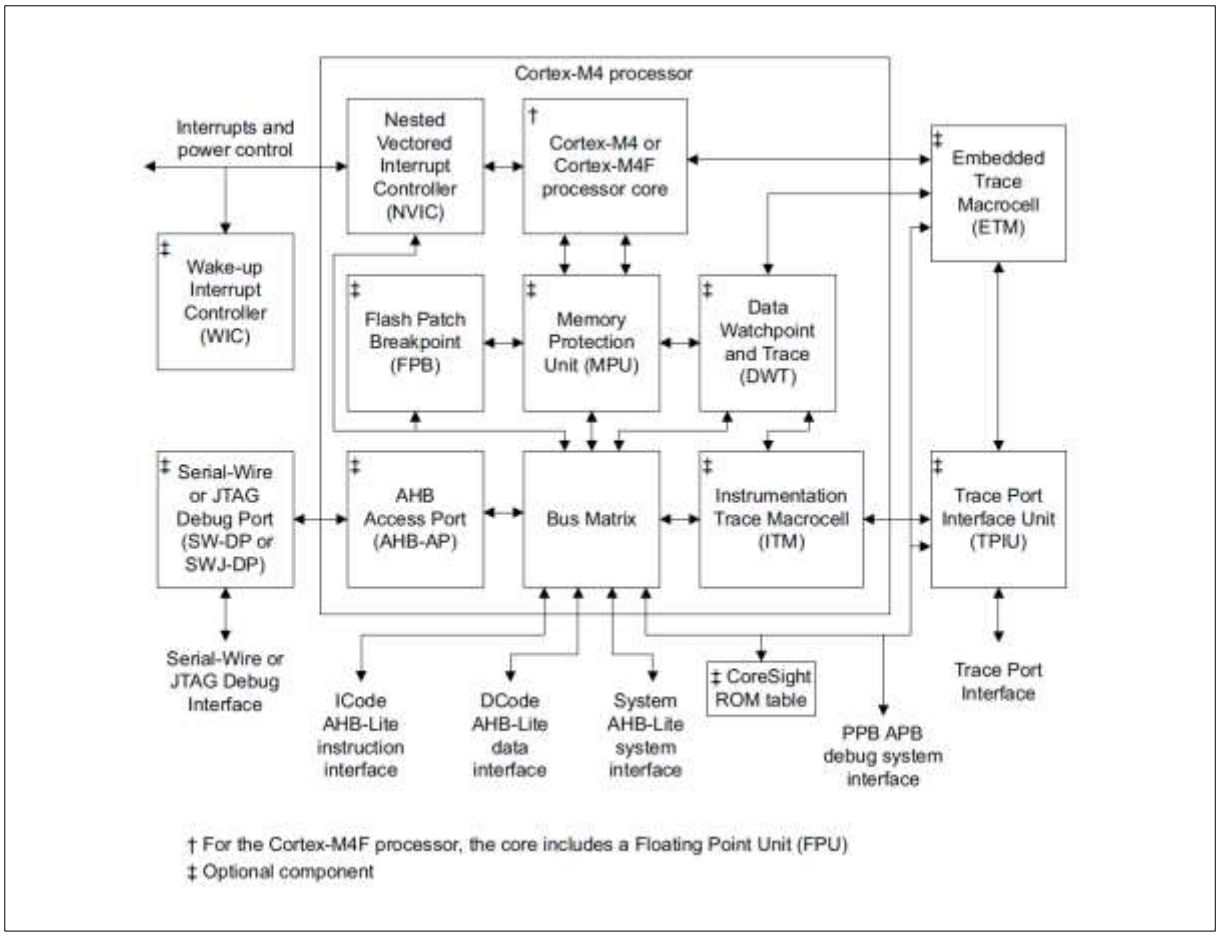


Figure 2.1-1:Cortex®-M4 Block Diagram

Cortex®-M4 processor features:

- A low gate count processor core, with low latency interrupt processing that has:
  - A subset of the Thumb instruction set, defined in the *ARMv7-M Architecture Reference Manual*
  - Banked Stack Pointer (SP)
  - Hardware integer divide instructions, SDIV and UDIV
  - Handler and Thread modes
  - Thumb and Debug states
  - Support for interruptible-continued instructions LDM, STM, PUSH, and POP for low interrupt latency
  - Automatic processor state saving and restoration for low latency *Interrupt Service Routine (ISR)* entry and exit
  - Support for ARMv6 big-endian byte-invariant or little-endian accesses
  - Support for ARMv6 unaligned accesses
- Floating Point Unit (FPU) in the Cortex®-M4F processor providing:
  - 32-bit instructions for single-precision (C float) data-processing operations
  - Combined Multiply and Accumulate instructions for increased precision (Fused MAC)
  - Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root
  - Hardware support for denormals and all IEEE rounding modes
  - 32 dedicated 32-bit single precision registers, also addressable as 16 double-word registers
  - Decoupled three stage pipeline
- Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing. Features include:
  - External interrupts. Configurable from 1 to 240 (the AX58200 configured with 64 interrupts)
  - Bits of priority, configurable from 3 to 8
  - Dynamic reprioritization of interrupts
  - Priority grouping which enables selection of preempting interrupt levels and nonpreempting interrupt levels
  - Support for tail-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
  - Processor state automatically saved on interrupt entry, and restored on interrupt exit with on instruction overhead
  - Support for Wake-up Interrupt Controller (WIC) with Ultra-low Power Sleep mode
- Memory Protection Unit (MPU). An optional MPU for memory protection, including:
  - Eight memory regions
  - Sub Region Disable (SRD), enabling efficient use of memory regions
  - The ability to enable a background region that implements the default memory map attributes
- Low-cost debug solution that features:
  - Debug access to all memory and registers in the system, including access to memory mapped devices, access to internal core registers when the core is halted, and access to

debug control registers even while SYSRESETn is asserted.

- Serial Wire Debug Port (SW-DP) or Serial Wire JTAG Debug Port (SWJ-DP) debug access
- Optional Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches
- Optional Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
- Optional Instrumentation Trace Macrocell (ITM) for support of printf() style debugging
- Optional Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer (TPA), including Single Wire Output (SWO) mode
- Optional Embedded Trace Macrocell (ETM) for instruction trace.

- Bus interfaces:
  - Three Advanced High-performance Bus-Lite (AHB-Lite) interfaces: ICode, Dcode, and System bus interfaces
  - Private Peripheral Bus (PPB) based on Advanced Peripheral Bus (APB) interface
  - Bit-band support that includes atomic bit-band write and read operations.
  - Memory access alignment
  - Write buffer for buffering of write data
  - Exclusive access transfers for multiprocessor systems

2.2 System Manager

2.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Organization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

2.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sources are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M4 core only by writing 1 to CPURST (SYS_IPRST0[1])

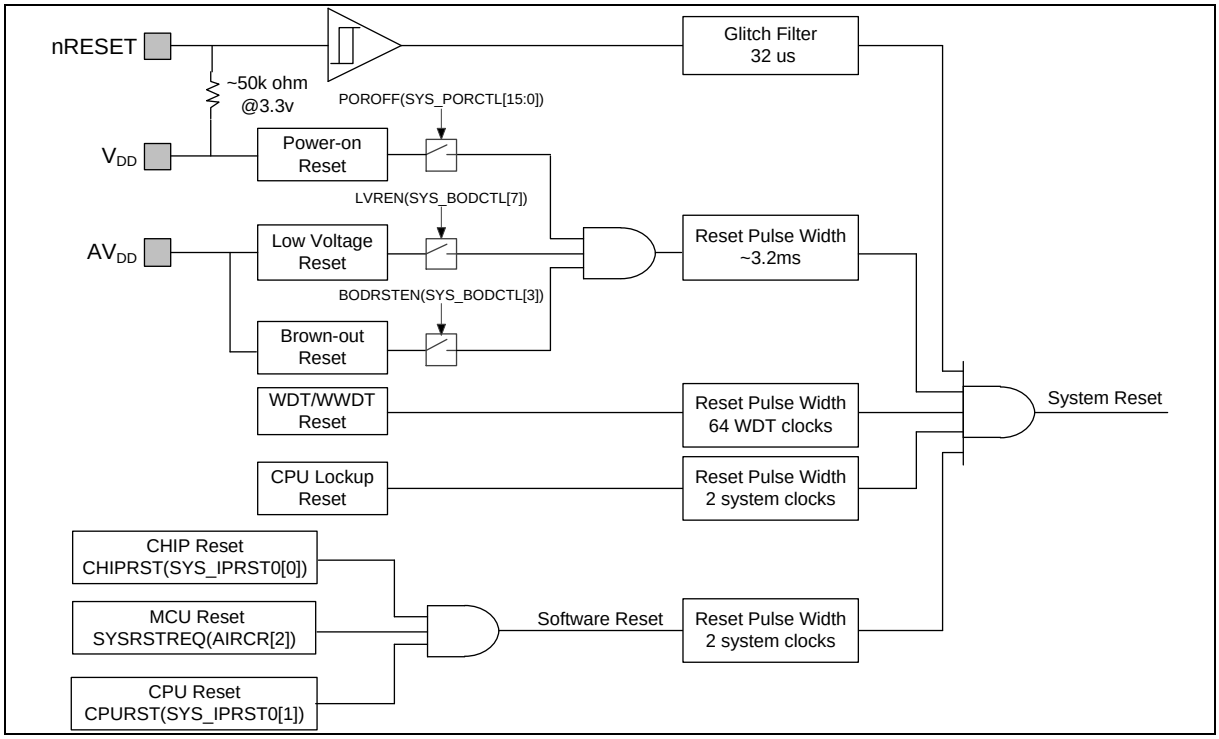


Figure 2.2-1: System Reset Sources

There are a total of 9 reset sources in the family. In general, CPU reset is used to reset Cortex®-M4 only; the other reset sources will reset Cortex®-M4 and all peripherals. However, there are small differences between each reset source and they are listed in Table 2.2-1.

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	MCU	CPU
SYS_RSTSTS	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[2:1])									
BODRSTEN (SYS_BODCTL[3])									
HXTEN (CLK_PWRCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	
LXTEN (CLK_PWRCTL[1])	0x0	-	-	-	-	-	-	-	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
HCLKSEL (CLK_CLKSEL0[2:0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
WDTSEL	0x3	0x3	-	-	-	-	-	-	-

(CLK_CLKSEL1[1:0])									
HXTSTB (CLK_STATUS[0])	0x0	-	-	-	-	-	-	-	-
LXTSTB (CLK_STATUS[1])	0x0	-	-	-	-	-	-	-	-
PLLSTB (CLK_STATUS[2])	0x0	-	-	-	-	-	-	-	-
HIRCSTB (CLK_STATUS[4])	0x0	-	-	-	-	-	-	-	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	-	-	-	-	-	-	-
RSTEN (WDT_CTL[1]) **WDTEN (WDT_CTL[7])**	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
WDT_CTL except bit 1 and bit 7.	0x0700	0x0700	0x0700	0x0700	0x0700	-	0x0700	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	-	0x3F	-	-
BS (FMC_ISPCTL[1]) **BL (FMC_ISPCTL[16])**	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
FMC_DFBA	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	-	Reload from CONFIG1	-	-
CBS (FMC_ISPSTS[2:1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
VECMAP (FMC_ISPSTS[23:9])	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	Reload base on CONFIG0	-	-
Other Peripheral Registers	Reset Value								-
FMC Registers	Reset Value								
Note: '-' means that the value of register keeps original setting.									

Table 2.2-1: Reset Value of Registers

2.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 32 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 32 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 2.2-2 shows the nRESET reset waveform.

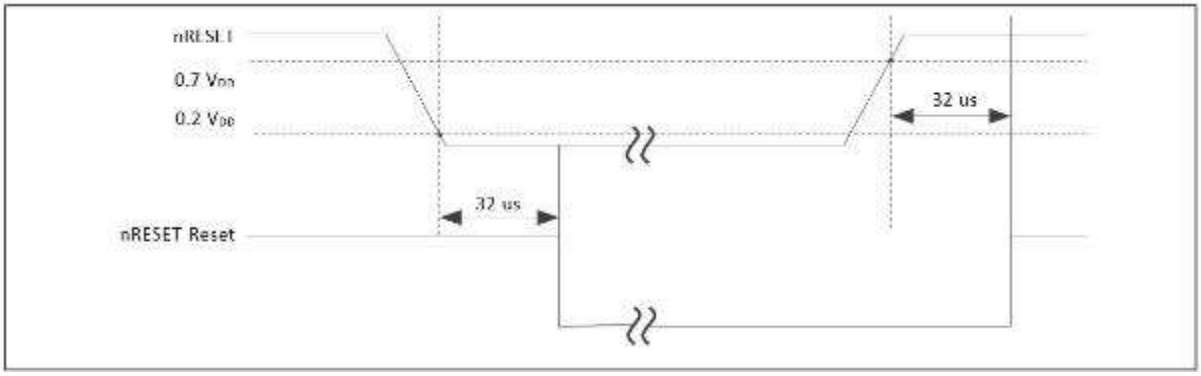


Figure 2.2-2: nRESET Reset Waveform

2.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and force the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 2.2-3 shows the power-on reset waveform.

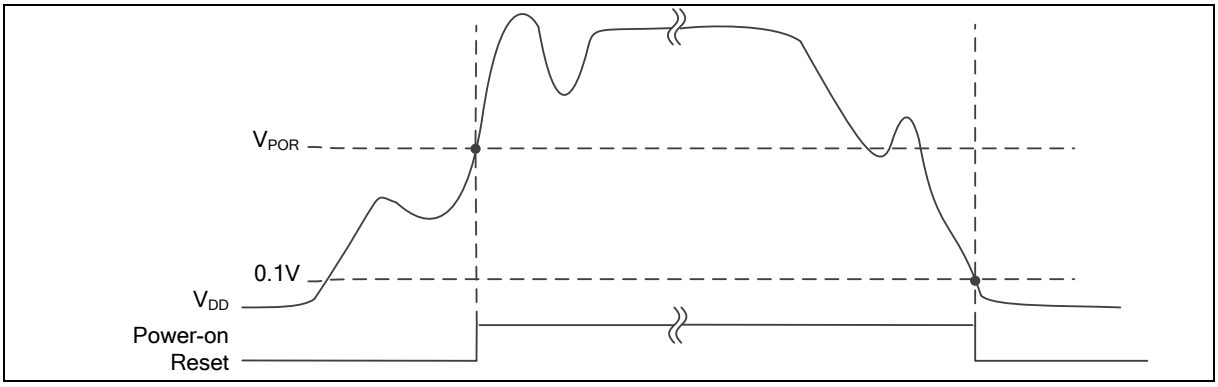


Figure 2.2-3: Power-on Reset (POR) Waveform

2.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 2.2-4 shows the Low Voltage Reset waveform.

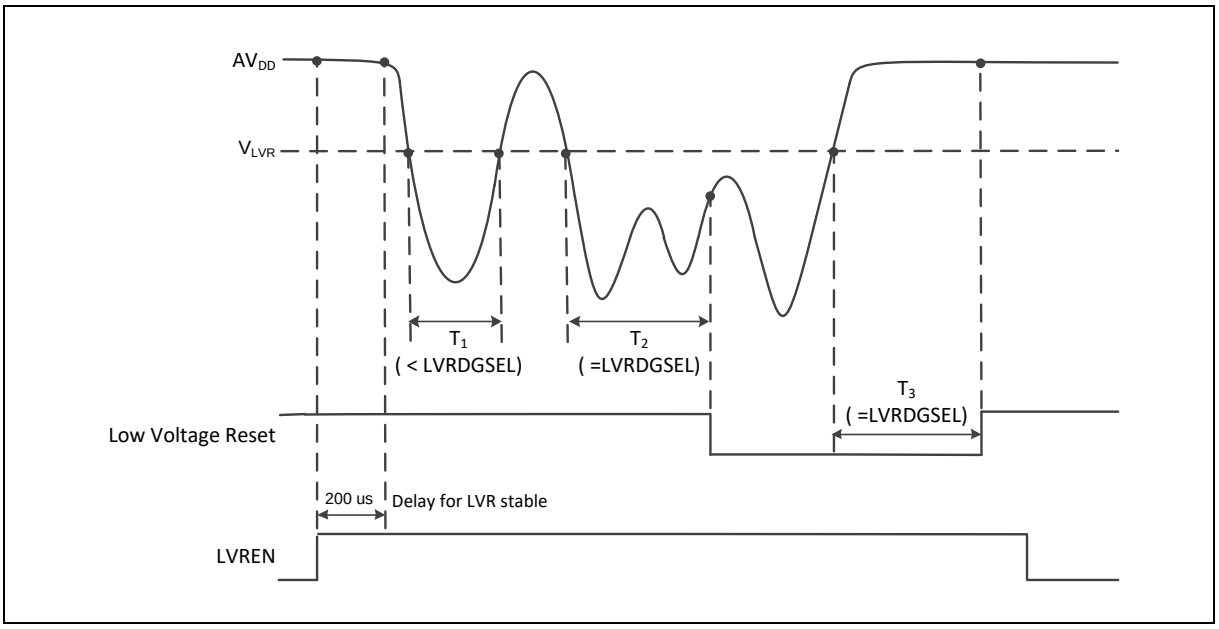


Figure 2.2-4: Low Voltage Reset (LVR) Waveform

2.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN and BODVL (SYS_BODCTL[18:16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by Flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 2.2-5 shows the Brown-out Detector waveform.

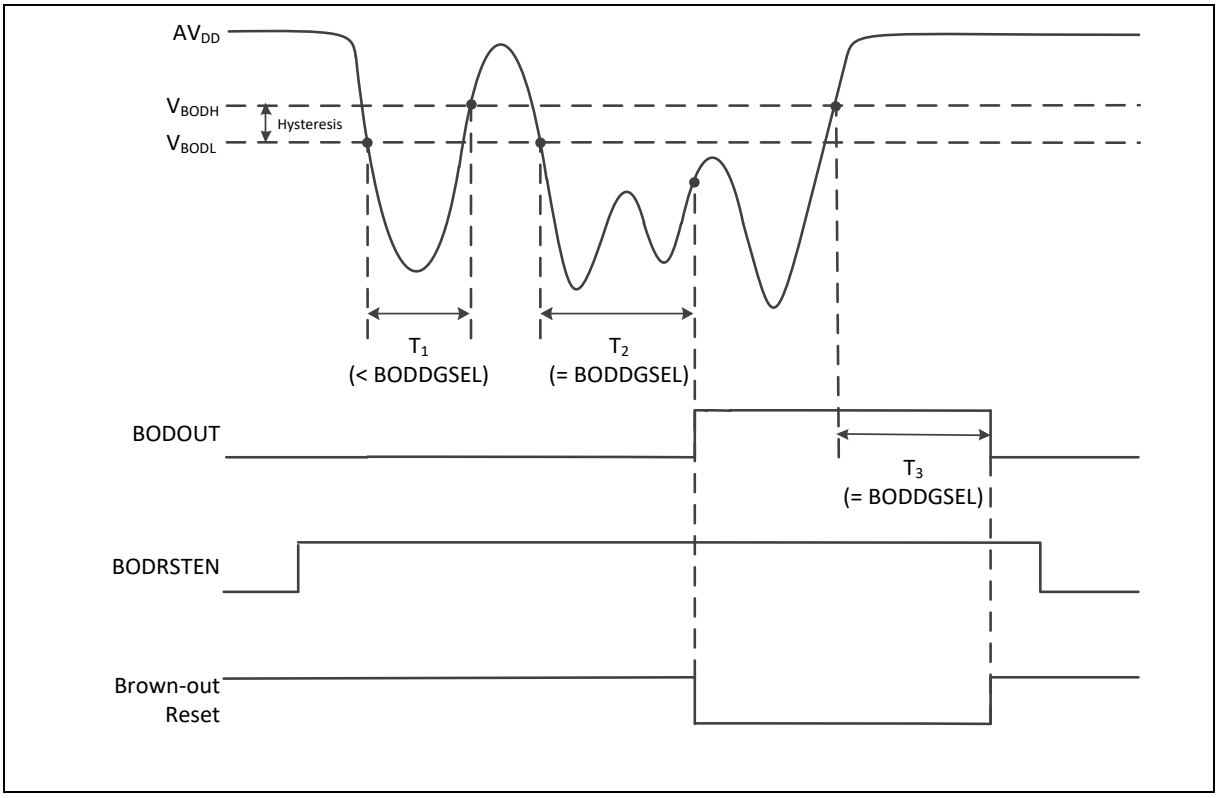


Figure 2.2-5: Brown-out Detector (BOD) Waveform

2.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer (WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

2.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built-in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

2.2.2.7 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex®-M4 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is the same with Power-on Reset. The CPU and all peripherals are reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[1]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

2.2.3 System Power Distribution

In this chip, power distribution is divided into four segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from VDD and VSS supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- USB transceiver power from VBUS offers the power for operating the USB transceiver.
- RTC power from VDD provides the power for RTC and 80 bytes backup registers.

The outputs of internal voltage regulators, LDO and VDD33, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 2.2-6 shows the AX58200 power distribution.

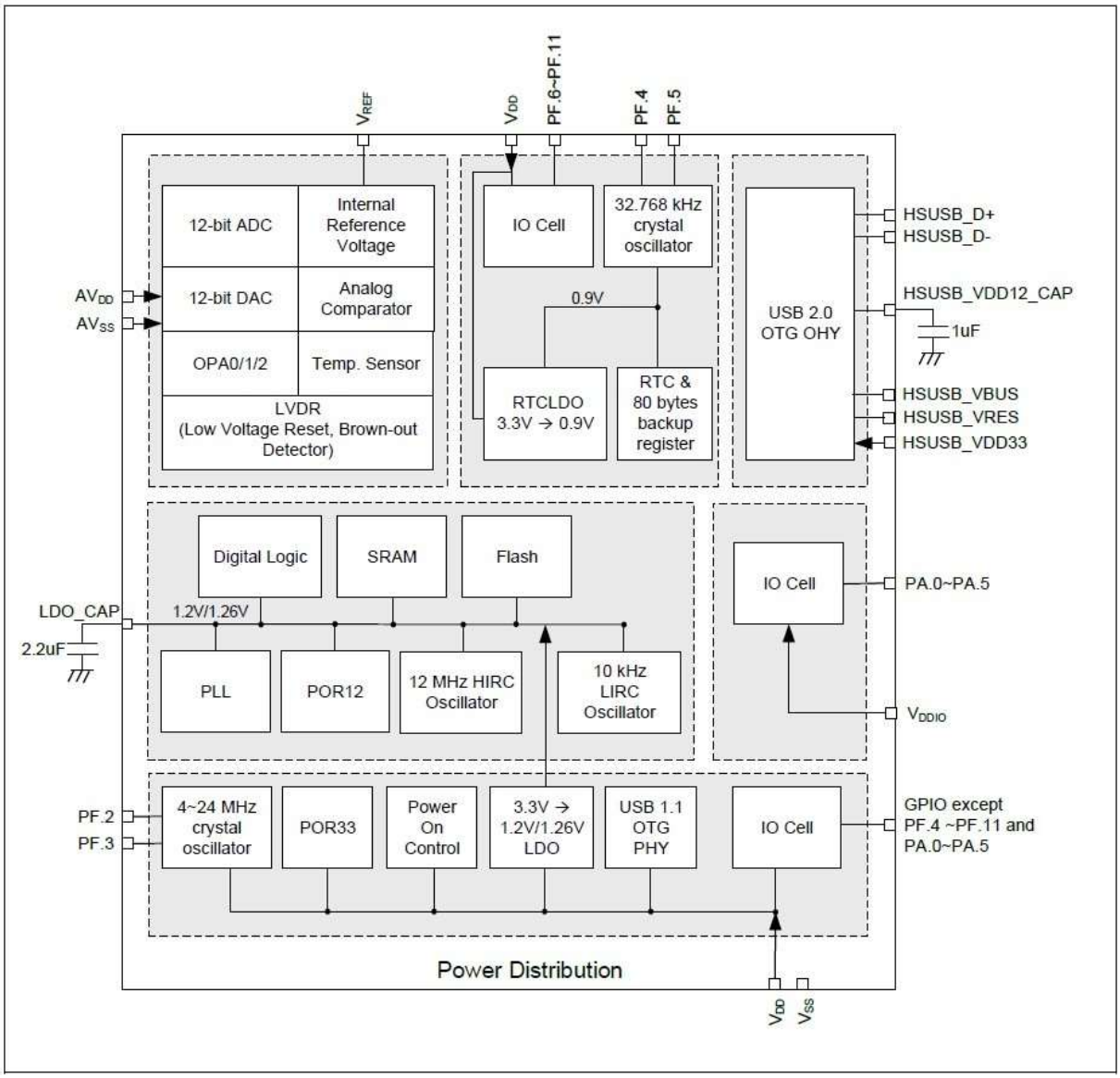


Figure 2.2-6: Power Distribution Diagram

2.2.4 Power Modes and Wake-up Sources

The AX58200 has power manager unit to support several operating modes for saving power. Table 2.2-2 lists all power modes in the AX58200.

Mode	CPU Operating Maximum Speed (MHz)	LDO_CAP (V)	Clock Disable
Normal mode	160	1.20	All clocks are disabled by control register.
Turbo mode	192	1.26	All clocks are disabled by control register.
Idle mode	CPU enter Sleep mode	1.20/1.26	Only CPU clock is disabled.
Fast Wakeup Power-down mode (FWPD)	CPU enters Deep Sleep mode	1.20/1.26	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Normal Power-down mode (NPD)	CPU enters Deep Sleep mode	1.20/1.26	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Low leakage Power-down mode (LLPD)	CPU enters Deep Sleep mode	0.9	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Standby Power-down mode 0 (SPD0) [1]	Power off	Floating	Only LIRC/LXT still enable for RTC function and wake-up timer usage
Standby Power-down mode 1 (SPD1) [1]	Power off	Floating	Only LIRC/LXT still enable for RTC function and wake-up timer usage
Deep Power-down mode (DPD)	Power off	Floating	Only LIRC/LXT still enable for RTC function and wake-up timer usage

Table 2.2-2: Power Mode Table

Note: [1]

User must turn on LIRC before entering SPD0/1 mode.

There are different power mode entry settings. Each power mode has different entry setting and leaving condition. Table 2.2-3 shows the entry setting for each power mode. When chip power-on, chip is running as normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCT:[7]) and PDMSEL (CLK_PMUCTL[2:0]) and execute WFI instruction.

Register/Instruction Mode	SLEEPDEEP (SCR[2])	PDEN (CLK_PWRCTL[7])	PDMSEL (CLK_PMUCTL [2:0])	CPU Run WFI Instruction
Normal mode	0	0	0	NO
Idle mode	0	0	0	YES
Fast Wakeup Power-down mode	1	1	2	YES
Normal Power-down mode	1	1	0	YES
Low leakage Power-down mode	1	1	1	YES
Standby Power-down mode 0	1	1	4	YES
Standby Power-down mode 1	1	1	5	YES
Deep Power-down mode	1	1	6	YES

Table 2.2-3: Power Mode Difference Table

There are several wake-up sources in Idle mode and Power-down mode. Table 2.2-4 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	RTC, WDT, I²C, Timer, UART, BOD, GPIO, EINT, USCI, USBD, ACMP and BOD.
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 2.2-4: Power Mode Definition Table

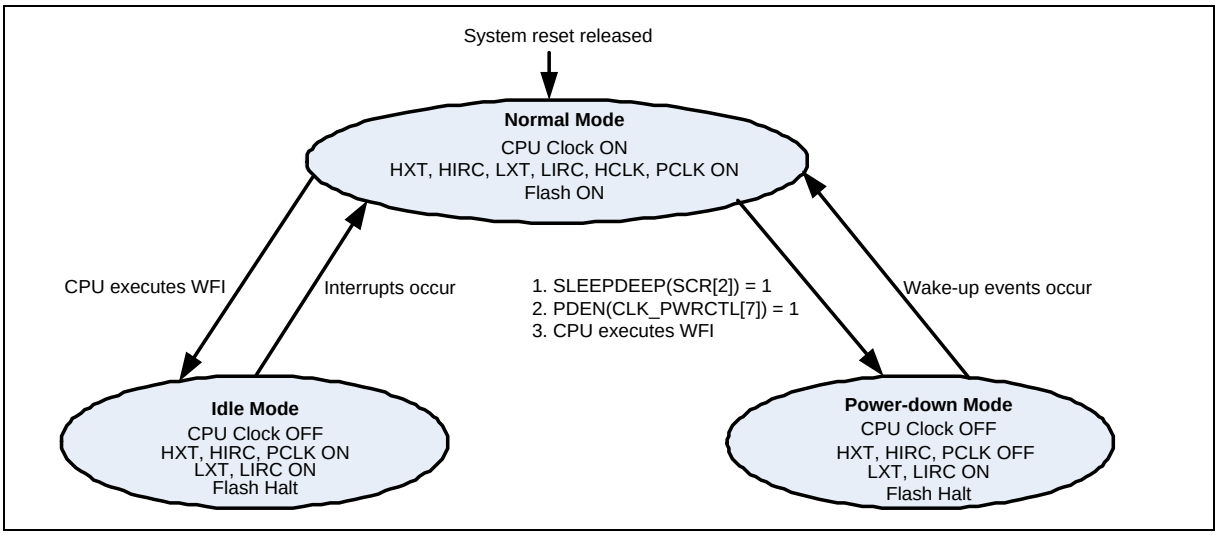


Figure 2.2-7: Power Mode State Machine

	Idle Mode	NPD, LLPD, FWPD	SPD0, SPD1,	DPD
HXT	ON	Halt	Halt	Halt
HIRC	ON	Halt	Halt	Halt
LXT	ON	ON/OFF[1]	ON/OFF[1]	ON/OFF[1]
LIRC	ON	ON/OFF[2]	ON/OFF[2]	ON/OFF[2]
PLL	ON	Halt	Halt	Halt
HCLK/PCLK	ON	Halt	Halt	Halt
CPU	Halt	Halt	Halt	Halt
SRAM Retention	ON	ON	Halt	Halt
FLASH	ON	Halt	Halt	Halt
TIMER	ON	ON/OFF[3]	ON/OFF[3]	Halt
WDT	ON	ON/OFF[4]	ON/OFF[4]	Halt
RTC	ON	ON/OFF[5]	ON/OFF[5]	ON/OFF[5]
UART	ON	ON/OFF[6]	ON/OFF[6]	Halt
Others	ON	Halt	Halt	Halt

Table 2.2-5: Clocks in Power Modes

Note:

1. LXT ON or OFF depends on SW setting in normal mode.
2. LIRC ON or OFF depends on S/W setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC and LIRC is on.
5. If RTC clock source is selected as LXT and LXT is on.
6. If UART clock source is selected as LXT and LXT is on.

Wake-up sources in Normal Power-down mode (NPD):

RTC, WDT, I²C, Timer, UART, USCI, BOD, EBOD, GPIO, USBD, and ACMP.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 2.2-6 lists the condition about how to enter Power-down mode again for each peripheral.

User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and executing WFI to enter Power-down mode.

Wake-Up Source	Wake-Up Condition	Power-Down Mode			Re-Entering Power-Down Mode Condition
		NPD/ FWPD/ LLPD	SPD0/1	DPD	
BOD	Brown-Out Detector Reset / Interrupt	V	-	-	After software writes 1 to clear BODIF (SYS_BODCTL[4]).
	Brown-Out Detector Reset	-	V	-	After software writes 1 to clear BODWK (CLK_PMUSTS[13]) when SPD mode is entered.
LVR	LVR Reset	V	-	-	After software writes 1 to clear LVRF (SYS_RSTSTS[3])
		-	V	-	After software writes 1 to clear LVRWK (CLK_PMUSTS[12]) when SPD mode is entered.

POR	POR Reset	V	V	-	After software writes 1 to clear PORF (SYS_RSTSTS[0])
INT	External Interrupt	V	-	-	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO	GPIO Interrupt	V	-	-	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO(PA~PD) Wake-up pin	rising or falling edge event, 64-pin	-	V	-	After software writes 1 to clear GPxWK (CLK_PMUSTS[11:8]) when SPD mode is entered.
GPIO(PC.0) Wake-up pin	rising or falling edge event, 1-pin	-	-	V	After software writes 1 to clear PINWK (CLK_PMUSTS[1]) when DPD mode is entered.
TIMER	Timer Interrupt	V	-	-	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
Wakeup timer	Wakeup by wake-up timer time-out	-	V	V	After software writes 1 to clear TMRWK (CLK_PMUSTS[1]) when SPD or DPD mode is entered.
WDT	WDT Interrupt	V	-	-	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
RTC	Alarm Interrupt	V	-	-	After software writes 1 to clear ALMIF (RTC_INTSTS[0]).
	Time Tick Interrupt	V	-	-	After software writes 1 to clear TICKIF (RTC_INTSTS[1]).
	Wakeup by RTC alarm	-	V	-	After software writes 1 to clear RTCWK (CLK_PMUSTS[2]) when SPD mode is entered.
	Wakeup by RTC tick time	-	V	-	After software writes 1 to clear RTCWK (CLK_PMUSTS[2]) when SPD mode is entered.
	Wakeup by tamper event	-	V	-	After software writes 1 to clear RTCWK (CLK_PMUSTS[2]) when SPD mode is entered.
UART	nCTS wake-up	V	-	-	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data wake-up	V	-	-	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	V	-	-	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-up	V	-	-	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	V	-	-	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
USCI UART	CTS Toggle	V	-	-	After software writes 1 to clear WKF (UUART_WKSTS[0]).
	Data Toggle	V	-	-	After software writes 1 to clear WKF (UUART_WKSTS[0]).
USCI I2C	Data toggle	V	-	-	After software writes 1 to clear WKF (UI2C_WKSTS[0]).
	Address match	V	-	-	After software writes 1 to clear WKAKDONE (UI2C_PROTSTS[16], then writes 1 to clear WKF (UI2C_WKSTS[0]).
USCI SPI	SS Toggle	V	-	-	After software writes 1 to clear WKF (USPI_WKSTS[0]).
I^2C	Address match wake-up	V	-	-	After software writes 1 to clear WKAKDONE (I2C_WKSTS[1]). Then software writes 1 to clear WKIF(I2C_WKSTS[0]).
USBD	Remote Wake-up	V	-	-	After software writes 1 to clear BUSIF (USBD_INTSTS[0]).
ACMP	Comparator Power-Down Wake-Up Interrupt	V	-	-	After software writes 1 to clear WKIF0 (ACMP_STATUS[8]) and WKIF1 (ACMP_STATUS[9]).
ACMP	ACMPO status change	-	V	-	After software writes 1 to clear ACMPWK (CLK_PMUSTS[14]) when SPD mode is entered.

Table 2.2-6: Re-Entering Power-down Mode Condition

2.2.5 Power Modes Transition

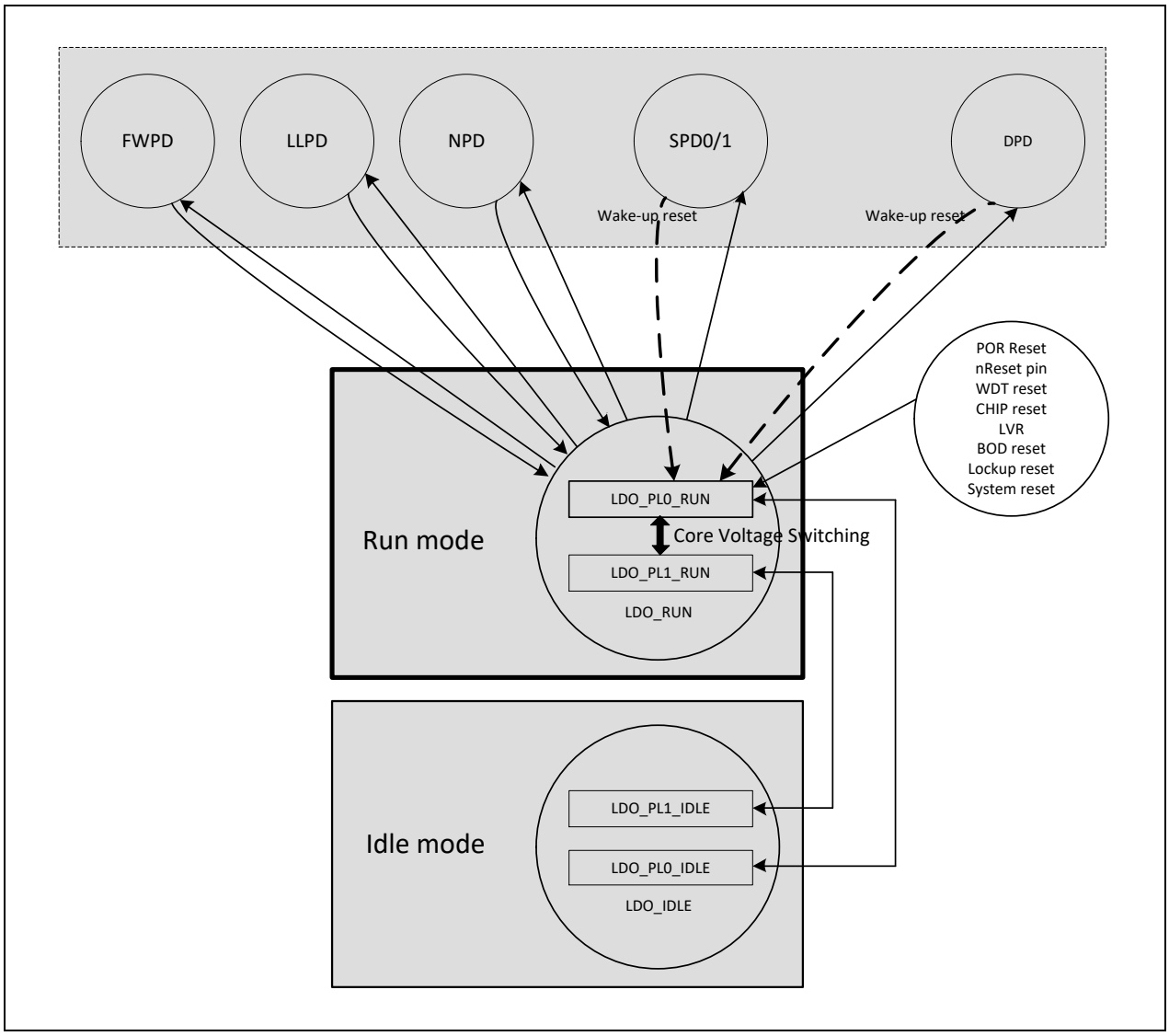


Figure 2.2-8: Power Distribution Diagram

2.2.6 System Memory Map

The AX58200 provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 2.2-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The AX58200 only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0003_FFFF	FLASH_BA	FLASH Memory Space (256KB)
0x0000_0000 – 0x0007_FFFF	FLASH_BA	FLASH Memory Space (512KB)
0x0800_0000 – 0x09FF_FFFF	SPIM_BA	SPIM Memory Space (32MB)
0x2000_0000 – 0x2000_7FFF	SRAM0_BA	SRAM Memory Space (32KB)
0x2000_8000 – 0x2001_FFFF	SRAM1_BA	SRAM Memory Space (96KB)
0x2002_0000 – 0x2002_7FFF	SRAM2_BA	SRAM Memory Space (32KB) for CPU only and share with SPIM cache
0x6000_0000 – 0x6FFF_FFFF	EXTMEM_BA	External Memory Space (256MB)
Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)		
0x4000_0000 – 0x4000_01FF	SYS_BA	System Control Registers
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers
0x4000_0300 – 0x4000_03FF	NMI_BA	NMI Control Registers
0x4000_4000 – 0x4000_4FFF	GPIO_BA	GPIO Control Registers
0x4000_7000 – 0x4000_7FFF	SPIM_BA	SPIM Control Registers
0x4000_8000 – 0x4000_8FFF	PDMA_BA	Peripheral DMA Control Registers
0x4000_9000 – 0x4000_9FFF	USBH_BA	USB Host Control Registers
0x4000_B000 – 0x4000_BFFF	EMAC_BA	Ethernet MAC Control Registers
0x4000_C000 – 0x4000_CFFF	FMC_BA	Flash Memory Control Registers
0x4000_D000 – 0x4000_DFFF	SDH0_BA	SDHOST0 Control Registers
0x4000_E000 – 0x4000_EFFF	SDH1_BA	SDHOST1 Control Registers
0x4001_0000 – 0x4001_0FFF	EBI_BA	External Bus Interface Control Registers
0x4001_9000 – 0x4001_9FFF	HSUSBD_BA	HSUSBD Control Registers
0x4001_A000 – 0x4001_AFFF	HSUSBH _BA	HSUSBH Host Control Registers
0x4003_1000 – 0x4003_1FFF	CRC_BA	CRC Generator Registers
0x4003_E000 – 0x4003_EFFF	SWDC_BA	SWD Control Registers
0x4003_F000 – 0x4003_FFFF	ETMC_BA	ETM Control Registers
0x5008_0000 – 0x5008_0FFF	CRYP_BA	Cryptographic Accelerator Registers
APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4004_0000 – 0x4004_0FFF	WDT_BA	Watchdog Timer Control Registers
0x4004_1000 – 0x4004_1FFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4004_3000 – 0x4004_3FFF	EADC_BA	Enhanced Analog-Digital-Converter (EADC) Control Registers
0x4004_5000 – 0x4004_5FFF	ACMP01_BA	Analog Comparator 0/ 1 Control Registers

0x4004_6000 – 0x4004_6FFF	OPA_BA	OP Amplifier Control Registers
0x4004_7000 – 0x4004_7FFF	DAC_BA	DAC Control Registers
0x4004_8000 – 0x4004_8FFF	I2S0_BA	I^2S0 Interface Control Registers
0x4004_D000 – 0x4004_DFFF	OTG_BA	OTG Control Registers
0x4004_F000 – 0x4004_FFFF	HSOTG_BA	HSOTG Control Registers
0x4005_0000 – 0x4005_0FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4005_1000 – 0x4005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4005_8000 – 0x4005_8FFF	EPWM0_BA	PWM0 Control Registers
0x4005_9000 – 0x4005_9FFF	EPWM1_BA	PWM1 Control Registers
0x4005_A000 – 0x4005_AFFF	BPWM0_BA	BPWM0 Control Registers
0x4005_B000 – 0x4005_BFFF	BPWM1_BA	BPWM1 Control Registers
0x4006_0000 – 0x4006_0FFF	QSPI0_BA	Quad SPI0 Control Registers
0x4006_1000 – 0x4006_1FFF	SPI0_BA	SPI0 Control Registers
0x4006_2000 – 0x4006_2FFF	SPI1_BA	SPI1 Control Registers
0x4006_3000 – 0x4006_3FFF	SPI2_BA	SPI2 Control Registers
0x4006_4000 – 0x4006_4FFF	SPI3_BA	SPI3 Control Registers
0x4007_0000 – 0x4007_0FFF	UART0_BA	UART0 Control Registers
0x4007_1000 – 0x4007_1FFF	UART1_BA	UART1 Control Registers
0x4007_2000 – 0x4007_2FFF	UART2_BA	UART2 Control Registers
0x4007_3000 – 0x4007_3FFF	UART3_BA	UART3 Control Registers
0x4007_4000 – 0x4007_4FFF	UART4_BA	UART4 Control Registers
0x4007_5000 – 0x4007_5FFF	UART5_BA	UART5 Control Registers
0x4008_0000 – 0x4008_0FFF	I2C0_BA	I^2C0 Control Registers
0x4008_1000 – 0x4008_1FFF	I2C1_BA	I^2C1 Control Registers
0x4008_2000 – 0x4008_2FFF	I2C2_BA	I^2C2 Control Registers
0x4009_0000 – 0x4009_0FFF	SC0_BA	Smartcard Host 0 Control Registers
0x4009_1000 – 0x4009_1FFF	SC1_BA	Smartcard Host 1 Control Registers
0x4009_2000 – 0x4009_2FFF	SC2_BA	Smartcard Host 2 Control Registers
0x4009_3000 – 0x4009_3FFF	SC3_BA	Smartcard Host 3 Control Registers
0x400A_0000 – 0x400A_0FFF	CAN0_BA	CAN0 Bus Control Registers
0x400A_1000 – 0x400A_1FFF	CAN1_BA	CAN1 Bus Control Registers
0x400B_0000 – 0x400B_0FFF	QEI0_BA	QEI0 Control Registers
0x400B_1000 – 0x400B_1FFF	QEI1_BA	QEI1 Control Registers
0x400B_4000 – 0x400B_4FFF	ECAP0_BA	ECAP0 Control Registers
0x400B_5000 – 0x400B_5FFF	ECAP1_BA	ECAP1 Control Registers
0x400C_0000 – 0x400C_0FFF	USBD_BA	USB Device Control Register
0x400D_0000 – 0x400D_0FFF	USCI0_BA	USCI0 Control Registers

0x400D_1000 – 0x400D_1FFF	USCI1_BA	USCI1 Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 2.2-7: Address Space Assignments for On-Chip Controllers

2.2.7 SRAM Memory Organization

The AX58200 supports embedded SRAM with total 160 Kbytes size and the SRAM organization is separated to three banks: SRAM bank0 and SRAM bank1 and SRAM bank2. The first bank has 32 Kbytes address space, the second bank has 96 Kbyte address space and the third bank has 32Kbyte. These three banks address space can be accessed simultaneously. The SRAM bank0 supports parity error check to make sure chip operating more stable. The SRAM bank2 is shared with SPIM cache, it can switch to external SPI Flash cache memory. Note that SRAM bank2 has additional two wait cycles when reading data.

- Supports total 160 Kbytes SRAM
- Supports byte / half word / word write
- Supports fixed 32 Kbytes SRAM bank0 for independent access
- Supports parity error check function for SRAM bank0
- Supports oversize response error
- Supports remap address to 0x1000_0000

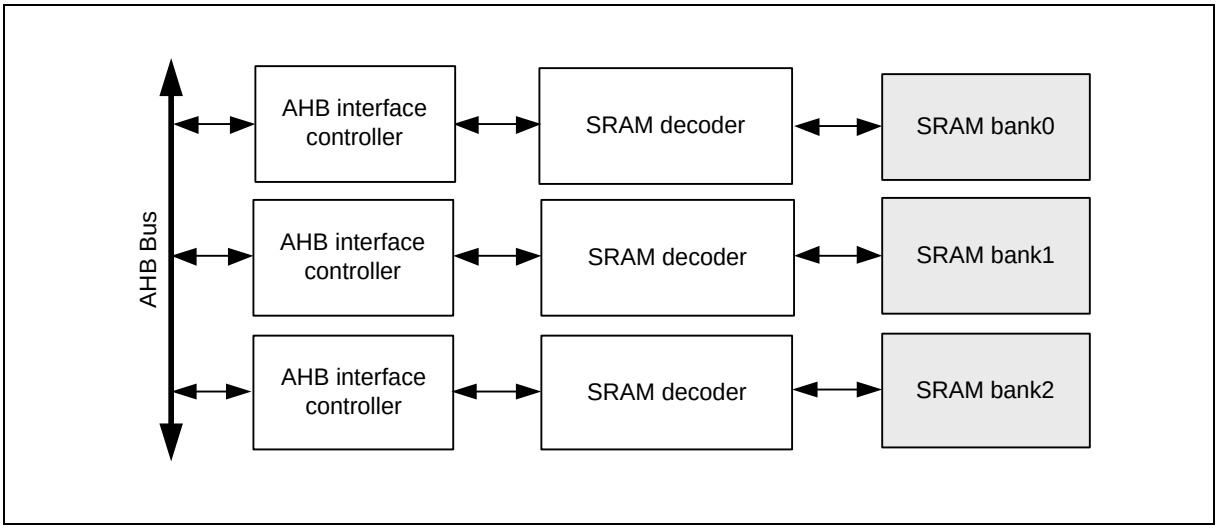


Figure 2.2-9: SRAM Block Diagram

Figure 2.2-9 shows the SRAM organization of AX58200. There are three SRAM banks in AX58200. The bank0 is addressed to 32 Kbytes, the bank1 is addressed to 96 Kbytes and the bank2 is addressed to 32 Kbyte. The bank0 address space is from 0x2000_0000 to 0x2000_7FFF. The bank1 address space is from 0x2000_8000 to 0x2001_FFFF. The bank2 address space is from 0x2002_0000 to 0x2002_7FFF. The address between 0x2002_8000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

The address of each bank is remapping from 0x2000_0000 to 0x1000_0000. CPU can access SRAM bank0 through 0x2000_0000 to 0x2000_7FFF or 0x1000_0000 to 0x1000_7FFF, and access SRAM bank1 through 0x2000_8000 to 0x2001_FFFF or 0x1000_8000 to 0x1001_FFFF, and access SRAM bank2 through 0x2002_0000 to 0x2002_7FFF or 0x1002_0000 to 0x1002_7FFF.

When setting the control register CCMEN(SPIM_CTL1[2]) to 0, SRAM bank2 is switched to external SPI Flash cache memory. In this case, the SRAM bank2 can't be accessed as general SRAM. If user access SRAM bank2 by AHB bus master, the SPI Flash controller will send error response via HRESP AHB bus signal to bus master.

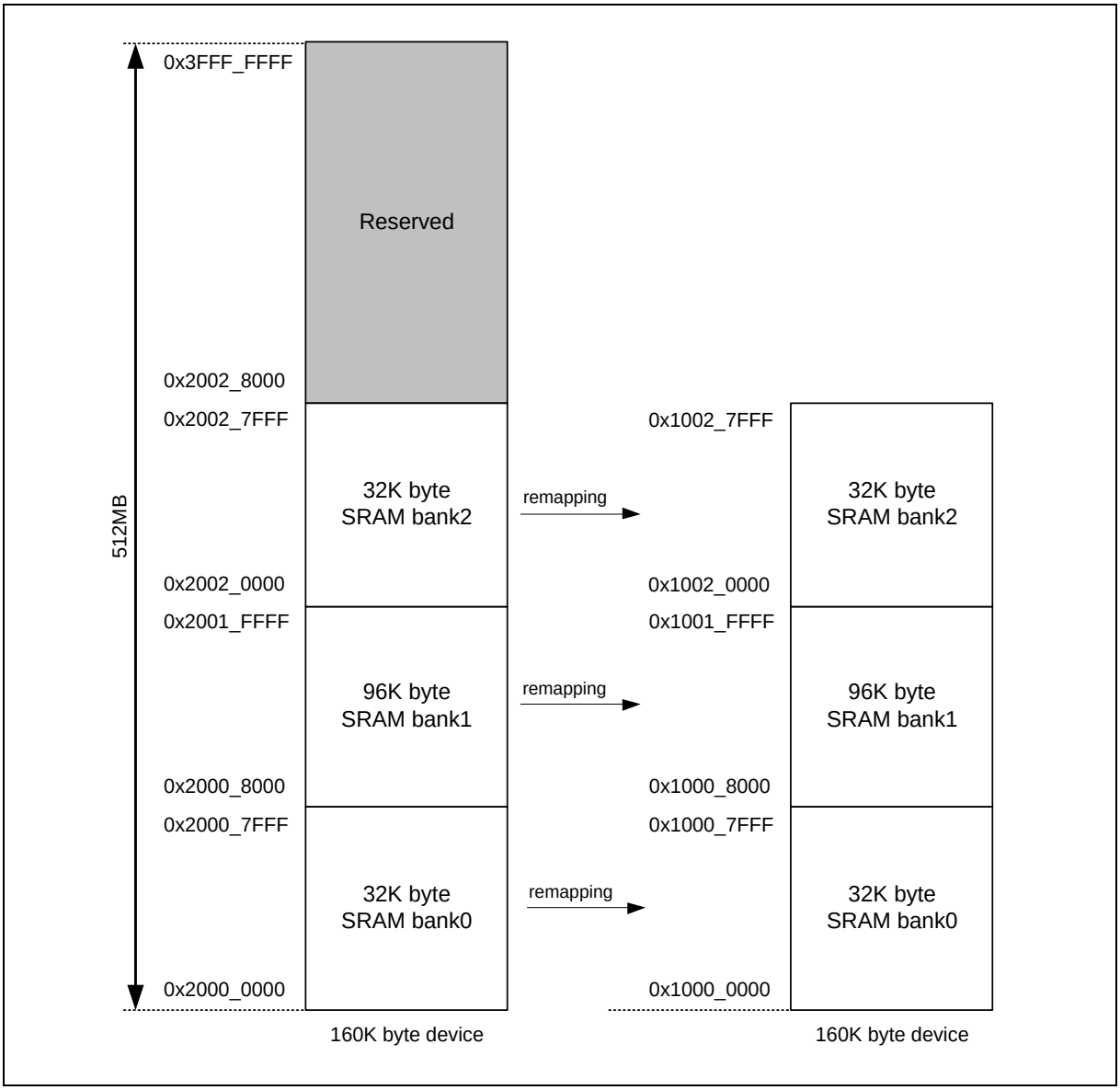


Figure 2.2-10: SRAM Memory Organization

SRAM bank0 has byte parity error check function. When CPU is accessing SRAM bank0, the parity error checking mechanism is dynamic operating. As parity error occurred, the PERRIF (SYS_SRAM_STATUS[0]) will be asserted to 1 and the SYS_SRAM_ERRADDR register will recode the address with parity error. Chip will enter interrupt when SRAM parity error occurred if PERRIEN (SYS_SRAM_INTCTL[0]) is set to 1. When SRAM parity error occurred, chip will stop detecting SRAM parity error until user writes 1 to clear the PERRIF(SYS_SRAM_STATUS[0]) bit.

2.2.8 Bus Matrix

The AX58200 supports Bus Matrix to manage the access arbitration between masters. The access arbitration can be selected by INTACTEN (SYS_AHBMCTL[0]) to use round-robin algorithm or set Cortex®-M4 CPU as the highest bus priority.

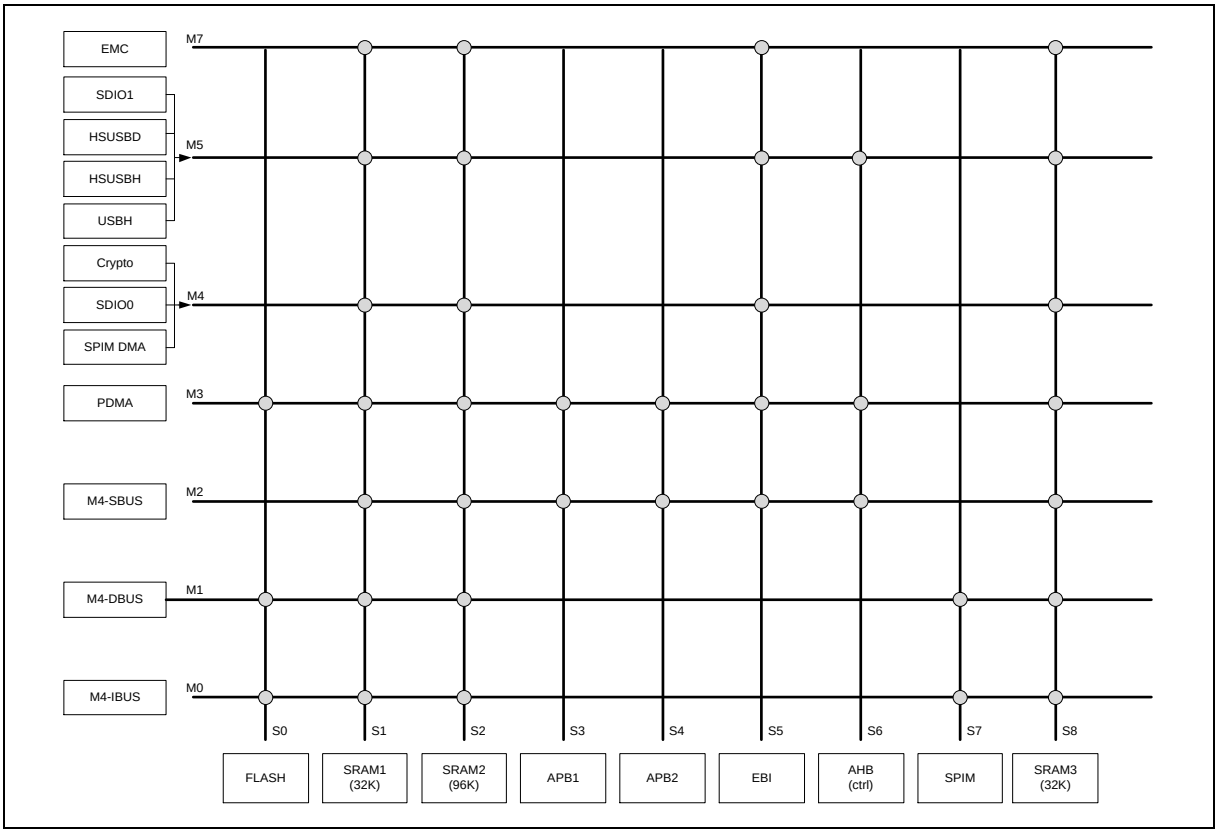


Figure 2.2-11: Bus Matrix Diagram

2.2.9 HIRC Auto Trim

This chip supports auto-trim function: the HIRC trim (48 MHz RC oscillator), according to the accurate external 32.768 KHz crystal oscillator or internal USB synchronous mode, automatically gets accurate HIRC output frequency, 0.25 % deviation within all temperature ranges.

For instance, the system needs an accurate 12 MHz clock. In such case, if neither using use PLL as the system clock source nor soldering 32.768 KHz crystal in system, user has to set REFCKSEL (SYS_IRCTCTL[10] reference clock selection) to “1”, set FREQSEL (SYS_IRCTCTL[1:0] trim frequency selection) to “01”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_IRCTISTS[8] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

2.2.10 Register Lock Control

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL address at 0x4000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

SYS_IPRST0	**Address 0x4000_0008**
SYS_ALTCTL	address 0x4000_0014
SYS_BODCTL	address 0x4000_0018
SYS_PORCTL	address 0x4000_0024
SYS_VREFCTL	address 0x4000_0028

SYS_USBPHY	address 0x4000_002C
SYS_SRAM_BISTCTL	address 0x4000_00D0
SYS_CVCTL	address 0x4000_01F8
CLK_PWRCTL	address 0x4000_0200
CLK_APBCLK0	address 0x4000_0208
CLK_CLKSEL0	address 0x4000_0210
CLK_CLKSEL1	address 0x4000_0214
CLK_PLLCTL	address 0x4000_0240
CLK_PMUCTL	address 0x4000_0290
NMIEN	address 0x4000_0300
AHBMCTL	address 0x4000_0400
FMC_FTCTL	address 0x4000_5018
FMC_ICPCMD	address 0x4000_501C
FMC_ISPCTL	address 0x4000_C000
FMC_ISPTRG	address 0x4000_C010
FMC_ISPSTS	address 0x4000_C040
FMC_CYCCTL	address 0x4000_C04C
FMC_KPKEYTRG	address 0x4000_C05C
FMC_KPKEYSTS	address 0x4000_C060
WDT_CTL	address 0x4004_0000
WDT_ALTCTL	address 0x4004_0004
TIMER0_CTL	address 0x4005_0000
TIMER1_CTL	address 0x4005_0100
TIMER2_CTL	address 0x4005_1000
TIMER3_CTL	address 0x4005_1100
TIMER0_PWMCTL	address 0x4005_0040
TIMER1_PWMCTL	address 0x4005_0140
TIMER2_PWMCTL	address 0x4005_1040
TIMER3_PWMCTL	address 0x4005_1140
TIMER0_PWMDTCTL	address 0x4005_0058
TIMER1_PWMDTCTL	address 0x4005_0158
TIMER2_PWMDTCTL	address 0x4005_1058
TIMER3_PWMDTCTL	address 0x4005_1158
TIMER0_PWMBRKCTL	address 0x4005_0070
TIMER1_PWMBRKCTL	address 0x4005_0170
TIMER2_PWMBRKCTL	address 0x4005_1070
TIMER3_PWMBRKCTL	address 0x4005_1170

TIMER0_PWMSWBRK	address 0x4005_007C
TIMER1_PWMSWBRK	address 0x4005_017C
TIMER2_PWMSWBRK	address 0x4005_107C
TIMER3_PWMSWBRK	address 0x4005_117C
TIMER0_PWMINTEN1	address 0x4005_0084
TIMER1_PWMINTEN1	address 0x4005_0184
TIMER2_PWMINTEN1	address 0x4005_1084
TIMER3_PWMINTEN1	address 0x4005_1184
TIMER0_PWMINTSTS1	address 0x4005_008C
TIMER1_PWMINTSTS1	address 0x4005_018C
TIMER2_PWMINTSTS1	address 0x4005_108C
TIMER3_PWMINTSTS1	address 0x4005_118C
EPWM_CTL0	address 0x4005_8000/0x4005_9000
EPWM_CTL1	address 0x4005_8000/0x4005_9000
EPWM_DTCTL0_1	address 0x4005_8070/0x4005_9070
EPWM_DTCTL2_3	address 0x4005_8074/0x4005_9074
EPWM_DTCTL4_5	address 0x4005_8078/0x4005_9078
EPWM_BRKCTL0_1	address 0x4005_80C8/0x4005_90C8
EPWM_BRKCTL2_3	address 0x4005_80CC/0x4005_90CC
EPWM_BRKCTL4_5	address 0x4005_80D0/0x4005_90D0
EPWM_SWBRK	address 0x4005_80DC/0x4005_90DC
EPWM_INTEN1	address 0x4005_80E4/0x4005_90E4
EPWM_INTSTS1	address 0x4005_80EC/0x4005_90EC
BPWM_CTL0	address 0x4005_A000/0x4005_B000
SYST_VAL	address 0xE000_E018

2.2.11 System Timer (SysTick)

The Cortex®-M4 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "ARM® Cortex®-M4 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

2.2.12 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode, but you can cause interrupts to enter a pending state in user mode if you enable the Configuration and Control Register. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

The NVIC supports:

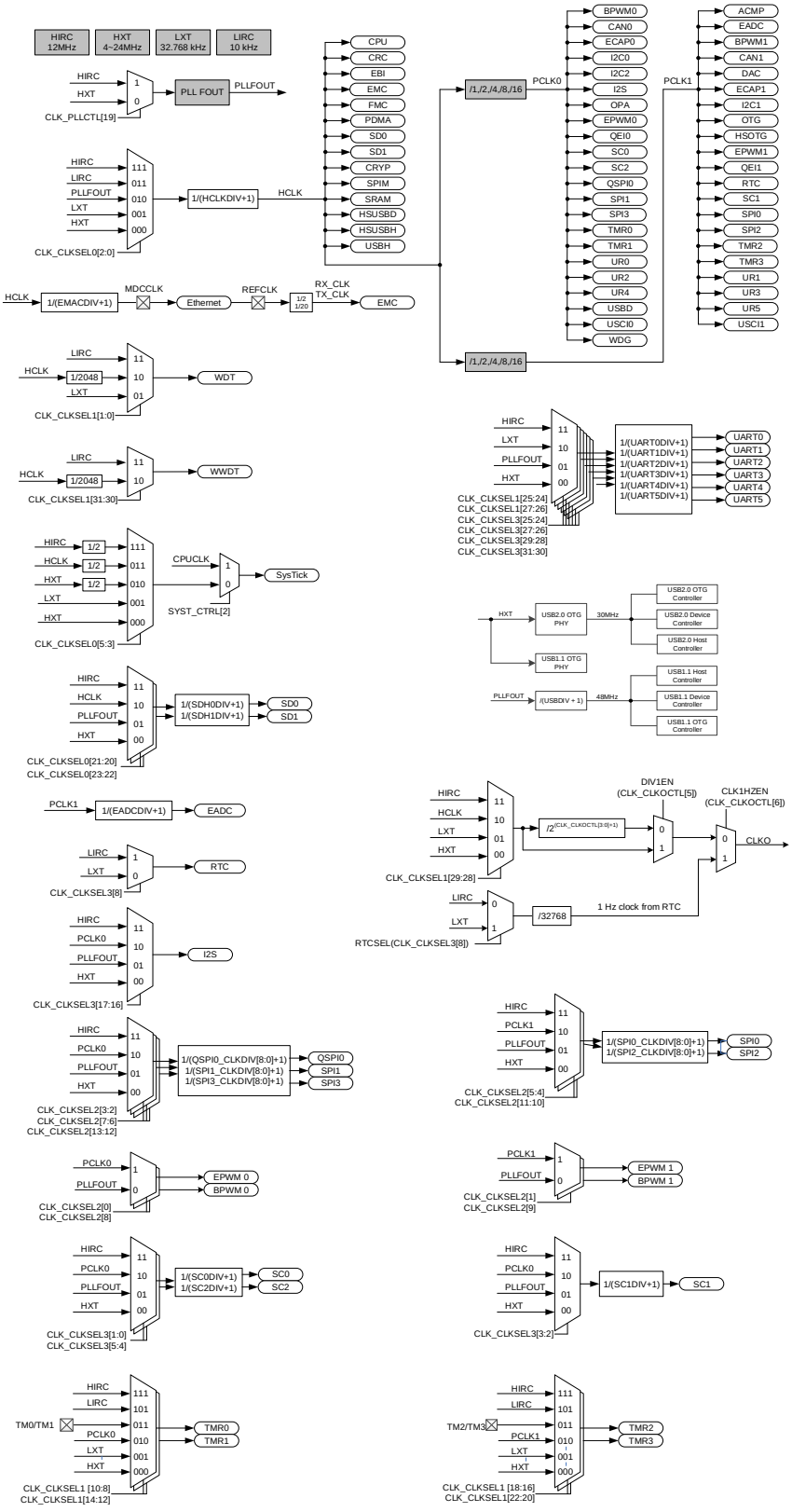
- An implementation-defined number of interrupts, in the range 1-240 interrupts.
- A programmable priority level of 0-16 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.
- An external Non Maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

2.3 Clock Controller

2.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex® -M4 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 12 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. Figure 2.3-1 shows the clock generator and the overview of the clock source control.



Note: For USB High-speed application, HXT should be 12 MHz.

Figure 2.3-1: Clock Generator Global View Diagram

2.3.2 Clock Generator

The clock generator consists of 5 clock sources, which are listed below:

- 32.768 KHz external low speed crystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~24 MHz external high speed crystal (HXT) or 12 MHz internal high speed oscillator (HIRC)
- 12 MHz internal high speed RC oscillator (HIRC)
- 10 KHz internal low speed RC oscillator (LIRC)

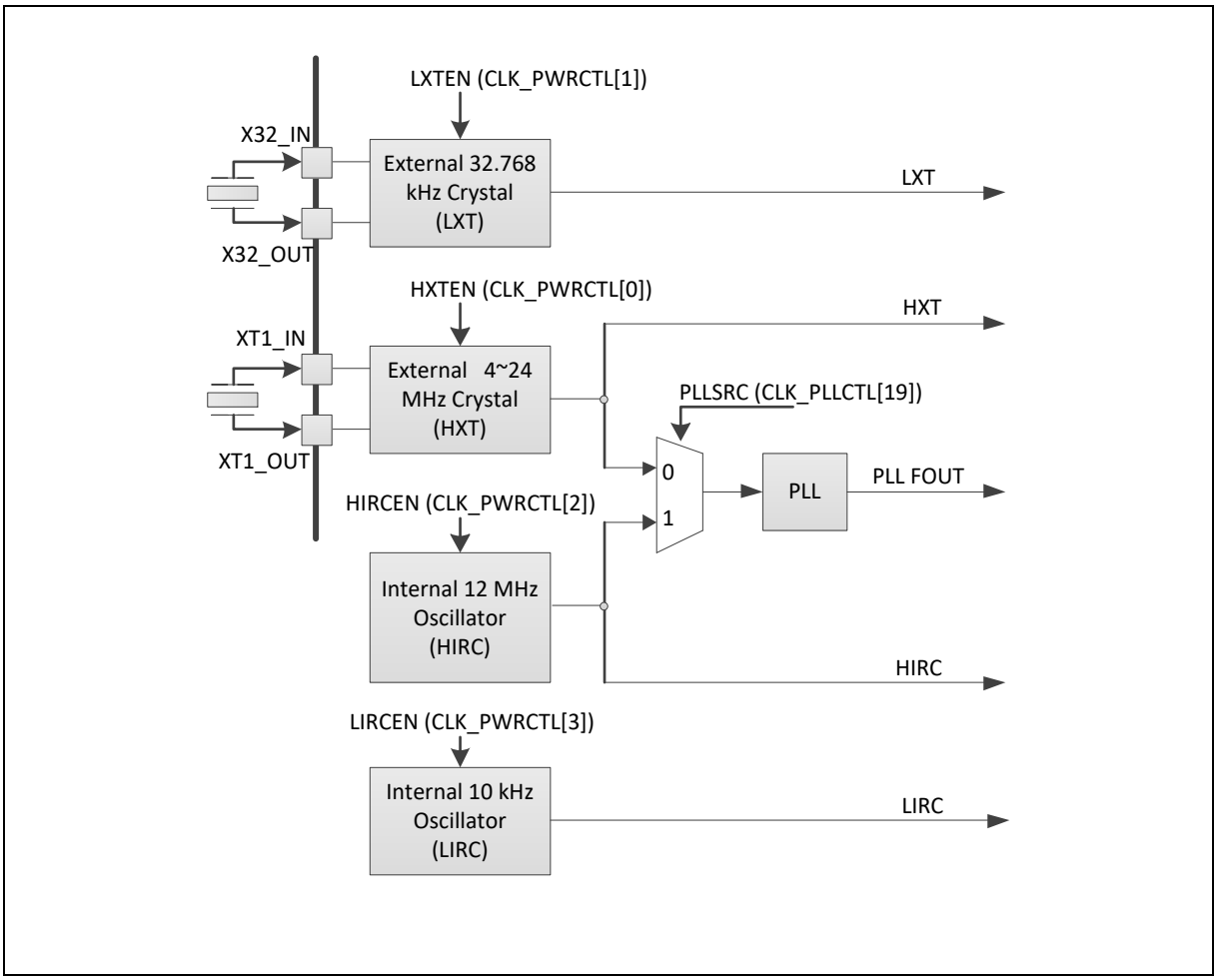


Figure 2.3-2: Clock Generator Block Diagram

2.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 2.3-3.

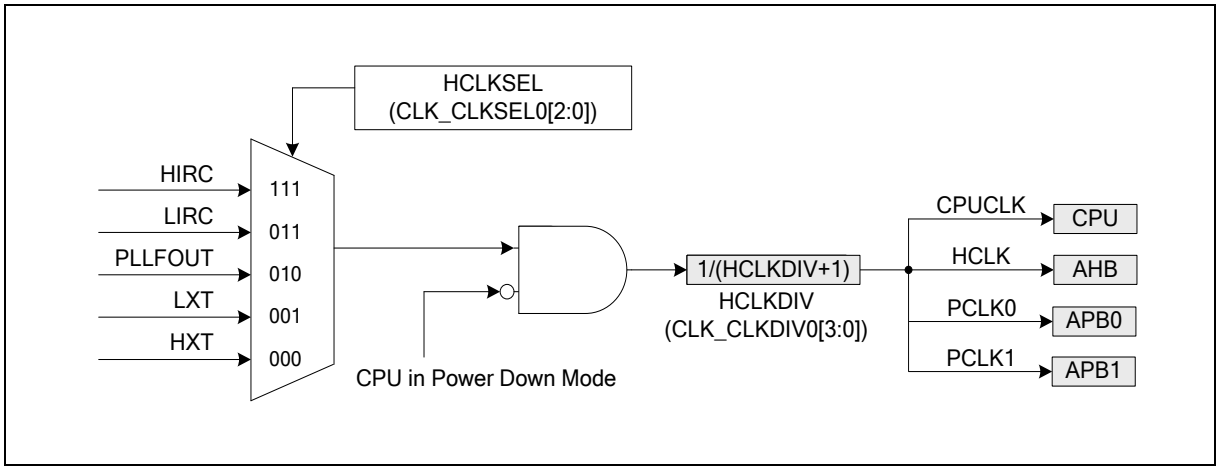


Figure 2.3-3: System Clock Block Diagrams

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIE (CLK_CLKDCTL[5]) is set to 1. User can try to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

Figure 2.3-4 shows the HXT clock stops detection and system clock switches to HIRC procedure.

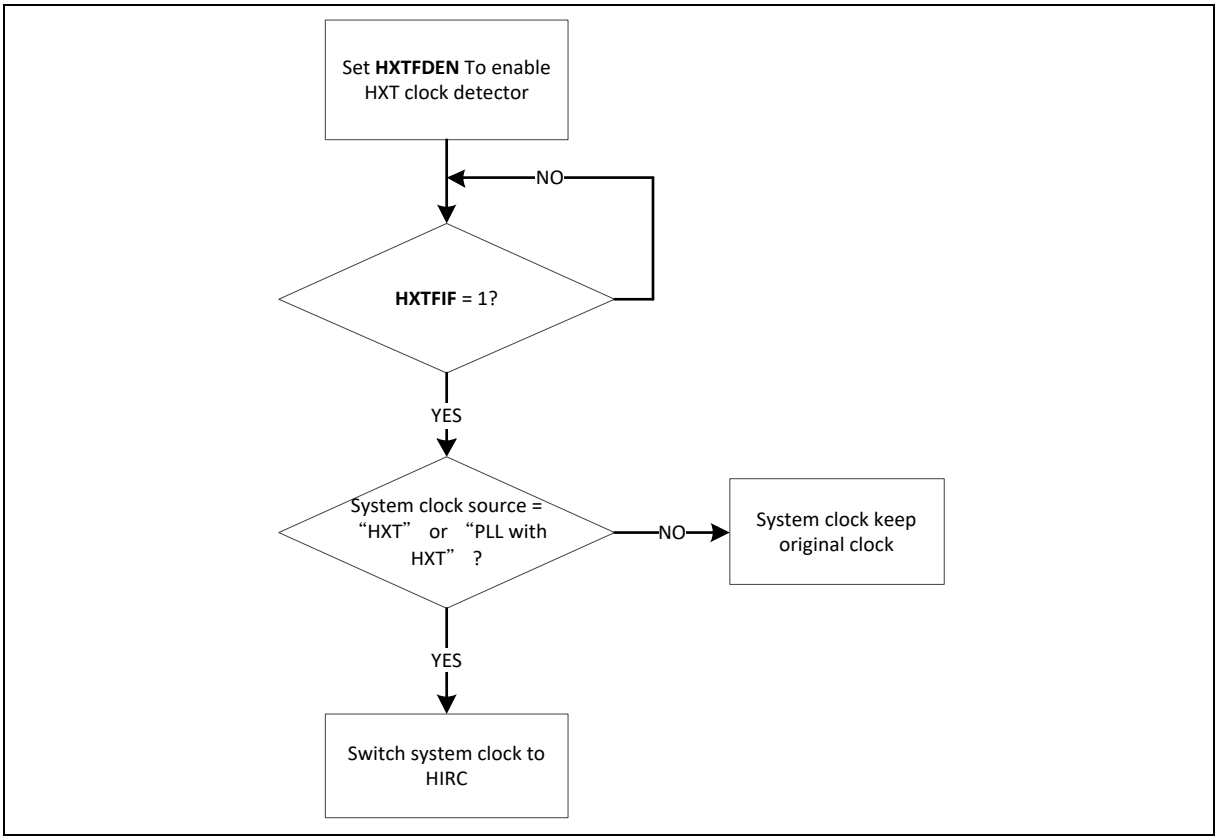


Figure 2.3-4: HXT Stop Protect Procedure

The clock source of SysTick in Cortex®-M4 core can use CPU clock or external clock (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 2.3-5.

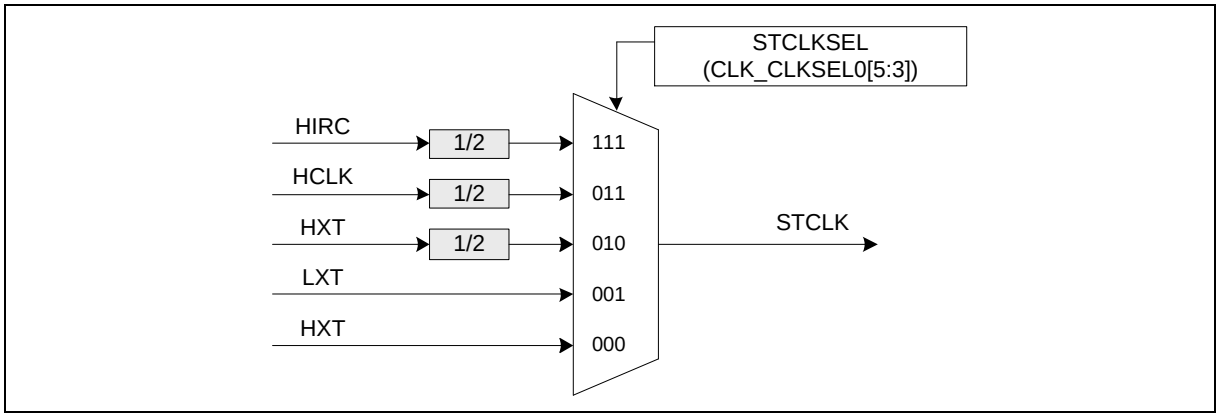


Figure 2.3-5: SysTick Clock Control Block Diagram

2.3.4 Peripherals Clock

Each peripheral clock has its own clock source selection. Refer to the CLK_CLKSEL1, CLK_CLKSEL2 and CLK_CLKSEL3 register.

2.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

For theses clocks, which still keep active, are listed below:

- Clock Generator
  - 10 KHz internal low speed RC oscillator (LIRC) clock
  - 32.768 KHz external low speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)

2.3.6 Clock Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore, there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

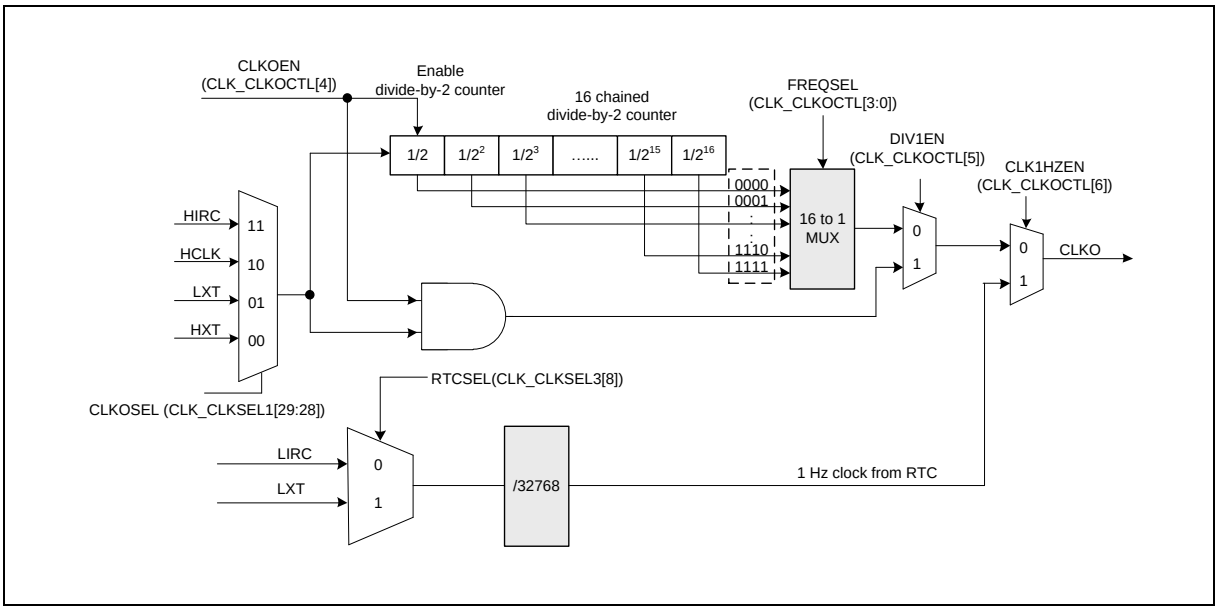


Figure 2.3-6: Clock Output Block Diagram

2.3.7 USB Clock Source

The clock sources of USB 1.0 and 2.0 systems are generated from USB2.0 PHY clock or programmable PLL output. The generated clocks are shown in Figure 2.3-7.

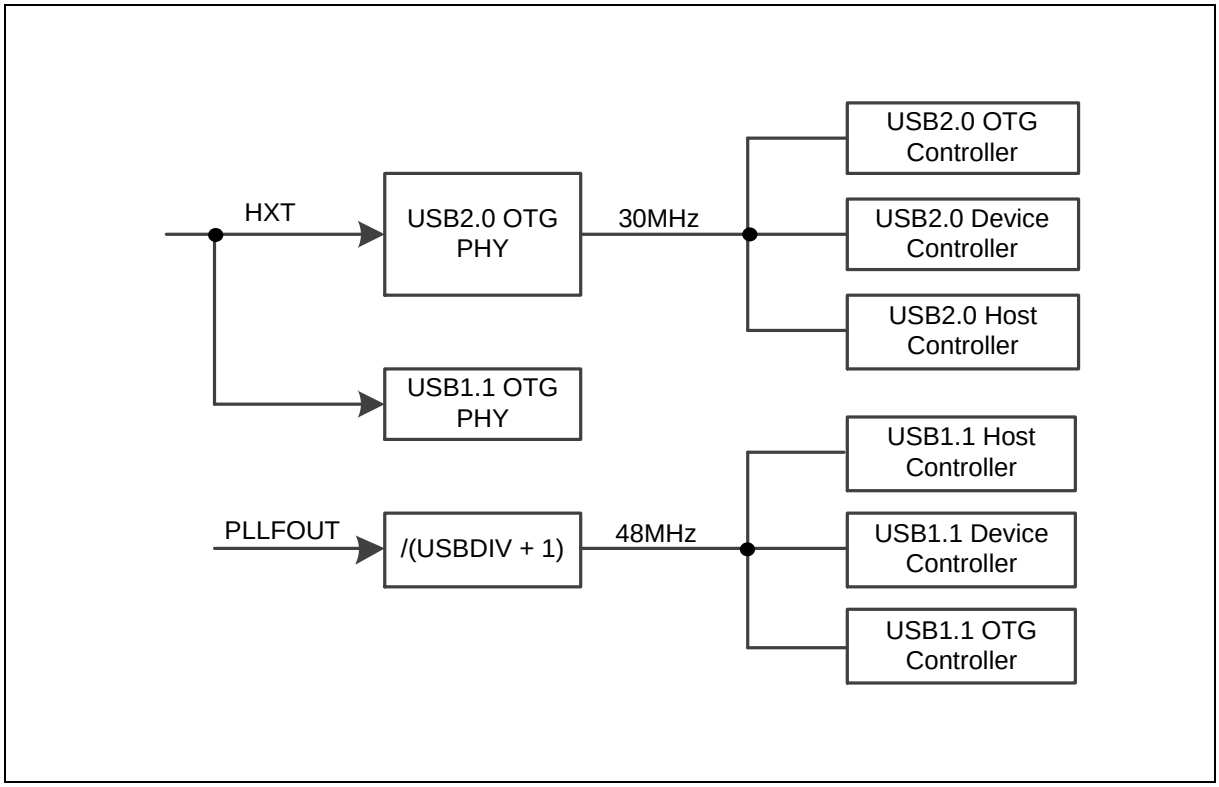


Figure 2.3-7: USB Clock Source

2.3.8 HXT clock

The High Speed Crystal (HXT) can be generated from two possible clock sources:

- HXT external crystal oscillator
- HXT user external clock

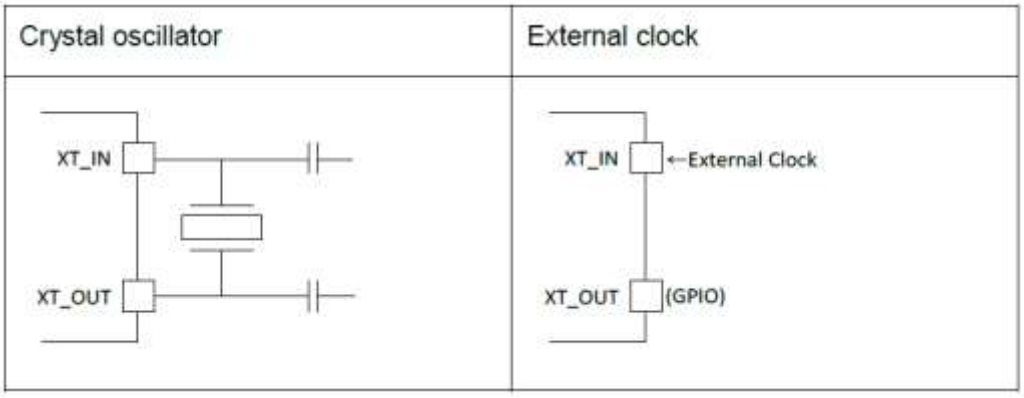


Figure 2.3-8:HXT Clock Source

External source (HXT OSC Mode)

The clock sources can be input from the external pin (PF.3).

When writing 1 to CFGXT1(CONFIG0[27]), HXT work as crystal mode. PF.2 and PF.3 are configured as external high speed crystal (HXT) pins. When writing 0 to CFGXT1 (CONFIG0[27]), HXT work as external clock mode. PF.3 is configured as external clock input pin. PF.3 MFP should be setting as GPIO mode. The DC characteristic of XT1_IN is the same as GPIO

2.4 True Random Number Generator (TRNG)

2.4.1 Overview

The True Random Number Generator (TRNG) is used to generate the randomness by extracting from physical phenomena.

2.4.2 Features

- Generates 800 random bits per second

2.5 Flash Memory Controller (FMC)

2.5.1 Overview

The FMC is equipped with dual-bank on-chip embedded Flash (BANK0 and BANK1) for application and configurable Data Flash to store some application dependent data. Both BANK0 and BANK1 have 64/128/256 Kbytes space. Thus, the total size of application rom (APROM) is 128K/256K/512K. A User Configuration block provides for system initiation in BANK0. A 4 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function in BANK0. A 4 Kbytes security protection ROM (SPROM) can conceal user program. A 2 Kbytes one-time-program ROM (OTP) is used for recording one-time-program data in BANK1. A 32K Boot Loader consists of native ISP functions. A 4KB cache with zero wait cycle is used to improve Flash access performance. This chip also supports In-Application-Programming (IAP) function. User switches the code executing without chip reset after the embedded Flash is updated.

2.5.2 Features

- Supports dual-bank Flash macro for safe firmware upgrade
- Supports 128/256/512 Kbytes application ROM (APROM)
- Supports 4 Kbytes loader ROM (LDROM)
- Supports 4 Kbytes security protection ROM (SPROM) to conceal user program
- Supports mirror SPROM in dual-bank Flash macro to read SPROM code while writing other ROM
- Supports Data Flash with configurable memory size
- Supports 16 bytes User Configuration block to control system initiation
- Supports 2 Kbytes one-time-program ROM (OTP)
- Supports 4 Kbytes page erase for all embedded Flash
- Supports Boot Loader with native In-System-Programming (ISP) functions
- Supports Security Key protection function for APROM, LDROM, SPROM, User Configuration block and KPROM protection
- Supports 32-bit/64-bit and multi-word Flash programming function
- Supports fast Flash programming verification function
- Supports CRC32 checksum calculation function
- Supports Flash all one verification function
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory
- Supports cache memory to improve Flash access performance and reduce power consumption
- Supports auto-tuning Flash access cycle function to optimize the Flash access performance

2.6 General Purpose I/O (GPIO)

2.6.1 Overview

This chip has up to 56 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 56 pins are arranged in 6 ports named as PA, PB, PC, PE, PF and PH. Each of the 56 pins is independent and has the corresponding register bits to control the pin mode function and data.

The EtherCAT slave controller (ESC) sub-system has up to 20 General Purpose I/O pins (names as IO[x]) to be shared with other function pins depending on the chip configuration.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOINI (CONFIG0[10]).

2.6.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Drive and High Slew Rate I/O mode
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in input mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the wake-up function

2.7 PDMA Controller (PDMA)

2.7.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 16 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

2.7.2 Features

- Supports 16 independently configurable channels
- Selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and SPI, UART, DAC, ADC and PWM request
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function on channel 0 and channel 1
- Supports stride function from channel 0 to channel 5

2.8 Timer Controller (TMR)

2.8.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

The timer controller also provides four PWM generators. Each PWM generator supports two PWM output channels in independent mode and complementary mode. The output state of PWM output pin can be controlled by pin mask, polarity and break control, and dead-time generator.

2.8.2 Features

2.8.2.1 Timer Function Features

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated

- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger EPWM, EADC, DAC and PDMA function
- Supports internal capture triggered while internal ACMP output signal transition
- Supports Inter-Timer trigger mode
- Supports event counting source from internal USB SOF signal

2.8.2.2 PWM Function Features

- Supports maximum clock frequency up to maximum PCLK
- Supports independent mode for PWM generator with two output channels
- Supports complementary mode for PWM generator with paired PWM output channel
  - 12-bit dead-time insertion with 12-bit prescale
- Supports 12-bit prescale from 1 to 4096
- Supports 16-bit PWM counter
  - Up, down and up-down count operation type
  - One-shot or auto-reload counter operation mode
- Supports mask function and tri-state enable for each PWM output pin
- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed, Brown-out detection, SRAM parity error and CPU lockup)
  - Brake pin noise filter control for brake source
  - Edge detect brake source to control brake state until brake status cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM zero point, period point, up-count compared or down-count compared point events
  - Brake condition happened
- Supports trigger EADC on the following events:
  - PWM zero point, period, zero or period point, up-count compared or down-count compared point events

2.9 Watchdog Timer (WDT)

2.9.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

2.9.2 Features

- 18-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{18}) and the time-out interval is 1.6 ms ~ 26.214 s if WDT_CLK = 10 KHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as 10 KHz or LXT.

2.10 Window Watchdog Timer (WWDT)

2.10.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software running to uncontrollable status by any unpredictable condition.

2.10.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

2.11 Real Time Clock (RTC)

2.11.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

2.11.2 Features

- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK.
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register.
- Supports Leap Year indication in RTC_LEAPYEAR register.
- Supports Day of the Week counter in RTC_WEEKDAY register.
- Frequency of RTC clock source compensate by RTC_FREQADJ register.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt.
- Supports 1 Hz clock output.
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated.
- Supports Daylight Saving Time software control in RTC_DSTCTL.
- Supports up 3 pairs dynamic loop tamper pin or 6 individual tamper pin.
- Supports 80 bytes spare registers and tamper pins detection to clear the content of these spare registers.

2.12 EPWM Generator and Capture Timer (EPWM)

2.12.1 Overview

The chip provides two EPWM generators — EPWM0 and EPWM1. Each EPWM supports 6 channels of EPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit EPWM counter with 16-bit comparator. The EPWM counter supports up, down and up-down counter types. EPWM uses comparator compared with counter to generate events. These events use to generate EPWM pulse, interrupt and trigger signal for EADC/DAC to start conversion.

The EPWM generator supports two standard EPWM output modes: Independent mode and Complementary mode, they have difference architecture. There are two output functions based on standard output modes: Group function and Synchronous function. Group function can be enabled under Independent mode or complementary mode. Synchronous function only enabled under complementary mode. Complementary mode has two comparators to generate various EPWM pulse with 12-bit dead-time generator and another free trigger comparator to generate trigger signal for EADC. For EPWM output control unit, it supports polarity output, independent pin mask and brake functions.

The EPWM generator also supports input capture function. It supports latch EPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also supports PDMA to transfer captured data to memory.

2.12.2 Features

2.12.2.1 EPWM Function Features

- Supports maximum clock frequency up to maximum PLL frequency
- Supports up to two EPWM modules, each module provides 6 output channels
- Supports independent mode for EPWM output/Capture input channel
- Supports complementary mode for 3 complementary paired EPWM output channel
  - Dead-time insertion with 12-bit resolution
  - Synchronous function for phase control
  - Two compared values during one period
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution EPWM counter
  - Up, down and up/down counter operation type
- Supports one-shot or auto-reload counter operation mode
- Supports group function
- Supports synchronous function
- Supports mask function and tri-state enable for each EPWM pin
- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed, SRAM parity error, Brown-out detection and CPU lockup).
  - Noise filter for brake source from pin
  - Leading edge blanking (LEB) function for brake source from analog comparator
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:

- EPWM counter matches 0, period value or compared value
- Brake condition happened

- Supports trigger EADC/DAC on the following events:
  - EPWM counter matches 0, period value or compared value
  - EPWM counter match free trigger comparator compared value (only for EADC)

2.12.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for EPWM all channels

2.13 Basic PWM Generator and Capture Timer (BPWM)

2.13.1 Overview

The chip provides two BPWM generators – BPWM0 and BPWM1. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for EADC to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

2.13.2 Features

2.13.2.1 BPWM Function Features

- Supports maximum clock frequency up to maximum PLL frequency.
- Supports up to two BPWM modules; each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit prescalar from 1 to 4096
- Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt in the following events:
  - BPWM counter matches 0, period value or compared value
- Supports trigger EADC in the following events:
  - BPWM counter matches 0, period value or compared value

2.13.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

2.14 Quadrature Encoder Interface (QEI)

2.14.1 Overview

There are two QEI controllers in this device. The Quadrature Encoder Interface (QEI) decodes speed of rotation and motion sensor information. It can be used in any application that uses a quadrature encoder for feedback.

2.14.2 Features

2.14.2.1 Quadrature Encoder Interface (QEI) Features

- Up to two QEI controllers, QEI0 and QEI1.
- Two QEI phase inputs, QEA and QEB; One Index input.
- A 32-bit up/down Quadrature Encoder Pulse Counter (QEI_CNT)
- A 32-bit software-latch Quadrature Encoder Pulse Counter Hold Register (QEI_CNTHOLD)
- A 32-bit Quadrature Encoder Pulse Counter Index Latch Register (QEI_CNTLATCH)
- A 32-bit Quadrature Encoder Pulse Counter Compare Register (QEI_CNTCMP) with a Pre-set Maximum Count Register (QEI_CNTMAX)
- One QEI control register (QEI_CTL) and one QEI Status Register (QEI_STATUS)
- Four Quadrature encoder pulse counter operation modes
  - Support x4 free-counting mode
  - Support x2 free-counting mode
  - Support x4 compare-counting mode
  - Support x2 compare-counting mode
- Encoder Pulse Width measurement mode
- Input frequency of QEA/QEB/IDX without noise filter must lower than PCLK/4
- Input frequency of QEA/QEB/IDX with noise filter must lower than Noise Filter Clk/8

2.15 Enhanced Input Capture Timer (ECAP)

2.15.1 Overview

This device provides up to two units of Input Capture Timer/Counter whose capture function can detect the digital edge-changed signal at channel inputs. Each unit has three input capture channels. The timer/counter is equipped with up counting, reload and compare-match capabilities.

2.15.2 Features

- Up to two Input Capture Timer/Counter units, CAP0 and CAP1.
- Each unit has 3 input channels.
- Each unit has its own interrupt vector.
- Each input channel has its own capture counter hold register.
- 24-bit Input Capture up-counting timer/counter.
- With noise filter in front end of input ports.
- Edge detector with three options:
  - Rising edge detection
  - Falling edge detection
  - Both edge detection
- Captured events reset and/or reload capture counter.
- Supports compare-match function.

2.16 UART Interface Controller (UART)

2.16.1 Overview

The chip provides six channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs Normal Speed UART and supports flow control function. The UART controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller also supports IrDA SIR, LIN and RS-485 function modes and auto-baud rate measuring function.

2.16.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - Support 9600 bps for UART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports LIN function mode (Only UART0 /UART1 with LIN function)
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detection function for receiver
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function

UART Feature	UART0/ UART1	UART2/ UART3/ UART4/ UART5	SC_UART	USCI-UART
FIFO	16 Bytes	16 Bytes	4 Bytes	TX: 1byte RX: 2byte
Auto Flow Control (CTS/RTS)	√	√	-	√
IrDA	√	√	-	-
LIN	√	-	-	-
RS-485 Function Mode	√	√	-	√
nCTS Wake-up	√	√	-	√
Imcoming Data Wake-up	√	√	-	√
Received Data FIFO reached threshold Wake-up	√	√	-	-
RS-485 Address Match (AAD mode) Wake-up	√	√	-	-
Auto-Baud Rate Measurement	√	√	-	√
STOP Bit Length	1, 1.5, 2 bit	1, 1.5, 2 bit	1, 2 bit	1, 2 bit
Word Length	5, 6, 7, 8 bits	5, 6, 7, 8 bits	5, 6, 7, 8 bits	6~13 bits
Even / Odd Parity	√	√	√	√
Stick Bit	√	√	-	-
Note: √= Supported				

Table 2.16-1: UART Features

2.17 Ethernet MAC Controller (EMAC)

2.17.1 Overview

This chip provides an Ethernet MAC Controller (EMAC) for Network application. The Ethernet MAC controller consists of IEEE 802.3/Ethernet protocol engine with internal CAM function for recognizing Ethernet MAC addresses, Transmit-FIFO, Receive-FIFO, TX/RX state machine controller, time stamping engine for IEEE 1588, Magic Packet parsing engine and status controller. The EMAC supports the RMII (Reduced MII) interface to connect with external Ethernet PHY.

2.17.2 Features

- Supports IEEE Std. 802.3 CSMA/CD protocol
- Supports Ethernet frame time stamping for IEEE Std. 1588 – 2002 protocol
- Supports both half and full duplex for 10 Mbps or 100 Mbps operation
- Supports RMII interface
- Supports MII Management function to control external Ethernet PHY
- Supports pause and remote pause function for flow control
- Supports long frame (more than 1518 bytes) and short frame (less than 64 bytes) reception
- Supports 16 entries CAM function for Ethernet MAC address recognition
- Supports Magic Packet recognition to wake system up from Power-down mode
- Supports 256 bytes transmit FIFO and 256 bytes receive FIFO
- Supports DMA function

2.18 Smart Card Host Interface (SC)

2.18.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal.

2.18.2 Features

- ISO 7816-3 T = 0, T = 1 compliant
- EMV2000 compliant
- Three ISO 7816-3 ports
- Separates receive/transmit 4 byte entry FIFO for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- Programmable guard time selection (11 ETU ~ 267 ETU)
- One 24-bit timer and two 8-bit timers for Answer to Request (ATR) and waiting times processing
- Supports auto direct / inverse convention function
- Supports transmitter and receiver error retry and error number limiting function
- Supports hardware activation sequence process, and the time between PWR on and CLK start is configurable
- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detected the card removal
- Supports UART mode
  - Full duplex, asynchronous communications
  - Separates receiving / transmitting 4 bytes entry FIFO for data payloads
  - Supports programmable baud rate generator
  - Supports programmable receiver buffer trigger level
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting EGT (SCn_EGT[7:0])
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1- or 2- stop bit generation

2.19 I²S Controller (I²S)

2.19.1 Overview

The I²S controller consists of I²S protocol to interface with external audio CODEC. Two 16-level depth FIFO for reading path and writing path respectively are capable of handling 8/16/24/32 bits audio data sizes. A PDMA controller handles the data movement between FIFO and memory.

2.19.2 Features

- Supports Master mode and Slave mode
- Capable of handling 8, 16, 24 and 32 bits data sizes in each audio channel
- Supports monaural and stereo audio data
- Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format
- Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format
- PCM protocol supports TDM multi-channel transmission in one audio sample, and the number of data channel can be set as 2, 4, 6, or 8
- Provides two 16-level FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Supports two PDMA requests, one for transmitting and the other for receiving

2.20 Serial Peripheral Interface (SPI)

2.20.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The AX58200 contains up to four sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer. Each SPI controller also supports I^2S mode to connect external audio CODEC.

2.20.2 Features

- SPI Mode
  - Up to four sets of SPI controllers
  - Supports Master or Slave mode operation
  - Master mode up to 100 MHz and Slave mode up to 100 MHz (when chip works at V_{DD} = 2.7~3.6V)
  - Configurable bit length of a transaction word from 8 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Supports PDMA transfer
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
- I^2S Mode
  - Supports Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Each provides two 4-level FIFO data buffers, one for transmitting and the other for receiving
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
  - Supports two PDMA requests, one for transmitting and the other for receiving

	QSPIx	SPIx
Dual/Quad I/O Mode	V	X
Two-bit Transfer Mode	V	X
FIFO Depth	8-level	SPI mode 8~16 bits data length: 8-level Otherwise: 4-level
Slave Time-out Function	V	X
Slave 3-Wired Mode	V	X
I^2S Mode	X	V

2.21 Quad Serial Peripheral Interface (QSPI)

2.21.1 Overview

The Quad Serial Peripheral Interface (QSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The AX58200 contains one QSPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device.

The QSPI controller supports 2-bit Transfer mode to perform full-duplex 2-bit data transfer and also supports Dual and Quad I/O Transfer mode and the controller supports the PDMA function to access the data buffer.

2.21.2 Features

- Supports Master or Slave mode operation
- Master mode up to 100 MHz and Slave mode up to 100 MHz (when chip works at VDD = 2.7~3.6V)
- Supports 2-bit Transfer mode
- Supports Dual and Quad I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-Wire, no slave selection signal, bi-direction interface
- Supports one data channel half-duplex transfer
- Supports receive-only mode

2.22 SPI Synchronous Serial Interface Controller (SPI Master mode)

2.22.1 Overview

The SPI Synchronous serial Interface Controller for SPI master mode performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data received from MCU. This SPI controller can drive one external peripheral (External SPI Flash) and it is seen as the SPI master mode. It can generate an interrupt signal when data transfer is finished and can be cleared by writing 1 to the interrupt flag. The active level of device/slave select signal can be chosen to low active or high active, which depends on the peripheral. Writing a divisor into the SPIM_CTL1 register can program the frequency of serial clock output to the peripheral.

In SPI Flash controller, normal I/O mode contains four 32-bit transmit/receive buffers, and can provide 1 to 4 burst mode operation. The number of bits in each transaction can be 8, 16, 24, or 32; data can be transmitted/received up to four successive transactions in one transfer.

By DMA write mode, user can move data from SRAM to external SPI Flash component. In DMA read mode, user can move data from external SPI Flash component to SRAM. In direct memory mapping mode (DMM mode), this SPI Flash controller will translate the AHB bus commands into SPI Flash operations without MCU setting related SPI Flash command. Therefore, users can access external SPI Flash as a ROM module.

In direct memory mapping mode with cache off mode, it will pre-fetch 4-word Flash data after a direct memory mapping access. When using direct memory mapping mode with cache on mode, it will use 32 Kbytes cache memory to reduce the number of accessing external SPI Flash component and the performance of SPI Flash access can be improved. To improve the read operation of SPI Flash without increasing the serial clock frequency, this SPI Flash controller supports DTR/DDR (Double Transfer Rate/Double Data Rate) read command codes that support Standard/Dual/Quad SPI modes. The one byte command code is still latched into the device on the rising edge of the serial clock similar to all other SPI commands. Once a DTR/DDR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

In core coupled memory mode (CCM mode), the cache function is disabled by hardware automatically, and MCU can access this 32 Kbytes cache memory as general SRAM. For data protection, this SPI Flash controller supports cipher encryption and decryption circuits to protect data which user places into external SPI Flash when DMA read/write mode and direct memory mapping mode are used.

2.22.2 Features

- Supports maximum 32M bytes SPI Flash size
- Supports SPI master mode
- Supports Direct Memory Mapping Mode and Normal I/O Mode
- Supports 8/16/24/32 bits transaction for Normal I/O mode
- Provides burst mode operation in Normal I/O mode, which can transmit/receive data up to four successive transactions in one transfer
- Supports DMA mode read/write
- Supports standard (1-bit), dual (2-bit), and quad (4-bit) I/O transfer mode
- Supports Double Transfer Rate (DTR) / Double Data Rate (DDR) transfer mode
- Supports 32 Kbytes cache memory
- Supports 32 Kbytes Core Coupled Memory (CCM) when cache function disable
- Supports Cipher encryption/decryption
- One slave/device select line for external SPI Flash component

2.23 I²C Serial Interface Controller (I²C)

2.23.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are two sets of I²C controllers which support Power-down wake-up function.

2.23.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to three I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports setup/hold time programmable
- Supports Bus Management (SM/PM compatible) function

2.24 USCI - Universal Serial Control Interface Controller (USCI)

2.24.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I^2C functional protocol.

2.24.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I^2C

2.25 USCI – UART Mode

2.25.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter being independent, frames can start at different points in time for transmission and reception.

The UART controller also provides auto flow control. There are two conditions to wake-up the system.

2.25.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Support 9-bit Data Transfer (Support 9-bit RS-485)
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports PDMA capability
- Supports Wake-up function (Data and nCTS Wakeup Only)

2.26 USCI - SPI Mode

2.26.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USCI_CTL[2:0]) = 0x1.

This SPI protocol can operate as master or Slave mode by setting the SLAVE (USCI_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in master and Slave mode are shown below.

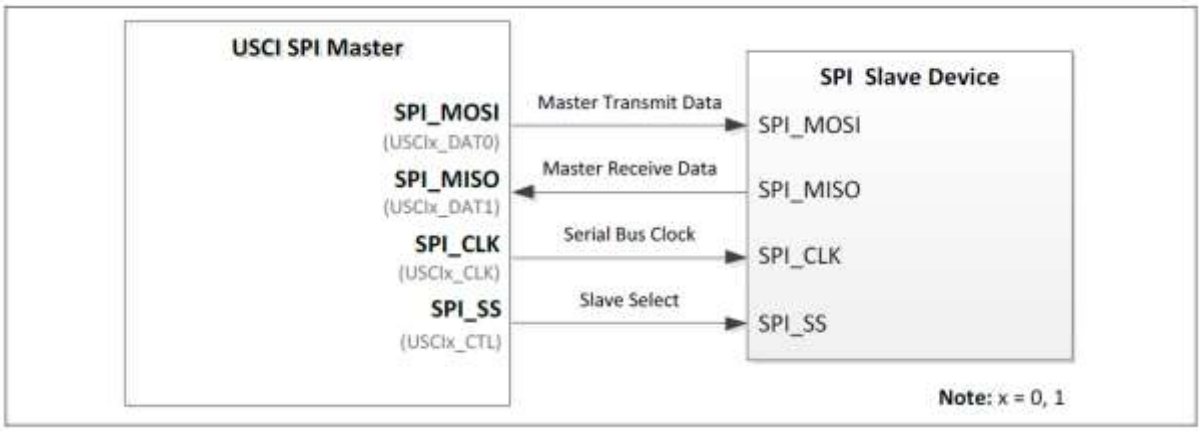


Figure 2.26-1: SPI Master Mode Application Block Diagram

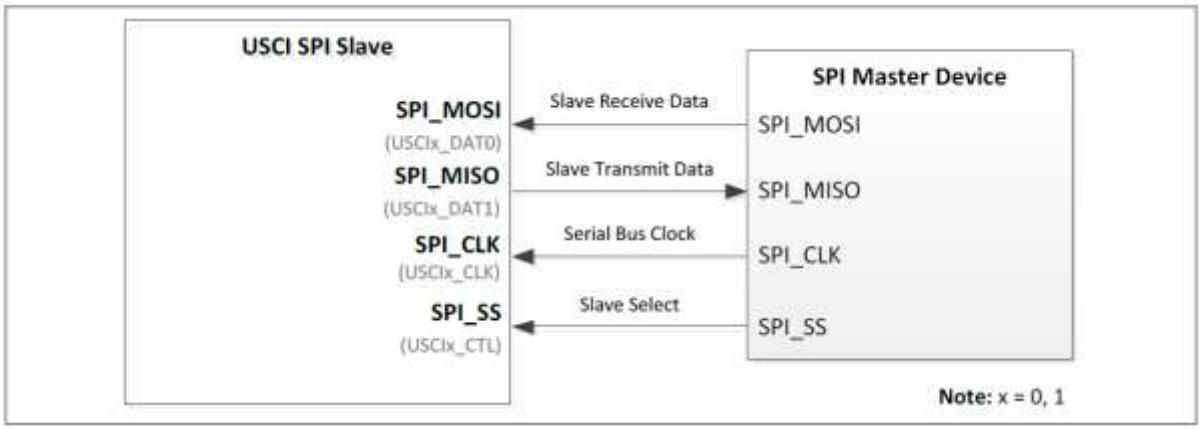


Figure 2.26-2: SPI Slave Mode Application Block Diagram

2.26.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master = f_{PCLK} / 2, Slave < f_{PCLK} / 5)
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence
- Supports Word Suspend function
- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface

- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

2.27 USCI - I²C Mode

2.27.1 Overview

On I²C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 2.27-1 for more detailed I²C BUS Timing.

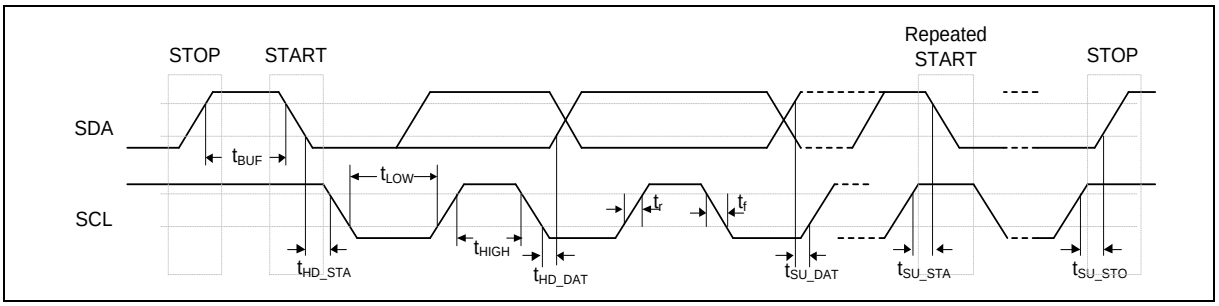


Figure 2.27-1: I²C Bus Timing

The device's on-chip I²C provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C mode is selected by FUNMODE (USCI_CTL [2:0]) = 100B. When enable this port, the USCI interfaces to the I²C bus via two pins: SDA and SCL. When I/O pins are used as I²C ports, user must set the pins function to I²C in advance.

Note: Pull-up resistor is needed for I²C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I²C operation mode.

2.27.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffer for data payload
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by data toggle or address match
- Supports setup/hold time programmable
- Supports multiple address recognition (two slave address with mask option)

2.28 Controller Area Network (CAN)

2.28.1 Overview

The C_CAN consists of the CAN Core, Message RAM, Message Handler, Control Registers and Module Interface. The CAN Core performs communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1MBit/s. For the connection to the physical layer, additional transceiver hardware is required.

For communication on a CAN network, individual Message Objects are configured. The Message Objects and Identifier Masks for acceptance filtering of received messages are stored in the Message RAM. All functions concerning the handling of messages are implemented in the Message Handler. These functions include acceptance filtering, the transfer of messages between the CAN Core and the Message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the C_CAN can be accessed directly by the software through the module interface. These registers are used to control/configure the CAN Core and the Message Handler and to access the Message RAM.

2.28.2 Features

- Supports CAN protocol version 2.0 part A and B
- Bit rates up to 1 MBit/s
- 32 Message Objects
- Each Message Object has its own identifier mask
- Programmable FIFO mode (concatenation of Message Objects)
- Maskable interrupt
- Disabled Automatic Re-transmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation
- 16-bit module interfaces to the AMBA APB bus
- Supports wake-up function

2.29 Secure Digital Host Controller (SDH)

2.29.1 Overview

The Secure Digital Host Controller (SD Host) has DMAC unit and SD unit. The DMAC unit provides a DMA (Direct Memory Access) function for SD to exchange data between system memory and shared buffer (128 bytes), and the SD unit controls the interface of SD/SDHC. The SDHOST controller can support SD/SDHC and cooperated with DMAC to provide a fast data transfer between system memory and cards.

2.29.2 Features

- AMBA AHB master/slave interface compatible, for data transfer and register read/write.
- Supports single DMA channel.
- Supports hardware Scatter-Gather function.
- Using single 128 Bytes shared buffer for data exchange between system memory and cards.
- Synchronous design for DMA with single clock domain, AHB bus clock (HCLK).
- Interface with DMAC for register read/write and data transfer.
- Supports SD/SDHC card.
- Completely asynchronous design for Secure Digital with two clock domains, HCLK and Engine clock, note that frequency of HCLK should be higher than the frequency of peripheral clock.

2.30 External Bus Interface (EBI)

2.30.1 Overview

This chip is equipped with an external bus interface (EBI) for external device use. To save the connections between an external device and a chip, EBI is operating at address bus and data bus multiplex mode. The EBI supports three chip selects that can connect three external devices with different timing setting requirements.

2.30.2 Features

- Supports up to three memory banks
- Supports dedicated external chip select pin with polarity control for each bank
- Supports accessible space up to 1 Mbytes for each bank, actually external addressable space is dependent on package pin out
- Supports 8-/16-bit data width
- Supports byte write in 16-bit data width mode
- Supports Address/Data multiplexed Mode
- Supports Timing parameters individual adjustment for each memory block
- Supports LCD interface i80 mode
- Supports PDMA mode
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R)
- Supports address bus and data bus separate mode

2.31 USB 1.1 Device Controller (USBD)

2.31.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports control/bulk/interrupt/ isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 1KBytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD_BUFSEGx).

There are 12 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of "Endpoint Control" is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the no-event-wake-up, device plug- in or plug-out event, USB events, like IN ACK, OUT ACK, etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USBD_EPSTS0 and USBD_EPSTS1) to acknowledge what kind of event occurring in this endpoint.

A software-disconnect function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD_SE0), the USB controller will force the output of USB_D+ and USB_D- to level low and its function is disabled. After disable the SE0 bit, host will enumerate the USB device again.

For more information on the Universal Serial Bus, please refer to Universal Serial Bus Specification Revision 1.1.

2.31.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 4 different interrupt events (NEVWK, VBUSDET, USB and BUS)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3 ms
- Supports 12 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1 Kbyte buffer size
- Provides remote wake-up capability

2.32 High Speed USB 2.0 Device Controller (HSUSBD)

2.32.1 Overview

The USB device controller interfaces the AHB bus and the UTMI bus. The USB controller contains both the AHB master interface and AHB slave interface. CPU programs the USB controller registers through the AHB slave interface. For IN or OUT transfer, the USB device controller needs to write data to memory or read data from memory through the AHB master interface. The USB device controller is complaint with USB 2.0 specification and it contains 12 configurable endpoints in addition to control endpoint. These endpoints could be configured to BULK, INTERRUPT or ISO. The USB device controller has a built-in DMA to relieve the load of CPU.

2.32.2 Features

- USB Specification reversion 2.0 compliant
- Supports 12 configurable endpoints in addition to Control Endpoint
- Each of the endpoints can be Isochronous, Bulk or Interrupt and either IN or OUT direction
- Three different operation modes of an in-endpoint — Auto Validation mode, Manual Validation mode, Fly mode
- Supports DMA operation
- 4092 Bytes Configurable RAM used as endpoint buffer
- Supports Endpoint Maximum Packet Size up to 1024 bytes

2.33 USB 2.0 Host Controller (USBH)

2.33.1 Overview

This chip is equipped with a USB 2.0 HS/FS Host Controller (USBH) that supports Enhanced Host Controller Interface (EHCI) and Open Host Controller Interface (OpenHCI, OHCI) Specification, a register-level description of a host controller, to manage the devices and data transfer of Universal Serial Bus (USB).

The USBH supports an integrated Root Hub with a USB port, a DMA for real-time data transfer between system memory and USB bus, port power control and port over current detection.

The USBH is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting over current of attached USB devices.

2.33.2 Features

- Compliant with Universal Serial Bus (USB) Specification Revision 2.0.
- Supports Enhanced Host Controller Interface (EHCI) Specification Revision 1.0
- Supports Open Host Controller Interface (OpenHCI) Specification Revision 1.0.
- Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt, Isochronous and Split transfers.
- Supports an integrated Root Hub.
- Supports a port routing logic to route full/low speed device to OHCI controller.
- Supports two USB host port shared with USB device (OTG function).
- Supports port power control and port over current detection.
- Supports DMA for real-time data transfer.

2.34 USB On-The-Go (OTG)

2.34.1 Overview

The OTG controller interfaces to USB PHY and USB controllers which consist of a USB 1.1 host controller and a USB 2.0 FS device controller. The OTG controller supports HNP and SRP protocols defined in the “On-The-Go and Embedded Host Supplement to the USB 2.0 Revision 2.0 Specification”.

USB frame, including USB host, USB device, and OTG controller, can be configured as Host-only, Device-only, ID-dependent or OTG Device mode defined in USBROLE (SYS_USBPHY[1:0]). In Host- only mode, USB frame acts as USB host. USB frame can support both full-speed and low-speed transfer. In Device-only mode, USB frame acts as USB device. USB frame only supports full-speed transfer. In ID-dependent mode, USB frame can be USB Host or USB device depending on USB_ID pin state. In OTG device mode, the role of USB frame depends on the definition of OTG specification. USB frame only supports full-speed transfer when OTG device acts as a peripheral.

2.34.2 Features

- Built-in USB PHY
- Configurable to operate as:
  - Host-only
  - Device-only
  - ID-dependent: The role of USB frame is only dependent on USB_ID pin value--as USB Host (USB_ID pin is low) or USB Device (USB_ID pin is high). Not support HNP or SRP protocol.
  - OTG device: dependent on USB_ID pin status to be A-device (USB_ID pin is low) or B-device (USB_ID pin is high). Support HNP and SRP protocols.

2.35 High Speed USB On-The-Go (HSOTG)

2.35.1 Overview

The HSOTG controller interfaces to USB PHY and USB controllers which consist of a USB 2.0 host controller and a USB 2.0 HS device controller. The OTG controller supports HNP and SRP protocols defined in the "On-The-Go and Embedded Host Supplement to the USB 2.0 Revision 1.3 Specification".

USB frame, including USB host, USB device, and OTG controller, can be configured as Host-only, Device-only, ID-dependent or OTG Device mode defined in HSUSBROLE (SYS_USBPHY[17:16]). In Host-only mode, USB frame acts as USB host. USB frame can support high-speed, full-speed and low- speed transfer. In Device-only mode, USB frame acts as USB device. USB frame supports high-speed and full-speed transfer. In ID-dependent mode, USB frame can be USB Host or USB device depends on USB_ID pin state. In OTG device mode, the role of USB frame depends on the definition of OTG specification. USB frame supports high-speed and full-speed transfer when OTG device acts as a peripheral.

2.35.2 Features

- Built in USB PHY
- Configurable to operate as:
  - Host-only
  - Device-only
  - ID-dependent: The role of USB frame is only dependent on USB_ID pin value--as USB Host (USB_ID pin is low) or USB Device (USB_ID pin is high). Not support HNP or SRP protocol.
  - OTG device: dependent on USB_ID pin status to be A-device (USB_ID pin is low) or B-device (USB_ID pin is high). Support HNP and SRP protocols.

2.36 CRC Controller (CRC)

2.36.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 settings.

2.36.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

2.37 Cryptographic Accelerator (CRYPTO)

2.37.1 Overview

The Crypto (Cryptographic Accelerator) includes a secure pseudo random number generator (PRNG) core and supports AES, DES/TDES, SHA and HMAC algorithms.

The PRNG core supports 64 bits, 128 bits, 192 bits, and 256 bits random number generation.

The AES accelerator is an implementation fully compliant with the AES (Advance Encryption Standard) encryption and decryption algorithm. The AES accelerator supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2, and CBC-CS3 mode.

The DES/TDES accelerator is an implementation fully compliant with the DES and Triple DES encryption/decryption algorithm. The DES/TDES accelerator supports ECB, CBC, CFB, OFB, and CTR mode.

The SHA accelerator is an implementation fully compliant with the SHA-160, SHA-224, SHA-256, SHA- 384, and SHA-512 and corresponding HMAC algorithms.

The ECC accelerator is an implementation fully compliant with elliptic curve cryptography by using polynomial basis in binary field and prime filed.

2.37.2 Features

- PRNG
  - Supports 64 bits, 128 bits, 192 bits, and 256 bits random number generation
- AES
  - Supports FIPS NIST 197
  - Supports SP800-38A and addendum
  - Supports 128, 192, and 256 bits key
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2, and CBC-CS3 mode
  - Supports key expander
- DES
  - Supports FIPS 46-3
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, and CTR mode
- TDES
  - Supports FIPS NIST 800-67
  - Implemented according to the X9.52 standard
  - Supports two keys or three keys mode
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, and CTR mode
- SHA
  - Supports FIPS NIST 180, 180-2
  - Supports SHA-160, SHA-224, SHA-256, SHA-384, and SHA-512
- HMAC

- Supports FIPS NIST 180, 180-2
- Supports HMAC-SHA-160, HMAC-SHA-224, HMAC-SHA-256, HMAC-SHA-384, and HMAC-SHA-512

- ECC
  - Supports both prime field GF(p) and binary filed GF(2^m)
  - Supports NIST P-192, P-224, P-256, P-384, and P-521
  - Supports NIST B-163, B-233, B-283, B-409, and B-571
  - Supports NIST K-163, K-233, K-283, K-409, and K-571
  - Supports point multiplication, addition and doubling operations in GF(p) and GF(2m)
  - Supports modulus division, multiplication, addition and subtraction operations in GF(p)

2.38 Enhanced 12-bit Analog-to-Digital Converter (EADC)

2.38.1 Overview

The chip contains one 12-bit successive approximation analog-to-digital converter (SAR ADC converter) with 16 external input channels and 3 internal channels. The ADC converter can be started by software trigger, PWM0/1 triggers, BPWM0/1 triggers, timer0~3 overflow pulse triggers, ADINT0, ADINT1 interrupt EOC (End of conversion) pulse trigger and external pin (EADC0_ST) input signal.

2.38.2 Features

- Analog input voltage range: 0~ V_{REF} (Max to 3.6V)
- Reference voltage from V_{REF} pin
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 16 single-end analog external input channels or 8 pair differential analog input channels
- Up to 3 internal channels, they are band-gap voltage (V_{BG}), temperature sensor (V_{TEMP}), and V_{DD} power
- Four ADC interrupts (ADINT0~3) with individual interrupt vector addresses
- Maximum ADC clock frequency is 72 MHz
- Up to 5.14 MSPS conversion rate
- Configurable ADC internal sampling time
- 12-bit, 10-bit, 8-bit, 6-bit configurable resolution
- Supports calibration and load calibration words capability
- Supports internal reference voltage V_{REF}: 1.6V, 2.0V, 2.5V, and 3.0V.
- Supports three power saving modes:
  - Deep Power-down mode
  - Power-down mode
  - Standby mode
- Up to 19 sample modules
  - Each of sample modules which is configurable for ADC converter channel EADC_CH0~15 and trigger source
  - Sample module 16~18 is fixed for ADC channel 16, 17, 18 input sources as band-gap voltage, temperature sensor, and V_{DD} power
  - Double buffer for sample control logic module 0~3
  - Configurable sampling time for each sample module
  - Conversion results are held in 19 data registers with valid and overrun indicators
- An ADC conversion can be started by:
  - Write 1 to SWTRGn (EADC_SWTRG[n], n = 0~18)
  - External pin EADC_ST
  - Timer0~3 overflow pulse triggers
  - ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers
  - EPWM/BPWM triggers
- Supports PDMA transfer
- Conversion Result Monitor by Compare Mode

2.39 Digital to Analog Converter (DAC)

2.39.1 Overview

The DAC module is a 12-bit, voltage output digital-to-analog converter. It can be configured to 12- or 8- bit output mode and can be used in conjunction with the PDMA controller. The DAC integrates a voltage output buffer that can be used to reduce output impendence and drive external loads directly without having to add an external operational amplifier.

2.39.2 Features

- Analog output voltage range: 0~AVDD.
- Supports 12- or 8-bit output mode.
- Rail to rail settle time 8us.
- Supports up to two 12-bit 1 MSPS voltage type DAC.
- Reference voltage from internal reference voltage (INT_VREF), V_{REF} pin.
- DAC maximum conversion updating rate 1 MSPS.
- Supports voltage output buffer mode and bypass voltage output buffer mode.
- Supports software and hardware trigger, including Timer0~3, EPWM0, EPWM1, and external trigger pin to start DAC conversion.
- Supports PDMA mode.
- Supports group mode of synchronized update capability for two DACs.

2.40 Analog Comparator Controller (ACMP)

2.40.1 Overview

The chip provides two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes.

2.40.2 Features

- Analog input voltage range: 0 ~ AVDD (voltage of AVDD pin)
- Up to two rail-to-rail analog comparators
- Supports hysteresis function
  - Supports programmable hysteresis window: 0mV, 10mV, 20mV and 30mV
- Supports wake-up function
- Supports programmable propagation speed and low power consumption
- Selectable input sources of positive input and negative input
- ACMP0 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP0_P0, ACMP0_P1, ACMP0_P2, or ACMP0_P3
  - 4 negative sources:
    - ACMP0_N
    - Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (VBG)
    - DAC0 output (DAC0_OUT)
- ACMP1 supports
  - 4 multiplexed I/O pins at positive sources:
    - ACMP1_P0, ACMP1_P1, ACMP1_P2, or ACMP1_P3
  - 4 negative sources:
    - ACMP1_N
    - Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (VBG)
    - DAC0 output (DAC0_OUT)
- Shares one ACMP interrupt vector for all comparators
- Interrupts generated when compare results change (Interrupt event condition is programmable)
- Supports triggers for break events and cycle-by-cycle control for EPWM
- Supports window compare mode and window latch mode

2.41 OP Amplifier (OPA)

2.41.1 Overview

This device is equipped with three operational amplifiers. Users can enable each of them individually, by their application purpose. One of these OP amplifier outputs is connected to ADC channel for measurement requirement. The OP amplifier circuit also can be used in the application of Programmable Gain Amplifier (PGA).

2.41.2 Features

- Analog input voltage range: 0~VDD.
- Supports up to 3 operator amplifiers.
- Supports to use Schmitt trigger buffer output for simple comparator function.
- Supports to Schmitt trigger buffer output interrupts.

2.42 Peripherals Interconnection

2.42.1 Overview

Some peripherals have interconnections which allow autonomous communication or synchronous action between peripherals without needing to involve the CPU. Peripherals interact without CPU saves CPU resources, reduces power consumption, operates with no software latency and fast responds.

2.42.2 Peripherals Interconnect Matrix Table

Source	Destination									
	BPWM	DAC	EADC	ECAP	EPWM	HIRC	IRCTRIM	RC48M	TIMERPWM	QEI
ACMP	-	-	-	-	3	-	-	-	3,6	
BOD	-	-	-	-	3	-	-	-	3	
BPWM	4	-	1	-	4	-	-	-	-	
Clock Fail	-	-	-	-	3	-	-	-	3	
CPU Lockup	-	-	-	-	3	-	-	-	3	
EADC	-	-	-	-	3	-	-	-	-	
EPWM	4	1	1	-	4	-	-	-	-	
IRCTRIM	-	-	-	-	-	2	-	2	-	
LIRC	-	-	-	-	-	-	-	-	6	
LXT	-	-	-	-	-	-	2	-	-	
QEI	-	-	-	8	-	-	-	-	-	
SRAM	-	-	-	-	3	-	-	-	3	
TIMERPWM	5	1	1	-	5	-	-	-	7	9
USB11Device	-	-	-	-	-	-	2	-	-	

Table 2.42-1: Peripherals Interconnect Matrix Table

2.42.3 Functional Description

2.42.3.1 From EPWM, TIMER to EADC/DAC

EPWM Trigger EADC Conversion
EPWM can be one of the EADC conversion trigger source.

EPWM Trigger DAC Conversion
EPWM can also be used to trigger DAC conversion.

BPWM Trigger EADC Conversion
BPWM can be one of the EADC conversion trigger source.

Timer Trigger EADC Conversion
Timer0 ~ Timer3 can be one of the EADC conversion trigger source. When timer counter value matches the timer compared value or when the TMx_EXT pin edge transition meets setting, timer will trigger the ADC to start the conversion.

Timer Trigger DAC Conversion

2.42.3.2 From LXT and USB 1.1 Device to HIRC TRIM & RC 48 MHz

Use LXT or USB Synchronous Mode to System Auto-trim HIRC Circuit
This chip supports auto-trim function: the HIRC trim (12 MHz RC oscillator) and RC 48 MHz oscillator, according to the accurate external 32.768 KHz crystal oscillator or internal USB synchronous mode, automatically gets accurate output frequency, 0.25 % deviation within all temperature ranges.

2.42.3.3 From ACMP, BOD, Clock Fail, SRAM Parity Error and CPU Lockup to EPWM/ TIMERPWM

EPWM Brake Source
EPWM brake source can be ACMP0/1_O output signal or EADC result monitor or several different system fail conditions include clock fail, Brown-out detect, and Core lockup and SRAM Parity Error. When system fault, EPWM brake signal generated, EPWM output will be set to protect the power switch controlled by EPWM.

TIMERPWM Brake Source
TIMERPWM brake source can be ACMP0/1_O output signal or several different system fail conditions include clock fail, Brown-out detect, and Core lockup and SRAM Parity Error. When system fault, EPWM brake signal generated, EPWM output will be set to protect the power switch controlled by EPWM.

2.42.3.4 From EPWM/ BPWM to EPWM/ BPWM

EPWM Synchronous Start Function
Select synchronous source from EPWM0 or EPWM1 or BPWM0 or BPWM1, and select EPWM channels. The chosen EPWM channels will start counting at the same time once the synchronous start function is enabled and CNTSEN(EPWM_SSTRG[0]) is set.

BPWM Synchronous Start Function
Select synchronous source from EPWM0 or EPWM1 or BPWM0 or BPWM1, and select BPWM channels. The chosen BPWM channels will start counting at the same time once the synchronous start function is enabled and CNTSEN(BPWM_SSTRG[0]) is set.

2.42.3.5 From TIMER to EPWM/BPWM

Timer Generates Trigger Pulses as EPWM External Clock Source

Timer0 ~ Timer3 can generates trigger pules as EPWM/BPWM external clock source.

2.42.3.6 From ACMP and LIRC to Timer Capture Function

Measure the Time Interval of ACMP0/1 Output Signal or LIRC Clock Speed

Sets the timer capture source from ACMP0/1 output signal or LIRC clock and measures the time interval of the signal by using timer capture function. Users can use the results of time interval to trim LIRC through software or to get the ACMP0/1 output pulse width.

2.42.3.7 From Timer0/2 to Timer1/3

Inter-Timer Trigger Capture Mode

Timer0/2 will be forced in event counting mode, counting with external event, and will generate an internal signal (INTR_TMR_TRG) to trigger Timer1/3 start or stop counting. The Timer1/3 will be forced in capture mode and start/stop trigger-counting by Timer0/2 counter status.

2.42.3.8 From QEI to ECAP

ECAP Input Noise Filter

The architecture of ECAP input noise filter is similar to that one used for QEI. With 6 sampling-rate options, it supports a wide range of filtering noise, the duration of filtered noise and the duration of the signal that is guaranteed to be sampled.

2.42.3.9 From TIMER to QEI

TIMER TIF Event to QEI

When QEI bit HOLDCNT(QEI_CTL[24]) set, the CNT(QEI_CNT[31:0]) content will be captured into QEI Counter Hold Register CNTHOLD(QEI_CNTHOLD[31:0]), the data will be held until the next HOLDCNT (QEI_CTL[24]) trigger comes. The bit HOLDCNT can be set by writing 1 to it or the rising edge of timers interrupt flags TIF (TIMERx_INTSTS[0]).

2.43 ESC (EtherCAT) Sub-system

2.43.1 Overview

The AX58200 implements a 2/3-port EtherCAT slave controller (ESC), licensed from Beckhoff Automation, with 9 Kbytes Process Data RAM, 8 Fieldbus Memory Management Units (FMMUs), 8 Sync-Managers and a 64-bit Distributed Clock.

Port 0 and 1 integrate embedded Ethernet PHYs, and port 2 is an optional MII interface which are multi-function pins shared with other interfaces (i.e. PWM, Hall, etc.). Packets are forwarded in the following order: **Port 0->EtherCAT Processing Unit->Port 1->Port 2**.

The AX58200 supports function register mirror from/to ESC memory space. The mirror registers located at process data memory address from 0x3000 to 0x33FF.

For detailed information about the EtherCAT technology, the EtherCAT core mechanisms, and major features, we refer to the official standard documentations and guidelines available from ETG (www.ethercat.org, ETG.1000), IEC (http://www.iec.ch, IEC61158, IEC61784-2, IEC 61800-7), and Beckhoff (http://www.beckhoff.de, technical specification) web sites.

The AX58200 requires a crystal (25MHz, ±25 PPM at room temperature) as the clock source. Internal PLL generates the 100MHz clock for EtherCAT Slave Controller (ESC) and also for other functions.

The AX58200 has three reset sources. First, during the VCCK power-on, the internal Power-On-Reset (POR) can generate a reset pulse to reset all the function blocks when the VCCK power pin rises to a certain threshold voltage level. The second reset is RSTn pin, which is to do the fundamental reset. And third, EtherCAT command reset, the EtherCAT master can send reset sequence to force AX58200 reset. AX58200 also supports a reset output RSTO polarity bootstrap configuration (RSTO_POL).

2.43.2 Features

- 2/3-port EtherCAT Slave Controller (ESC) with 2 Integrated Fast Ethernet PHYs
- Standard EtherCAT Slave Controller (ESC)
  - 8 Fieldbus Memory Management Units (FMMUs)
  - 8 Sync Managers
  - 64-bit distributed clock
  - 9K bytes RAM
- Integrated Fast Ethernet PHYs
  - Compliant with IEEE 802.3/802.3u 100BASE-TX/100BASE-FX
  - PHY loopback mode
  - Supports twisted pair crossover detection and auto-correction (HP Auto-MDIX)
  - Automatic polarity detection and correction
- 3rd Ethernet MII Port for Flexible EtherCAT Network Configurations
- SPI Slave Interface for PDI and Function Access
- 3-channel PWM Controller for simple Motion Control
- Step & Direction Controller for simple Motion Control
- Incremental and Hall Encoder Interface for simple Motion Control
- Emergency Stop Input
- Configurable Watchdog for Outputs and Inputs Monitoring
- IRQ Event Output
- SPI Master Interface for ADC/DAC application
- Supports I2C Master Interface

2.43.3 Block Diagram

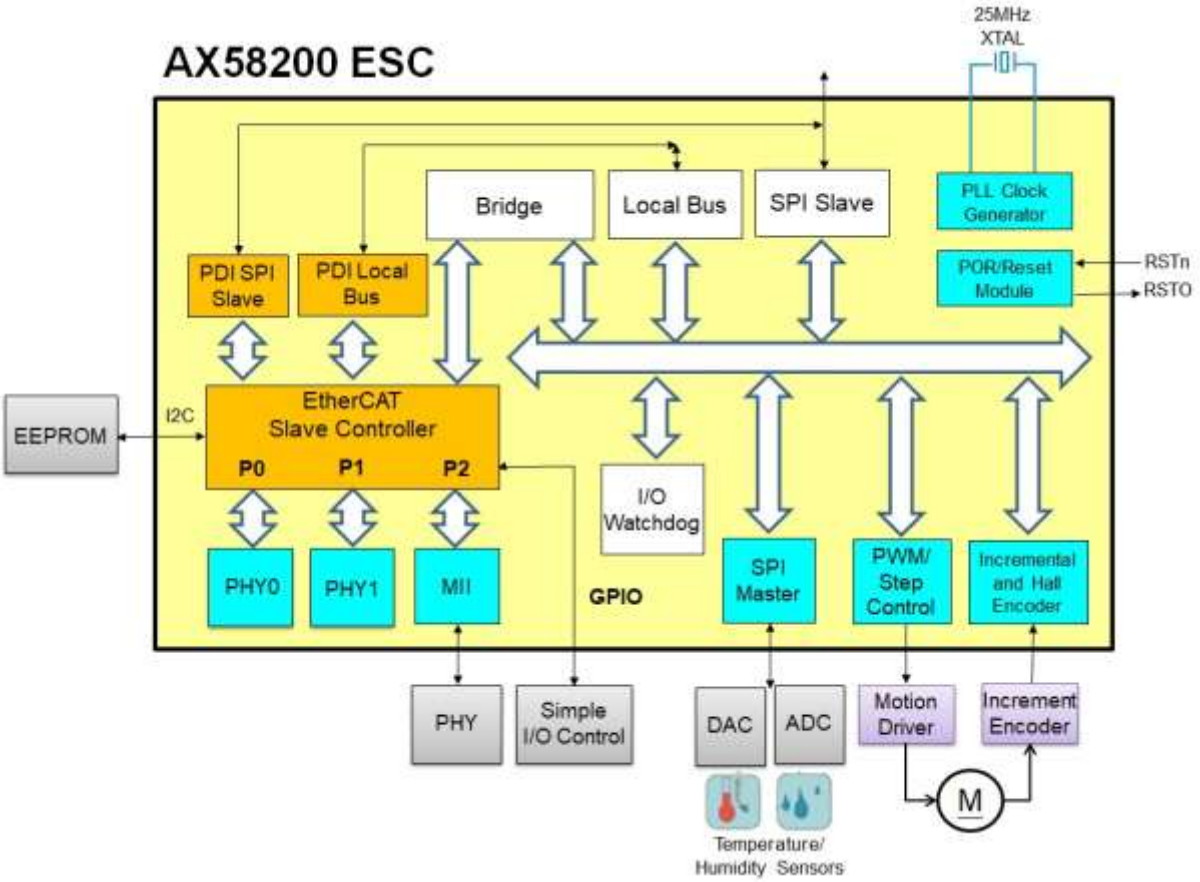


Figure 2.43-1: ESC Sub-system Block Diagram

2.43.4 ESC Configuration

2.43.4.1 Bootstrap Pins for Chip Configuration

The AX58200 supports five multi-function bootstrap pins (pin L1, L2, E9, J10 and J11) for five hardware configurations, i.e. external I^2C EEPROM size, ESC supported port number, RSTO polarity and integrated port 0/1 PHY media mode; and it also supports other three multi-function bootstrap pins (pin A9, H9, G11) for the configuration of port 2 MII signals. User needs to utilize an external resistor to pull up / down these bootstrap pins.

Pins	Signal Name	Description
L1	EEP_SIZE	I^2C EEPROM Size 0: 1 Kbit to 16Kbit 1: 32Kbit to 4Mbit
L2	3PORT_MODE	ESC port number 0: 2 ports mode 1: 3 ports mode
E9	RSTO_POL	RSTO Reset Output Polarity 0: Active Low 1: Active High
B10	PDI_EMU	Device emulation (0x0141.0) 0: Device status register is controlled by PDI 1: Device status register is identical to device control register
J10	P0_FIBER	Port 0 PHY media mode 0: Copper mode 1: Fiber mode
J11	P1_FIBER	Port 1 PHY Media mode 0: Copper mode 1: Fiber mode
A9	TX_SH [1]	Port 2 MII TXD Align position 2‘b00: Align with MCLK, 2’b01: Delay 1/4 phase with MCLK 2’b10: Delay 1/2 phase with MCLK 2’b11: Delay 3/4 phase with MCLK
H9	TX_SH [0]	
G11	LINK_POL	Port 2 MII LINK Polarity 0: Active Low 1: Active High

Table 2.43-1: ESC Bootstrap Pins Configuration

2.43.4.2 Hardware Configuration EEPROM (HWCFGEE)

The AX58200 I²C master controller supports the communication to external I²C devices and an I²C Hardware Configuration EEPROM Loader to support loading the EtherCAT Slave Information (ESI) from external I²C EEPROM during chip reset. The AX58200 supports I²C EEPROM with EEPROM size from 1 Kbit (128 bytes) to 4 Mbit (500Kbytes).

The AX58200 I²C Hardware Configuration EEPROM layout is shown in following table.

EEPROM Byte Offset	EEPROM Word Offset	Parameter	ESC Register Offset
ESC Configuration Area			
0x00	0x00	PDI Control	0x0140
0x01		ESC Configuration (bit 2 is also mapped to ESC register 0x0110.2)	0x0141
0x02	0x01	PDI Configuration	0x0150
0x03		Sync/Latch [1:0] Configuration	0x0151
0x05 - 0x04	0x02	Pulse Length of SyncSignals	0x0983 - 0x0982
0x07 - 0x06	0x03	Extended PDI Configuration	0x0153 - 0x0152
0x09 - 0x08	0x04	Configured Station Alias	0x0013 - 0x0012
0x0A	0x05	Host Interface Extend Setting and Drive Strength	
0x0B		Reserved, shall be zero	
0x0C	0x06	Reserved, shall be zero	
0x0D		Multi-Function Select and Drive Strength	
0x0F - 0x0E	0x07	Checksum	
0x13 - 0x10	0x09 – 0x08	Vendor ID	
0x17 - 0x14	0x0B – 0x0A	Product Code	
0x1B - 0x18	0x0D – 0x0C	Revision Number	
0x1F - 0x1C	0x0F – 0x0E	Serial Number	
0x27 - 0x20	0x13 – 0x10	Reserved	
Bootstrap Mailbox Config			
0x29 - 0x28	0x14	Bootstrap Receive Mailbox Offset	
0x2B - 0x2A	0x15	Bootstrap Receive Mailbox Size	
0x2D - 0x2C	0x16	Bootstrap Send Mailbox Offset	
0x2F - 0x2E	0x17	Bootstrap Send Mailbox Size	
Mailbox Sync Man Config			
0x31 - 0x30	0x18	Standard Receive Mailbox Offset	
0x33 - 0x32	0x19	Standard Receive Mailbox Size	
0x35 - 0x34	0x1A	Standard Send Mailbox Offset	
0x37 - 0x36	0x1B	Standard Send Mailbox Size	
0x39 - 0x38	0x1C	Mailbox Protocol	
0x3F - 0x3A	0x1F – 0x1D	Reserved	
0x7B - 0x40	0x3D – 0x20	Reserved	
0x7D - 0x7C	0x3E	Size	
0x7F - 0x7E	0x3F	Version	
ESC Category 1 (for AX58200 Bridge Access Configuration if used) *Note1			
0x81 ~ 0x80	0x40	Category 1 Type (Default: **0x0001**)	
0x83 ~ 0x82	0x41	Category 1 Data Size (words) (Default: **0x0021**)	
0x84	0x42	MCTLR Access Control	0x0580
0x85		PXCFGR Access Control	0x0581

EEPROM Byte Offset	EEPROM Word Offset	Parameter	ESC Register Offset
0x86	0x43	PTAPPR Access Control	0x0582
0x87		PTBPPR Access Control	0x0583
0x88	0x44	PPCR Access Control	0x0584
0x89		PBBMR Access Control	0x0585
0x8A	0x45	P1CTRLR Access Control	0x0586
0x8B		P1SHR Access Control	0x0587
0x8C	0x46	P1HPWR Access Control	0x0588
0x8D		P2CTRLR Access Control	0x0589
0x8E	0x47	P2SHR Access Control	0x058A
0x8F		P2HPWR Access Control	0x058B
0x90	0x48	P3CTRLR Access Control	0x058C
0x91		P3SHR Access Control	0x058D
0x92	0x49	P3HPWR Access Control	0x058E
0x93		SGTR Access Control	0x058F
0x94	0x4A	SHPWR Access Control	0x0590
0x95		TDLYR Access Control	0x0591
0x96	0x4B	STNR Access Control	0x0592
0x97		SCFGR Access Control	0x0593
0x98	0x4C	SCTRLR Access Control	0x0594
0x99		SCNTR Access Control	0x0595
0x9A	0x4D	ECNTVR Access Control	0x0596
0x9B		ECNSTR Access Control	0x0597
0x9C	0x4E	ELATR Access Control	0x0598
0x9D		EMODR Access Control	0x0599
0x9E	0x4F	ECLRR Access Control	0x059A
0x9F		HALSTR Access Control	0x059B
0xA0	0x50	WTR Access Control	0x059C
0xA1		WCFGR Access Control	0x059D
0xA2	0x51	WTPVCR Access Control	0x059E
0xA3		WMSPR Access Control	0x059F
0xA4	0x52	WMMR Access Control	0x05A0
0xA5		WOMR Access Control	0x05A1
0xA6	0x53	WOER Access Control	0x05A2
0xA7		WOPR Access Control	0x05A3
0xA8	0x54	WTPVR Access Control	0x05A4
0xA9		SPICFGR Access Control	0x05A5
0xAA	0x55	SPIBRR Access Control	0x05A6
0xAB		SPIDBSR Access Control	0x05A7
0xAC	0x56	SPIDTR Access Control	0x05A8
0xAD		SPIRPTR Access Control	0x05A9
0xAE	0x57	SPILTR Access Control	0x05AA
0xAF		SPIPRLR Access Control	0x05AB
0xB0	0x58	SPI01BCR Access Control	0x05AC
0xB1		SPI23BCR Access Control	0x05AD
0xB2	0x59	SPI45BCR Access Control	0x05AE
0xB3		SPI67BCR Access Control	0x05AF
0xB4	0x5A	SPI03SSR Access Control	0x05B0
0xB5		SPI47SSR Access Control	0x05B1

EEPROM Byte Offset	EEPROM Word Offset	Parameter	ESC Register Offset
0xB6	0x5B	SPIINTSR Access Control	0x05B2
0xB7		SPITSR Access Control	0x05B3
0xB8	0x5C	SPIPOSR Access Control	0x05B4
0xB9		SPI Data Status (SPIDSR and SPIDSMR) Access Control	0x05B5
0xBA	0x5D	SPIC0DR Access Control	0x05B6
0xBB		SPIC1DR Access Control	0x05B7
0xBC	0x5E	SPIC2DR Access Control	0x05B8
0xBD		SPIC3DR Access Control	0x05B9
0xBE	0x5F	SPIC4DR Access Control	0x05BA
0xBF		SPIC5DR Access Control	0x05BB
0xC0	0x60	SPIC6DR Access Control	0x05BC
0xC1		SPIC7DR Access Control	0x05BD
0xC2	0x61	SPIMCR Access Control	0x05BE
0xC3		INTCR Access Control	0x05BF
0xC4	0x62	INTSR Access Control	0x05C0
0xC5		Function Mirror Enable	0x05C1
Other ESC Categories Information (Subdivided in Categories)			
		…	
		Category Strings	
		Category Generals	
		Category FMMU	
		Category SyncManager	
		Category Tx - / RxPDO for each PDO	

Table 2.43-2: ESC I²C EEPROM Layout

Note 1: Reserved words or reserved bits of the ESC Configuration Area should be filled with 0.
Note 2: When (re-) configuring the EEPROM from an EtherCAT master system special care must be taken. Not every master allows writing a category 1 entry to the EEPROM. There are different ways to write this into the EEPROM for automatically loading access control configuration when AX58200 booting.
1. Use preprogrammed I²C EEPROM.
2. Use a different category, e.g., 2049, first. Then overwrite the upper byte with 0 with a single EEPROM byte writes.

The AX58200 HWCFGEE contents from offset 0x00 to 0x7F are mandatory, as well as the general category (at least the minimum I2C EEPROM size is 2Kbit, and for the complex devices with many categories should be equipped with 32 Kbit EEPROMs or larger one). The ESC Configuration Area is used for AX58200 hardware configuration. All other areas are used by the EtherCAT master or the local application.

The ESC Configuration Area (EEPROM offset 0x00 to 0x0F) is automatically read by AX58200 after power-on or reset. It contains the PDI configuration, Distributed Clocks settings, and Configured Station Alias. The consistency of the ESC Configuration Area data is secured with a checksum.

The EtherCAT Master can invoke reloading the EEPROM contents. In this case, the Configured Station Alias register 0x0012:0x0013 and ESC Configuration register bits 0x0141 [1,4,5,6,7] (enhanced link detection) are not transferred into the registers. They are only transferred at the initial EEPROM loading after power-on or reset.

To use AX58200 bridge functionalities, users should define the Bridger Access Configuration parameters in the first category located at EEPROM offset 0x80. The Category Type must be 0x0001and the Category Data Size must be 0x0020 so the AX58200 will automatically load the EEPROM Bridger Access Configuration parameters into the Bridge Access Configuration registers memory area starting at 0x0580 after power-on or reset.

2.43.4.3 EEPROM Contents Detailed Descriptions

PDI Control (0x00)

Bit	Description
7:0	PDI Control [7:0] 0x00: Interface deactivated (no PDI) 0x04: Digital I/O 0x05: SPI Slave 0x08: 16-bit Asynchronous Local Bus 0x09: 8-bit Asynchronous Local Bus Others: reserved

ESC Configuration (0x01)

Bit	Description
0	Device emulation enables (control of AL status)
1	Enhanced Link detection all ports
3:2	Reserved
4	Enhanced Link port 0
5	Enhanced Link port 1
6	Enhanced Link port 2
7	Reserved

PDI Configuration (0x02)

Digital I/O

Bit	Description
0	OUTVALID polarity
1	OUTVALID mode
2	Unidirectional/Bidirectional mode
3	Watchdog behavior
5:4	Input DATA is sampled
7:6	Output DATA is updated

SPI Slave

Bit	Description
1:0	SPI mode
3:2	SPI_IRQ output driver/polarity
4	SPI_SEL polarity
5	Data Out sample mode
7:6	Reserved

Asynchronous Local Bus

Bit	Description
1:0	BUSY/RDY driver/polarity
3:2	IRQ driver/polarity
4	BHE/Byte Enable polarity
7:5	Reserved

Sync/Latch[1:0] Configuration (0x03)

Bit	Description
1:0	SYNC0 output driver/polarity
2	SYNC0/LATCH0 configuration
3	SYNC0 mapped to AL Event Request
5:4	SYNC1 output driver/polarity
6	SYNC1/LATCH1 configuration
7	SYNC1 mapped to AL Event Request

Pulse Length SyncSignals (0x05 - 0x04)

Bit	Description
15:0	Pulse length of SyncSignal

Extended PDI Configuration (0x07 - 0x06)

Digital I/O / SPI Slave (for GPIO)

Bit	Description
0	Digital I/O or GPIO Digital I/O or GPIO are configured in pairs (1:0) as inputs or outputs: 0: Input 1: Output
1	3:2 pair (0: Input, 1: Output)
2	5:4 pair (0: Input, 1: Output)
3	7:6 pair (0: Input, 1: Output)
4	9:8 pair (0: Input, 1: Output)
5	11:10 pair (0: Input, 1: Output)
6	13:12 pair (0: Input, 1: Output)
7	15:14 pair (0: Input, 1: Output)
8	17:16 pair (0: Input, 1: Output)
9	19:18 pair (0: Input, 1: Output)
10	21:20 pair (0: Input, 1: Output)
11	23:22 pair (0: Input, 1: Output)
12	25:24 pair (0: Input, 1: Output)
13	27:26 pair (0: Input, 1: Output)
14	29:28 pair (0: Input, 1: Output)
15	31:30 pair (0: Input, 1: Output)

Asynchronous Local Bus

Bit	Description
0	Read BUSY delay
1	Perform internal write
10:2	Reserved
11	23:22 pair (data bus 8-bit width only) (0: Input, 1: Output)
12	25:24 pair (data bus 8-bit width only) (0: Input, 1: Output)
13	27:26 pair (data bus 8-bit width only) (0: Input, 1: Output)
14	29:28 pair (data bus 8-bit width only) (0: Input, 1: Output)
15	31:30 pair (data bus 8-bit width only) (0: Input, 1: Output)

Configured Station Alias (0x09 - 0x08)

Bit	Description
15:0	Alias Address used for node addressing

Host Interface Extend Setting and Drive Strength (0x0A)

Digital I/O

Bit	Description
4:0	Reserved
5	Control Driving Select: 0: 4mA 1: 8mA
6	IO [9:0] Driving Select: 0: 4mA 1: 8mA
7	IO [15:10] Driving Select: 0: 4mA 1: 8mA

SPI Slave / Asynchronous Local Bus

Bit	Description
3:0	Interrupt Edge Pulse Length (INTP_LEN) Interrupt Edge Pulse = (INTP_LEN+1) * 100ns
4	The trigger type of interrupt signal, SINT / LINT 0: Level trigger. 1: Edge trigger.
5	Control Driving Select: 0: 4mA 1: 8mA
6	IO [9:0] Driving Select: 0: 4mA 1: 8mA
7	IO [15:10] Driving Select: 0: 4mA 1: 8mA

Multi-Function Select and Drive Strength (0x0D)

Bit	Description
0	IO [9:0] select: 0: IO [9:0] 1: MTRG, MDRLD, MSS [3:0], MINT, MMISO, MMOSI, MSCLK, Note: in Local Bus mode this bit no function
1	IO [15:10] (SPI slave separates) select: 0: IO [15:10] 1: IO [15:14], FMOSI, FSCLK, FMISO, SFINT Note: in Local Bus mode this bit no function
2	IO [21:16] select: 0: IO [21:16] 1: PULA, PULB, PULZ, PULZ, PULAB, IO [16] Note: in Local Bus mode this bit no function
3	IO [25:22] select: 0: IO [25:22] 1: PWM2L, PWM2H, PWM3L, PWM3H Note: in Local Bus 16 bits mode this bit no function
4	IO [28:26] select: 0: IO [28:26] 1: EM, PWM1L, PWM1H Note: in Local Bus 16 bits mode this bit no function
5	IO [31:29] select: 0: IO [31:29] 1: ENCZ, ENCB, ENCA Note: in Local Bus 16 bits mode this bit no function

6	IO [21:16] Driving Select: 0: 4mA 1: 8mA
7	IO [31:22] Driving Select: 0: 4mA 1: 8mA

Note: When MII port 2 enable, the IO [31:16] pins are forced to MII port 2

Checksum (0x0F - 0x0E)

Bit	Description
15:0	Checksum Low byte contains remainder of division of EEPROM offset 0x00 to 0x0D as unsigned number divided by the polynomial X^8+X^2+X+1 (initial value 0xFF) For debugging purposes, it is possible to disable the checksum validation with a checksum value of 0x88A4. **Note that NEVER use this for production!**

Category 1 Type (0x81 - 0x80)

Bit	Description
15:0	Category 1 Type MUST be 0x0001

Category 1 Data Size (0x83 - 0x82)

Bit	Description
15:0	Category 1 Data Size (words) MUST be 0x0021

MCTLR Access Control (0x84)

Bit	Description
3:0	Sync. Source Select 0x0: Always triggered 0x1: Start Of Frame (SOF) 0x2: End Of Frame (EOF) 0x3: SYNC0 signal 0x4: LATCH0 signal 0x5: SYNC1 signal 0x6: LATCH1 signal 0x7: After write access 0x8: Trigger when data value changes 0x9: PDI Chip Select Assert 0xA: PDI Chip Select De-assert 0xB: FUNC Chip Select Assert 0xC: FUNC Chip Select De-assert 0xD: Trigger at start of MFC PWM cycle Others: Always triggered
4	ESC Access Enable 0: Writeable with Function Host Interface 1: Writeable with ESC
7:5	Reserved

The Bit Definitions of the other parameters from EEPROM offset 0x85 to 0xC4 are the same as the Bit Definitions of EEPROM offset 0x84.

Function mirror enable (0xC5)

Bit	Description
0	PWM function register mirror: 0: Disable PWM function register mirror 1: Enable PWM function register mirror
1	ENC function register mirror: 0: Disable ENC function register mirror 1: Enable ENC function register mirror
2	SPI Master function register mirror: 0: Disable SPI Master function register mirror 1: Enable SPI Master function register mirror
3	IO Watchdog function register mirror: 0: Disable IO Watchdog function register mirror 1: Enable IO Watchdog function register mirror
7:4	Reserved

2.43.5 Memory Map

This section introduces the memory mapping in AX58200. AX58200 provides SPI and Local Bus slave interfaces for both ESC PDI and Function to access the internal registers. Section 2.43.5.1 introduces the ESC memory map which can be accessed by PDI SPI or Local bus interface ,and section 2.43.5.2 introduces the Function register map which can be accessed by Function SPI or Local Bus interface. Due to the Function registers can be accessed by PDI interface and EtherCAT Master directly. So, section 2.43.5.3 introduces the relationship between Function and ESC PDI through the Bridge function.

2.43.5.1 ESC Memory Map

ESC Address	Length (Bytes)	Description
ESC Information		
0x0000	1	Type
0x0001	1	Revision
0x0002	2	Build
0x0004	1	FMMUs supported
0x0005	1	SyncManagers supported
0x0006	1	RAM Size
0x0007	1	Port Descriptor
0x0008	2	ESC Features supported
Station Address		
0x0010	2	Configured Station Address
0x0012	2	Configured Station Alias
Write Protection		
0x0020	1	Write Register Enable
0x0021	1	Write Register Protection
0x0030	1	ESC Write Enable
0x0031	1	ESC Write Protection
Data Link Layer		
0x0040	1	ESC Reset ECAT
0x0041	1	ESC Reset PDI
0x0100	4	ESC DL Control
0x0108	2	Physical Read/Write Offset
0x0110	2	ESC DL Status
Application Layer		
0x0120	2	AL Control
0x0130	2	AL Status
0x0134	2	AL Status Code
0x0138	1	RUN LED Override
0x0139	1	ERR LED Override
PDI		
0x0140	1	PDI Control
0x0141	1	ESC Configuration
0x0150	1	PDI Configuration
0x0151	1	Sync/Latch PDI Configuration
0x0152	2	Extended PDI Configuration
Interrupts		
0x0200	2	ECAT Event Mask
0x0204	4	AL Event Mask
0x0210	2	ECAT Event Request
0x0220	4	AL Event Request
Error Counters		

0x0300	4x2	RX Error Counter [3:0]
0x0308	4x1	Forwarded RX Error counter [3:0]
0x030C	1	ECAT Processing Unit Error Counter
0x030D	1	PDI Error Counter
0x030E	1	PDI Error Code
0x0310	4x1	Lost Link Counter [3:0]
Watchdogs		
0x0400	2	Watchdog Divider
0x0410	2	Watchdog Time PDI
0x0420	2	Watchdog Time Process Data
0x0440	2	Watchdog Status Process Data
0x0442	1	Watchdog Counter Process Data
0x0443	1	Watchdog Counter PDI
I^2C EEPROM Interface		
0x0500	1	EEPROM Configuration
0x0501	1	EEPROM PDI Access State
0x0502	2	EEPROM Control/Status
0x0504	4	EEPROM Address
0x0508	4	EEPROM Data
MII Management Interface		
0x0510	2	MII Management Control/Status
0x0512	1	PHY Address
0x0513	1	PHY Register Address
0x0514	2	PHY Data
0x0516	1	MII Management ECAT Access State
0x0517	1	MII Management PDI Access State
0x0518	4	PHY Port Status
Bridge Access Configuration		
0x0580	1	MCTLR Access Control Register
0x0581	1	PXCFGR Access Control Register
0x0582	1	PTAPPR Access Control Register
0x0583	1	PTBPPR Access Control Register
0x0584	1	PPCR Access Control Register
0x0585	1	PBBMR Access Control Register
0x0586	1	P1CTRLR Access Control Register
0x0587	1	P1SHR Access Control Register
0x0588	1	P1HPWR Access Control Register
0x0589	1	P2CTRLR Access Control Register
0x058A	1	P2SHR Access Control Register
0x058B	1	P2HPWR Access Control Register
0x058C	1	P3CTRLR Access Control Register
0x058D	1	P3SHR Access Control Register
0x058E	1	P3HPWR Access Control Register
0x058F	1	Step Gap Time Access Control Register
0x0590	1	SHPWR Access Control Register
0x0591	1	TDLYR Access Control Register
0x0592	1	Step Target Number Access Control Register
0x0593	1	SCFGR Access Control Register
0x0594	1	SCTRLR Access Control Register
0x0595	1	Step Counter Content Access Control Register
0x0596	1	Encoder Counter Value Access Control Register
0x0597	1	Encoder Constant Access Control Register
0x0598	1	Encoder Latched Access Control Register

0x0599	1	EMODR Access Control Register
0x059A	1	ECLRR Access Control Register
0x059B	1	HALSTR Access Control Register
0x059C	1	Watchdog Timer Access Control Register
0x059D	1	WCFGR Access Control Register
0x059E	1	WTPVCR Access Control Register
0x059F	1	Watchdog monitored Polarity Access Control Register
0x05A0	1	Watchdog monitored Mask Access Control Register
0x05A1	1	Watchdog Output Mask Access Control Register
0x05A2	1	Watchdog Output Enable Access Control Register
0x05A3	1	Watchdog Output Polarity Access Control Register
0x05A4	1	Watchdog Timer Peak value Access Control Register
0x05A5	1	SPICFGR Access Control Register
0x05A6	1	SPIBRR Access Control Register
0x05A7	1	SPIDBSR Access Control Register
0x05A8	1	SPIDTR Access Control Register
0x05A9	1	SPIRPTR Access Control Register
0x05AA	1	SPILTR Access Control Register
0x05AB	1	SPIPRLR Access Control Register
0x05AC	1	SPI01BCR Access Control Register
0x05AD	1	SPI23BCR Access Control Register
0x05AE	1	SPI45BCR Access Control Register
0x05AF	1	SPI67BCR Access Control Register
0x05B0	1	SPI03SSR Access Control Register
0x05B1	1	SPI47SSR Access Control Register
0x05B2	1	SPINTSR Access Control Register
0x05B3	1	SPITSR Access Control Register
0x05B4	1	SPIPOSR Access Control Register
0x05B5	1	SPI Data Status (SPIDSR and SPIDSMR) Access Control Register
0x05B6	1	SPIC0DR Access Control Register
0x05B7	1	SPIC1DR Access Control Register
0x05B8	1	SPIC2DR Access Control Register
0x05B9	1	SPIC3DR Access Control Register
0x05BA	1	SPIC4DR Access Control Register
0x05BB	1	SPIC5DR Access Control Register
0x05BC	1	SPIC6DR Access Control Register
0x05BD	1	SPIC7DR Access Control Register
0x05BE	1	SPIMCR Access Control Register
0x05BF	1	INTCR Access Control Register
0x05C0	1	INTSR Access Control Register
0x05C1	1	Function Mirror Enable Register
0x0600:0x067F	**FMMU[7:0]**	
+0x0	4	Logical Start Address
+0x4	2	Length
+0x6	1	Logical Start bit
+0x7	1	Logical Stop bit
+0x8	2	Physical Start Address
+0xA	1	Physical Start bit
+0xB	1	Type
+0xC	1	Activate
+0xD	3	Reserved
0x0800:0x083F	**SyncManager[7:0]**	
+0x0	2	Physical Start Address

+0x2	2	Length
+0x4	1	Control Register
+0x5	1	Status Register
+0x6	1	Activate
+0x7	1	PDI Control
0x0900:0x09FF	**Distributed Clocks (DC)**	
DC – Receive Times		
0x0900	4	Receive Time Port 0
0x0904	4	Receive Time Port 1
0x0908	4	Receive Time Port 2
0x090C	4	Receive Time Port 3
DC – Time Loop Control Unit		
0x0910	4(W)/8(R)	System Time
0x0918	8	Receive Time ECAT Processing Unit
0x0920	8	System Time Offset
0x0928	4	System Time Delay
0x092C	4	System Time Difference
0x0930	2	Speed Counter Start
0x0932	2	Speed Counter Diff
0x0934	1	System Time Difference Filter Depth
0x0935	1	Speed Counter Filter Depth
DC – Cyclic Unit Control		
0x0980	1	Cyclic Unit Control
DC – SYNC Out Unit		
0x0981	1	Activation
0x0982	2	Pulse Length of SyncSignals
0x0984	1	Activation Status
0x098E	1	SYNC0 Status
0x098F	1	SYNC1 Status
0x0990	8	Start Time Cyclic Operation/Next SYNC0 Pulse
0x0998	8	Next SYNC1 Pulse
0x09A0	4	SYNC0 Cycle Time
0x09A4	4	SYNC1 Cycle Time
DC – Latch In Unit		
0x09A8	1	Latch0 Control
0x09A9	1	Latch1 Control
0x09AE	1	Latch0 Status
0x09AF	1	Latch1 Status
0x09B0	8	Latch0 Time Positive Edge
0x09B8	8	Latch0 Time Negative Edge
0x09C0	8	Latch1 Time Positive Edge
0x09C8	8	Latch1 Time Negative Edge
DC – SyncManager Event Times		
0x09F0	4	EtherCAT Buffer Change Event Time
0x09F8	4	PDI Buffer Start Event Time
0x09FC	4	PDI Buffer Change Event Time
ESC specific		
0x0E00	8	Product ID
0x0E08	8	Vendor ID
Digital Input/Output		
0x0F00	4	Digital I/O Output Data
0x0F10	4	General Purpose Outputs

0x0F18	4	General Purpose Inputs
User RAM/Extended ESC features		
0x0F80	128	User RAM/Extended ESC Features
Process Data RAM		
0x1000	4	Digital I/O Input Data
0x1000	8KB	Process Data RAM
Function Register Mirror		
Write / Read		
0x3000	2	Motor Control Register
0x3002	2	PWM Pulse X Configure Register
0x3004	2	PWM Trigger A Pulse Position Register
0x3006	2	PWM Trigger B Pulse Position Register
0x3008	2	PWM Period Cycle Register
0x300A	2	PWM Pulse Break Before Make Register
0x300C	2	PWM1Control Register
0x300E	2	PWM1 Counter Shift Register
0x3010	2	PWM1 High Pulse Width Register
0x3012	2	PWM2 Control Register
0x3014	2	PWM2 Shift Register
0x3016	2	PWM2 High Pulse Width Register
0x3018	2	PWM3 Control Register
0x301A	2	PWM3 Counter Shift Register
0x301C	2	PWM3 High Pulse Width Register
0x3020	4	Step Gap Time Register
0x3024	2	Step High Pulse Width Register
0x3026	2	Direction Transform Delay Step Register
0x3028	4	Step Target Number Register
0x302C	2	Step Configure Register
0x302E	2	Step Control Register
0x3040	4	Encoder Counter Value Register
0x3044	4	Encoder Constant Register
0x304C	2	Encoder Mode configuration Register
0x304E	2	Encoder Clear Register
0x3060	4	Watchdog Timer Register
0x3064	2	Watchdog Control Register
0x3066	2	Watchdog Timer Peak Value Clear Register
0x3068	4	Watchdog Monitored Signals Polarity Register
0x306C	4	Watchdog Monitored Signals Mask Register
0x3070	4	Watchdog Output Mask Register
0x3074	4	Watchdog Output Enable Register
0x3078	4	Watchdog Output Polarity Register
0x3080	2	SPI Configure Register
0x3082	2	SPI Baud Rate Register
0x3084	2	SPI Delay Byte and SS Register
0x3086	2	SPI Delay Transfer Register
0x3088	2	SPI RDY / Pulse Time Register
0x308A	2	SPI LDAC Time Register
0x308C	2	SPI Pulse/ RDY/ LDAC Register
0x3090	2	SPI 0/1 Byte Count Register
0x3092	2	SPI 2/3 Byte Count Register
0x3094	2	SPI 4/5 Byte Count Register
0x3096	2	SPI 6/7 Byte Count Register
0x3098	2	SPI 0/1/2/3 slave Select Register
0x309A	2	SPI 4/5/6/7 slave Select Register

0x30B0	8	SPI Channel 0 Data Register
0x30B8	8	SPI Channel 1 Data Register
0x30C0	8	SPI Channel 2 Data Register
0x30C8	8	SPI Channel 3 Data Register
0x30D0	8	SPI Channel 4 Data Register
0x30D8	8	SPI Channel 5 Data Register
0x30E0	8	SPI Channel 6 Data Register
0x30E8	8	SPI Channel 7 Data Register
0x30F2	2	SPI Master Control Register
0x3100	2	Interrupt Configure Register
0x3102	2	Interrupt Status Register
Read Only		
0x3230	4	Step Counter Content Register
0x3248	4	Encoder Latched Register
0x3250	2	Hall State Register
0x327C	4	Watchdog Timer Peak Value Register
0x32A8	2	SPI Interrupt Status Register
0x32AA	2	SPI Timeout Status Register
0x32AC	2	SPI Pulse Overrun Status Register
0x32AE	2	SPI Data Status Register
0x32B0	8	SPI Channel 0 Data Register
0x32B8	8	SPI Channel 1 Data Register
0x32C0	8	SPI Channel 2 Data Register
0x32C8	8	SPI Channel 3 Data Register
0x32D0	8	SPI Channel 4 Data Register
0x32D8	8	SPI Channel 5 Data Register
0x32E0	8	SPI Channel 6 Data Register
0x32E8	8	SPI Channel 7 Data Register
0x32F0	2	SPI Data Status Mirror Register

Table 2.43-3: ESC Memory Map

2.43.5.2 Function Register Map

Address Offset	Name	Description
0x000	MCTLR	Motor Control Register
0x002	PXCFGR	PWM Pulse X Configure Register
0x004	PTAPPR	PWM Trigger A Pulse Position Register
0x006	PTBPPR	PWM Trigger B Pulse Position Register
0x008	PPCR	PWM Period Cycle Register
0x00A	PBBMR	PWM Pulse Break Before Make Register
0x00C	P1CTRLR	PWM1Control Register
0x00E	P1SHR	PWM1 Counter Shift Register
0x010	P1HPWR	PWM1 High Pulse Width Register
0x012	P2CTRLR	PWM2 Control Register
0x014	P2SHR	PWM2 Shift Register
0x016	P2HPWR	PWM2 High Pulse Width Register
0x018	P3CTRLR	PWM3 Control Register
0x01A	P3SHR	PWM3 Counter Shift Register
0x01C	P3HPWR	PWM3 High Pulse Width Register
0x020	SGTLR	Step Gap Time Low Register
0x022	SGTHR	Step Gap Time High Register
0x024	SHPWR	Step High Pulse Width Register
0x026	TDLYR	direction Transform Delay step Register
0x028	STNLR	Step Target Number Low Word Register
0x02A	STNHR	Step Target Number High Word Register
0x02C	SCFGR	Step Configure Register
0x02E	SCTRLR	Step Control Register
0x030	SCNTLR	Step Counter Content Low Register
0x032	SCNTHR	Step Counter Content High Register
0x040	ECNTVLR	Encoder Counter value Low Register
0x042	ECNTVHR	Encoder Counter value High Register
0x044	ECNSTLR	Encoder Constant Low Register
0x046	ECNSTHR	Encoder Constant High Register
0x048	ELATLR	Encoder Latched Low Register
0x04A	ELATHR	Encoder Latched High Register
0x04C	EMODR	Encoder Mode Configuration Register
0x04E	ECLRR	Encoder Clear Register
0x050	HALSTR	Hall State Register
0x060	WTLR	Watchdog Timer Low Register
0x062	WTHR	Watchdog Timer High Register
0x064	WCFGR	Watchdog Configure Register
0x066	WTPVCR	Watchdog Timer Peak Value Clear Register
0x068	WMPLR	Watchdog Monitored Polarity Low Register
0x06A	WMPHR	Watchdog Monitored Polarity High Register
0x06C	WMMLR	Watchdog Monitored Mask Low Register
0x06E	WMMHR	Watchdog Monitored Mask High Register
0x070	WOMLR	Watchdog Output Mask Low Register
0x072	WOMHR	Watchdog Output Mask High Register
0x074	WOELR	Watchdog Output Enable Low Register
0x076	WOEHR	Watchdog Output Enable High Register
0x078	WOPLR	Watchdog Output Polarity Low Register
0x07A	WOPHR	Watchdog Output Polarity High Register
0x07C	WTPVLR	Watchdog Timer Peak Value Low Register
0x07E	WTPVHR	Watchdog Timer Peak Value High Register
0x080	SPICFGR	SPI Configure Register
0x082	SPIBRR	SPI Baud Rate Register
0x084	SPIDBSR	SPI Delay Byte and SS Register

0x086	SPIDTR	SPI Delay Transfer Register
0x088	SPIRPTR	SPI RDY / Pulse Time Register
0x08A	SPILTR	SPI LDAC Time Register
0x08C	SPIPRLR	SPI Pulse/ RDY/ LDAC Register
0x090	SPI01BCR	SPI 0/1 Byte Count Register
0x092	SPI23BCR	SPI 2/3 Byte Count Register
0x094	SPI45BCR	SPI 4/5 Byte Count Register
0x096	SPI67BCR	SPI 6/7 Byte Count Register
0x098	SPI03SSR	SPI 0/1/2/3 slave Select Register
0x09A	SPI47SSR	SPI 4/5/6/7 slave Select Register
0x0A8	SPINTSR	SPI Interrupt Status Register
0x0AA	SPITSR	SPI Timeout Status Register
0x0AC	SPIPOSR	SPI Pulse Overrun Status Register
0x0AE	SPIDSR	SPI Data Status Register
0x0B0	SPIC0DR	SPI Channel 0 Data Register
0x0B8	SPIC1DR	SPI Channel 1 Data Register
0x0C0	SPIC2DR	SPI Channel 2 Data Register
0x0C8	SPIC3DR	SPI Channel 3 Data Register
0x0D0	SPIC4DR	SPI Channel 4 Data Register
0x0D8	SPIC5DR	SPI Channel 5 Data Register
0x0E0	SPIC6DR	SPI Channel 6 Data Register
0x0E8	SPIC7DR	SPI Channel 7 Data Register
0x0F0	SPIDSMR	SPI Data Status Mirror Register
0x0F2	SPIMCR	SPI Master Control Register
0x100	INTCR	Interrupt Configure Register
0x102	INTSR	Interrupt Status Register
0x104	ESTOR	ESC State Override register
0x106	HSTSR	Host interface Status Register
Others	Reserved	Reserved

Table 2.43-4: ESC Function Register Map

2.43.5.3 Memory Map between ESC Memory and Function Registers

Function Address	ESC Address		Name	Description
	R/W	RO		
0x000	0x3000	-	MCTLR	Motor Control Register
0x002	0x3002	-	PXCFGR	PWM Pulse X Configure Register
0x004	0x3004	-	PTAPPR	PWM Trigger A Pulse Position Register
0x006	0x3006	-	PTBPPR	PWM Trigger B Pulse Position Register
0x008	0x3008	-	PPCR	PWM Period Cycle Register
0x00A	0x300A	-	PBBMR	PWM Pulse Break Before Make Register
0x00C	0x300C	-	P1CTRLR	PWM1Control Register
0x00E	0x300E	-	P1SHR	PWM1 Counter Shift Register
0x010	0x3010	-	P1HPWR	PWM1 High Pulse Width Register
0x012	0x3012	-	P2CTRLR	PWM2 Control Register
0x014	0x3014	-	P2SHR	PWM2 Shift Register
0x016	0x3016	-	P2HPWR	PWM2 High Pulse Width Register
0x018	0x3018	-	P3CTRLR	PWM3 Control Register
0x01A	0x301A	-	P3SHR	PWM3 Counter Shift Register
0x01C	0x301C	-	P3HPWR	PWM3 High Pulse Width Register
0x020	0x3020	-	SGTLR	Step Gap Time Low Register
0x022			SGTHR	Step Gap Time High Register
0x024	0x3024	-	SHPWR	Step High Pulse Width Register
0x026	0x3026	-	TDLYR	direction Transform Delay step Register
0x028	0x3028	-	STNLR	Step Target Number Low Word Register
0x02A			STNHR	Step Target Number High Word Register
0x02C	0x302C	-	SCFGR	Step Configure Register
0x02E	0x302E	-	SCTRLR	Step Control Register
0x030	-	0x3230	SCNTLR	Step Counter Content Low Register
0x032			SCNTHR	Step Counter Content High Register
0x040	0x3040	-	ECNTVLR	Encoder Counter value Low Register
0x042			ECNTVHR	Encoder Counter value High Register
0x044	0x3044	-	ECNSTLR	Encoder Constant Low Register
0x046			ECNSTHR	Encoder Constant High Register
0x048	-	0x3248	ELATLR	Encoder Latched Low Register
0x04A			ELATHR	Encoder Latched High Register
0x04C	0x304C	-	EMODR	Encoder Mode Configuration Register
0x04E	0x304E	-	ECLRR	Encoder Clear Register
0x050	-	0x3250	HALSTR	Hall State Register
0x060	0x3060	-	WTLR	Watchdog Timer Low Register
0x062			WTHR	Watchdog Timer High Register
0x064	0x3064	-	WCFGR	Watchdog Configure Register
0x066	0x3066	-	WTPVCR	Watchdog Timer Peak Value Clear Register
0x068	0x3068	-	WMPLR	Watchdog Monitored Polarity Low Register
0x06A			WMPHR	Watchdog Monitored Polarity High Register
0x06C	0x306C	-	WMMLR	Watchdog Monitored Mask Low Register
0x06E			WMMHR	Watchdog Monitored Mask High Register
0x070	0x3070	-	WOMLR	Watchdog Output Mask Low Register
0x072			WOMHR	Watchdog Output Mask High Register
0x074	0x3074	-	WOELR	Watchdog Output Enable Low Register
0x076			WOEHR	Watchdog Output Enable High Register
0x078	0x3078	-	WOPLR	Watchdog Output Polarity Low Register
0x07A			WOPHR	Watchdog Output Polarity High Register
0x07C	-	0x327C	WTPVLR	Watchdog Timer Peak Value Low Register
0x07E			WTPVHR	Watchdog Timer Peak Value High Register
0x080	0x3080	-	SPICFGR	SPI Configure Register
0x082	0x3082	-	SPIBRR	SPI Baud Rate Register
0x084	0x3084	-	SPIDBSR	SPI Delay Byte and SS Register

0x086	0x3086	-	SPIDTR	SPI Delay Transfer Register
0x088	0x3088	-	SPIRPTR	SPI RDY / Pulse Time Register
0x08A	0x308A	-	SPILTR	SPI LDAC Time Register
0x08C	0x308C	-	SPIPRLR	SPI Pulse/ RDY/ LDAC Register
0x090	0x3090	-	SPI01BCR	SPI 0/1 Byte Count Register
0x092	0x3092	-	SPI23BCR	SPI 2/3 Byte Count Register
0x094	0x3094	-	SPI45BCR	SPI 4/5 Byte Count Register
0x096	0x3096	-	SPI67BCR	SPI 6/7 Byte Count Register
0x098	0x3098	-	SPI03SSR	SPI 0/1/2/3 slave Select Register
0x09A	0x309A	-	SPI47SSR	SPI 4/5/6/7 slave Select Register
0x0A8	-	0x32A8	SPINTSR	SPI Interrupt Status Register
0x0AA	-	0x32AA	SPITSR	SPI Timeout Status Register
0x0AC	-	0x32AC	SPIPOSR	SPI Pulse Overrun Status Register
0x0AE	-	0x32AE	SPIDSR	SPI Data Status Register
0x0B0	0x30B0	0x32B0	SPIC0DR	SPI Channel 0 Data Register
0x0B8	0x30B8	0x32B8	SPIC1DR	SPI Channel 1 Data Register
0x0C0	0x30C0	0x32C0	SPIC2DR	SPI Channel 2 Data Register
0x0C8	0x30C8	0x32C8	SPIC3DR	SPI Channel 3 Data Register
0x0D0	0x30D0	0x32D0	SPIC4DR	SPI Channel 4 Data Register
0x0D8	0x30D8	0x32D8	SPIC5DR	SPI Channel 5 Data Register
0x0E0	0x30E0	0x32E0	SPIC6DR	SPI Channel 6 Data Register
0x0E8	0x30E8	0x32E8	SPIC7DR	SPI Channel 7 Data Register
0x0F0	-	0x32F0	SPIDSMR	SPI Data Status Mirror Register
0x0F2	0x30F2	-	SPIMCR	SPI Master Control Register
0x100	0x3100	-	INTCR	Interrupt Configure Register
0x102	0x3102	-	INTSR	Interrupt Status Register

Table 2.43-5: ESC Memory and Function Registers Mirror Mapping Table

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DD}, AV_{DD}	DC Power Supply and Analog Voltage	- 0.3 to 4	V
V_{DDIO}	V_{DDIO} Power Supply Voltage	- 0.3 to 4	V
VCC3IO, VCC33A	Power supply of 3.3V I/O for ESC sub-system and Ethernet PHY	- 0.3 to 4	V
VCCK	Digital core power supply for ESC sub-system	- 0.5 to 1.6	V
VCC12A_PLL	Analog power supply for PLL for ESC sub-system	- 0.5 to 1.6	V
$\lvert V_{DDIO} - V_{DD} \rvert$	Variations between different power pins	<50	mV
$\lvert V_{DD} - AV_{DD} \rvert$	Variations between different power pins	<50	mV
$\lvert GND - AV_{SS} \rvert$	Variations between different ground pins	<50	mV
V_{IN}	Input voltage of 3.3V I/O with 5V tolerant. Input Voltage on RTC domain (PF.6) Input Voltage on any other pin(2)	- 0.3 to 5.5 V_{DD} V_{DD}	V
T_{STG}	Storage temperature.	- 65 to 150	℃
I_{IN}	DC input current.	50	mA
I_{OUT}	Output short circuit current.	50	mA

(1): Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted in the recommended operating condition section of this datasheet. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

(2): Non 5V-tolerance PIN: PA.8 ~ 11; PB.0 ~ 15; PF.2, 3, 4, 5; All USB High Speed pins and nRESET pin.

3.2 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{HCLK}	Internal AHB clock frequency				192	MHz
V_{DD}	DC Power Supply Voltage		1.8		3.6	V
AV_{DD}(1)	Analog Operation Voltage			V_{DD}		V
V_{DDIO}	Power supply for PA.0 ~ 5		1.8		3.6	V
V_{REF}	Analog reference voltage		1.8		AV_{DD}	V
V_{LDO}	LDO Output Voltage			1.26		V
~~V_{BG}~~	~~Band-gap Voltage for ADC~~	~~VDD = 1.8 V ~ 3.6 V~~	~~1.17~~		~~1.23~~	~~V~~
VCC3IO	Power supply of 3.3V I/O for ESC sub-system		2.97	3.3	3.63	V
VCC33A	Analog power supply for Ethernet PHY		2.97	3.3	3.63	V
VCCK	Digital core power supply for ESC sub-system		1.08	1.2	1.32	V
VCC12A_PLL	Analog power supply for PLL for ESC sub-system		1.08	1.2	1.32	V
C_{LDO}(2)	LDO Output capacitance on each pin			2.2		uF
t_{VDD}	VDD rise time rate		10			us/V
	VDD fall time rate	BOD Disabled, LVR Enabled(3)	400			
		BOD Disabled, LVR Enabled(4)	500			
		BOD 1.6V Enabled	80			
		BOD 3.0V Enabled	60			
T_J	Operating junction temperature		-40	25	125	℃
T_A	Operating ambient temperature		-40	-	105	℃

(1): It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3 V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation.
(2): To ensure stability, an external 2.2 µF output capacitor, C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 2.2 uF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
(3): LVR in active mode
(4): LVR in low power mode

3.3 DC Electrical Characteristics

3.3.1 Leakage Current and Capacitance

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IN}	Input leakage current. No pull-up or pull-down.	3.3V with 5V tolerant I/O pins. Vin = 5 or 0V.	-	< ±1	-	µA
C_{IN}	Input capacitance.	3.3V with 5V tolerant I/O pins.	-	2.3	-	pF

3.3.2 DC Characteristics of 3.3V (with 5V Tolerant) I/O Pins

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input low voltage.	V_{DD}=V_{DDIO}=VCC3IO= 3.6V			0.8	V
		V_{DD}=V_{DDIO}=1.8V			0.56	V
V_{IH}	Input high voltage.	V_{DD}=V_{DDIO}=VCC3IO= 3.6V	2.0			V
		V_{DD}=V_{DDIO}=1.8V	1.04			V
Vt-	Schmitt trigger negative going threshold voltage.	V_{DD}=V_{DDIO}	0.3* V_{DD}	0.4* V_{DD}		V
		VCC3IO=3.6V	0.8	1.1		V
Vt+	Schmitt trigger positive going threshold voltage	V_{DD}=V_{DDIO}		0.6* V_{DD}	0.7* V_{DD}	V
		VCC3IO=3.6V		1.6	2.0	
Vol	Output low voltage.	Iol = 4 ~ 8mA	-	-	0.4	V
Voh	Output high voltage.	Ioh = 4 ~ 8mA	2.4	-	-	V
Vopu (1)	Output pull-up voltage for 5V tolerant IO	With internal pull-up resistor	VCC 3IO – 0.9	-	-	V
Rpu	Input pull-up resistance.	For V_{DD} and V_{DDIO} IO pad		50		KΩ
		For VCC3IO IO pad	40	75	190	KΩ
Rpd	Input pull-down resistance.	For V_{DD} and V_{DDIO} IO pad		50		KΩ
		For VCC3IO IO pad	40	75	190	KΩ
Iin	Input leakage current.	Vin = 5 or 0V	-	±1	-	µA
	Input leakage current with pull-up resistance.	Vin = 0 V	-	-45	-	µA
	Input leakage current with pull-down resistance.	Vin = VCC3IO	-	45	-	µA
C_{IO}	I/O pin capacitance			5		pF

Note: This parameter indicates that the pull-up resistor for the 5V tolerant I/O pins cannot reach VCC3IO DC level even without DC loading current.

3.4 AC Electrical Characteristics

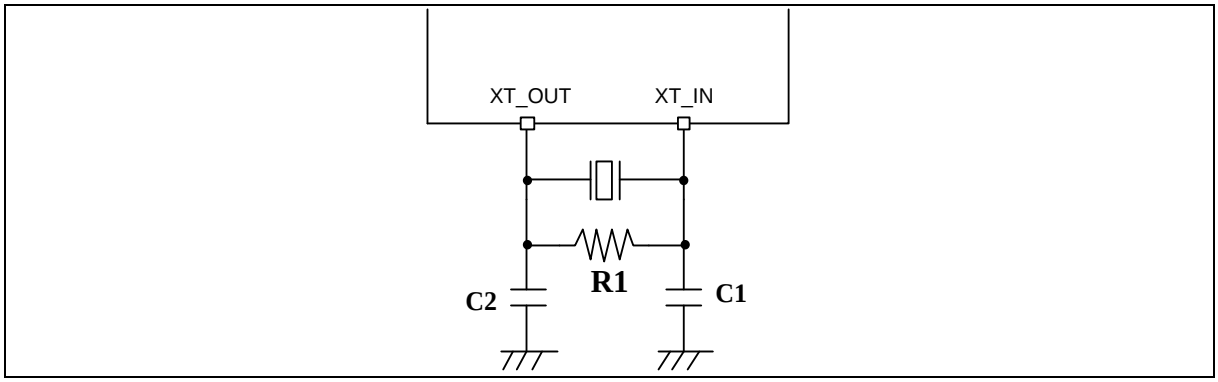
3.4.1 External 4~24 MHz High Speed Crystal (HXT) Characteristics

HXT Crystal AC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_f	Feedback resister			1000		kΩ
f_{HXT}	Oscillator frequency	V_{DD} = 1.8 ~ 3.6V	4		24	MHz
T_{HXT}	Temperature Range		-40		105	°C
I_{HXT_INV}	Current Consumption (INV-type Crystal)	4MHz		650		µA
		12MHz		1600		
		16MHz		2000		
		24MHz		4000		
I_{HXT_GM}	Current Consumption (GM-type Crystal)	4MHz		160		µA
		12MHz		280		
		16MHz		400		
		24MHz		600		
T_{S_GM}	Stable time (GM-type)	4MHz, -40 ˚C	1545		1752	µs
		4MHz, 25 ˚C	1630		1757	
		4MHz, 105 ˚C	1054		1988	
		12MHz, -40 ˚C	484		512	
		12MHz, 25 ˚C	484		544	
		12MHz, 105 ˚C	386		606	
		16MHz, -40 ˚C	349		375	
		16MHz, 25 ˚C	337		399	
		16MHz, 105 ˚C	281		444	
		24MHz, -40 ˚C	259		303	
		24MHz, 25 ˚C	248		330	
		24MHz, 105 ˚C	210		403	
T_{S_INV}	Stable time (INV-type)	4MHz, -40 ˚C	1490		23432	µs
		4MHz, 25 ˚C	1479		2352	
		4MHz, 105 ˚C	1052		2105	
		12MHz, -40 ˚C	464		558	
		12MHz, 25 ˚C	481		554	
		12MHz, 105 ˚C	417		663	
		16MHz, -40 ˚C	317		420	
		16MHz, 25 ˚C	326		407	
		16MHz, 105 ˚C	290		472	
		24MHz, -40 ˚C	226		382	
		24MHz, 25 ˚C	228		388	
		24MHz, 105 ˚C	210		441	
	Clock Duty		45	50	55	%

HXT Crystal Typical Crystal Application Circuits

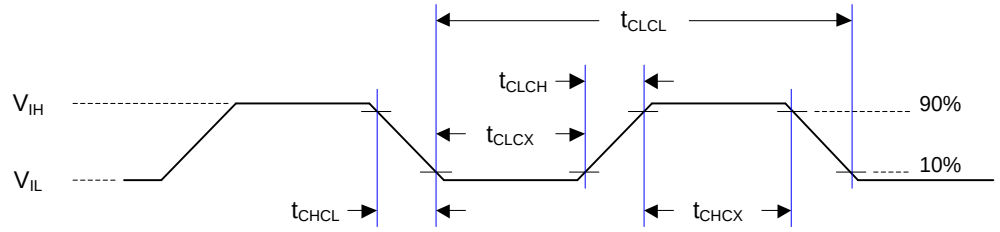
CRYSTAL	C1	C2	R
4MHz ~ 24 MHz	20pF	20pF	without



3.4.2 External 4~24 MHz High Speed Clock Input (OSC) Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{CHCX}	Clock High Time		18	-	-	nS
t_{CLCX}	Clock Low Time		18	-	-	nS
t_{CLCH}	Clock Rise Time		-	-	10	nS
t_{CHCL}	Clock Fall Time		-	-	10	nS
V_{IH}	Input High Voltage		0.7*V_{DD}			V
V_{IL}	Input Low Voltage				0.3*V_{DD}	V

Note: Duty cycle is 50%.



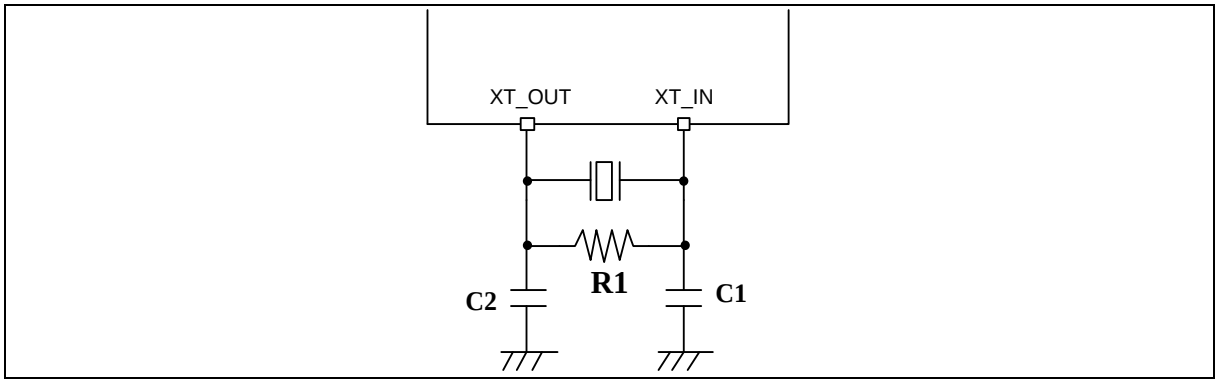
3.4.3 External 32.768 KHz Low Speed Crystal (LXT) characteristics

LXT Crystal AC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Operation Voltage		1.8		3.6	V
f_{LXT}	Oscillator frequency	V_{DD} = 1.8 ~ 3.6 V		32.768		KHz
T_{LXT}	Temperature		-40		105	°C
I_{LXT}	Operating current	V_{DD} = 3.3V			0.5	µA
	Duty cycle		45		55	%
T_S	Stable Time				500	ms

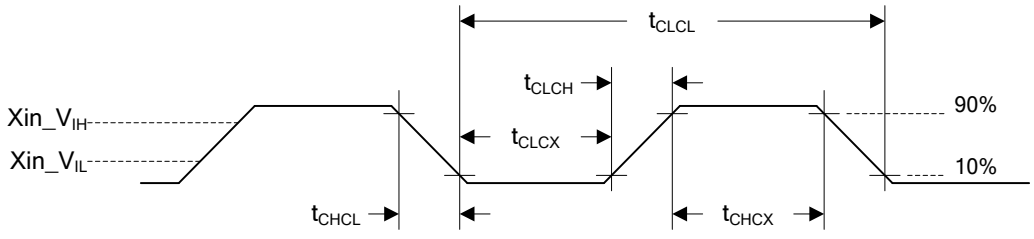
LXT Crystal Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
32.768 KHz	20pF	20pF	without



3.4.4 External 32.768 KHz Low Speed Clock Input (OSC) Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{CHCX}	Clock High Time		450	-	-	nS
t_{CLCX}	Clock Low Time		450	-	-	nS
t_{CLCH}	Clock Rise Time		-	-	50	nS
t_{CHCL}	Clock Fall Time		-	-	50	nS
Xin_VIH	LXT Input Pin Input High Voltage		0.7*V_{DD}			V
Xin_VIL	LXT Input Pin Input Low Voltage				0.3*V_{DD}	V



Note: *Duty cycle is 50%.*

3.4.5 12 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{HRC}	Supply voltage		1.8		3.6	V
f_{HRC}	Center Frequency			12		MHz
	Internal Oscillator Frequency[*1]	T_A = 25 °C, V_{DD} = 3.3V	-1		1	%
I_{HRC}		-40°C ~ +105 °C, V_{DD} = 1.8 ~ 3.6V	-2		2	%
T_S	Operating current			155		µA

3.4.6 10 KHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{LRC}	Supply voltage		1.8		3.6	V
F_{LRC}	Oscillator Frequency[*1]	V_{DD}=1.8V~3.6V, T_A=-40~105°C	5		20	KHz
I_{LRC}	Operating current	V_{DD} = 3.3V			0.5	µA
T_S	Stable time			200		µs

3.4.7 PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{PLL_IN}	PLL input clock		4		24	MHz
f_{PLL_OUT}	PLL multiplier output clock		50		500	MHz
T_S	PLL stable time[*1]		100		200	µs
Jitter	Cycle-to-cycle Jitter[*2]	Peak to peak @ 480M		250		ps
I_{DD}	Power consumption	VDD=3.3V@500MHz			3	mA

3.4.8 External Ethernet Crystal Characteristics

TDB

3.4.9 External Ethernet Clock Input (OSC) Characteristics

TBD

3.5 Analog Electrical Characteristics

3.5.1 LDO

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	DC Power Supply		1.8		3.6	V
V_{LDO}	Output Voltage		1.08	1.26	1.32	V
T_A	Temperature		-40		105	℃

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 2.2μF capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.

3.5.2 Low-Voltage Reset

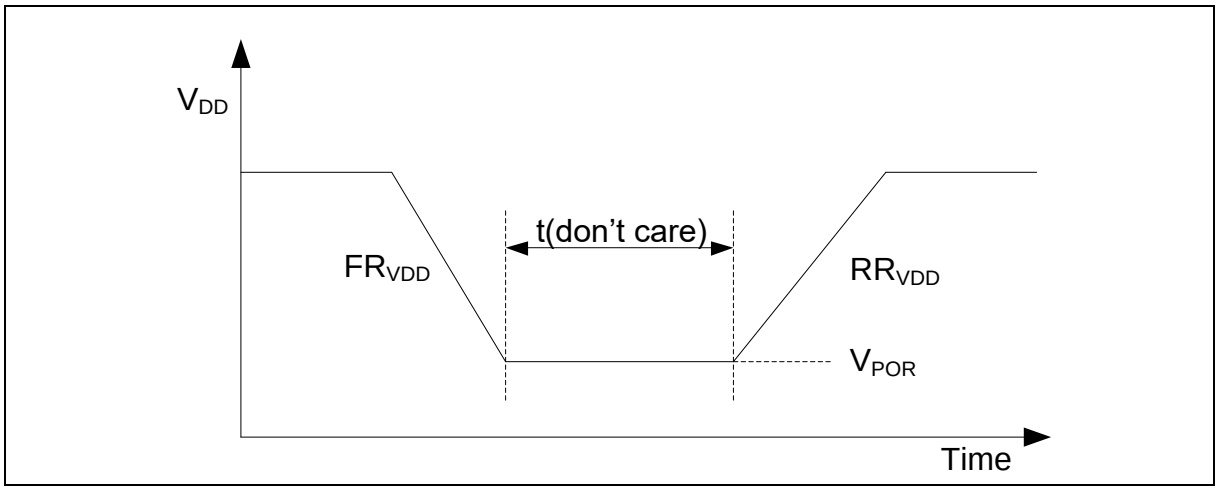
Symbol	Parameter	Conditions	Min	Typ	Max	Units
AV_{DD}	Supply Voltage		0		3.6	V
T_A	Temperature	-	-40		105	℃
I_{LVR}	Operating Current	AV_{DD} = 3.6V		0.5		uA
V_{LVR}	Threshold Voltage	T_A = 105 ℃	1.40	1.48	1.56	V
		T_A = 25 ℃	1.40	1.48	1.56	V
		T_A = -40 ℃	1.40	1.48	1.56	V

3.5.3 Brown-out Detector

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AV_{DD}	Supply Voltage	-	0		3.6	V
T_A	Temperature	-	-40		105	℃
I_{BOD}	Operating Current	AV_{DD} = 3.6V		66		μA
V_{BOD_F}	Brown-out Voltage (Falling edge)	BODVL [2:0] = 111	2.9	3.0	3.1	V
		BODVL [2:0] = 110	2.7	2.8	2.9	V
		BODVL [2:0] = 101	2.5	2.6	2.7	V
		BODVL [2:0] = 100	2.3	2.4	2.5	V
		BODVL [2:0] = 011	2.1	2.2	2.3	V
		BODVL [2:0] = 010	1.9	2.0	2.1	V
		BODVL [2:0] = 001	1.7	1.8	1.9	V
		BODVL [2:0] = 000	2.9	3.0	3.1	V
V_{BOD_R}	Brown-out Voltage (Rising edge)	BODVL [2:0] = 111	3.0	3.1	3.2	V
		BODVL [2:0] = 110	2.8	2.9	3.0	V
		BODVL [2:0] = 101	2.6	2.7	2.8	V
		BODVL [2:0] = 100	2.4	2.5	2.6	V
		BODVL [2:0] = 011	2.2	2.3	2.4	V
		BODVL [2:0] = 010	2.0	2.1	2.2	V
		BODVL [2:0] = 001	1.8	1.9	2.0	V
		BODVL [2:0] = 000	1.6	1.7	1.8	V
T_{BOD_RE}	Respond Time	Respond Time		1		ms

3.5.4 Power-on Reset for V_{DD}

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_A	Temperature		-40	-	+105	℃
V_{POR}	Reset Voltage			1.47		V
RRV_{DD}	V_{DD} Raising Rate to Ensure Power-on Reset[*1]		10			us/V
FRV_{DD}	V_{DD} Falling Rate to Ensure Power-on Reset[*1]		320			us/V



Power-up Ramp Condition

3.5.5 Power-on Reset for VCCK

Below figures and table show the two POR circuit spec during power ramp-up/down.

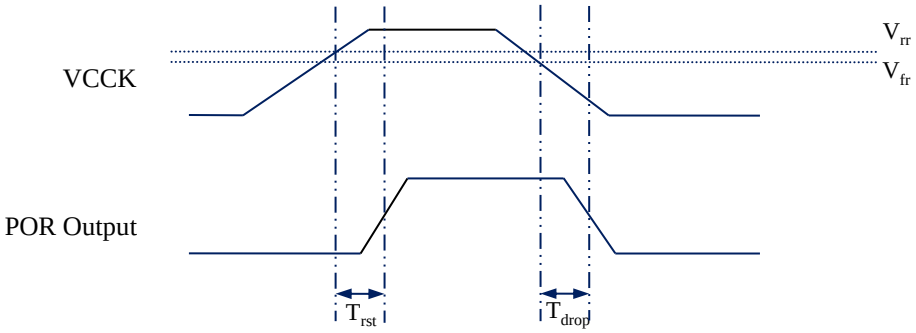


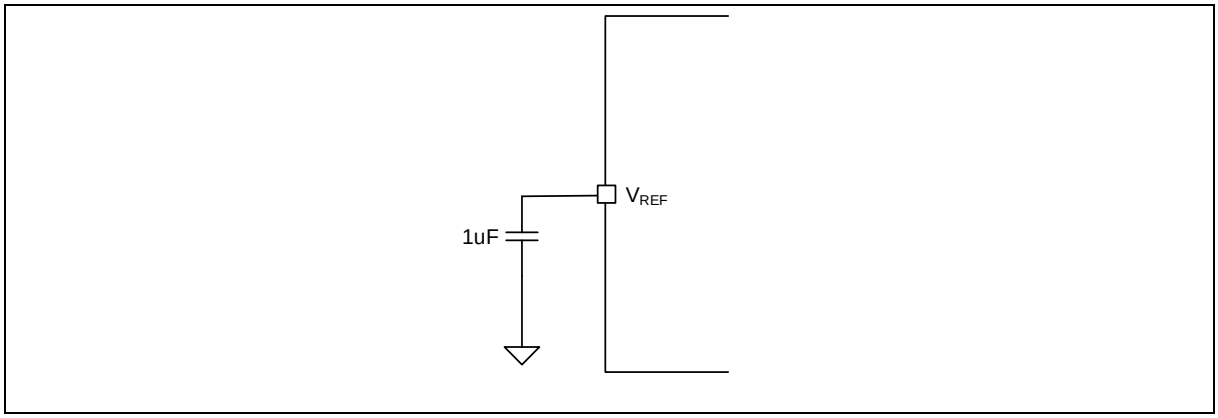
Figure 3.5-1: Power On Reset (POR) Timing Diagram

Symbol	Description	Conditions	Min.	Typ.	Max.	Units
VCCK	Power supply voltage to be detected	-	1.0	1.2	1.32	V
V_{rr}	VCCK rise relax voltage	-	-	0.72	0.9	V
V_{fr}	VCCK fall release voltage	-	-	0.63	0.85	V
T_{rst}	Reset time after POR trigger up	VCCK slew rate = 1.0V / 1µs	1.8	2.5	4.8	µs
T_{drop}	Drop time of VCCK to reset	VCCK slew rate = 2.5V / 1µs	0.2	0.4	0.9	µs

Table 3.5-1: Power On Reset (POR) Timing Table

3.5.6 Internal Voltage Reference

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{REF_INT}	Internal reference voltage			1.6		V
				2.0		
				2.5		
				3.0		
AV_{DD_min}	AV_{DD} minimum voltage		2			V
			2.2			
			2.7			
			3.2			
T_s	Stable time	C_L =4.7 uF, V_{REF} initial=0		0.7	2	ms
		C_L =0.1 uF, V_{REF} initial=0		35	48	us



Typical connection with internal voltage reference

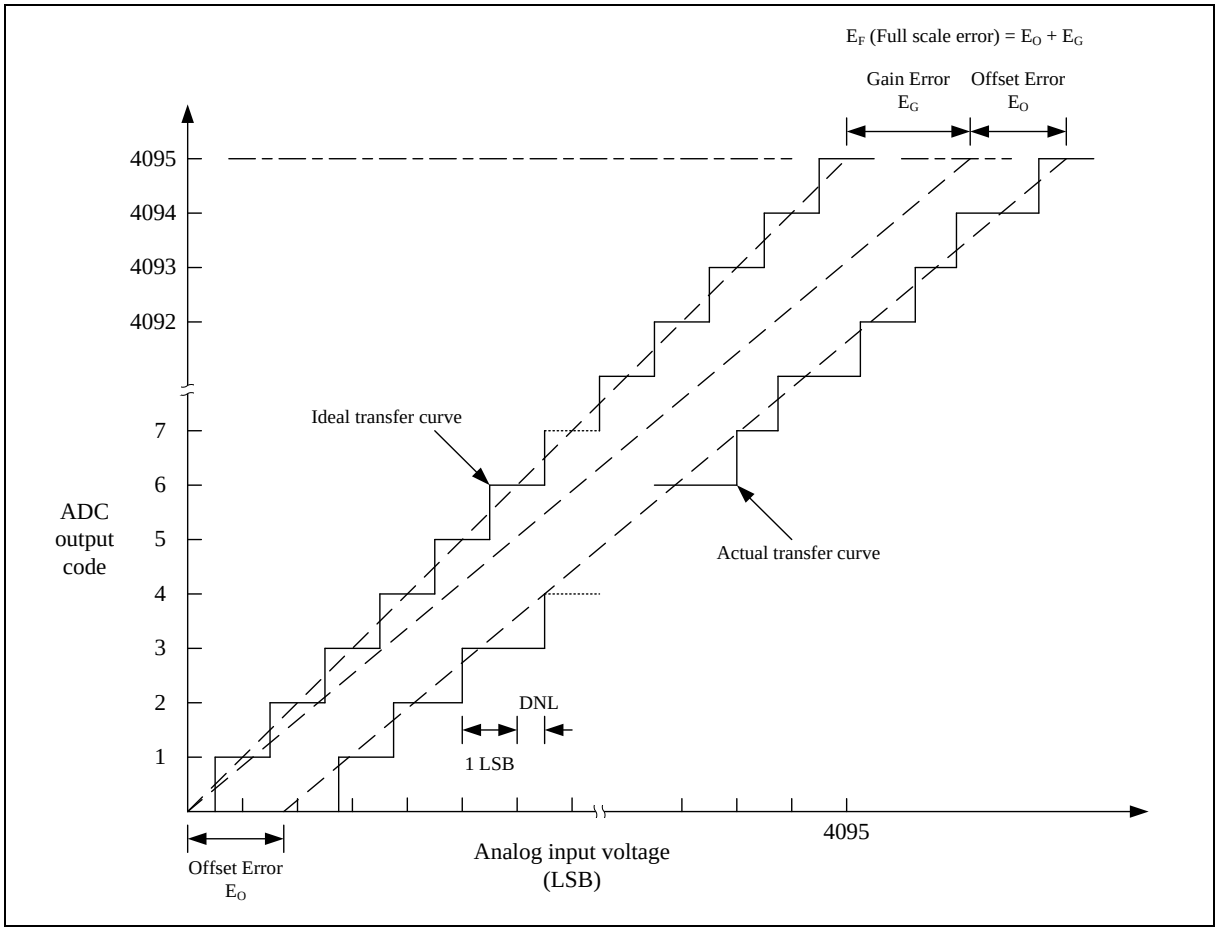
3.5.7 12-bit ADC

Fast Speed Channel

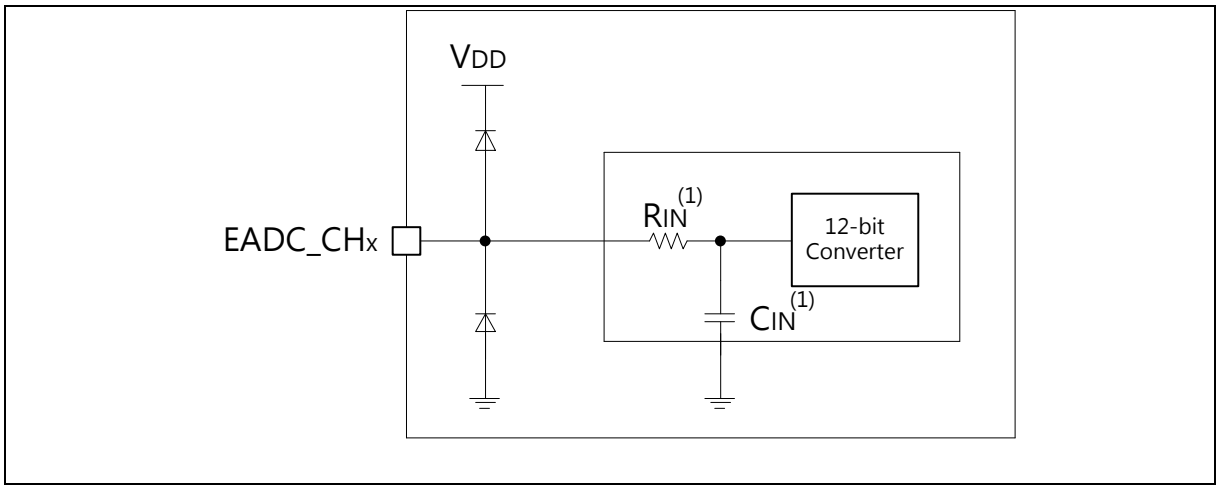
Symbol	Parameter	Conditions	Min	Typ	Max	Units
AV_{DD}	Operating voltage	$AV_{DD} = V_{DD}$	1.8		3.6	V
V_{REF}	Reference voltage		1.6		AV_{DD}	V
T_A	Temperature		-40		105	℃
I_{ADC}	Operating current (AV_{DD} current) (Enable ADC and disable all other analog modules)	$AV_{DD} = V_{DD} = V_{REF}$ = 3.3V ADC Clock Rate = 70 MHz High speed channel	478		523	uA
	Resolution				12	Bit
V_{IN}	ADC channel input voltage		0		V_{REF}	V
F_{ADC}	ADC Clock frequency	High speed channel	0.14		70	MHz
T_{SMP}	Sampling Time			2		$1/F_{ADC}$
T_{CONV}	Conversion time	$T_{CONV} = T_{SMP} + 12$		14		$1/F_{ADC}$
F_{SPS}	Sampling Rate (F_{ADC}/T_{CONV})	High speed channel			5	MSPS
T_{PU}	Power-up time		20			µs
INL	Integral Non-Linearity Error	$V_{REF} = AV_{DD}$	-4.29		-3.71	LSB
DNL	Differential Non-Linearity Error	$V_{REF} = AV_{DD}$	3.25		3.28	LSB
E_G	Gain error	$V_{REF} = AV_{DD}$	2.25		2.31	LSB
E_{OFFSET}	Offset error	$V_{REF} = AV_{DD}$	1.56		2.87	LSB
E_A	Absolute Error	$V_{REF} = AV_{DD}$	4.5		4.94	LSB
C_{IN}	Internal Capacitance[*1]			5		pF
-	Monotonic		Guaranteed			

Low Speed Channel

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AV_{DD}	Operating voltage	$AV_{DD} = V_{DD}$	1.8		3.6	V
V_{REF}	Reference voltage			AV_{DD}		V
T_A	Temperature		-40		105	℃
I_{ADC1}	Operating current (AV_{DD} current) (Enable ADC and disable all other analog modules)	$AV_{DD} = V_{DD} = V_{REF}$ = 3.3V ADC Clock Rate = 28 MHz low speed channel	210		231	uA
		$AV_{DD} = V_{DD} = V_{REF}$ = 1.8V ADC Clock Rate = 28 MHz low speed channel	131		142	
I_{ADC2}		$AV_{DD} = V_{DD} = V_{REF}$ = 3.3V ADC Clock Rate = 14 MHz low speed channel	111		123	
		$AV_{DD} = V_{DD} = V_{REF}$ = 1.8V ADC Clock Rate = 14 MHz low speed channel	70		78	
	Resolution				12	Bit
V_{IN}	ADC channel input voltage		0		V_{REF}	V
F_{ADC}	ADC Clock frequency	Low speed channel	0.14		28	MHz
T_{SMP}	Sampling Time			2		$1/F_{ADC}$
T_{CONV}	Conversion time	$T_{CONV} = T_{SMP} + 12$		14		$1/F_{ADC}$
F_{SPS}	Sampling Rate (F_{ADC}/T_{CONV})	Low speed channel			2	MSPS
T_{PU}	Power-up time		20			µs
INL	Integral Non-Linearity Error	$V_{REF} = AV_{DD}$	-2.94		-1.32	LSB
DNL	Differential Non-Linearity Error	$V_{REF} = AV_{DD}$	1.25		2	LSB
E_G	Gain error	$V_{REF} = AV_{DD}$	2.5		3.12	LSB
E_{OFFSET}	Offset error	$V_{REF} = AV_{DD}$	2.44		3.69	LSB
E_A	Absolute Error	$V_{REF} = AV_{DD}$	4.69		6.75	LSB
C_{IN}	Internal Capacitance[*1]			5		pF
-	Monotonic		Guaranteed			



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.



Note: GND < EADC_CHx < V_{REF}

(1) Refer to ADC spec for the values of R_{IN}, C_{IN}

3.5.8 Temperature sensor

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Operating Voltage		1.8		3.6	V
T_A	Temperature Range		-40		105	°C
I_{TEMP}	Current Consumption [*3]			16		µA
T_c	Temperature Coefficient [*3]		-1.77	-1.82	-1.84	mV/ °C
V_{os}	Offset Voltage when T_A = 0°C [*3]		710.2		716.8	mV
t_S	Stable time[*2]			1		µs
T_{S_temp}	ADC sampling time when reading the temperature (5pF cap load) [*1]			3		µs

Note:

1. V_{TEMP} (mV) = T_c (mV/°C) x Temperature (°C) + V_{os} (mV)
2. Guaranteed by design, not tested in production
3. Guaranteed by characteristic, not tested in production

3.5.9 Digital to Analog Converter (DAC)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AV_{DD}	Analog supply voltage		1.8	-	3.6	V
N_R	Resolution			12		bit
V_{REF}	Reference supply voltage	$V_{REF} \leq AV_{DD}$	1.5	-	AV_{DD}	V
DNL	Differential non-linearity error[*4]	12-bit mode	-	-	±2	LSB
		10-bit mode	-	-	±0.5	LSB
INL	Integral non-linearity error[*4]	12-bit mode	-	-	±4	LSB
		10-bit mode	-	-	±1	LSB
OE	Offset Error[*4]	12-bit mode DACOUT buffer ON	-	-	±6	LSB
		12-bit mode DACOUT buffer OFF	-	-	±4	LSB
		10-bit mode	-	-	±2	LSB
GE	Gain Error[*4]	12-bit mode DACOUT buffer ON	-	-	±5	LSB
		12-bit mode DACOUT buffer OFF	-	-	±4	LSB
		10-bit mode	-	-	±2	LSB
AE	Absolute Error[*4]	12-bit mode DACOUT buffer ON	-	-	±8	LSB
		12-bit mode DACOUT buffer OFF	-	-	±4	LSB
		10-bit mode	-	-	±2	LSB
-	Monotonic		10-bit guaranteed			
V_O	Output Voltage	DACOUT buffer ON	0.2		AV_{DD} - 0.2	V
R_{LOAD}	Resistive load[*2]	DACOUT buffer ON	7.5	-	-	kΩ
Ro	Output impedance[*4]	DACOUT buffer OFF		10	12	kΩ
C_{LOAD}	Capacitive load[*3]	-	-	-	50	pF
I_{AVDD}	Current consumption on AV_{DD} supply[*4]	AV_{DD} = 3.6V, no load, lowest code (0x000)	-	-	180	µA
		AV_{DD} = 3.6V, no load, middle code (0x800)	-	-	420	
I_{REF}	Current consumption on V_{REF} supply[*4]	V_{REF} =3.6V, no load, middle code (0x800)	-	150	240	µA
T_S	Settling Time	Full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value +/-1 LSB, $C_{LOAD} \leq 50pF$, $R_{LOAD} \geq 7.5k\Omega$	-	5	6	µs
F_s	Update Rate	Max. frequency for a correct DAC_OUT change from core i to i+1LSB, $C_{LOAD} \leq 50pF$, $R_{LOAD} \geq 7.5k\Omega$	-	-	1	M_{SPS}
T_{WAKEUP}	Wake-up Time	Wakeup time from OFF state. Input code between lowest and highest possible codes. DAC clock source = 1MHz	-	9	15	µs
PSRR	Power Supply Rejection Ratio[*1]	No R_{LOAD}, C_{LOAD} = 50pF	-	-60	-40	dB

Note:

1. Guaranteed by design, not tested in production.
2. Resistive load between DACOUT and AV_{SS}.
3. Capacitive load at DACOUT pin.
4. Guaranteed based on test during characterization.

3.5.10 Analog Comparator Controller (ACMP)

The maximum values are obtained for VDD = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AV_{DD}	Analog supply voltage		1.8		3.6	V
T_A	Temperature		-40		105	℃
I_{DD}	Operating current	MODESEL[1:0] = 00		1.2		µA
		MODESEL[1:0] = 01		3		
		MODESEL[1:0] = 10		10		
		MODESEL[1:0] = 11		75		
V_{CM}	Input common mode voltage range [*2]		0.1	1/2 AV_{DD}	AV_{DD} -0.1	
V_{DI}	Differential input voltage sensitivity [*2]	Hysteresis disable	10	20		mV
V_{offset}	Input offset voltage	Hysteresis disable,		5	10	mV
V_{hys}	Hysteresis window	HYSSEL[1:0] = 00		0		mV
		HYSSEL[1:0] = 01		10		
		HYSSEL[1:0] = 10		20		
		HYSSEL[1:0] = 11		30		
A_v	DC voltage Gain[*1]			70		dB
T_d	Propagation delay[*2]	Hysteresis disable MODESEL[1:0] = 00			0.2	uS
		Hysteresis disable MODESEL[1:0] = 01			0.6	
		Hysteresis disable MODESEL[1:0] = 10			2	
		Hysteresis disable MODESEL[1:0] = 11			4.5	
T_{Setup}	Setup time[*2]	Hysteresis disable MODESEL[1:0] = 00			0.45	uS
		Hysteresis disable MODESEL[1:0] = 01			0.85	
		Hysteresis disable MODESEL[1:0] = 10			2.25	
		Hysteresis disable MODESEL[1:0] = 11			4.75	

Note:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production

3.5.11 OP Amplifier (OPA)

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A = 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AV_{DD}	Analog supply voltage		2.4		3.6	V
T_A	Temperature		-40		105	℃
I_{DD}	Consumption current	A_{VDD}=3.3V, Temperature=25 ℃		690		μA
CMIR	Common mode input range		0		AV_{DD}	V
$V_{OFFSET0}$	Input offset voltage(maximum calibration range) [*2]	Tj = 25°C, No Load			4	mV
		V_{CM} = AV_{DD}-10mV ~ AV_{DD}-0.8V, All Temp.			6	
$V_{OFFSET1}$	Input offset voltage(After offset calibration) [*2]	CALRVS =0: Other V_{CM}			3.2	mV
		CALRVS=0: V_{CM} = AV_{DD}-10mV ~ AV_{DD}-0.8V			6.5	
$V_{OFFSET2}$	Input offset voltage(After offset calibration) [*2]	CALRVS =1: Other VCM			3	mV
		CALRVS =1: V_{CM} = AV_{DD}-10mV ~ AV_{DD}-0.8V			5.2	
CMRR	Common Mode Rejection Ratio [*1]			90		dB
PSRR	Power Supply Rejection Ratio [*1]		73	117		dB
GBW	Bandwidth [*2]			8.2		MHz
SR	Slew rate [*2]			4.7		V/μs
V_{OHSAT}	High saturation voltage [*2]	Rload=min. INPUT at AVDD	AV_{DD}-0.1			V
		Rload=20K, INPUT at AVDD	AV_{DD}-0.02			
V_{OLSAT}	Low saturation voltage [*2]	Rload=min. INPUT at 0			100	mV
		Rload=20K, INPUT at 0			20	
PM	Phase Margin [*1]			62		degree
T_{WAKEUP}	Wake up time from OFF state [*2]			2.8	5	μs
R_{LOAD}	Resistive load		4			kΩ
C_{LOAD}	Capacitive load				50	pF

Note:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production

3.6 USB Electrical Characteristics

USB Full-Speed

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IH}	Input High (driven)	2.0	-	-	V	-
V_{IL}	Input Low	-	-	0.8	V	-
V_{DI}	Differential Input Sensitivity	0.2	-	-	V	|PADP-PADM|
V_{CM}	Differential Common-mode Range	0.8	-	2.5	V	Includes V_{DI} range
V_{SE}	Single-ended Receiver Threshold	0.8	-	2.0	V	-
	Receiver Hysteresis	-	200	-	mV	-
V_{OL}	Output Low (driven)	0	-	0.3	V	-
V_{OH}	Output High (driven)	2.8	-	3.6	V	-
V_{CRS}	Output Signal Cross Voltage	1.3	-	2.0	V	-
R_{PU}	Pull-up Resistor	1.425	-	1.575	kΩ	-
R_{PD}	Pull-down Resistor	14.25	-	15.75	kΩ	
V_{TRM}	TERMINATION Voltage for Uptream port pull up (RPU)	3.0	-	3.6	V	
Z_{DRV}	Driver Output Resistance	-	13	-	Ω	Steady state drive*
C_{IN}	Transceiver Capacitance	-	-	20	pF	Pin to GND

USB Full-Speed PHY characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
T_{FR}	Rise Time	4	-	20	ns	C_L=50p
T_{FF}	Fall Time	4	-	20	ns	C_L=50p
T_{FRFF}	Rise and Fall Time Matching	90	-	111.11	%	$T_{FRFF}=T_{FR}/T_{FF}$

USB High-Speed characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_{FR}	High Speed Driver Rise Time	500	-		ps	CL=5pF
T_{FF}	High Speed Driver Fall Time	500	-		ps	CL=5pF
T_{FRFF}	Rise and Fall Time Matching	90		111.11	%	$T_{FRFF}=T_{FR}/T_{FF}$

3.7 Ethernet PHY Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{PPTX}	Peak-to-peak differential output voltage	100BASE-TX mode	1.9	2.0	2.1	V
Tr/Tf	Signal rise/fall time	100BASE-TX mode	3.0	4.0	5.0	ns
	Output Jitter	100BASE-TX mode, Scrambled idle signal			1.4	ns
	Overshoot	100BASE-TX mode			5.0	%
	Error-free cable length	meter	100			m
Fiber Mode						
VOL	TX Output low voltage		1.0	1.5	2.0	V
VOH	TX Output high voltage		2.0	2.4	2.75	V
|VOD|	TX Differential threshold voltage		0.52	0.83	1.3	V
Vicm	RX Input common-mode voltage		1.67	2.0	2.33	V
|Vidth|	RX Input differential threshold voltage		0.2	0.83	1.0	V
SD	Copper mode	SD < 0.2V				
	Fiber mode without detected signal Generate far-end fault	1.0V < SD < 1.8V				
	Fiber mode with detected signal	SD > 2.4V				

3.8 Flash Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{FLA}[1]	Supply Voltage	T_A = 25℃	1.08		1.32	V
N_{ENDUR}	Endurance		10000	-	-	cycles[2]
T_{RET}	Data Retention		10	-	-	year
T_{ERASE}	Page Erase Time		92	-	160	mS
T_{MER}	Mass Erase Time		201	-	320	mS
T_{PROG}	Program Time		42	-	50	uS
I_{DD1}	Read Current		-	-	4.12	mA
I_{DD2}	Program Current		-	-	5	mA
I_{DD3}	Erase Current		-	-	5	uA

Note:

1. V_{FLA} is source from chip LDO output voltage.
2. Number of program/erase cycles.
3. This table
4. is guaranteed by design, not test in production.

3.9 Power Consumption

3.9.1 Main System

TBD

3.9.2 ESC Sub-system

Item	Conditions	VCCIO + VCC33A	VCCK + VCC12A_PLL	Units
Digital IO	20 I/O Output (Typ.)	160	50	mA

Note: Above current value are typical values measured on AX58200 Test board.

Table 3.9-1: Power Consumption

3.9.3 Package Thermal Characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
Θ_{JC}	Thermal resistance of junction to case		-	13.4	-	°C/W
Θ_{JA}	Thermal resistance of junction to ambient	Still air	-	24.24	-	°C/W
Ψ_{JT}	Junction to Top of the Package Characterization Parameter		-	8.64	-	°C/W

Note: Above information is based on using 6 layers PCB.

Table 3.9-2: Thermal Characteristics

3.10 Power–up Sequence

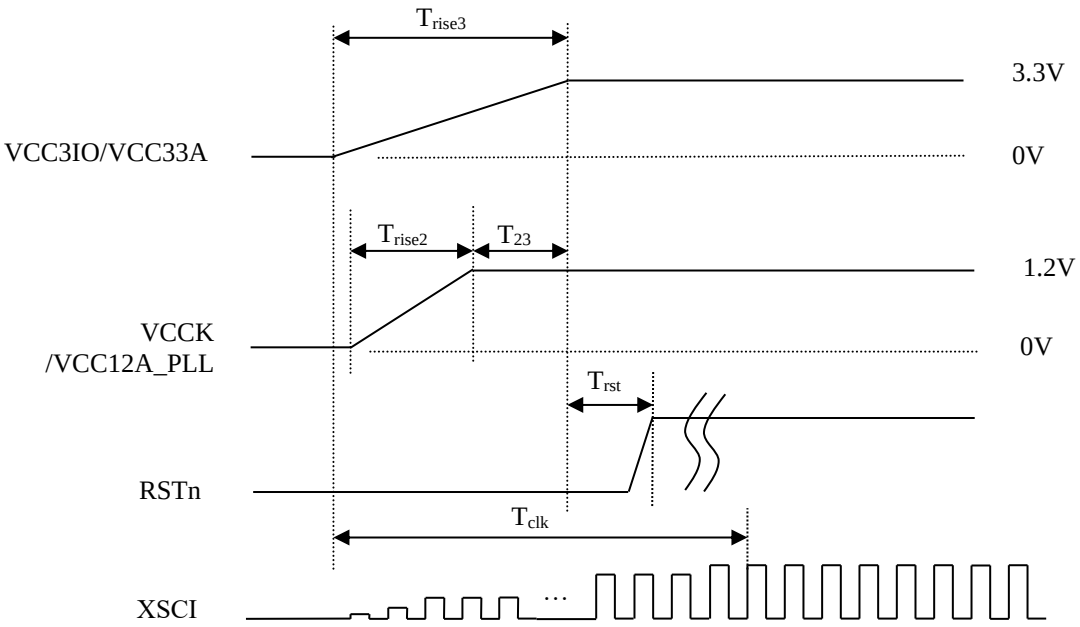


Figure 3.10-1: Power-up Sequence Timing Diagram

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{rise3}	3.3V power supply rise time.	From 0V to 3.3V.	-	400	-	us
T_{rise2}	1.2V power supply rise time.	From 0V to 1.2V.	-	200	-	us
T_{23}	VCCK rising to 1.2V to VCC3IO rising to 3.3V interval.		-	200	-	us
T_{rst}	RSTn asserted low level interval.	From VCC3IO rising to 3.3V to RSTn going high.	-	40	-	us
T_{clk}	25MHz crystal oscillator start-up time.	From VCC3IO rising to 3.3V to clock stable of 25MHz crystal oscillator.	-	-	60	ms
$T_{Startup}$	Startup time	PDI operational after power good, without I2C EEPROM loading error	-	-	70	ms

Note: The above typical timing data is measured from AX58200 test board.

Table 3.10-1: Power-up Sequence Timing Table

3.11 AC Timing Characteristics

3.11.1 I2C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Units
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.2	-	uS
t_{HIGH}	SCL high period	4	-	0.6	-	uS
$t_{SU;STA}$	Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;STA}$	START condition hold time	4	-	0.6	-	uS
$t_{SU;STO}$	STOP condition setup time	4	-	0.6	-	uS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r	SCL/SDA rise time	-	1000	$20+0.1C_b$	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

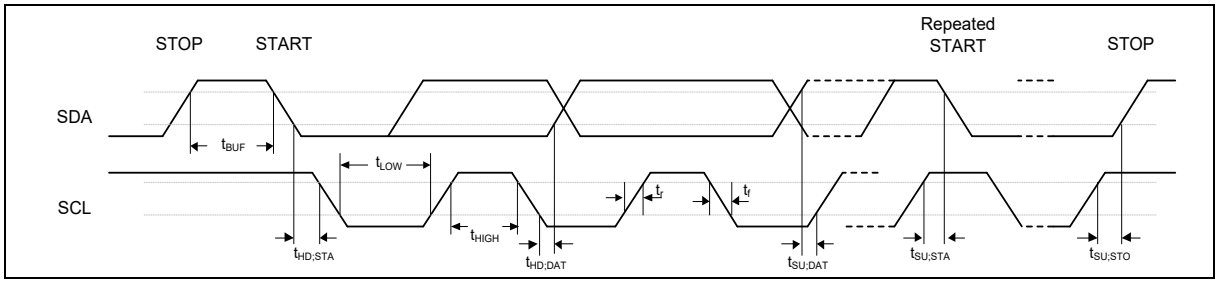


Figure 3.11-1 I²C Timing Diagram

3.11.2 SPI Dynamic Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI MASTER MODE (VDD = 3.0~3.6 V, 30 PF LOADING CAPACITOR)					
t_{CLKH}	Clock output High time [*1]			T_{SPICLK} / 2	ns
t_{CLKL}	Clock output Low time [*1]			T_{SPICLK} / 2	ns
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2	-	-	ns
t_V	Data output valid time	-	0	1	ns
SPI MASTER MODE (VDD = 1.8~2.0 V, 30 PF LOADING CAPACITOR)					
t_{CLKH}	Clock output High time [*1]			T_{SPICLK} / 2	ns
t_{CLKL}	Clock output Low time [*1]			T_{SPICLK} / 2	ns
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2	-	-	ns
t_V	Data output valid time	-	-	1	ns

Note:

1. The minimum clock period for SPICLK is 10.4 ns (96 MHz).

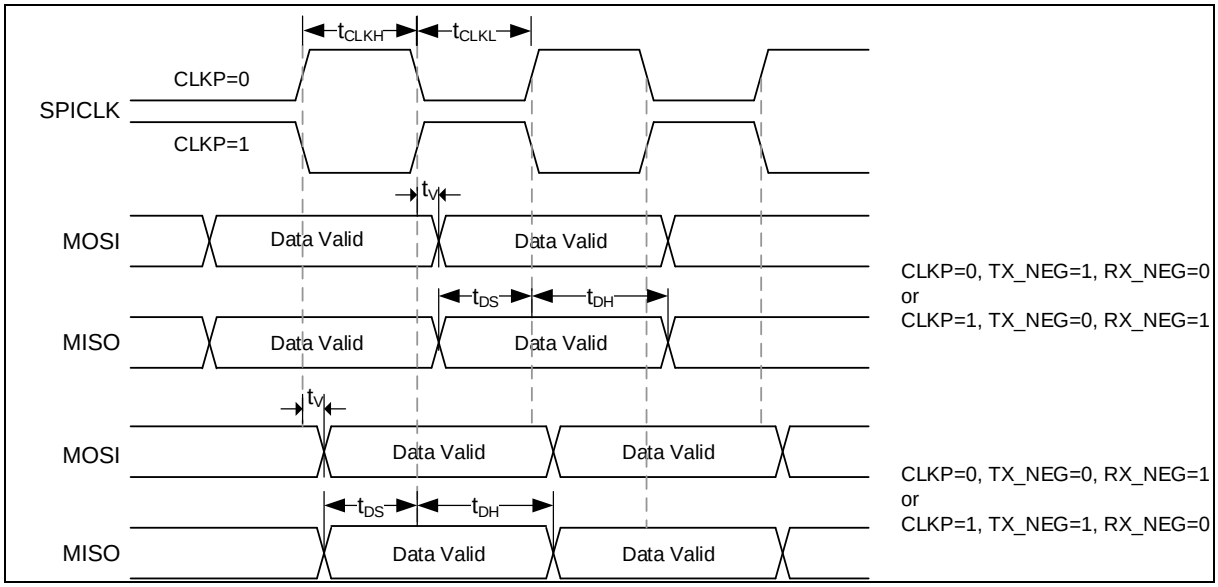


Figure 3.11-2 SPI Master Mode Timing Diagram

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI SLAVE MODE (VDD = 3.0~3.6V, 30 PF LOADING CAPACITOR)					
t_{CLKH}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns
t_{CLKL}	Clock output Low time [*1]	-		T_{SPICLK} / 2	ns
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	ns
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns
t_{DS}	Data input setup time	0	-	-	ns
t_{DH}	Data input hold time	2	-	-	ns
t_V	Data output valid time	-		8	ns
t_{CLKH}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns
SPI SLAVE MODE (VDD = 1.8 V ~ 2.0 V, 30 PF LOADING CAPACITOR)					
t_{CLKH}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns
t_{CLKL}	Clock output Low time [*1]	-	-	T_{SPICLK} / 2	ns
t_{SS}	Slave select setup time	1 T_{SPICLK} + 3ns	-	-	ns
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns
t_{DS}	Data input setup time	0	-	-	ns
t_{DH}	Data input hold time	2	-	-	ns
t_V	Data output valid time	-		10	ns

Note:

1. The minimum clock period for SPICLK is 10.4 ns (96 MHz).

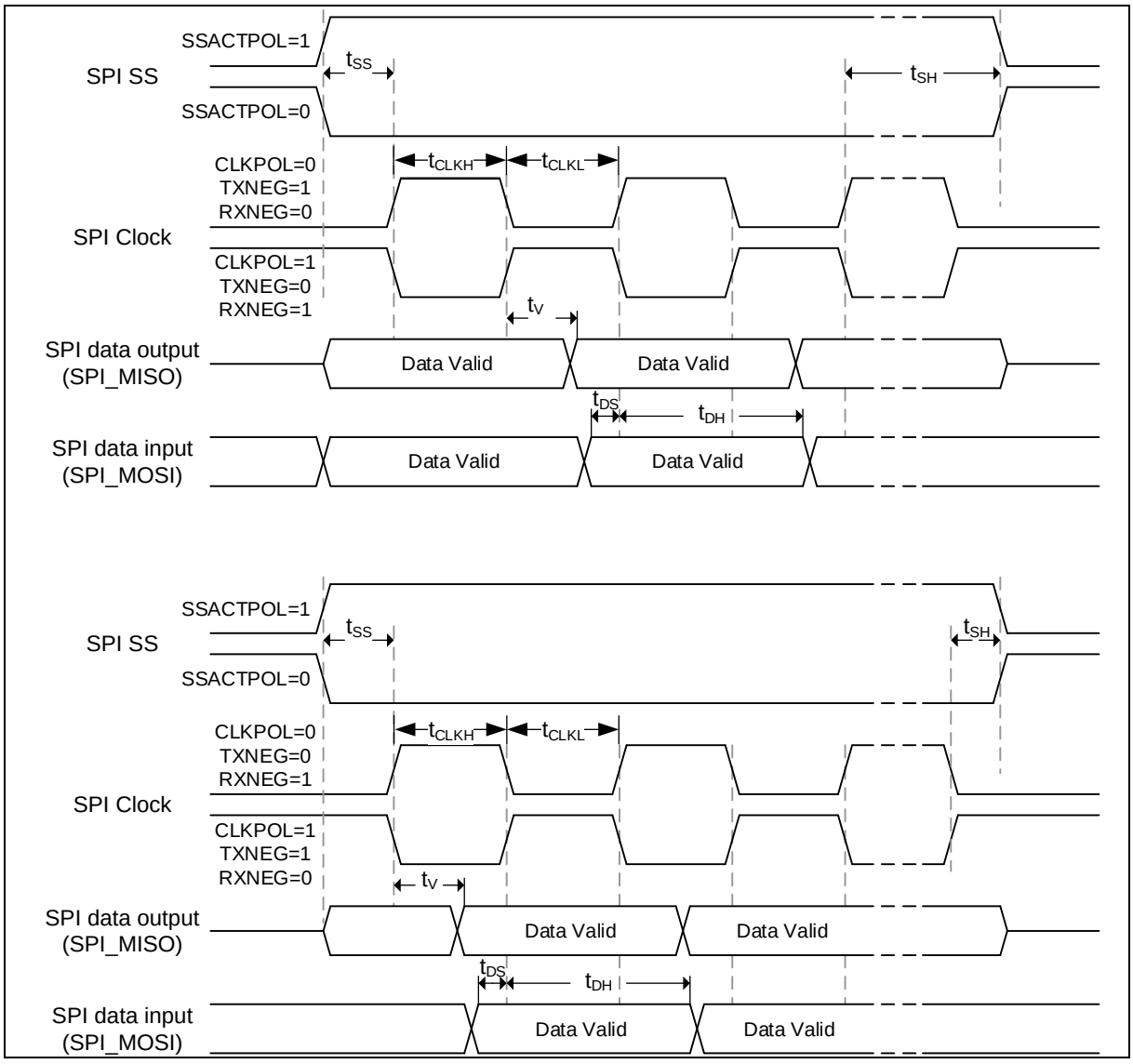


Figure 3.11-3 SPI Slave Mode Timing Diagram

3.11.3 I2S Dynamic Characteristics

Symbol	Parameter	Min	Max	Unit	Test Conditions
$t_{w(CKH)}$	I^2S clock high time	40	-	ns	Master f_{PCLK} = MHz, data: 24 bits, audio frequency = 256 KHz
$t_{w(CKL)}$	I^2S clock low time	40	-		
$t_{v(WS)}$	WS valid time	4	16		Master mode
$t_{h(WS)}$	WS hold time	1	-		Master mode
$t_{su(WS)}$	WS setup time	24	-		Slave mode
$t_{h(WS)}$	WS hold time	0	-		Slave mode
$DuCy_{(SCK)}$	I^2S slave input clock duty cycle	30	70	%	Slave mode
$t_{su(SD\_MR)}$	Data input setup time	10	-	ns	Master receiver
$t_{su(SD\_SR)}$		7	-		Slave receiver
$t_{h(SD\_MR)}$	Data input hold time	7	-		Master receiver
$t_{h(SD\_SR)}$		4	-		Slave receiver
$t_{v(SD\_ST)}$	Data output valid time	-	10		Slave transmitter (after enable edge)
$t_{h(SD\_ST)}$	Data output hold time	4	-		Slave transmitter (after enable edge)
$t_{v(SD\_MT)}$	Data output valid time	-	4		Master transmitter (after enable edge)
$t_{h(SD\_MT)}$	Data output hold time	0	-		Master transmitter (after enable edge)

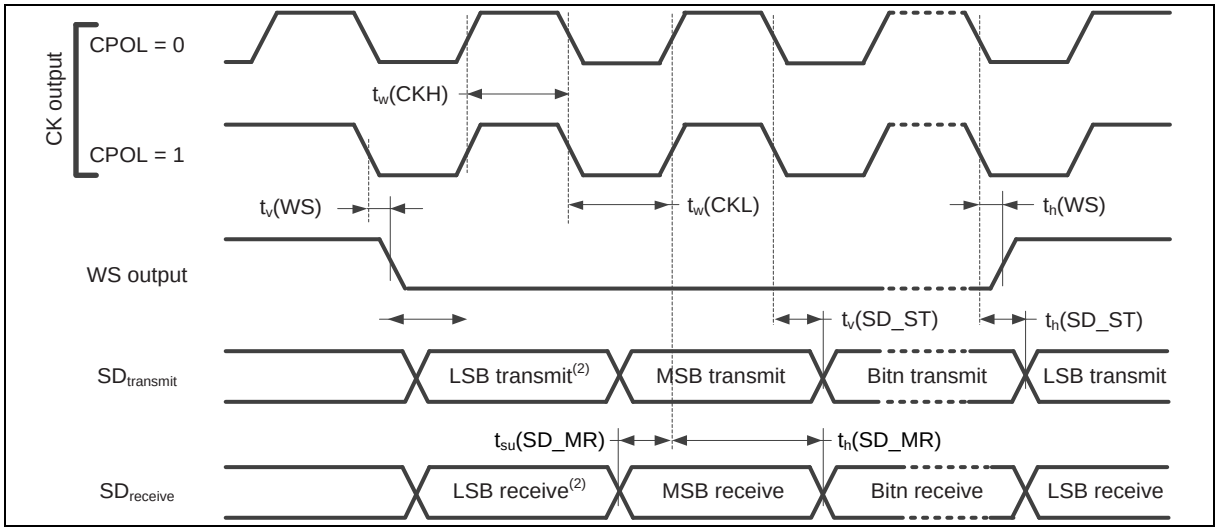


Figure 3.11-4 I2S Master Mode Timing Diagram

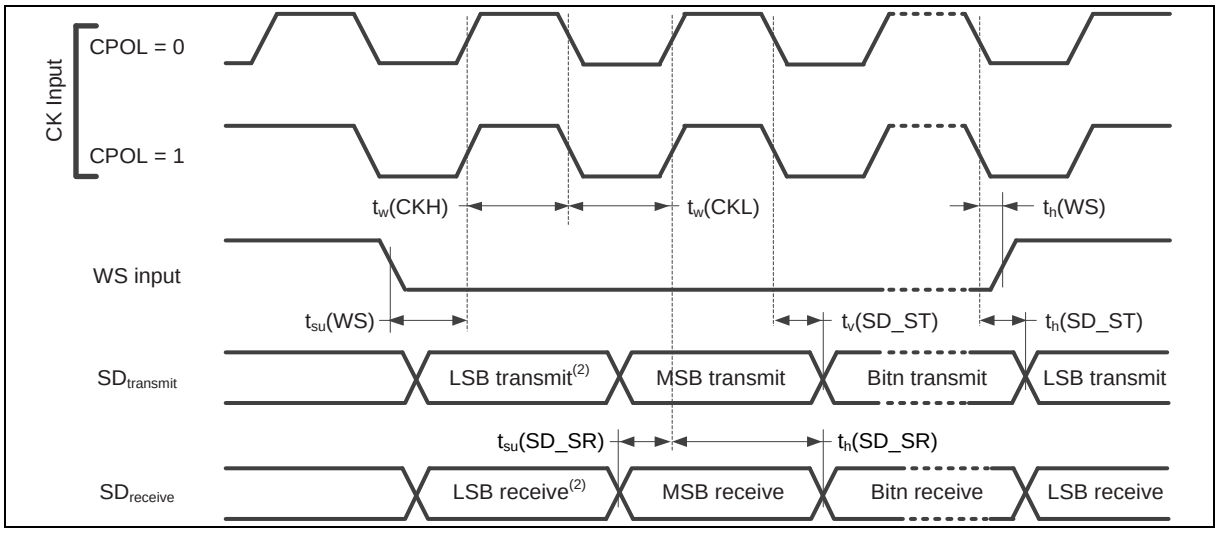


Figure 3.11-5 I²S Slave Mode Timing Diagram

3.11.4 USCI - I2C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min.	Max.	Min.	Max.	
t_{LOW}	SCL low period	4.7	-	1.2	-	uS
t_{HIGH}	SCL high period	4	-	0.6	-	uS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	uS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	uS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r	SCL/SDA rise time	-	1000	$20+0.1C_b$	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I^2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I^2C frequency.
3. I^2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

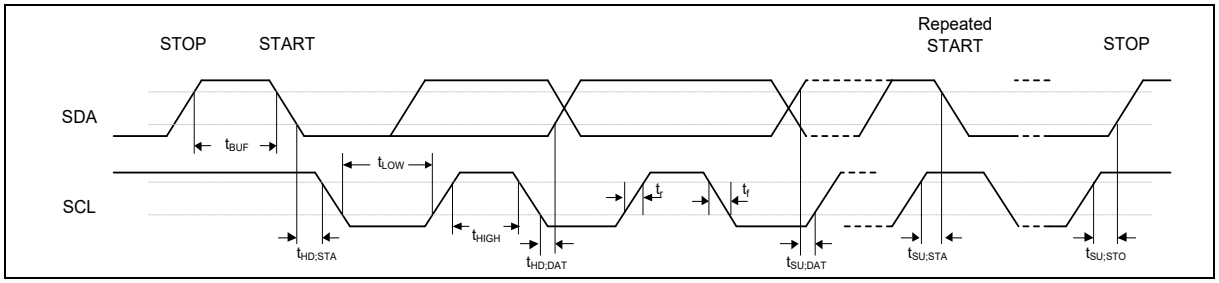


Figure 3.11-6 I^2C Timing Diagram

3.11.5 USCI - SPI Dynamic Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI MASTER MODE (VDD = 3.0~3.6 V, 30 PF LOADING CAPACITOR)					
t_{CLKH}	Clock output High time [*1]			T_{SPICLK} / 2	ns
t_{CLKL}	Clock output Low time [*1]			T_{SPICLK} / 2	ns
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2	-	-	ns
t_V	Data output valid time	-	0	1	ns
SPI MASTER MODE (VDD = 1.8~2.0 V, 30 PF LOADING CAPACITOR)					
t_{CLKH}	Clock output High time [*1]			T_{SPICLK} / 2	ns
t_{CLKL}	Clock output Low time [*1]			T_{SPICLK} / 2	ns
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2	-	-	ns
t_V	Data output valid time	-	-	1	ns

Note:

1. The minimum clock period for SPICLK is 10.4 ns (96 MHz).

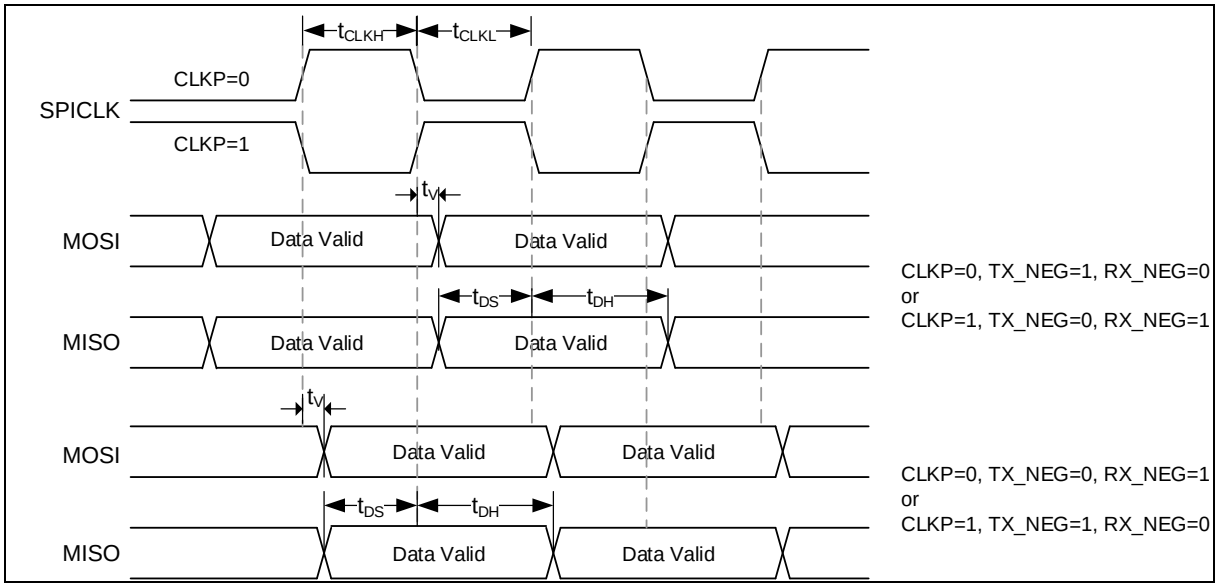


Figure 3.11-7 SPI Master Mode Timing Diagram

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI SLAVE MODE (VDD = 3.0~3.6V, 30 PF LOADING CAPACITOR)					
t_{CLKH}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns
t_{CLKL}	Clock output Low time [*1]	-		T_{SPICLK} / 2	ns
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	ns
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns
t_{DS}	Data input setup time	0	-	-	ns
t_{DH}	Data input hold time	2	-	-	ns
t_V	Data output valid time	-		8	ns
t_{CLKH}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns
SPI SLAVE MODE (VDD = 1.8 V ~ 2.0 V, 30 PF LOADING CAPACITOR)					
t_{CLKH}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns
t_{CLKL}	Clock output Low time [*1]	-	-	T_{SPICLK} / 2	ns
t_{SS}	Slave select setup time	1 T_{SPICLK} + 3ns	-	-	ns
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns
t_{DS}	Data input setup time	0	-	-	ns
t_{DH}	Data input hold time	2	-	-	ns
t_V	Data output valid time	-		10	ns

Note:

1. The minimum clock period for SPICLK is 10.4 ns (96 MHz).

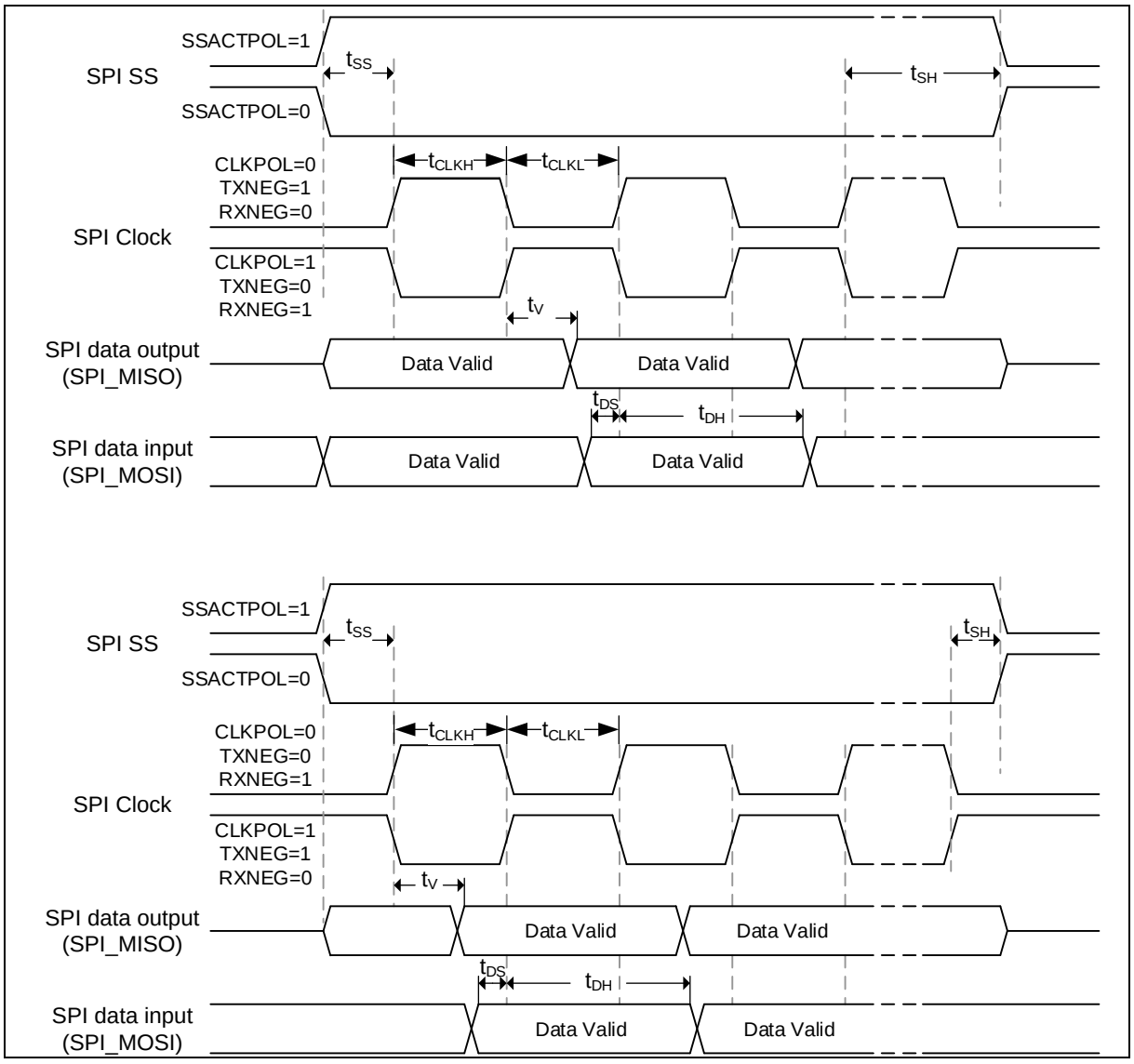


Figure 3.11-8 SPI Slave Mode Timing Diagram

3.11.6 Ethernet Characteristics

RMII Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_RMII\_REFCLK}$	RMII_REFCLK Period	-	20.0 +/- 50 ppm	-	ns	-
$T_{H\_RMII\_REFCLK}$	RMII_REFCLK High Time	8.0	10.0	12.0	ns	-
$T_{L\_RMII\_REFCLK}$	RMII_REFCLK Low Time	8.0	10.0	12.0	ns	-
$T_{DLY\_RMII\_TX}$	RMII_REFCLK Rising to Valid RMII_TXEN, RMII_TXDATA0 and RMII_TXDATA1 Delay	-	-	10	ns	-
$T_{SU\_RMII\_RX}$	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Setup Time to RMII_REFCLK Rising	5	-	-	ns	-
$T_{HD\_RMII\_RX}$	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Hold Time from RMII_REFCLK Rising	2	-	-	ns	-

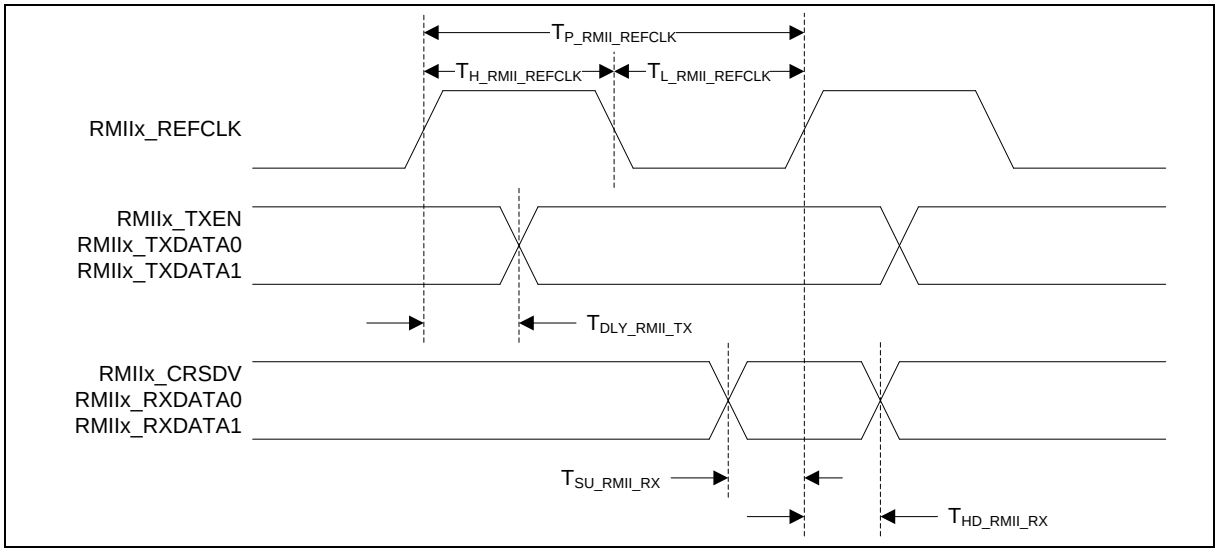


Figure 3.11-9 RMII Interface Timing Diagram

Ethernet PHY Management Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_RMII\_MDC}$	RMII_MDC Period	400	-	-	ns	-
$T_{H\_RMII\_MDC}$	RMII_MDC High Time	200	-	-	ns	-
$T_{L\_RMII\_MDC}$	RMII_MDC Low Time	200	-	-	ns	-
$T_{DLY\_RMII\_MDIOWR}$	RMII_MDC Falling to Valid RMII_MDIO Delay	-	-	10	ns	-
$T_{SU\_RMII\_MDIORD}$	RMII_MDIO Setup Time to RMII_MDC Rising	10	-	-	ns	-
$T_{HD\_RMII\_MDIORD}$	RMII_MDIO Hold Time from RMII_MDC Rising	10	-	-	ns	-

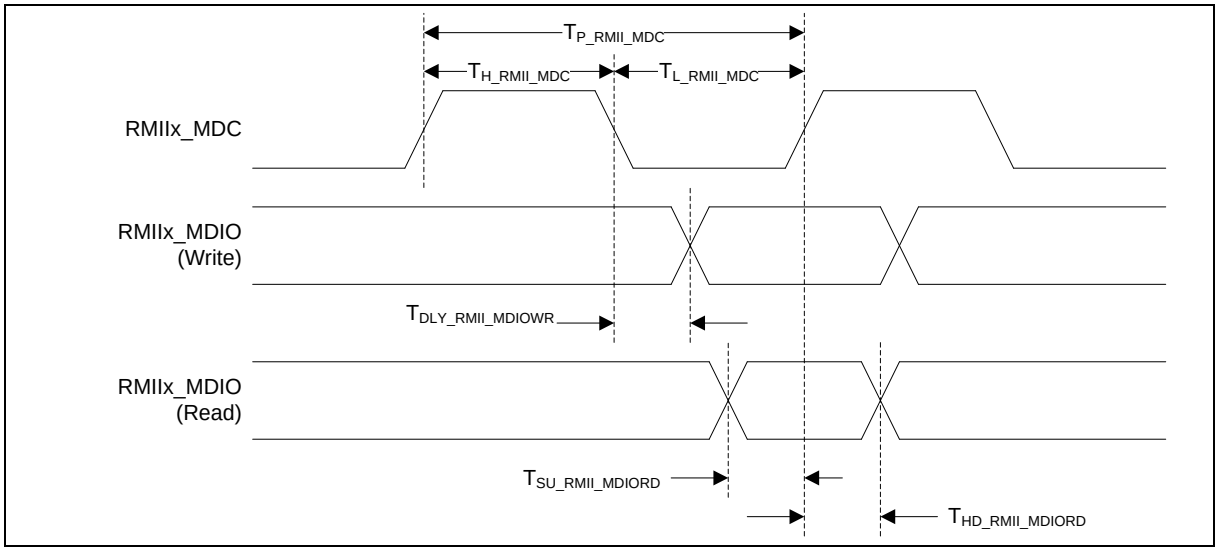


Figure 3.11-10 Ethernet PHY Management Interface Timing Diagram

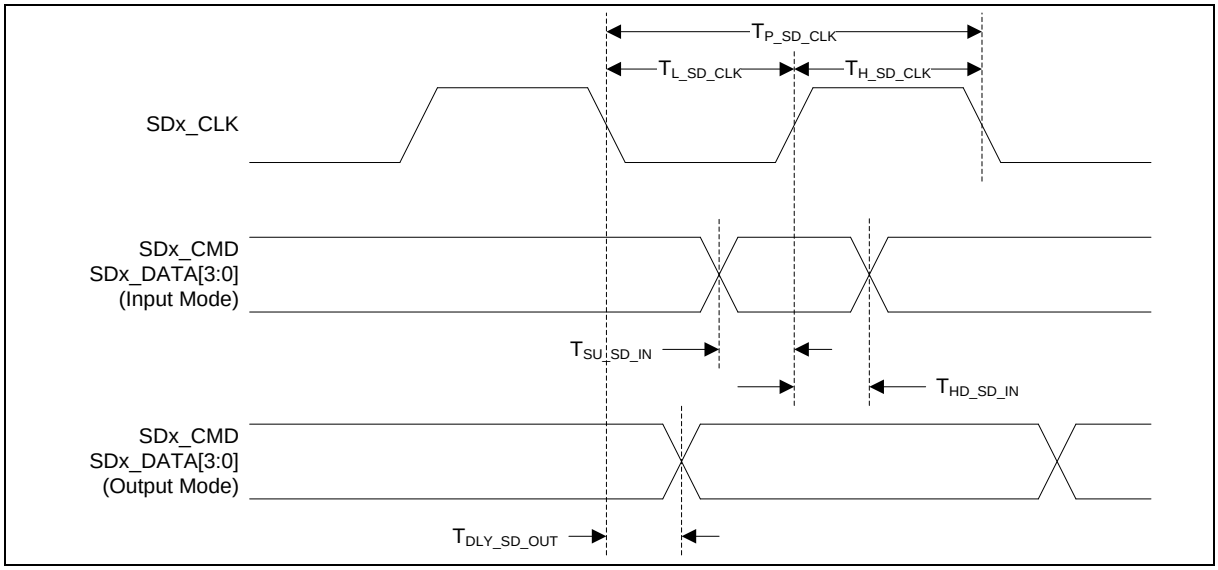


Figure 3.11-11 SDIO default mode

3.11.7 SDIO Dynamic characteristics

SDIO Default Mode Timing

在嗎	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_SD\_CLK}$	SD_CLK Period (Data Transfer Mode)	40	-	-	ns	-
$T_{P\_SD\_CLK\_ID}$	SD_CLK Period (Identification Mode)	2,500	-	-	ns	
$T_{H\_SD\_CLK}$	SD_CLK High Time	-	20	-	ns	-
$T_{L\_SD\_CLK}$	SD_CLK Low Time	-	20	-	ns	-
$T_{SU\_SD\_IN}$	SD_DATA Setup Time to SD_CLK Rising	5	-	-	ns	-
$T_{HD\_SD\_IN}$	SD_DATA Hold Time from SD_CLK Rising	5	-	-	ns	-
$T_{DLY\_SD\_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-

SDIO high-speed mode

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_SD\_CLK}$	SD_CLK Period	20	-	-	ns	-
$T_{H\_SD\_CLK}$	SD_CLK High Time	7	-	-	ns	-
$T_{L\_SD\_CLK}$	SD_CLK Low Time	7	-	-	ns	-
$T_{SU\_SD\_IN}$	SD_DATA Setup Time to SD_CLK Rising	6	-	-	ns	-
$T_{HD\_SD\_IN}$	SD_DATA Hold Time from SD_CLK Rising	2	-	-	ns	-
$T_{DLY\_SD\_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-
$T_{HD\_SD\_OUT}$	SD_DATA Hold Time from SD_CLK Rising	2.5	-	-	ns	-

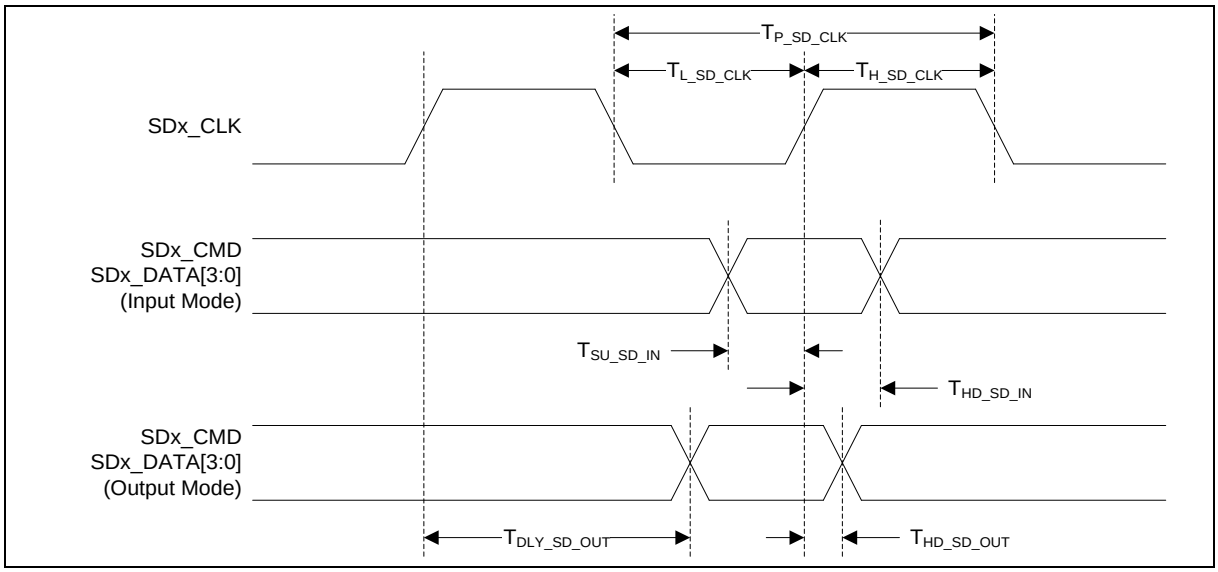


Figure 3.11-12 SDIO high-speed mode

3.11.8 ESC I2C Timing

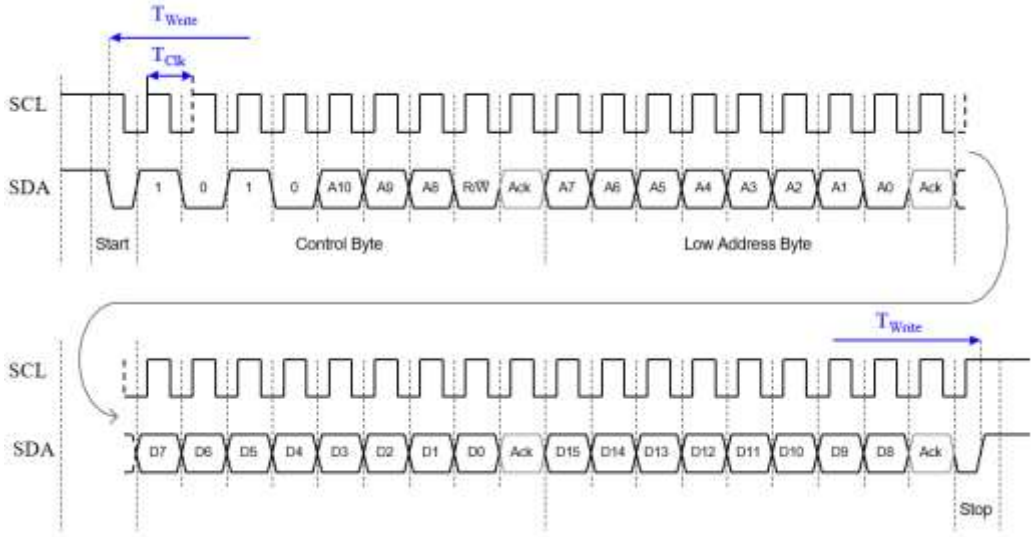


Figure 3.11-13: Write access (1 address byte, up to 16 Kbit EEPROMs)

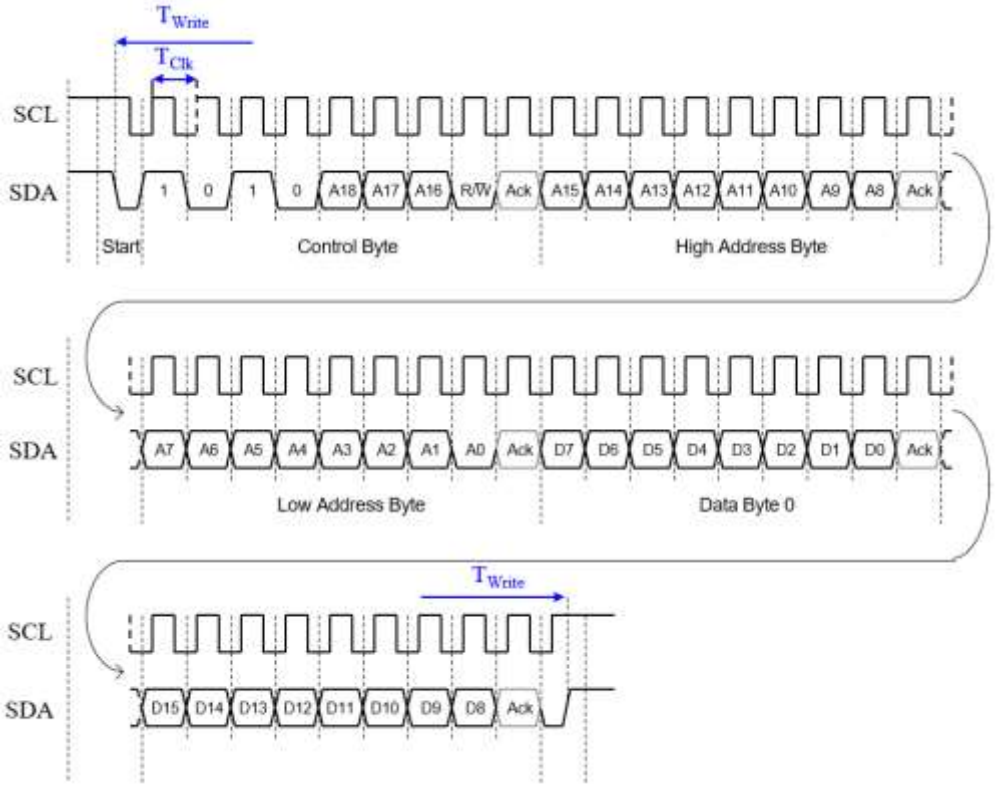


Figure 3.11-14: Write access (2 address bytes, 32 Kbit - 4 Mbit EEPROMs)

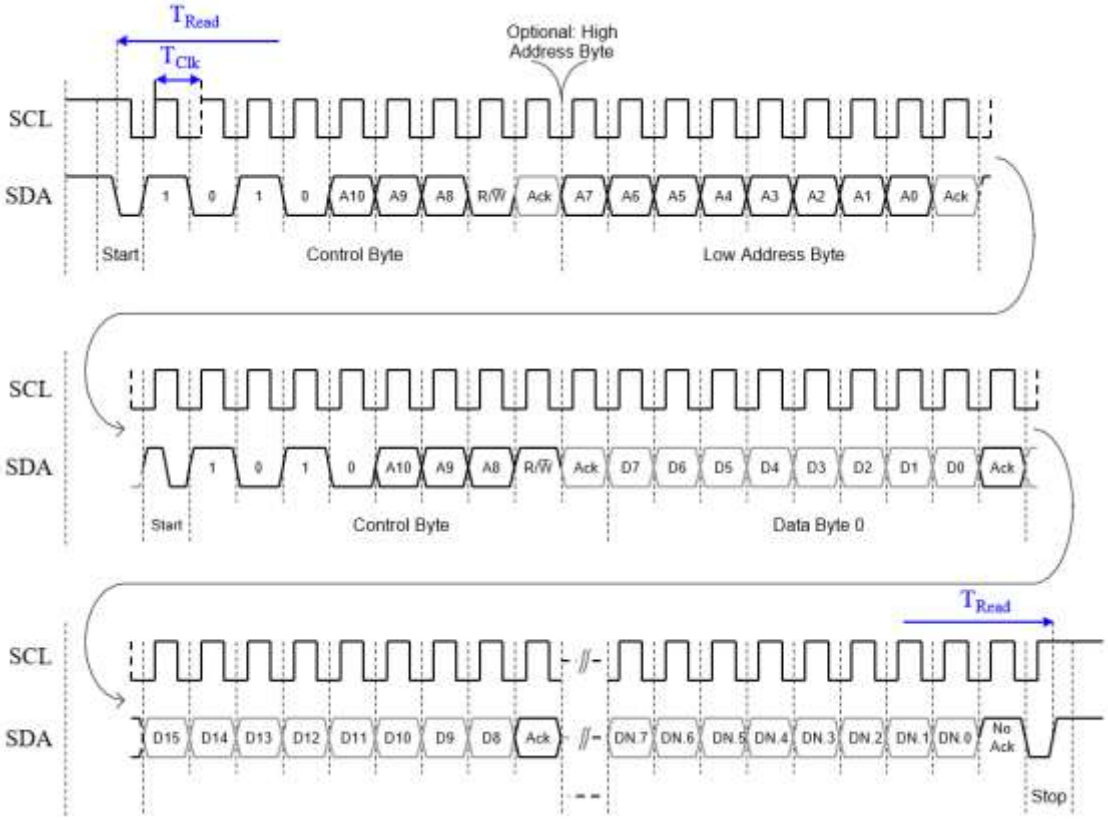


Figure 3.11-15: Read access (1 address byte, up to 16 Kbit EEPROMs)

Symbol	Parameter		Typical		Units
			Up to 16 Kbit	32 Kbit-4 Mbit	
T_{Clk}	EEPROM clock period		6.72 (≈ 150 KHz)		us
T_{Write}	Write access time (without errors)		250	310	us
T_{Read}	Read access time (without errors):	2 words	440	500	us
		configuration (8 Words)	1.16	1.22	ms
T_{Delay}	Time until configuration loading begins after Reset is gone		65.5		us

Table 3.11-1: I²C EEPROM Timing Table

3.11.9 ESC Port 2 MII Timing

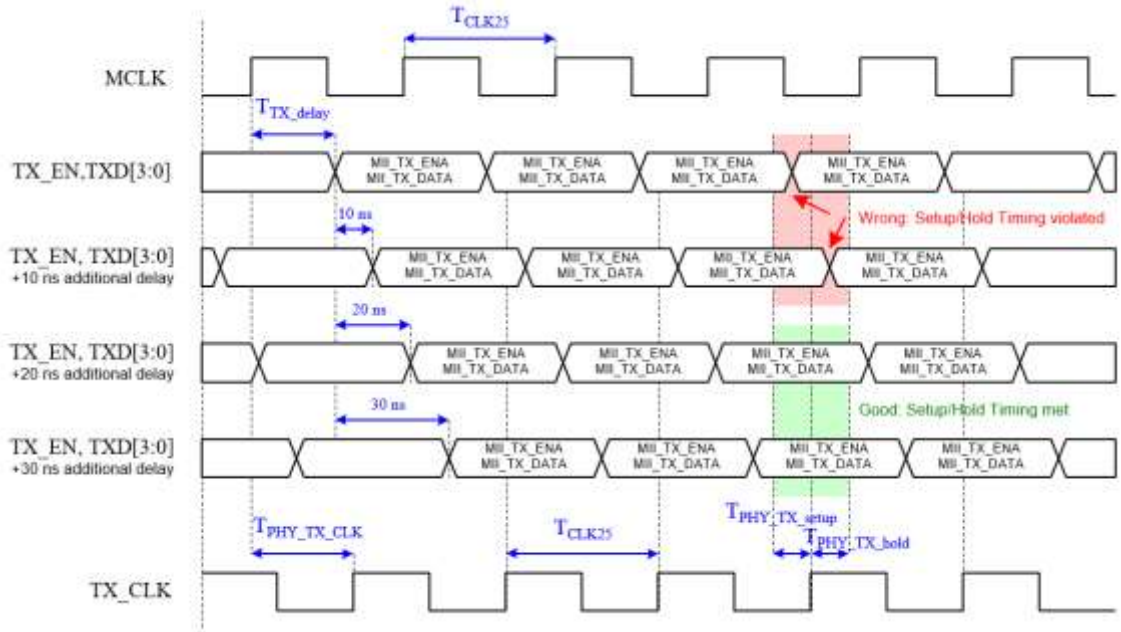


Figure 3.11-16: Port 2 MII TX Timing Diagram

Symbol	Description	Min	Typ	Max	Units
T_{CLK25}	MCLK output	-	40	-	ns
T_{TX_delay}	TX_EN/TXD[3:0] delay after rising edge of MCLK	-	-	2	ns
$T_{PHY\_TX\_CLK}$	Delay between MCLK and TX_CLK output of the PHY	-	PHY dependent	-	ns
$T_{PHY\_TX\_setup}$	PHY setup time	PHY dependent	-	-	ns
$T_{PHY\_TX\_hold}$	PHY hold time	PHY dependent	-	-	ns

Table 3.11-2: Port 2 MII TX Timing Table

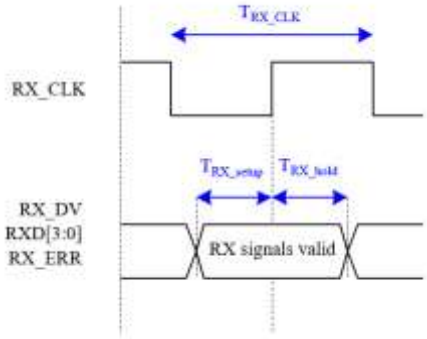


Figure 3.11-17: Port 2 MII RX Timing Diagram

Symbol	Description	Min	Typ	Max	Units
T_{RX_CLK}	RX_CLK period (100 PPM with maximum FIFO Size only)	-	40	-	ns
T_{RX_setup}	RX_DV/RX_ER/RXD[3:0] valid before rising edge of RX_CLK	2.1	-	-	ns
T_{RX_hold}	RX_DV/RX_ER/RXD[3:0] valid after rising edge of RX_CLK	0.5	-	-	ns

Table 3.11-3: Port 2 MII RX Timing Table

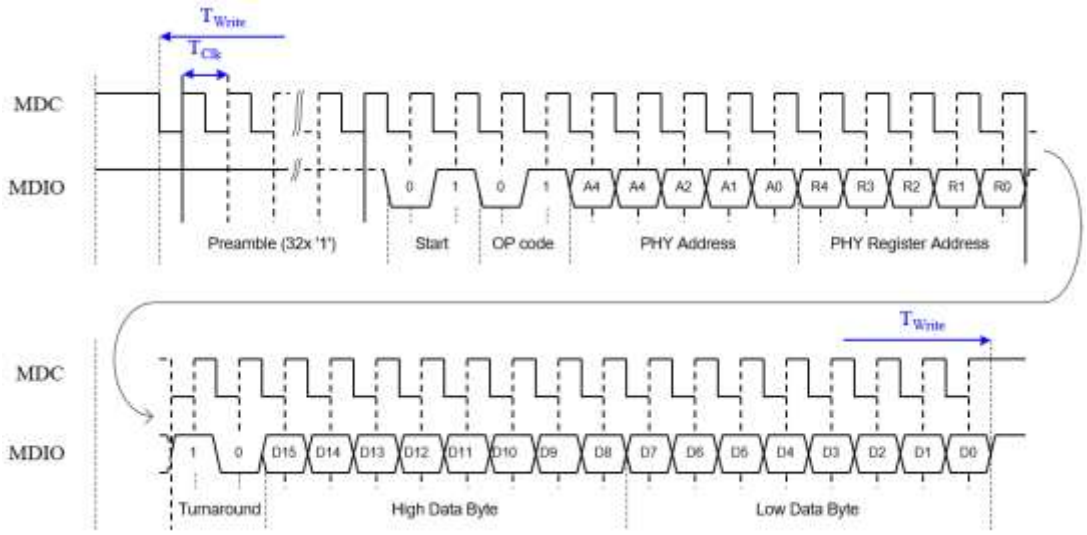


Figure 3.11-18: MDC/MDIO Write access

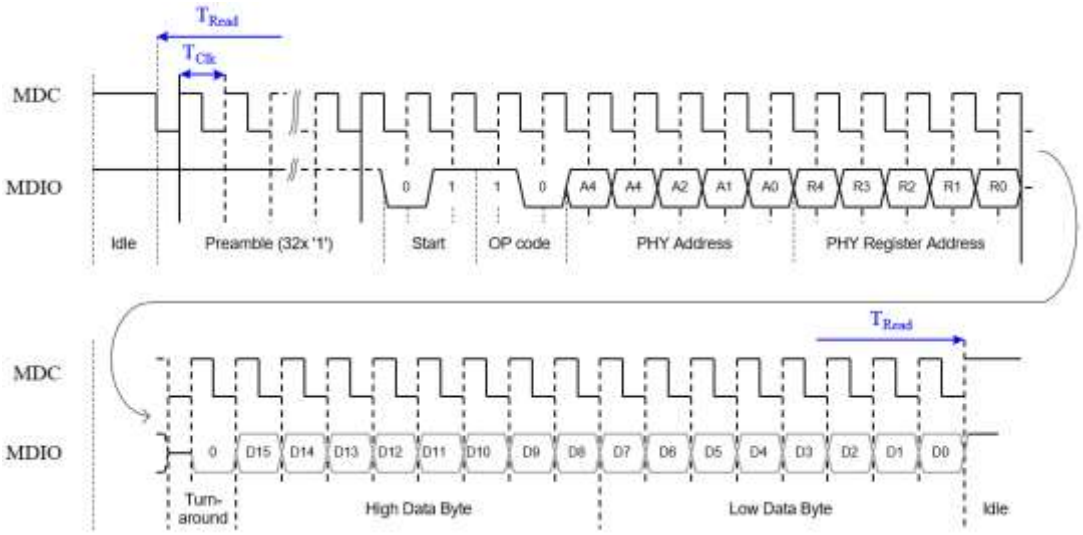


Figure 3.11-19: MDC/MDIO Read access

Symbol	Description	Min	Typ	Max	Units
T_{MDC}	MDC period		400 (≈ 2.5 MHz)		ns
T_{Write}	MI Write access time		25.6		us
T_{Read}	MI Read access time		25.4		us
$T_{MI\_startup}$	Time between reset end and the first access of MI Link detection and configuration		1.34		ms

Table 3.11-4: MDC/MDIO Timing Table

3.11.10 Distributed Clocks SYNC/LATCH

Symbol	Description	Min	Typ	Max	Units
T_{DC_LATCH}	Time between LATCH 0/1 events	12			ns
$T_{DC\_SYNC\_Jitter}$	SYNC 0/1 output jitter			12	ns

Table 3.11-5: DC SYNC/LATCH timing characteristics

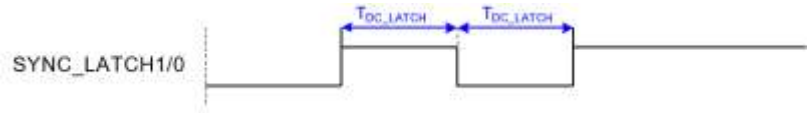


Figure 3.11-20: LATCH timing

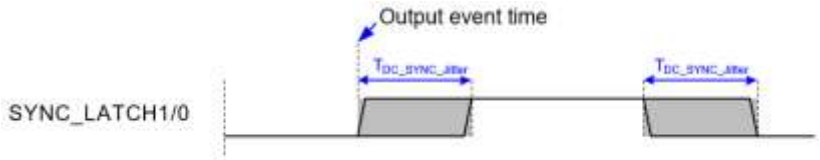


Figure 3.11-21: SYNC timing

3.11.11 ESC Digital I/O Timing

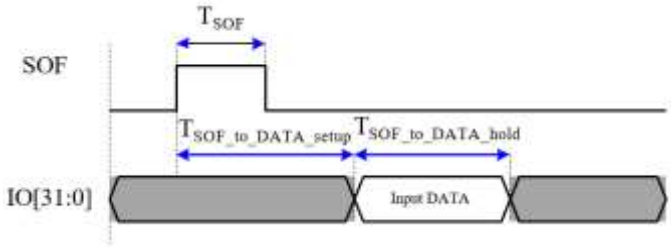


Figure 3.11-22: Digital Input: Input data sampled at SOF, IO can be read in the same frame

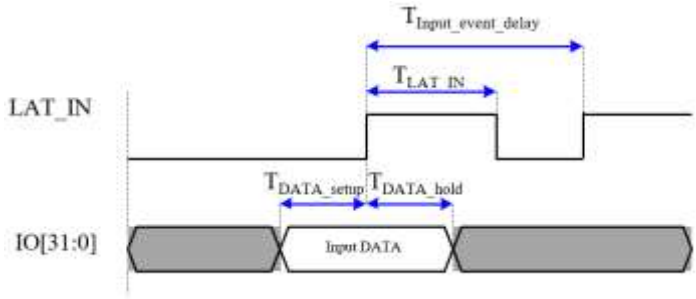


Figure 3.11-23: Digital Input: Input data sampled with LATCH_IN

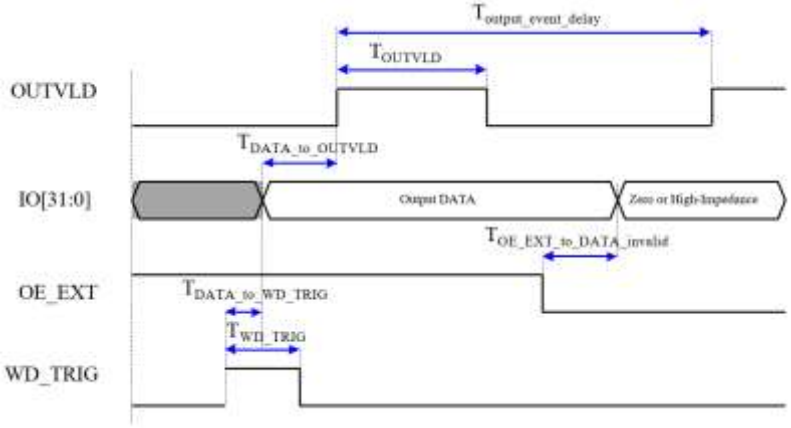


Figure 3.11-24: Digital Output timing

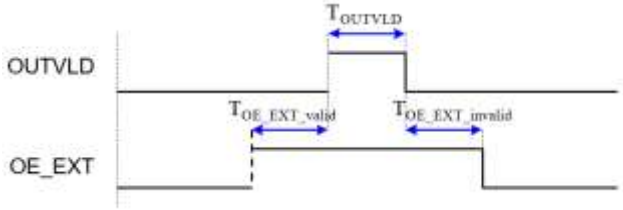


Figure 3.11-25: OE_EXT timing

Symbol	Description	Min	Typ	Max	Units
T_{DATA_setup}	Input data valid before LAT_IN	5	-	-	ns
T_{DATA_hold}	Input data valid after LAT_IN	2	-	-	ns
T_{LAT_IN}	LAT_IN high time	4	-	-	ns
T_{SOF}	SOF high time	-	40	-	ns
$T_{SOF\_to\_DATA\_setup}$	Input data valid after SOF, so that Inputs can be read in the same frame	0	-	1.2	us
$T_{SOF\_to\_DATA\_hold}$	Input data invalid after SOF	1.6	-	-	us
$T_{input\_event\_delay}$	Time between consecutive input events	440	-	-	ns
T_{OUTVLD}	OUTVLD high time	-	80	-	ns
$T_{DATA\_to\_OUTVLD}$	Output data valid before OUTVLD	79	-	-	ns
T_{WD_TRIG}	WD_TRIG high time	-	40	-	ns
$T_{DATA\_to\_WD\_TRIG}$	Output data valid after WD_TRIG	-	-	20	ns
$T_{OE\_EXT\_to\_DATA\_invalid}$	Outputs zero or Outputs hi-Z after OE_EXT set to low	0	-	9.5	ns
$T_{output\_event\_delay}$	Time between consecutive output events	320	-	-	ns
$T_{OUT\_EXT\_valid}$	OUT_EXT valid before OUTVLD	-	80	-	ns
$T_{OUT\_EXT\_invalid}$	OUT_EXT invalid after OUTVLD	-	80	-	ns

Table 3.11-6: Digital I/O timing Table

3.11.12 ESC PDI SPI Slave Timing

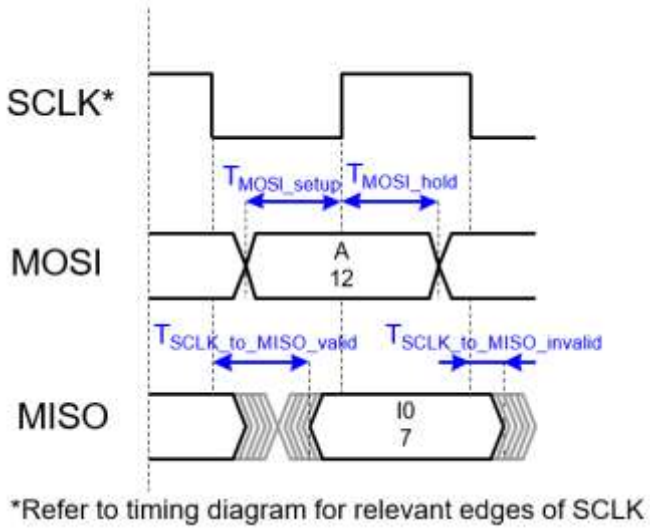


Figure 3.11-26: Basic MOSI/MISO timing

Symbol	Description		Min	Typ	Max	Units
T_{SCLK}	SCLK frequency		21 (≤47MHz)	-	-	ns
$T_{SEL\_to\_CLK}$	First SCLK cycle after SCS_ESC asserted		5	-	-	ns
$T_{CLK\_to\_SEL}$	Deassertion of SCS_ESC after last SCLK cycle	SPI mode 0/2, SPI mode 1/3 with normal data out sample	5	-	-	ns
		SPI mode 1/3 with late data out sample	T_{CLK}/2+ 5			
T_{read}	Only for read access between address/command and first data byte. Can be ignored if BUSY or Wait State Bytes are used.		240	-	-	ns
T_{access_delay}	Delay between SPI accesses		40	-	-	ns
T_{MOSI_setup}	MOSI valid before SCLK edge		3	-	-	ns
T_{MOSI_hold}	MOSI valid after SCLK edge		0	-	-	ns
$T_{SCLK\_to\_MISO\_valid}$	MISO valid after SCLK edge		-	-	10.5	ns
$T_{SCLK\_to\_MISO\_invalid}$	MISO invalid after SCLK edge		0	-	-	ns
T_{IRQ_delay}	Internal delay between AL event and SINT output to enable correct reading of the interrupt registers.		-	180	-	ns

Table 3.11-7: PDI SPI Slave Timing Table

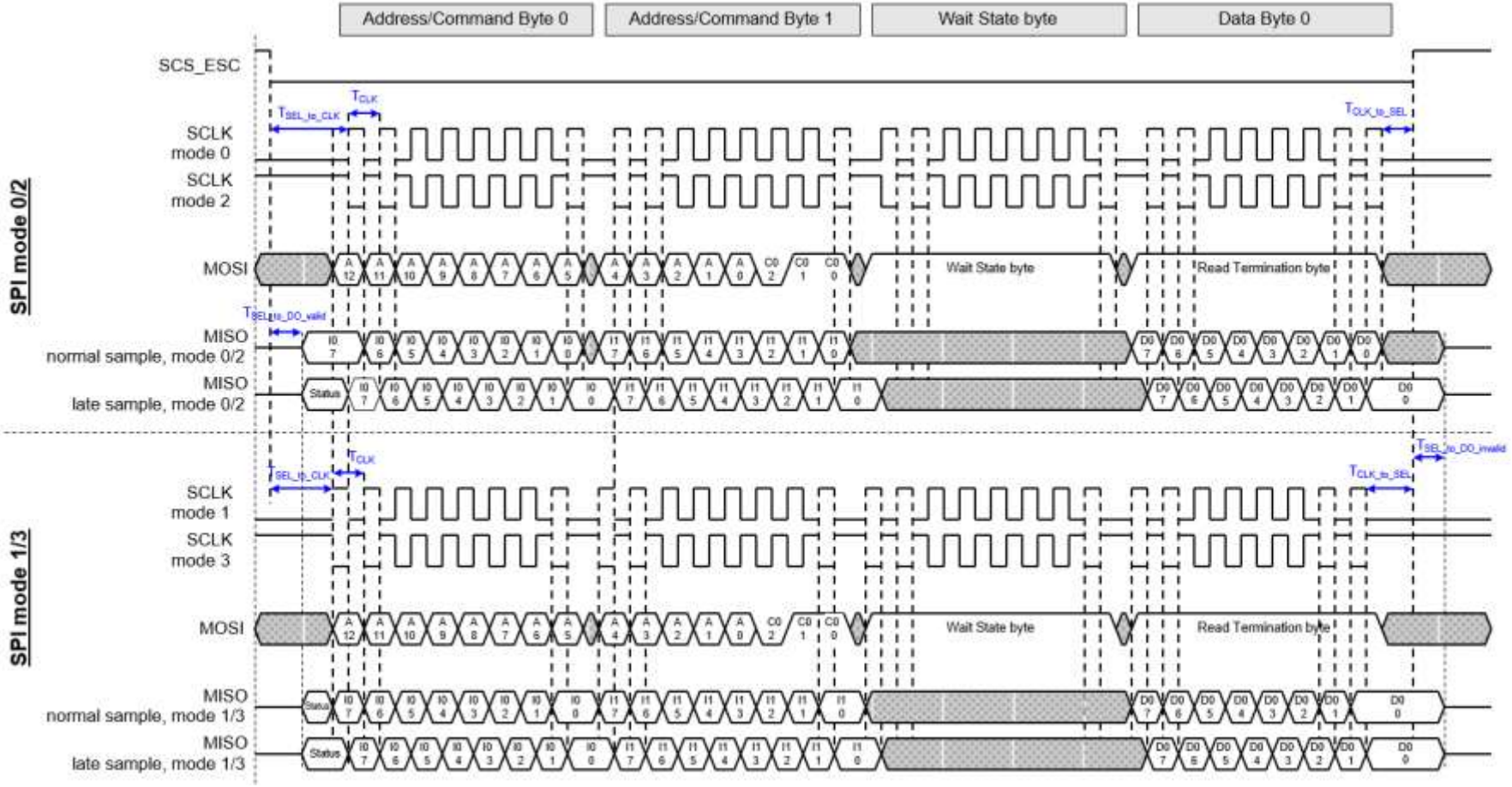


Figure 3.11-27: PDI SPI Slave read access (2 byte addressing, 1 byte read data) with Wait State byte

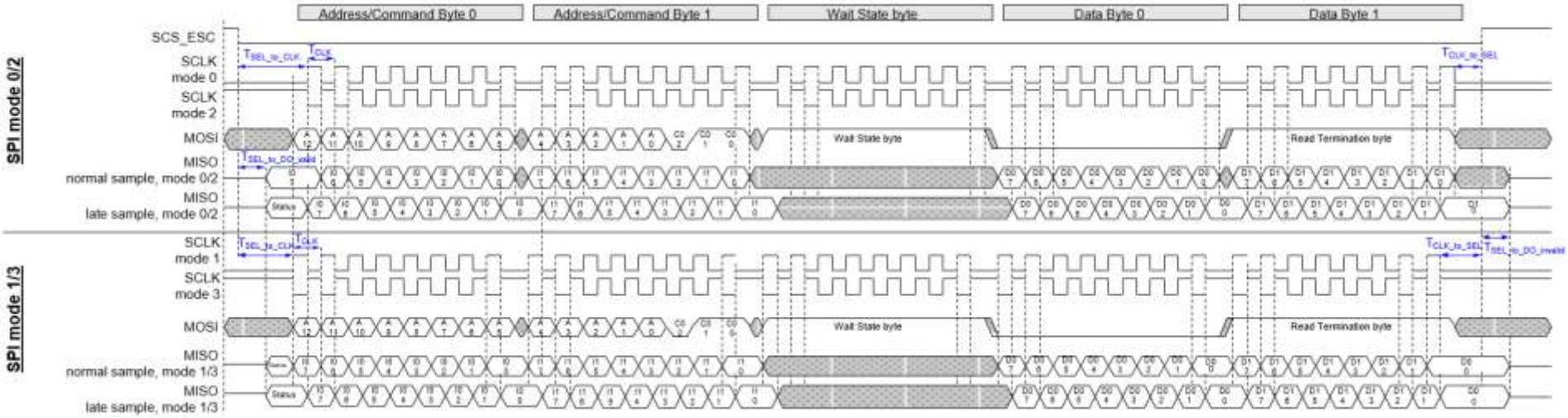


Figure 3.11-28: PDI SPI Slave read access (2 byte addressing, 2 byte read data) with Wait State byte

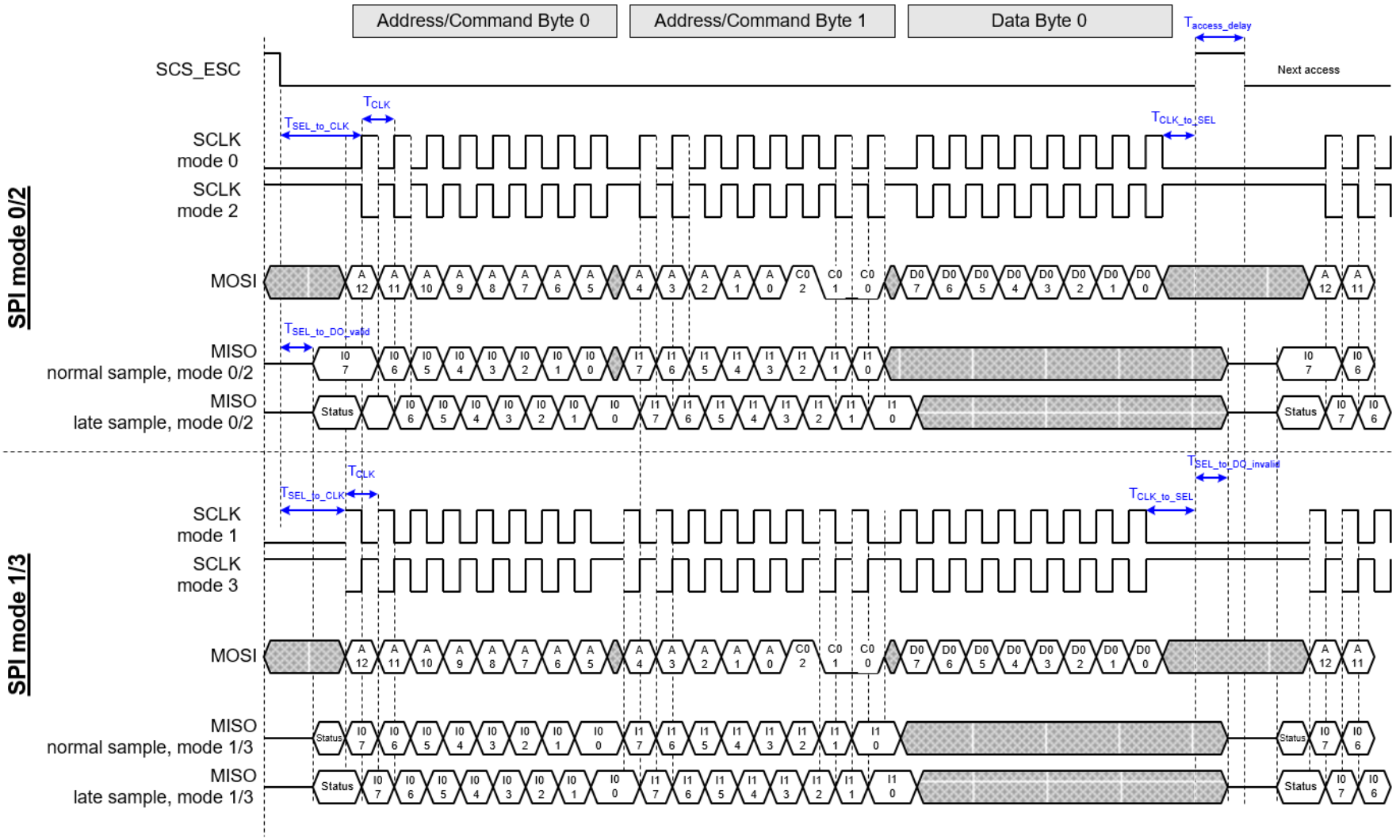


Figure 3.11-29: PDI SPI Slave write access (2 byte addressing, 1 byte write data)

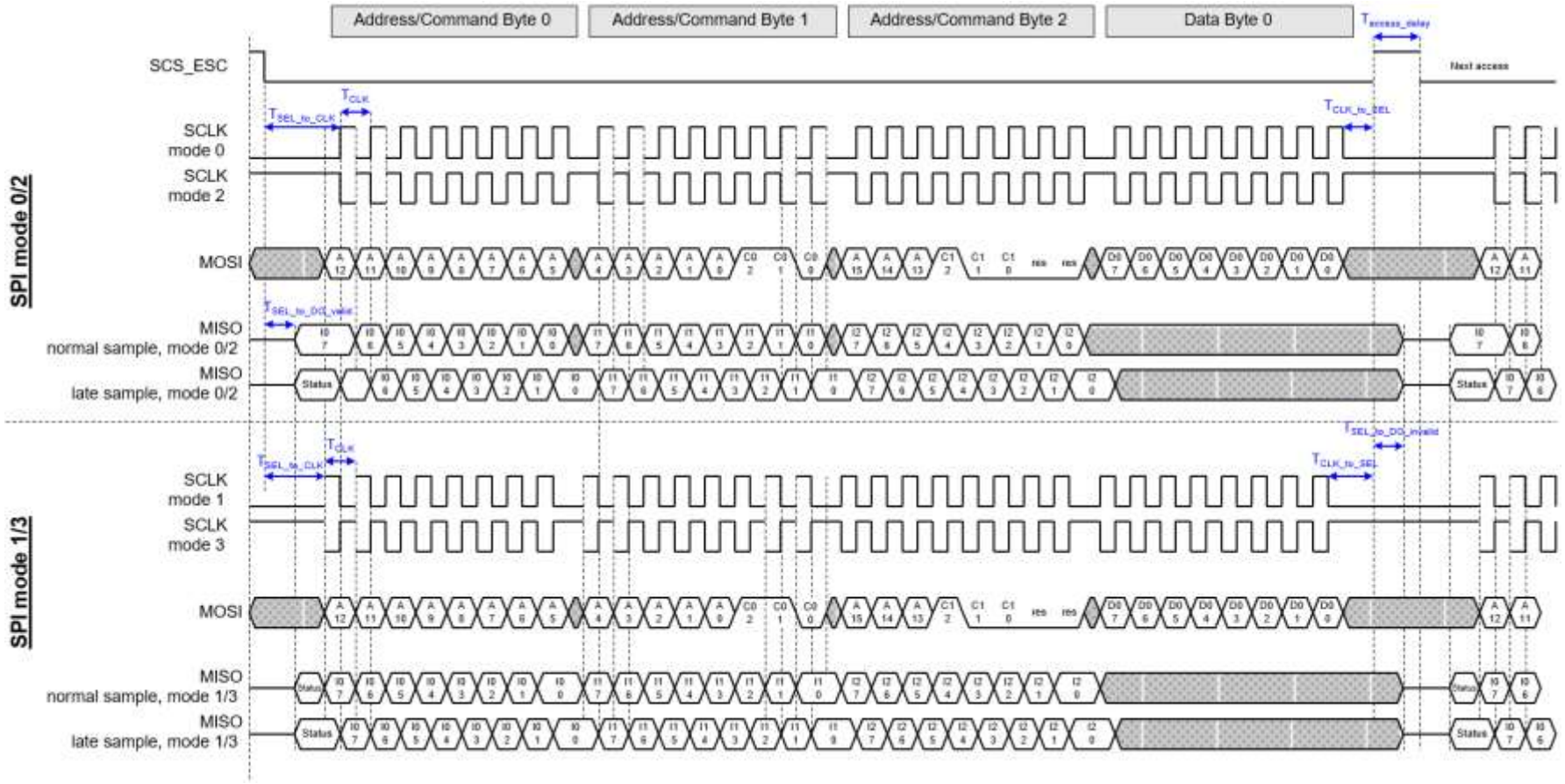


Figure 3.11-30: PDI SPI Slave write access (3 byte addressing, 1 byte write data)

3.11.13 Function SPI Slave Timing

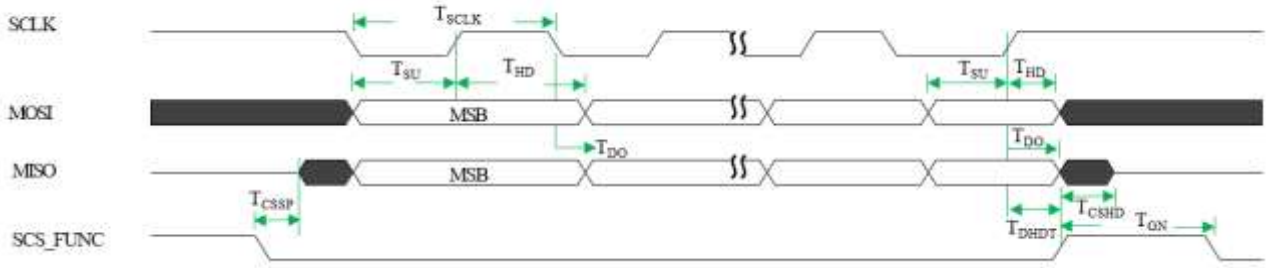


Figure 3.11-31: Function SPI Slave with share pin Timing Diagram

Symbol	Description	Min	Typ	Max	Units
T_{SCLK}	SCLK clock frequency	-	-	50	MHz
T_{DO}	MISO data valid time after SCLK edge	9.2	-	-	ns
T_{SU}	MOSI data setup time before SCLK edge	2	-	-	ns
T_{HD}	MOSI data hold time after SCLK edge	2	-	-	ns
T_{CSSP}	SCS setup time before MISO active	7.6	-	-	ns
T_{DHD}	SCS hold time after SCLK edge	21	-	-	ns
T_{CSHD}	MISO data hold time after SCS de-assert	2.6	-	-	ns
T_{GN}	SCS negation to next SCS assertion time	40	-	-	ns

Table 3.11-8: Function SPI with share pin Timing Table

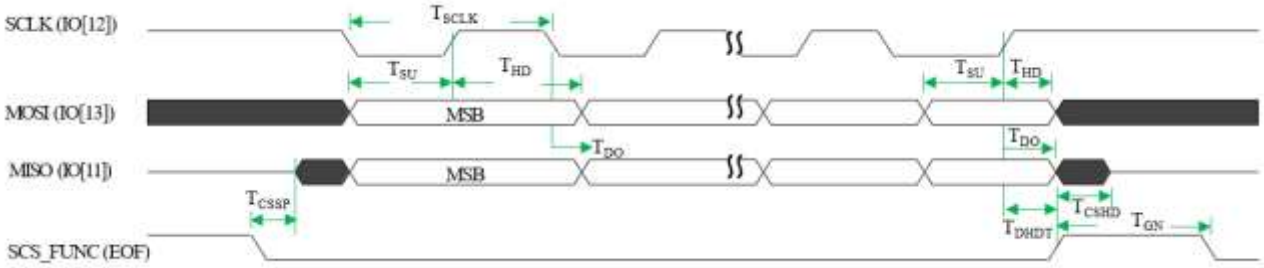


Figure 3.11-32: Function SPI Slave with individual pin Timing Diagram

Symbol	Description	Min	Typ	Max	Units
T_{SCLK}	SCLK clock frequency	-	-	47.5	MHz
T_{DO}	MISO data valid time after SCLK edge	10.5	-	-	ns
T_{SU}	MOSI data setup time before SCLK edge	2	-	-	ns
T_{HD}	MOSI data hold time after SCLK edge	2	-	-	ns
T_{CSSP}	SCS setup time before MISO active	7.7	-	-	ns
T_{DHD}	SCS hold time after SCLK edge	21	-	-	ns
T_{CSHD}	MISO data hold time after SCS de-assert	2.5	-	-	ns
T_{GN}	SCS negation to next SCS assertion time	40	-	-	ns

Table 3.11-9: Function SPI with individual pin Timing Table

3.11.14 PWM Motor Controller Timing

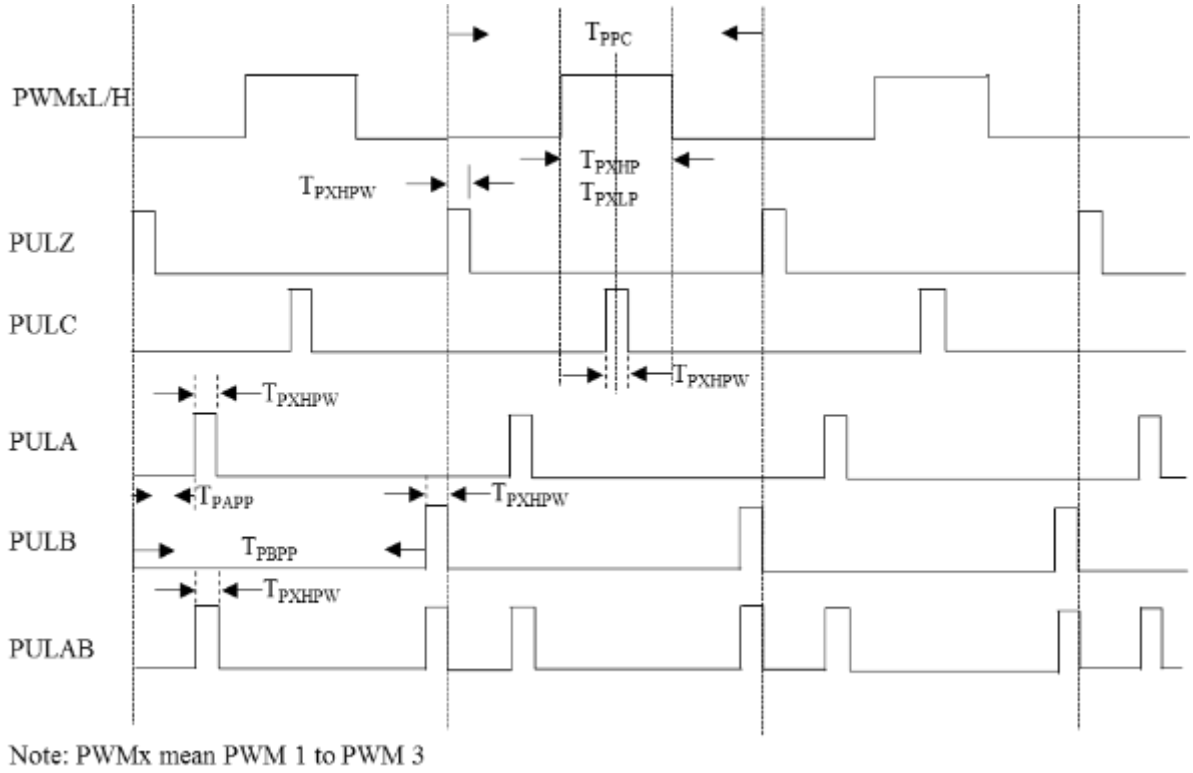


Figure 3.11-33: PWMx Timing

Symbol	Description	EN8X	Min	Typ	Max	Units
T_{PPC}	PWM Period Cycle	x1	-	PPC * 10	-	ns
		x8	-	PPC * 80	-	ns
T_{PxHP}	PWM x High pulse Width set by PxHPWR	x1	-	PxHPV * 10*1	-	ns
		x8	-	PxHPV * 80*1	-	ns
T_{PxLP}	PWM x Low pulse Width set by PxHPWR	x1	-	PxHPV * 10*1	-	ns
		x8	-	PxHPV * 80*1	-	ns
T_{PXHPW}	Pulse width for PULZ, PULC, PULA, PULB, and PULAB	x1	-	PXHPW * 10	-	ns
		x8	-	PXHPW * 80	-	ns
T_{PAPP}	PWM Trigger Pulse A Position in PWM Period Cycle	x1	-	PTAPP * 10	-	ns
		x8	-	PTAPP * 80	-	ns
T_{PBPP}	PWM Trigger Pulse B Position in PWM Period Cycle	x1	-	PTBPP * 10	-	ns
		x8	-	PTBPP * 80	-	ns

Note *1: “x” = 1 ~ 3

Table 3.11-10: PWMx Timing Table

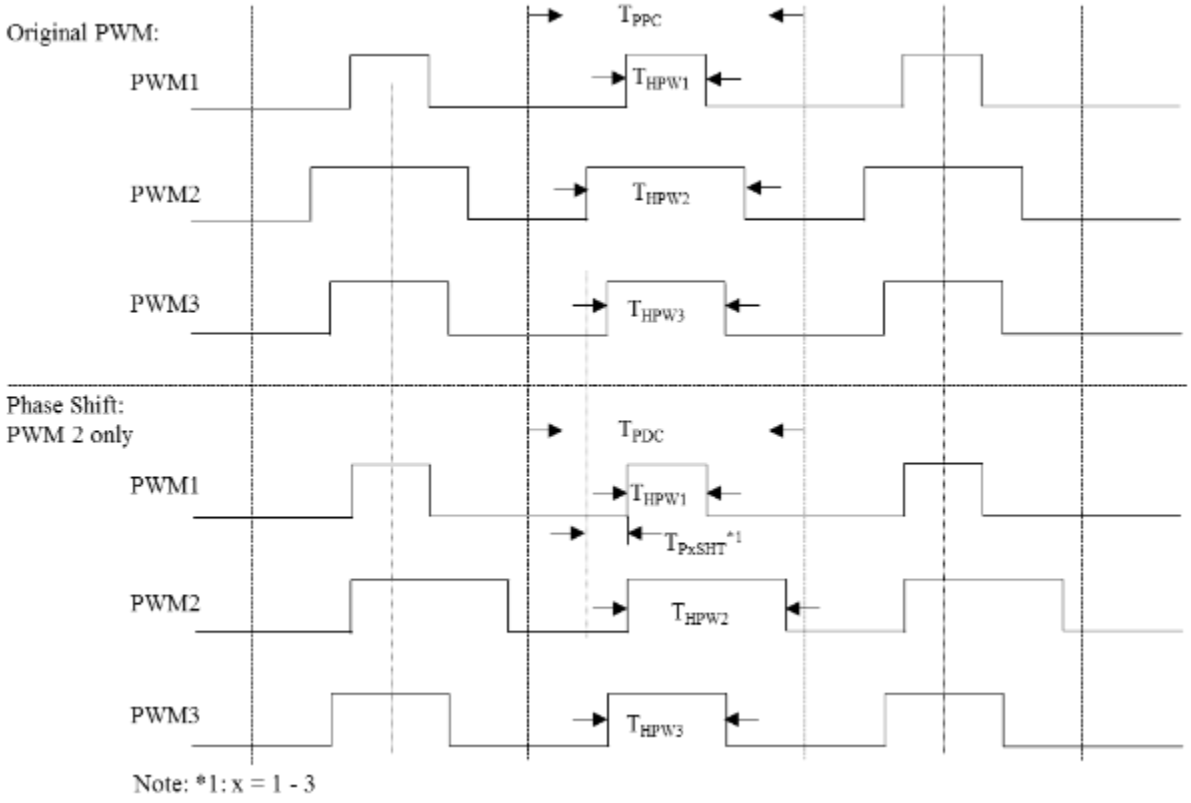


Figure 3.11-34: Only PWM Channel 2 Shift Diagram

Symbol	Description	EN8X	Min	Typ	Max	Units
T_{P1SHT}	PWM pulse was postponed raising time (addition with P1SHR) and the pulse width stays the same	x1	-	P1SHIFT * 10	-	ns
		x8	-	P1SHIFT * 80	-	ns
T_{P2SHT}	Please reference T_{P1SHT} content	x1	-	P2SHIFT * 10	-	ns
		x8	-	P2SHIFT * 80	-	ns
T_{P3SHT}	Please reference T_{P1SHT} content	x1	-	P3SHIFT * 10	-	ns
		x8	-	P3SHIFT * 80	-	ns

Table 3.11-11: PWMx Shift Timing Table

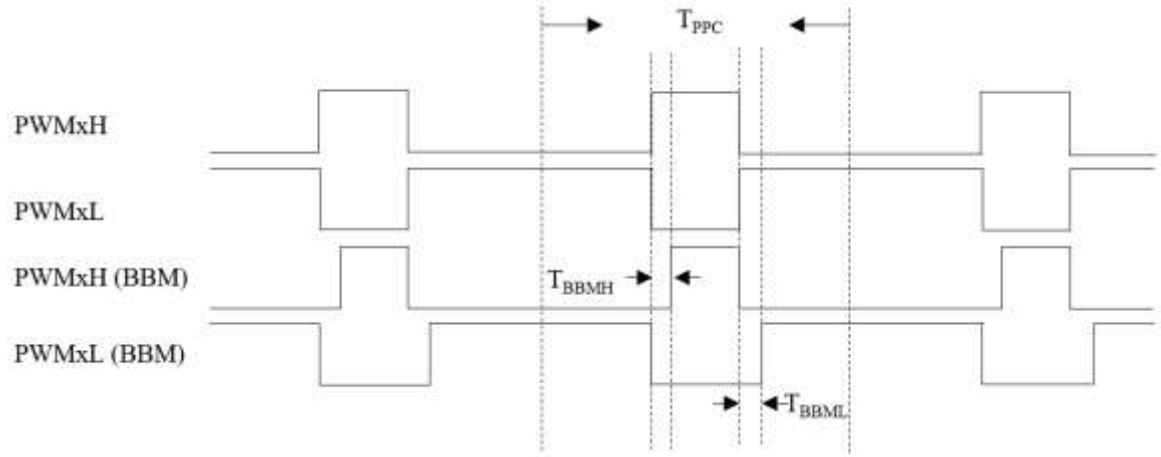


Figure 3.11-35: BBM (Break Before Make) Timing Diagram

Symbol	Description	EN8X	Min	Typ	Max	Units
T_{BBMH}	High pulse was postponed raising and reduce pulse width	x1	-	PBBMH * 10	-	ns
		x8	-	PBBMH * 80	-	ns
T_{BBML}	Low pulse was postponed falling and addition pulse width	x1	-	PBBML * 10	-	ns
		x8	-	PBBML * 80	-	ns

Table 3.11-12: PWMx BBM Timing Table

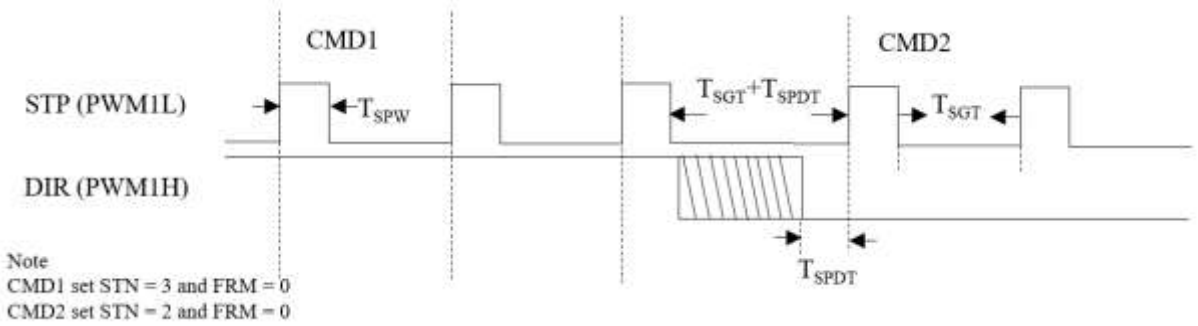


Figure 3.11-36: One Shot with multi Step Timing Diagram

Symbol	Description	Min	Typ	Max	Units
T_{SGT}	Step Pulse to Pulse Gap time set by SGTLR and SGTHR	-	SGT * 10	-	ns
T_{SPW}	Step Pulse Width set by SHPWR Note: Step frequency = 1/ (T_{SPW} +T_{SGT})	-	SPW * 10	-	ns
T_{SPDY}	Direction Transform Delay Time set by TDLYR	-	SPDT * 10	-	ns

Table 3.11-13: Step function timing table

3.11.15 Incremental and Hall Encoder Interface Timing

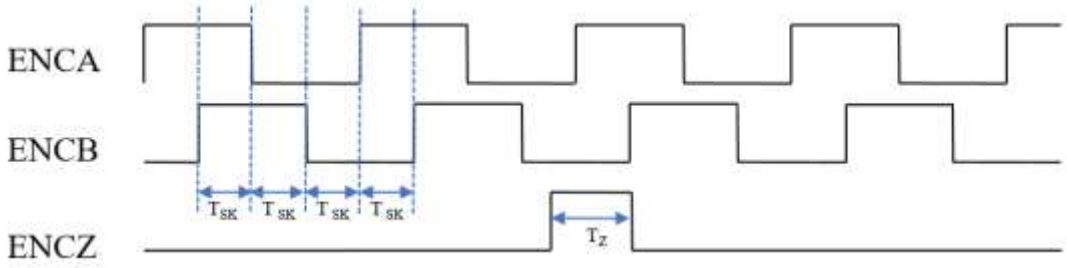


Figure 3.11-37: ABZ Timing Diagram

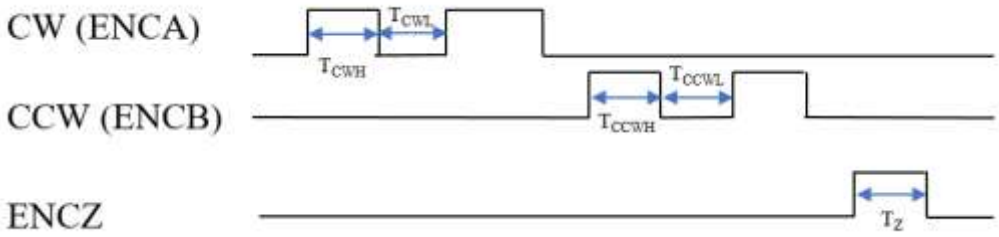


Figure 3.11-38: CW/CCW Timing Diagram

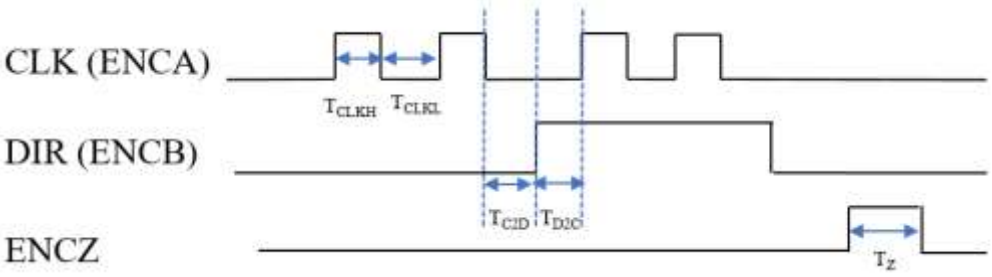


Figure 3.11-39: CLK/DIR Timing Diagram

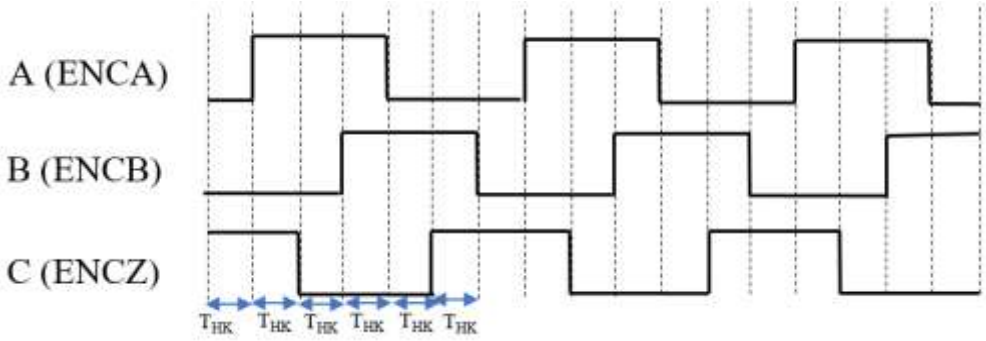


Figure 3.11-40: Hall Timing Diagram

Symbol	Description	Min	Typ	Max	Units
T_{SK}	AB state keep time	30	-	-	ns
T_{Z}	Z Pulse Width	30	-	-	ns
T_{CWH}	CW high time	30	-	-	ns
T_{CWL}	CW low time	30	-	-	ns
T_{CCWH}	CCW high time	30	-	-	ns
T_{CCWL}	CCW low time	30	-	-	ns
T_{CLKH}	CLK high time	30	-	-	ns
T_{CLKL}	CLK low time	30	-	-	ns
T_{C2D}	CLK to DIR time	30	-	-	ns
T_{D2C}	DIR to CLK time	30	-	-	ns
T_{HK}	Hall state keeps time	60	-	-	ns

Table 3.11-14: Incremental and Hall Encoder Timing Table

3.11.16 ESC SPI Master Timing

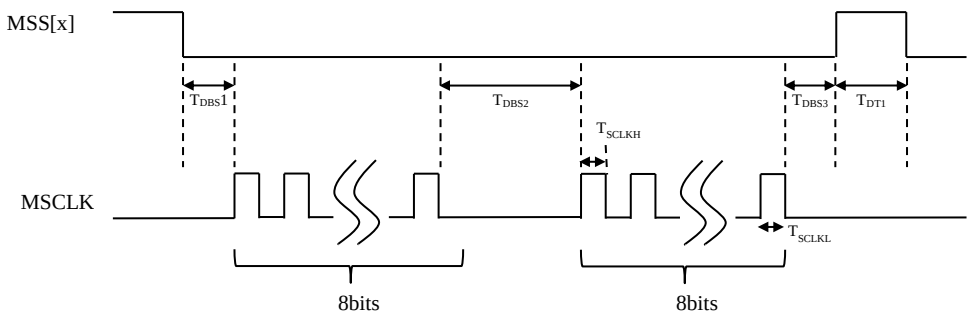


Figure 3.11-41: SPI Master Timing

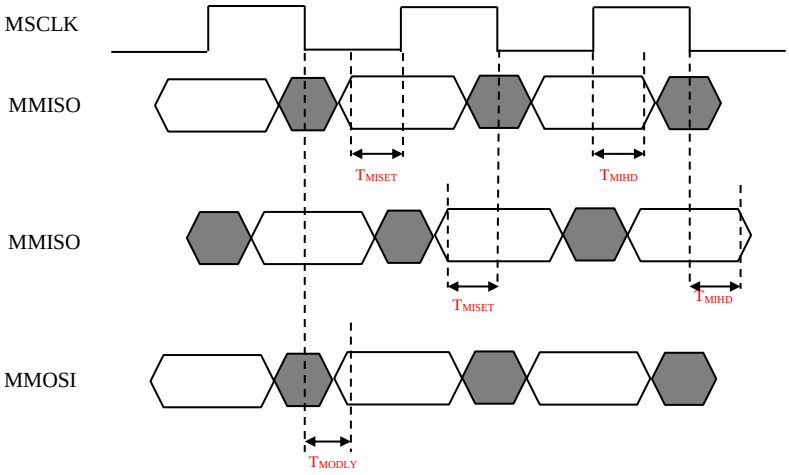


Figure 3.11-42: MMISO /MMOSIO Timing

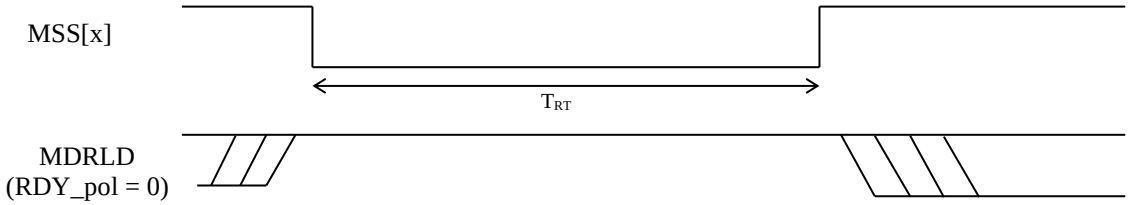


Figure 3.11-43: SPI MDRLD Ready Timeout Timing

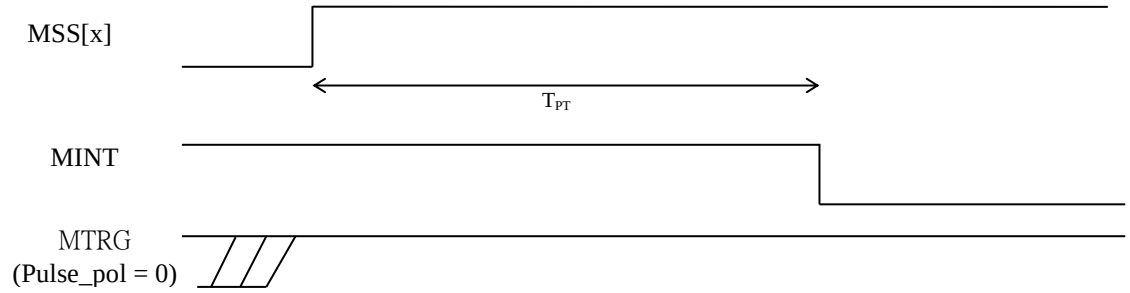


Figure 3.11-44: SPI MTRG Trigger Pulse Timeout

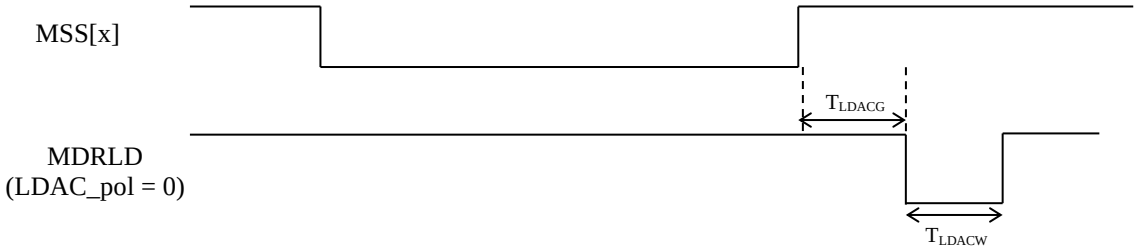
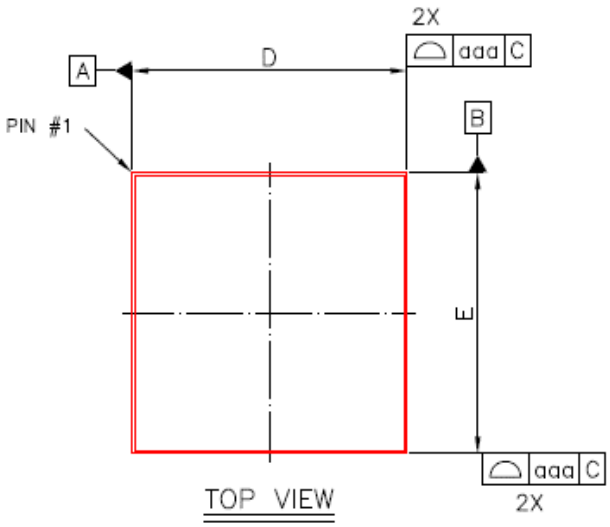


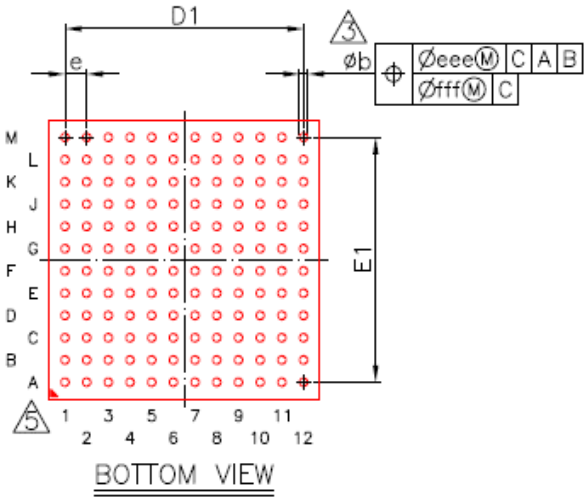
Figure 3.11-45: SPI MDRLD Trigger LDAC Gap and Width Timing

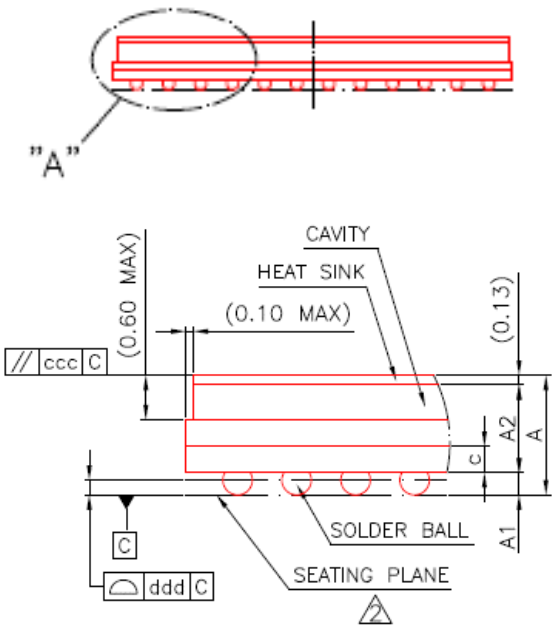
Symbol	Description	Min	Typ	Max	Units
Clock					
T_{SCLK}	MSCLK Period	-	T_{SCLKH} + T_{SCLKL}	-	ns
T_{SCLKH}	MSCLK high	-	5 * Divide	-	ns
T_{SCLKL}	MSCLK low	-	5 * Divide	-	ns
Bus Timing					
T_{DBS1}	MSS[x] to MSCLK (Mode0/1 without DBS1K)	-	(DBS + 1) * Tsclk	-	ns
	MSS[x] to MSCLK (Mode2/3 without DBS1K)	-	(DBS + 0.5) * Tsclk	-	ns
	MSS[x] to MSCLK (Mode0/1 with DBS1K)	-	((1024 * (DBS + 1)) + 1) * Tsclk	-	ns
	MSS[x] to MSCLK (Mode2/3 with DBS1K)	-	((1024 * (DBS + 1)) + 0.5) * Tsclk	-	ns
T_{DBS2}	Byte to byte (Mode0/1 without DBS1K)	-	(DBS + 0.5) * Tsclk	-	ns
	Byte to byte (Mode2/3 without DBS1K)	-	(DBS + 0.5) * Tsclk	-	ns
	Byte to byte (Mode0/1 with DBS1K)	-	((1024 * (DBS + 1)) + 0.5) * Tsclk	-	ns
	Byte to byte (Mode2/3 with DBS1K)	-	((1024 * (DBS + 1)) + 0.5) * Tsclk	-	ns
T_{DBS3}	MSCLK to MSS[x] (Mode0/1 without DBS1K)	-	(DBS + 0.5) * Tsclk	-	ns
	MSCLK to MSS[x] (Mode2/3 without DBS1K)	-	(DBS + 1.0) * Tsclk	-	ns
	MSCLK to MSS[x] (Mode0/1 with DBS1K)	-	((1024 * (DBS + 1)) + 0.5) * Tsclk	-	ns
	MSCLK to MSS[x] (Mode2/3 with DBS1K)	-	((1024 * (DBS + 1)) + 1.0) * Tsclk	-	ns
T_{DT1}	MSS[x] gap (without DT1K)	-	(DT + 2) * Tsclk	-	ns
	MSS[x] gap (with DT1K)	-	(1024 * (DT + 1) + 2) * Tsclk	-	ns
T_{MISET}	MMISO setup time	10.5	-	-	ns
T_{MIHD}	MMISO hold time	0	-	-	ns
T_{MODLY}	MMOSI output delay	-	-	0.5	ns
T_{RT}	MDRLD ready timeout (RDY mode)	-	(1 + SPIRPT) * 1024 * Tsclk	-	ns
T_{PT}	MTRG timeout	-	(1 + SPIRPT) * 1024 * Tsclk	-	ns
T_{LDACG}	MDRLD Gap (LDAC mode)	-	((LDACG1K * 1023) + 1) * (LDGAP + 1) * Tsclk	-	ns
T_{LDACW}	MDRLD Width (LDAC mode)	-	(LDACG1K * 1023 + 1) * (LDWID + 1) * Tsclk	-	ns

Table 3.11-15: SPI Master Timing Table

4 Package Information







Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.23	1.30	1.37	0.048	0.051	0.054
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
D1	---	8.80	---	---	0.346	---
E1	---	8.80	---	---	0.346	---
e	---	0.80	---	---	0.031	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa		0.15			0.006	
ccc		0.10			0.004	
ddd		0.08			0.003	
eee		0.15			0.006	
fff		0.08			0.003	
MD/ME	12/12					

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: ccc, ddd (SPIL STANDARD)
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .
6. REFERANCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5

5 Ordering Information

Part Number	Description
AX58200 BI	144-pin HSFBGA RoHS compliant package, temperature range: -40 to 85°C.
AX58200 BT	144-pin HSFBGA RoHS compliant package, temperature range: -40 to 105°C.

6 Revision History

Revision	Date	Comments
V0.10	2019/11/22	Preliminary release.

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