DESCRIPTION

The MPM3530 is an easy-to-use fully integrated 55V input, 3A step-down DC/DC power module. It integrates the monolithic DC/DC converter, power inductor, input capacitors and the necessary resistors/capacitors in a compact QFN 12mmX10mmX4mm package. This total power solution only requires a few external components.

The MPM3530 uses peak current mode control to regulate the output voltage. The module provides over current protection with valley current detection which is used to avoid current running away. Also it has accurate and reliable over voltage protection, and auto recovery thermal protection. The optional external soft start is available. Enable and power good indicator are provided. In order to increase the efficiency, MPM3530 will automatically scaling down the switching frequency when load is light.

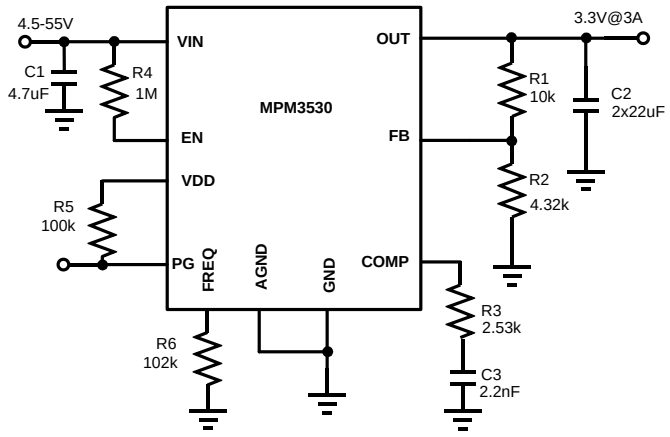
FEATURES

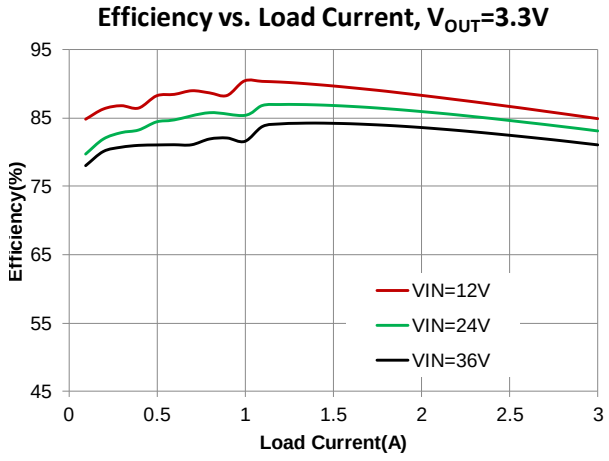
- Wide 4.5V to 55V Operating Input Range
- Wide Output Voltage Adjustable: 1V to 15V
- Programmable Switching Frequency with External SYNC Function
- External Soft Start
- Over Current Protection
- High Efficiency for Light Load Operation
- Over Voltage Protection and Thermal Shutdown Protection
- Power Good Indication
- Meet EN55022 Class B Emission
- Operating Temperature Range: -40°C to 85°C
- Available in QFN-44 (12mm x 10mm x 4mm)

APPLICATIONS

- Industrial Power Systems
- Automotive Test Equipment
- Distributed Power Systems

TYPICAL APPLICATION CIRCUIT





ORDERING INFORMATION

Part Number*	Package	Top Marking
MPM3530GRF	QFN 12 x 10 x 4mm	See below

*****For Tape & Reel, add suffix –Z (e.g. MPM3530);

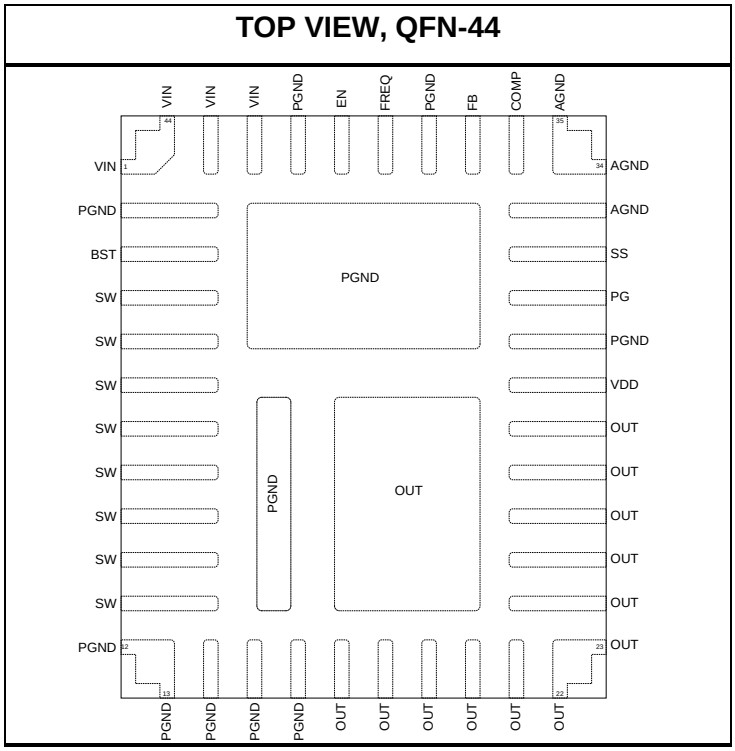
TOP MARKING

MPSYYWW
MP3530
LLLLLLLLL
M

MPS: MPS prefix;
YY: year code;
WW: week code;
MP3530: first six digits of the part number;
LLLLLLLLL: lot number;
M: Module.

PACKAGE REFERENCE

TOP VIEW, QFN-44



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN}……..60V
V_{SW} …….. -0.5 to (VIN+0.5V)
V_{BST}…….....V_{SW} + 6V
V_{OUT}…… 16.5V
All Other Pins……-0.3V to 6V
EN Sink Current…….150µA
All Other Pins…… ..... -0.3V to 4V
Continuous Power Dissipation (T_A = +25°C) (2)
……TBD
Junction Temperature……150°C
Lead Temperature……260°C
Storage Temperature……-65°C to 150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN}……..4.5V to 55V
Output Voltage V_{OUT}…… 1V to 15V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN(12x10x4 mm)….. ….. TBD.....TBD . °C/W

V_{BST}…… V_{SW}

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, V_{EN} = 3.3V, T_J = -40°C to 125°C (5), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage Range						
Input Voltage Range	V_{IN}		4.5		55	V
Output Voltage Range						
Output Voltage Range	V_{OUT}		1		15	V
Load Regulation(5)	$V_{OUT\_DC\_Load}$	V_{IN}=24V, load current from 0 to 3A		1		% V_{OUT}
Line Regulation(5)	$V_{OUT\_DC\_Line}$	I_{OUT}=3A, V_{IN} from 4.5V to 55V		1		% V_{OUT}
Quiescent Current						
Quiescent Current	I_Q	V_{EN}=3.3V, V_{FB}=1.05V		450	600	µA
Current Limit						
Peak Current Limit	I_{LIMIT}	10% Duty Cycle	5.5	7	9.5	A
VDD Regulator						
VDD Regulator Output Voltage	V_{DD}		3.4	3.6	3.8	V
Switching Frequency						
Switching Frequency	f_{SW}	R_{FREQ}=100k	400	520	640	kHz
Over-voltage and Under-voltage Protection						
OVP Threshold	V_{OVP_TH}	$V_{FB(OVP)}/V_{FB}$	108	115	122	%
VIN UVLO Rising Threshold	V_{INUV_R}		3.7	3.9	4.1	V
VIN UVLO Falling Threshold	V_{INUV_F}		3.3	3.5	3.7	V
Error Amplifier						
Feedback Voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 55V	0.985	1	1.015	V
FB Current	I_{FB}	V_{FB} =1.07V		10	50	nA
COMP Sink/Source Current	I_{COMP}		10	20	52	µA

Notes:

5) Not tested in production and guaranteed by over-temperature correlation.
6) Not tested in production and guaranteed by sample characterization.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, V_{EN} = 3.3V, T_J = -40°C to 125°C(5), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PWM Comparator						
Minimum On Time(5)	t_{ON_MIN}			90		ns
Minimum Off Time	t_{OFF_MIN}			100		ns
Enable						
EN Rising Threshold	V_{EN_R}		1.4	1.6	1.8	V
EN Falling Threshold	V_{EN_F}		1.1	1.3	1.5	V
EN Threshold Hysteresis	V_{EN_HYS}			300		mV
Soft Start						
Soft Start Time(5)	t_{SS}			1.2		ms
Power Good						
Power Good Threshold	V_{PG_TH}	V_{OUT} Rising, $V_{FB(PG)}/V_{FB}$	86	90	94	%
		V_{OUT} Falling, $V_{FB(PG)}/V_{FB}$	81	85	89	
Power Good Hysteresis	V_{PG_HYS}	$\Delta V_{FB(PG)}/V_{FB}$		5		%
Power Good Delay	t_{PG_DL}	V_{OUT} Rising	8	22	37	µs
		V_{OUT} Falling	8	21	33	µs
Thermal						
Thermal Shutdown (6)	T_{SD}			170		°C
Thermal Hysteresis (6)	T_{SD_HYS}			10		°C

Notes:

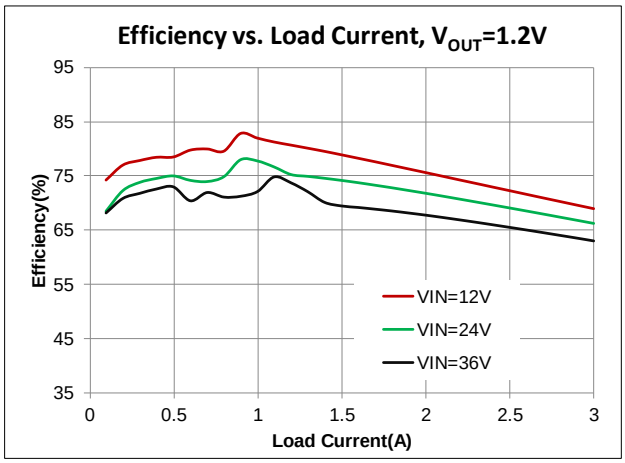
5) Not tested in production and guaranteed by over-temperature correlation.
6) Not tested in production and guaranteed by sample characterization.

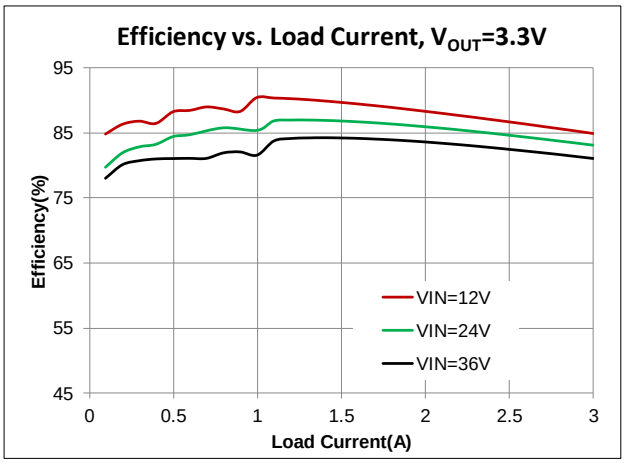
PIN FUNCTIONS

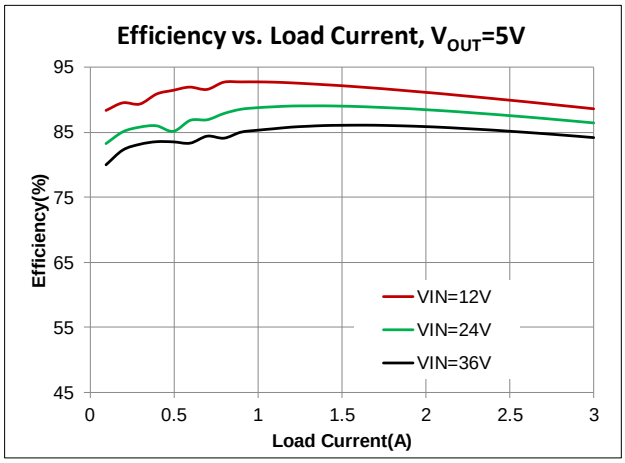
Pin #	Name	Description
1, 42-44	VIN	Input Supply. This supplies power to all the internal control circuitry, VDD regulator. A decoupling capacitor to ground must be placed close to this pin to minimize switching spikes. Use wide trace to connect these pins.
2, 12-16, 30, 38, 41	PGND	Module power ground pin.
3	BST	Bootstrap. This is the positive power supply for the internal floating high-side MOSFET driver. Keep it floating.
4-11	SW	Switch Output. Keep them floating.
17-28	OUT	Module Voltage Output node. Use wide trace to connect these pins.
29	VDD	Power for internal MOSFET driver and BST charging circuit.
31	PG	Power good indication. Connect a resistor to a pull up power source if used.
32	SS	Soft Start. Floating this pin has a default 1.2ms SS time. The SS time can be extended by connecting an external capacitor between SS and AGND pins.
33-35	AGND	Ground for internal logic and signal circuit.
36	COMP	Compensation Networks Setting. Connect an external resistor series with a capacitor between this pin and AGND. See Application Information for compensation network configuration.
37	FB	Feedback. This is the input to the PWM comparator. Please put an external resistive divider connected between the output and AGND.
39	FREQ	Frequency Set Pin. Connect a resistor from FREQ pin to ground to set the switching frequency. If external SYNC clock is applied to this pin, the converter will follow this SYNC clock frequency.
40	EN	Enable Input. Pulling this pin below the specified threshold shuts the chip down. There is no internal pull-up or pull-down circuit, so do not float the pin.

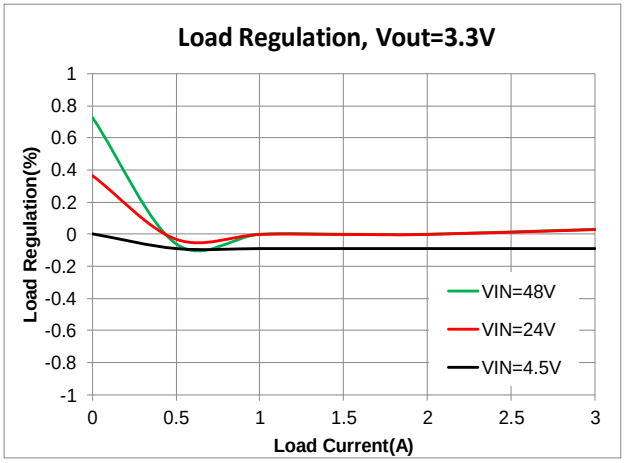
TYPICAL PERFORMANCE CHARACTERISTICS

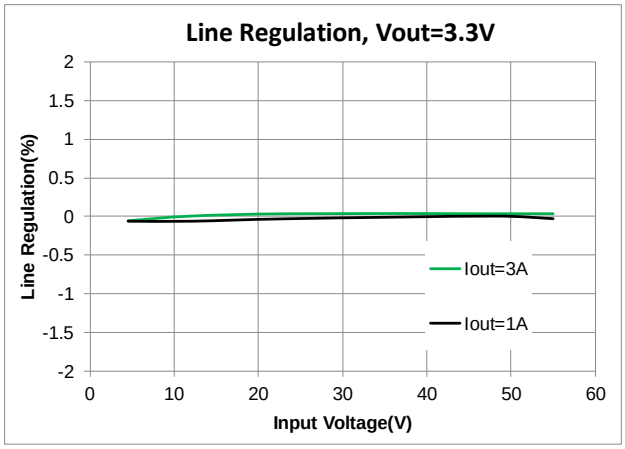
Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 24V, T_A = 25°C, unless otherwise noted.







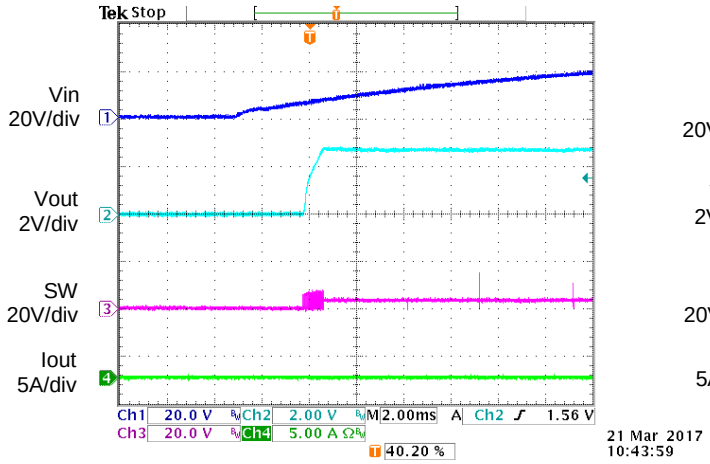




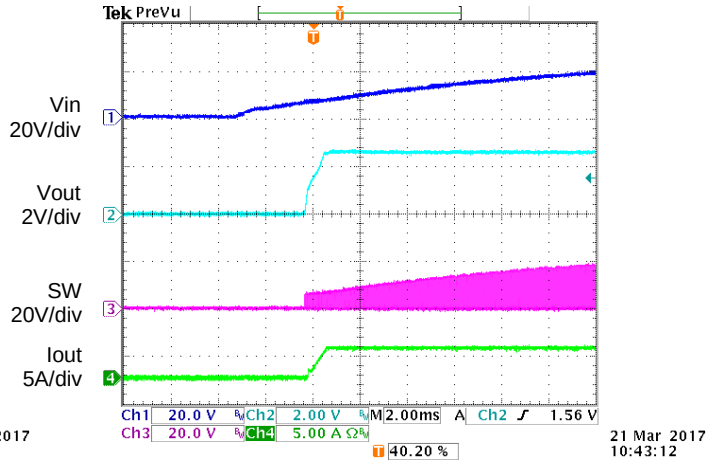
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

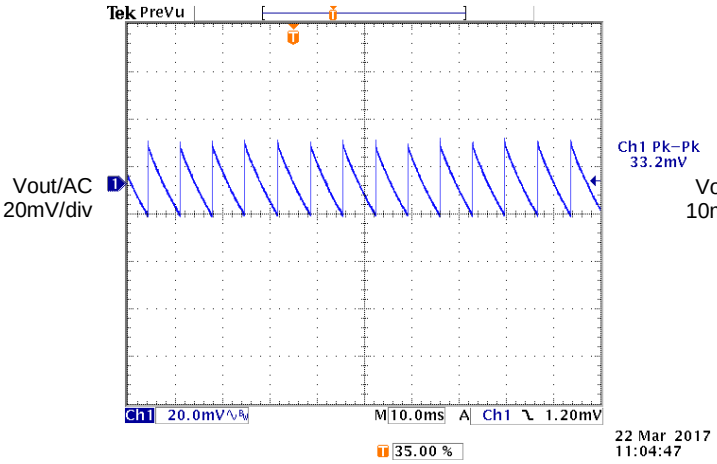
Start-up through VIN
Vout=3.3V, Iout=0A



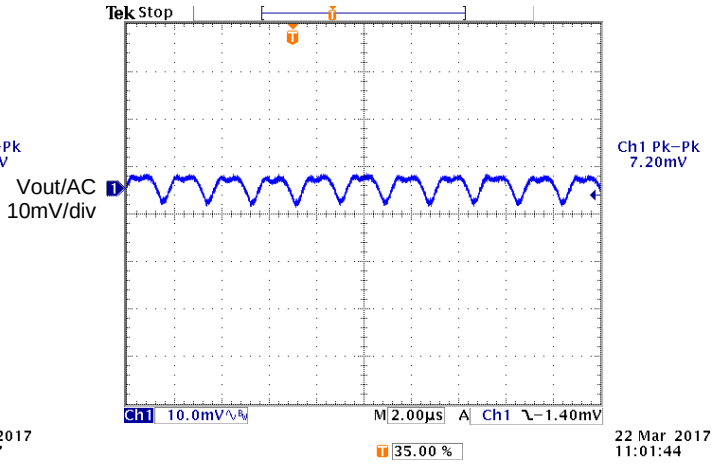
Start-up through VIN
Vout=3.3V, Iout=3A



Output Ripple
Vout=3.3V, Iout=0A, 4x22uF caps

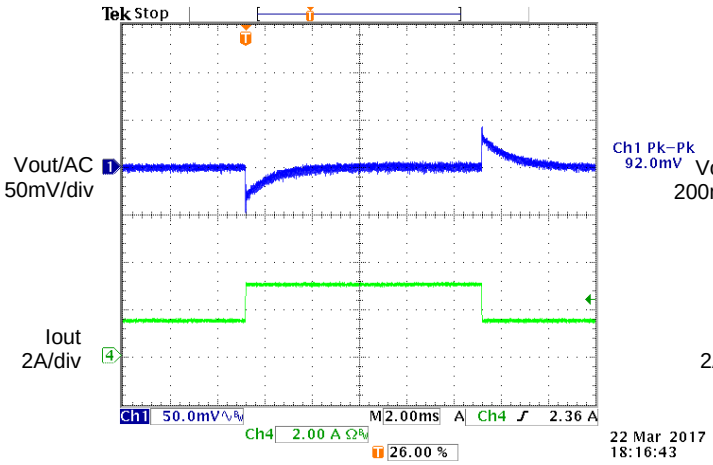


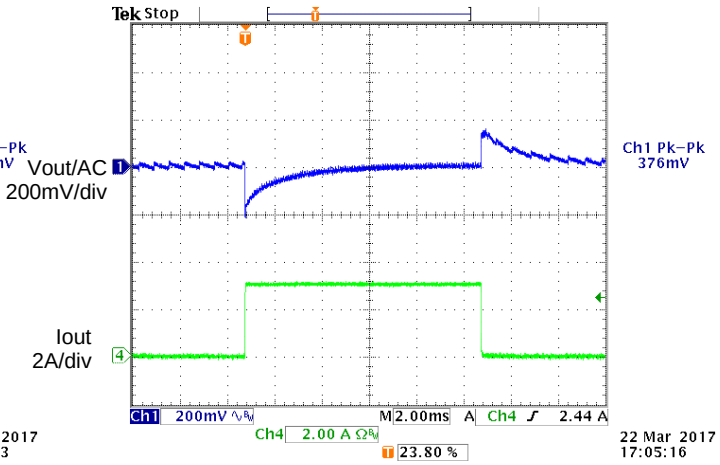
Output Ripple
Vout=3.3V, Iout=3A, 4x22uF caps



Load Transient Response
Vout=3.3V, 1.5 to 3A, 4x22uF caps

Load Transient Response
Vout=3.3V, Iout=0 to 3A, 4x22uF caps

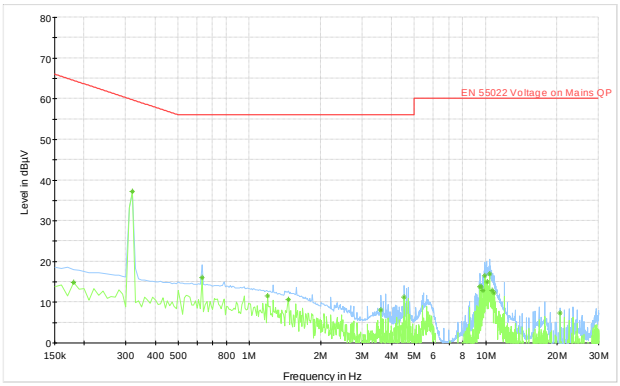




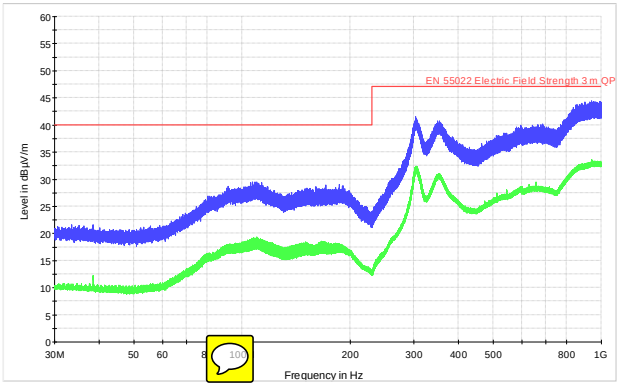
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Conducted Emission, EN55022 Class B
Vout=3.3V Input Pi Filter: 10uF, 4.7uH, 10uF



Radiated Emission, EN55022 Class B
Vout=3.3V Input Pi Filter: 10uF, 4.7uH, 10uF



FUNCTIONAL BLOCK DIAGRAM

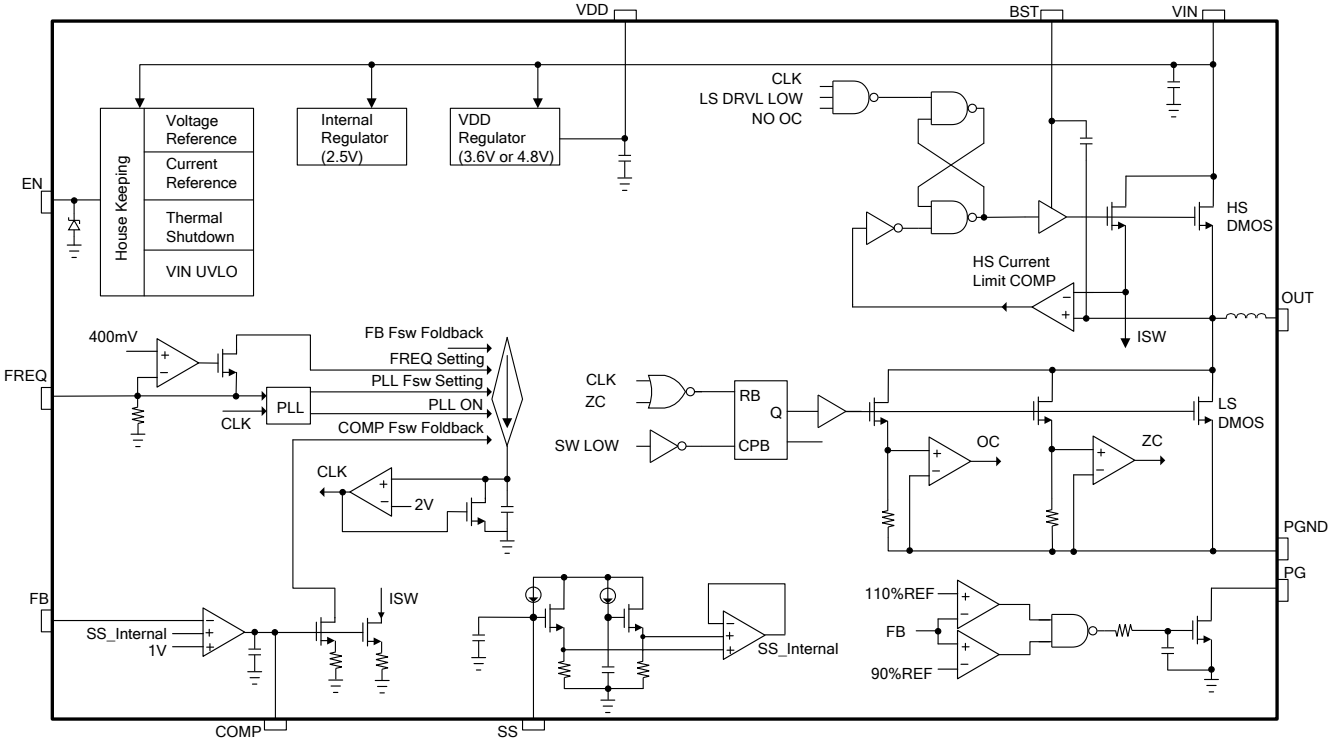


Figure 1: Functional Block Diagram

OPERATION

The MPM3530 is a high-performance and complete power solution. It features as wide input voltage range, high efficiency, external internal soft-start, frequency programmable and comprehensive protection mode, i.e. OVP, OCP, OTP.

PWM Control

The MPM3530 uses peak current mode control to regulate the output voltage. A PWM cycle is initiated by the internal clock at the beginning of every cycle. After the high side MOSFET turns on, the inductor current will rise linearly to provide the energy to the load. The high side MOSFET remains on until its current hits the COMP voltage which is the output of the internal error amplifier (EA). The output voltage of error amplifier depends on the difference of output feedback voltage and the internal high precision reference and it will decide how much energy should be transferred to the load. The higher load current, the higher COMP voltage. After the high switch is off, the low side switch is on and the inductor current will flow through the low side switch. In order to avoid shoo-through issue, the dead time is inserted to avoid the high side and low side MOSFETS to turn on at the same time. For each turn on and off in a switching cycle, the high side MOSFET will keep on and off with minimum on and off time limit.

Light Load Operation

In order to get high efficiency, MPM3530 has two features during light load: 1).When the load current decreases, the inductor current will drop at same time. The low side MOSFET will turn off in order to save driver loss when inductor current drops to zero. 2) When the load decreases, the switching frequency will be scaled down in order to reduce switching loss after COMP voltage drops down lower than certain threshold.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal reference and outputs a current proportional to the difference between the two. This current is used to charge the external compensation networks to form the COMP voltage, which is used to control the high side MOSFET peak current and to regulate the output voltage.

Oscillator and SYNC Function

The internal oscillator frequency is set by frequency set resistor (R_{FREQ}) connected between FREQ pin and GND. The relationship between oscillator frequency and R_{FREQ} refer to table 1 in APPLICATION INFORMATION section. During light load, the switching frequency will be scaled down according to the COMP voltage. The switching frequency will start to decrease when the COMP voltage is lower than around 0.8V. And the switching will be disabled when the COMP voltage drops lower than around 0.7V. In order to reduce the switching loss and the thermal dissipation, the switching frequency will be decreased according to the FB voltage. When the FB is lower than 25%xRFE, the switching frequency starts to decrease from the normal value, and finally drops to 5% of the normal value when the FB is zero.

The FREQ pin can be used to synchronize the internal oscillator rising edge to an external clock falling edge. Make sure the HIGH amplitude of SYNC clock is higher than 1.5V and LOW amplitude is lower than 1V to drive the internal logic. The recommended external SYNC frequency is in the range of 100kHz and 1MHz. There is no pulse width requirement but please note that there is always parasitic capacitance of the pad there, so, if the pulse width is too short, a clear rising and falling edge may not be seen due to the parasitic capacitance. The pulse longer than 100ns is recommended in application.

EN Control

EN is a control pin that turns the module on and off: Drive EN higher than 1.6V to turn on the regulator, drive it lower than 1.3V to turn off. There is no internal pull-up or pull-down at EN, so when it is floating, the EN status is uncertain. The EN pin is clamped internally using a 6.5V zener diode between EN and GND, as shown in the functional block diagram. Connecting the EN pin directly to a voltage source without any pull up resistor requires limiting voltage amplitude to ≤6V to prevent damage to the zener diode. EN pin can be connected to higher voltage (e.g. VIN) through pull-up resistor if the system doesn't have another logic signal acting as enable signal. Just make sure the pull-up resistor is high enough to make sure the sink current into EN pin less than 150uA to avoid damaging the zener diode. For example, when connecting EN to V_{IN}=12V, $R_{PULL-UP}$ ≥ (12V – 6.5V) ÷ 150μA = 37kΩ.

Soft Start

The soft start is implemented to ensure the smooth up output voltage during the power on and off. In addition, the soft start function also helps to reduce the inrush current value at the startup. The soft start function is achieved by ramping SS up slowly and using SS to override the internal reference (REF) when SS-900mV is lower than REF. When SS-900mV is higher than REF, REF regains the control. The 900mV above is the offset voltage of SS which means SS is detected as 0 internally when it is lower than 900mV. To minimize the delay for SS to reach 0.9V, an internal pull-up circuit with about 30uA average current pulls SS up to 600mV first. Then use 4uA constant current to charge SS until it reaches to 2.5V. When SS is in the range of 0.9V to 1.9V, it overrides the REF as reference voltage of the error amplifier. During this period, output voltage ramps up from 0 to the regulated value following SS rising.

An internal 4.7nF SS capacitor is used in MPM3530. The default SS time can be estimated by the following equation:

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)}$$

So the default SS time is about 1.2ms. If longer SS time is needed, an external SS capacitor can be added between SS pin and AGND pin. The external capacitor value can be determined as:

$$C_{SS}(nF) = \frac{T_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} - 4.7(nF)$$

Over Voltage Protection

The MPM3530 monitors the feedback output voltage to achieve the over voltage protection. If the FB voltage is higher than the 103%xREF, MPM3530 will change to sleep mode and the high side MOSFET will turn off and low side MOSFET will turn on to discharge the output energy. It will return to normal after the FB drops to lower than 103%xREF. If the FB voltage is higher than 110%xRFE, the high side and low side MOSFET will be turned off immediately. Then both MOSFETs will be latched and PG signal will be asserted to inform the fault status and it needs EN or VIN recycling to clear the protection.

Over Current Protection

The MPM3530 has cycle-by-cycle peak current limit protection and valley current detection protection. The inductor current is monitored during the high side MOSFET on state. If the inductor current exceeds the current limit value set by COMP voltage, the high side MOSFET turns off immediately. Then, the low side MOSFET will be turned on to discharge the energy and inductor current will decrease. The high side MOSFET will not be on again unless the inductor valley current is lower than a certain current threshold which is called the valley current limit. It is very useful to avoid the inductor current to run away. Also, both the peak current limit and the valley current limit value are dependent on the FB voltage. If the feedback output voltage is higher than the

50%xREF, the current limit value is as the normal value. If the feedback output voltage is lower than 50%xRFF, the current limit will decrease and drop to the half normal value when the feedback output voltage is zero. This feature is very helpful to reduce the OCP thermal dissipation which may especially get worse when the output voltage is shorted. Also, it is very helpful to reduce the high inrush current during the startup.

UVLO Protection

The MPM3530 has input under voltage lockout protection (UVLO). Assuming the EN is active, the MPM3530 is powered on when the input voltage is higher than the UVLO rising threshold and is powered off when input voltage drops below the UVLO falling threshold.

Thermal Shutdown Protection

The thermal shutdown is employed in MPM3530 by monitoring the temperature internally. If the junction temperature exceeds the threshold (typically 170°C), the regulator shuts off and it will turns on again when the temperature drops below 160°C. There is a ~10°C hysteresis.

Power Good

MPM3530 has one power good (PG) pin out to indicate the normal operation after soft start time. The PG pin is the open drain of an internal MOSFET. It should be connected to VDD or external voltage source through a resistor (i.e. 100kohm). After the input voltage is applied, the MOSFET is turned on and the PG pin is pulled to GND before SS is ready. After the FB voltage reaches 90% REF voltage, the MOSFET turns off and PG pin is pulled to high by external voltage source. When the FB voltage drops to 85% REF voltage, the PG voltage is pulled to GND to indicate a failure output status.

Floating Driver and Bootstrap Charging

An internal bootstrap capacitor (0.1μF typically) between BST pin and SW pin powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.3V with a hysteresis of 300mV. The driver's UVLO is soft-start related: When the bootstrap voltage hits its UVLO threshold, the soft-start circuit resets. When bootstrap UVLO is gone, the reset is off and then the soft-start process resumes.

The dedicated internal bootstrap regulator regulates and charges the bootstrap capacitor to 4.2V. When the voltage between the BST and SW nodes is less than its regulation, a PMOS pass transistor from VIN to BST turns ON. The charging current path is from VIN, BST and then to SW.

As long as V_{IN} is sufficiently higher than V_{SW}, the bootstrap capacitor can be charged. When the high side MOSFET is ON, $V_{IN} \approx V_{SW}$ so the bootstrap capacitor can't be charged. When low side MOSFET is ON, the difference between V_{IN} and V_{SW} is at its largest, thus making it the best period to charge. When there is no current in the inductor, $V_{SW}=V_{OUT}$ so the difference between V_{IN} and V_{OUT} can charge the bootstrap capacitor. At higher duty cycles, the time period available for bootstrap charging is shorter so the bootstrap capacitor may not be sufficiently charged. If the internal circuit does not have sufficient voltage and the bootstrap capacitor is not charged, extra external circuitry can be used to ensure the bootstrap voltage is within the normal operational region.

APPLICATION INFORMATION

Setting the Switching Frequency

The MPM3530 has an externally adjustable frequency. The switching frequency (f_{SW}) can be set using a resistor at FREQ (R_{FREQ}). Table 1 shows recommended R_{FREQ} values for various f_{SW} values.

Table 1: f_{SW} vs. R_{FREQ}

f_{SW} (kHz)	R_{FREQ} (kΩ)
1000	47.5
900	56
800	63.4
700	73.2
600	84.5
500	102
400	133
300	178
200	261
100	523

Setting the Output Voltage

A resistive voltage divider from the output voltage to FB sets the output voltage. The voltage divider divides the output voltage down to the feedback voltage by the ratio shown in Equation (3):

$$V_{FB}=V_{OUT}\times\frac{R2}{R1+R2} \quad (3)$$

Calculated the output voltage with Equation (4):

$$V_{OUT}=V_{FB}\times\frac{R1+R2}{R2} \quad (4)$$

For example, if R1 is 10kΩ, then R2 can be calculated with Equation (5):

$$R2=\frac{10}{V_{OUT}-1}k\Omega \quad (5)$$

So for a 3.3V output voltage, R1 is 10kΩ, and R1 is 4.32kΩ.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use capacitors with low equivalent series resistances (ESR) for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also be sufficient.

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitor (C1) can be electrolytic, tantalum, or ceramic.

When using electrolytic or tantalum capacitors, place a small, high-quality, ceramic capacitor (0.1μF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be approximated with Equation (8):

$$\Delta V_{IN}=\frac{I_{LOAD}}{f_{SW}\times C1}\times\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. Low ESR capacitors are recommended to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_{SW}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times f_{SW}\times C2}\right) \quad (9)$$

Where L is the inductor value, and R_{ESR} is the ESR value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and contributes the most to the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPM3530 can be optimized for a wide range of capacitances and ESR values.

Compensation Components

The MPM3530 employs current-mode control for easy compensation and fast transient response. COMP is the output of the internal error amplifier and controls system stability and transient response. A series resistor-capacitor combination sets a pole-zero combination to control the control system's characteristics. The DC gain of the voltage feedback loop can be calculated with Equation (12):

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{VEA} \times \frac{V_{FB}}{V_{OUT}} \quad (12)$$

Where A_{VEA} is the error amplifier voltage gain (1000V/V), G_{CS} is the current-sense transconductance (12A/V), and R_{LOAD} is the load resistor value.

The system has two important poles: one from the compensation capacitor (C3) and the output resistor of error amplifier, and the other due to the output capacitor and the load resistor. These poles can be determined with Equation (13) and Equation (14):

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}} \quad (13)$$

$$f_{P2} = \frac{1}{2\pi \times C2 \times R_{LOAD}} \quad (14)$$

Where G_{EA} is the error-amplifier transconductance (540μA/V).

The system has one important zero due to the compensation capacitor and the compensation resistor (R3). This zero can be determined with Equation (15):

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3} \quad (15)$$

The system may have another significant zero if the output capacitor has a large capacitance or a high ESR value. This zero can be determined with Equation (16):

$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}} \quad (16)$$

In this case, a third pole set by the compensation capacitor (C4) and the compensation resistor can compensate for the effect of the ESR zero. This pole can be determined with Equation (17):

$$f_{P3} = \frac{1}{2\pi \times C4 \times R3} \quad (17)$$

The goal of compensation design is to shape the converter transfer function for a desired loop gain. The system crossover frequency where the feedback loop has unity gain is important, since lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies lead to system instability. Generally, set the crossover frequency to ~0.1xf_{SW}.

Use the following steps to design the compensation:

1. Choose R3 to set the desired crossover frequency. R3 can be determined with Equation (18):

$$R3 = \frac{2\pi \times C2 \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} \quad (18)$$

   Where f_C is the desired crossover frequency.

2. Choose C3 to achieve the desired phase margin. For applications with typical inductor values, set the compensation zero (f_{Z1}) to <0.25xf_C to provide a sufficient phase

margin. C3 can be calculated with Equation (19):

$$C3 > \frac{4}{2\pi \times R3 \times f_C} \quad (19)$$

3. Determine if C4 is required. C4 is required if the ESR zero of the output capacitor is located at <0.5xf_{SW}, or Equation (20) is valid:

$$\frac{1}{2\pi \times C2 \times R_{ESR}} < \frac{f_{SW}}{2} \quad (20)$$

If this is the case, use C4 to set the pole (f_{P3}) at the location of the ESR zero. Determine C4 with Equation (21):

$$C4 = \frac{C2 \times R_{ESR}}{R3} \quad (21)$$

External Bootstrap Diode

For high duty-cycle operations where V_{OUT}/VIN > 65%, the time period available to the bootstrap charging is less, so the bootstrap capacitor may not be charged sufficiently. This affects efficiency and normal operation. An external bootstrap diode from the 3V - 5V rail to BST can help charge the bootstrap capacitor and enhance efficiency (see Figure 2). The output voltage is a good choice for this power supply if it is in above range. The bootstrap diode can be a low-cost one such as IN4148 or BAT54.

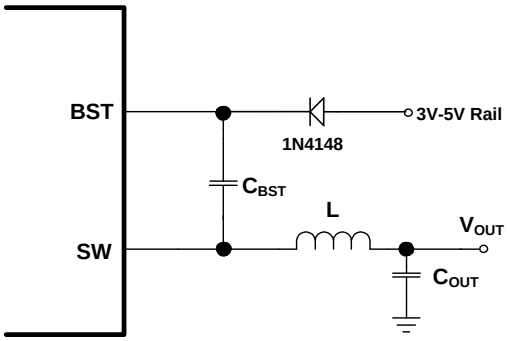


Figure 2: External Bootstrap Diode

At no load or light load, the converter may operate in pulse-skipping mode to maintain the output-voltage regulation. Under this condition, V_{SW} = V_{OUT} for most of the time, so the diode from V_{OUT} to BST cannot charge the bootstrap capacitor. For a sufficient gate voltage during pulse-skipping mode, VIN - V_{OUT} should be no less than 3V. For example, if V_{OUT} = 3.3V, then VIN must exceed 3.3V + 3V = 6.3V to maintain a sufficient bootstrap voltage at no load or light load. To meet this requirement, EN can program the input UVLO voltage to V_{OUT} + 3V.

TYPICAL APPLICATION CIRCUIT

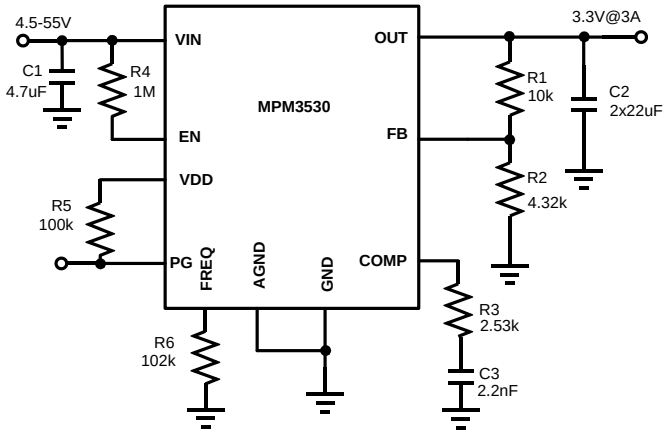
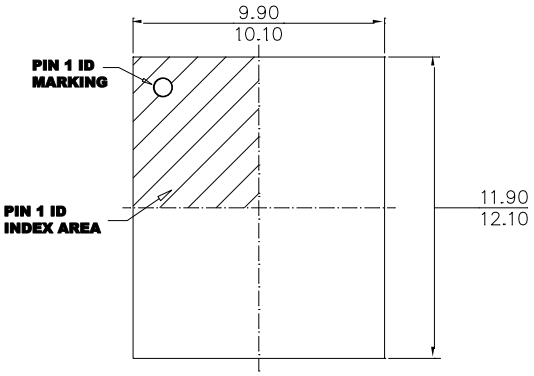


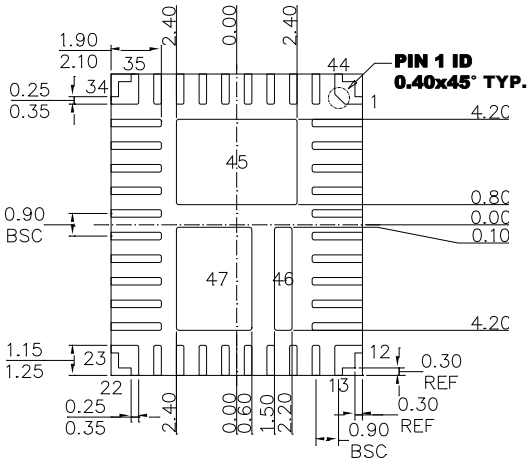
Figure 3: 3.3V Output Typical Application Circuit

PACKAGE INFORMATION

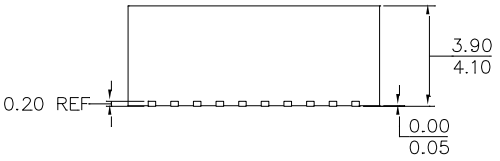
PACKAGE OUTLINE DRAWING FOR 47L WBMQFN (10X12MM)
MF-PO-D-0286 revision0.0



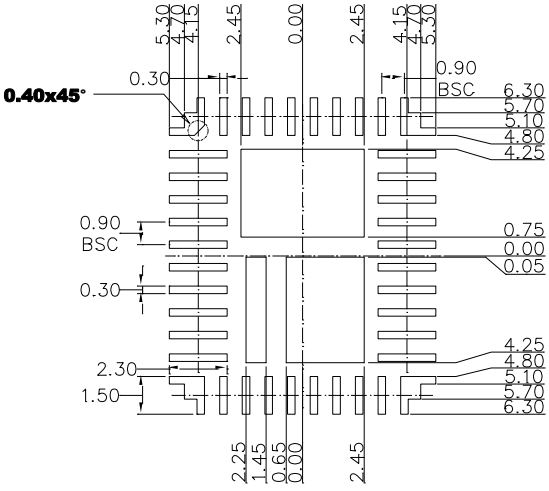
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.