### Low Phase Jitter MEMS Oscillator



# MO8208



#### Features

- ●Any frequency between 1and 80 MHz accurate 6 decimal places
- Standard 4-pin packages: 2.7 x 2.4 (compatible with 2.5 x 2.0 footprint), 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm
- Frequency stability as low as  $\pm 10 \times 10^{-6}$
- Oltra-Low phase Jitter: 0.5 ps (12 kHz to 20 MHz)
- Outstanding silicon reliability of 2 FIT or 500 million hour MTBF

### Applications

- •Computing, storage, networking, telecom, industrial control
- ●SATA, SAS, Ethernet, PCI Express, video, WiFi



### Standard Specification

Item	Symbol	Min.	Тур.	Max.	Unit	Condition
Output Frequency Range	f	1	-	80	MHz	
Supply Voltage	Vdd	+1.71 +2.25 +2.52 +2.97	+1.8 +2.5 +2.8 +3.3	+1.89 +2.75 +3.08 +3.63	v	Supply voltages between +2.5V and +3.3V can be supported.
Operating Temperature Range	T_use	-20	-	+70	°C	Extended Commercial
		-40	-	+85		Industrial
Frequency Stability	F_stab	-10 -20 -25 -50	_ _ _ _	+10 +20 +25 +50	x10⁻ <sup>6</sup>	Inclusive of initial tolerance at +25°C,and variations over operating temperature, rated power supply voltage and load.
Fist year Aging		-1.5	-	+1.5	x10 <sup>-6</sup>	T <sub>A</sub> =+25°C
10-year Aging	F_aging	-5.0	-	+5.0		T <sub>A</sub> =+25°C
Current Consumption	ldd		+31 +29	+33 +31	mA	No load condition, f = 20 MHz, Vdd = +2.5V, +2.8V or +3.3V No load condition, f = 20 MHz. Vdd = +1.8V
OE Disable Current	I_od		_	+31 +30	mA	Vdd = +2.5V, +2.8V or +3.3V, OE = GND, output is Weakly Pulled Down Vdd = +1.8 V. OE = GND, output is Weakly Pulled Down
Standby Current	I_std	-	-	+70	μA	Vdd = +2.5V +2.8V or +3.3V ST = GND output is Weakly Pulled Down
		_	-	+10		Vdd = +1.8 V. $\overline{ST}$ = GND, output is Weakly Pulled Down
Duty Cycle	DC	45	-	55	%	
Output Low Voltage	V <sub>OL</sub>	-	-	Vdd x 0.1	V	I <sub>OH</sub> = -6.0 mA, I <sub>OL</sub> = +6.0 mA, (Vdd = +3.3V, +2.8V, +2.5V)
Output High Voltage	V <sub>OH</sub>	Vdd x 0.9	-	-	V	I <sub>OH</sub> = -3.0 mA, I <sub>OL</sub> = +3.0 mA, (Vdd = +1.8V)
Rise/Fall Time	tr,tf	-	1.2	2.0	ns	15 pF load, 10% - 90% Vdd
Input Low Voltage	VIL	-	-	Vdd x 0.3	V	Pin 1, OE or ST
Input High Voltage	V <sub>IH</sub>	Vdd x 0.7	-	-	V	Pin 1, OE or ST
Startup Time	T_start	-	7.0	10	ms	Measured from the time Vdd reaches its rated minimum value
Enable/Disable Time	T_oe	-	-	150	ns	f = 80 MHz, For other frequencies, T_oe = 100 ns + 3 cycles
Resume Time	T_resume	I	6.0	10	ms	In standby mode, measured from the time $\overline{ST}$ pin crosses 50% threshold.
RMS Period Jitter	Tiitt	-	1.5	2.0	DS	
		-	2.0	3.0	P	t = 75 MHz, Vdd = +1.8V
RIVIS Phase Jitter (random)	I_phj	-	0.5	1.0	ps	t = 10 MHz, Integration bandwidth = 12 kHz to 20 MHz

Consult our sales representative for other specifications.

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#### Notes:

1. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device. 2. A capacitor of value 0.1 µF between Vdd and GND is required.