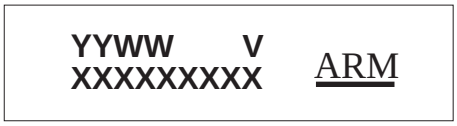
Your contact: www.codico.com mailto: office@codico.com phone: +43/1/86305-0 fax: +43/1/86305-5000

1. Errata - AT91SAM7S256/128 Version B

1.1 Marking

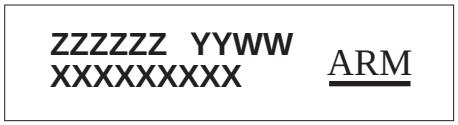
All devices are marked with the Atmel logo and the ordering code.

Additional marking may be in one of the following formats:



where

- “YY”: manufactory year
- “WW”: manufactory week
- “V”: revision
- “XXXXXXXXX”: lot number



where

- “ZZZZZZ”: manufacturing number
- “YY”: manufactory year
- “WW”: manufactory week
- “XXXXXXXXX”: lot number

1.2 AT91SAM7S256 Errata - Revision B Parts

Refer to Section 1.1 ”Marking”, on page 1.

Note: AT91SAM7S256 Revision B chip ID is: 0x270D 0941

1.2.1 Non Volatile Memory Bits (NVM Bits)

1.2.1.1 NVM Bits: Write/Erase Cycles Number

The maximum number of write/erase cycles for Non Volatile Memory bits is 100. This includes Lock Bits (LOCKx), General Purpose NVM bits (GPNVMx) and the Security Bit.

This maximum number of write/erase cycles is not applicable to 256 KB Flash memory, it remains at 10K for the Flash memory.

Problem Fix/Workaround

None.

1.2.2 Parallel Input/Output Controller (PIO)

1.2.2.1 PIO: Electrical Characteristics on NRST and PA0-PA16 and PA21-31

When NRST or PA0-PA16 or PA21-PA31 are set as digital inputs with pull-up enabled, the voltage of the I/O stabilizes at VPull-up.

Vpull-up

VPull-up Min	VPull-up Max
VDDIO - 0.65 V	VDDIO - 0.45 V

This condition causes a leakage through VDDIO. This leakage is 45 µA per pad in worst case at 3.3 V and 25 µA at 1.8V.

I Leakage

Parameter	Typ	Max
I Leakage at 3,3V	2.5 µA	45 µA
I Leakage at 1.8V	1 µA	25 µA

Problem Fix/Workaround

It is recommended to use an external pull-up if needed.

1.2.2.2 PIO: Drive Low NRST, PA0-PA16 and PA21-PA31

When NRST or PA0-PA16 and or PA21-PA31 are set as digital inputs with pull-up enabled, driving the I/O with an output impedance higher than 500 ohms may not drive the I/O to a logical zero.

Problem Fix/Workaround

Output impedance must be lower than 500 ohms.

1.2.3 Pulse Width Modulation Controller (PWM)

1.2.3.1 PWM: Update when PWM_CCNTx = 0 or 1

If the Channel Counter Register value is 0 or 1, the Channel Period Register or Channel Duty Cycle Register is directly modified when writing the Channel Update Register.

Problem Fix/Workaround

Check the Channel Counter Register before writing the update register.

1.2.3.2 PWM: Update when PWM_CPRDx = 0

When Channel Period Register equals 0, the period update is not operational.

Problem Fix/Workaround

Do not write 0 in the period register.

1.2.3.3 PWM: Counter Start Value

In left aligned mode, the first start value of the counter is 0. For the other periods, the counter starts at 1.

Problem Fix/Workaround

None.

1.2.3.4 PWM: Constraints on Duty Cycle Value

Setting Channel Duty Cycle Register (PWM_CDTYx) at 0 in center aligned mode or at 0 or 1 in left aligned mode may change the polarity of the signal.

Problem Fix/Workaround

Do not set PWM_CDTYx at 0 in center aligned mode.

Do not set PWM_CDTYx at 0 or 1 in left aligned mode.

1.2.3.5 PWM: Behavior of CHIDx Status Bits in the PWM_SR Register

Erratic behavior of the CHIDx status bit in the PWM_SR Register. When a channel is disabled by writing in the PWM_DIS Register just after enabling it (before completion of a Clock Period of the clock selected for the channel), the PWM line is internally disabled but the CHIDx status bit in the PWM_SR stays at 1.

Problem Fix/Workaround

Do not disable a channel before completion of one period of the selected clock.

1.2.4 Real Time Timer (RTT)

1.2.4.1 RTT: Possible Event Loss when Reading RTT_SR

If an event (RTTINC or ALMS) occurs within the same slow clock cycle during which the RTT_SR is read, the corresponding bit might be cleared. This can lead to the loss of this event.

Problem Fix/Workaround:

The software must handle the RTT event as an interrupt and should not poll RTT_SR.

1.2.5 Serial Peripheral Interface (SPI)

1.2.5.1 SPI: Bad tx_ready Behavior when CSAAT = 1 and SCBR = 1

If the SPI is programmed with CSAAT = 1, SCBR(baudrate) = 1 and two transfers are performed consecutively on the same slave with an IDLE state between them, the tx_ready signal does not rise after the second data has been transferred in the shifter. This can imply for example, that the second data is sent twice.

Problem Fix/Workaround

Do not use the combination CSAAT = 1 and SCBR = 1.

1.2.5.2 SPI: LASTXFER (Last Transfer) Behavior

In FIXED Mode, with CSAAT bit set, and in “PDC mode” the Chip Select can rise depending on the data written in the SPI_TDR when the TX_EMPTY flag is set. If for example, the PDC writes a “1” in the bit 24 (LASTXFER bit) of the SPI_TDR, the chip select will rise as soon as the TXEMPTY flag is set.

Problem Fix/Workaround

Use the CS in PIO mode when PDC mode is required and CS has to be maintained between transfers.

1.2.5.3 SPI: SPCK Behavior in Master Mode

SPCK pin can toggle out before the first transfer in Master Mode.

Problem Fix/Workaround

In Master Mode, MSTR bit must be set (in SPI_MR register) before configuring SPI_CSRx registers.

1.2.5.4 SPI: Chip Select and Fixed Mode

In fixed Mode, if a transfer is performed through a PDC on a Chip select different from the Chip select 0, the output spi_size sampled by the PDC will depend on the field, BITS (Bits per Transfer) of SPI_CSR0 register, whatever the selected Chip select is. For example, if SPI_CSR0 is configured for a 10-bit transfer whereas SPI_CSR1 is configured for an 8-bit transfer, when a transfer is performed in Fixed mode through the PDC, on Chip select 1, the transfer will be considered as a HalfWord transfer.

Problem Fix/Workaround

If a PDC transfer has to be performed in 8 bits, on a Chip select y (y as different from 0), the BITS field of the SPI_CSR0 must be configured in 8 bits, in the same way as the BITS field of the CSRy Register.

1.2.5.5 SPI: Baudrate Set to 1

When Baudrate is set at 1 (i.e. when serial clock frequency equals the system clock frequency) and when the BITS field of the SPI_CSR register (number of bits to be transmitted) equals an ODD value (in this case 9,11,13 or 15), an additional pulse will be generated on output SPCK.

Everything is OK if the BITS field equals 8,10,12,14 or 16 and Baudrate = 1.

Problem Fix/Workaround

None.

1.2.5.6 SPI: Disable In Slave Mode

The SPI disable is not possible in slave mode.

Problem Fix/Workaround

Read first the received data, then perform the software reset.

1.2.6 Synchronous Serial Controller (SSC)

1.2.6.1 SSC: Periodic Transmission Limitations in Master Mode

If the Least Significant Bit is sent first (MSBF = 0), the first TAG during the frame synchro is not sent.

Problem Fix/Workaround

None.

1.2.6.2 SSC: Transmitter Limitations in Slave Mode

If TK is programmed as output and TF is programmed as input, it is impossible to emit data when the start of edge (rising or falling) of synchro has a Start Delay equal to zero.

Problem Fix/Workaround

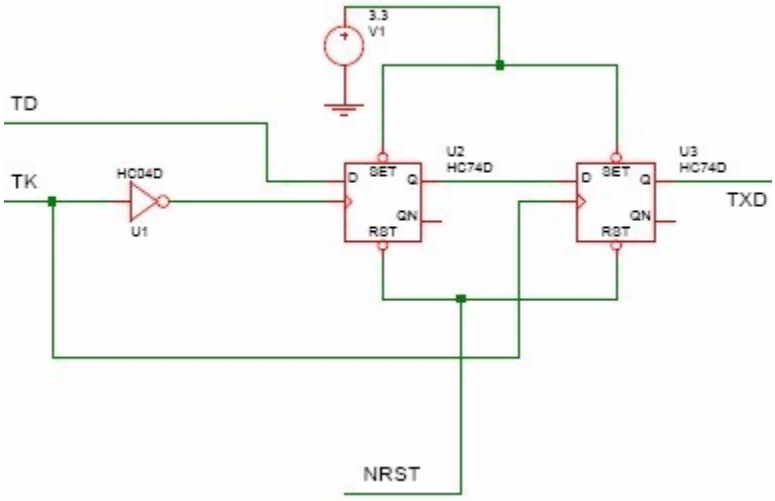
None.

1.2.6.3 SSC: Transmitter Limitations in Slave Mode

If TK is programmed as an input and TF is programmed as an output and requested to be set to low/high during data emission, the Frame Synchro signal is generated one bit clock period after the data start and one data bit is lost. This problem does not exist when generating a periodic synchro.

Problem Fix/Workaround

The data need to be delayed for one bit clock period with an external assembly. In the following schematic, TD, TK and NRST are AT91SAM7S signals, TXD is the delayed data to connect to the device.



1.2.7 Two-wire Interface (TWI)

1.2.7.1 TWI: Clock Divider

The value of CLDIV x 2^{CKDIV} must be less than or equal to 8191, the value of CHDIV x 2^{CKDIV} must be less than or equal to 8191·

Problem Fix/Workaround

None.

1.2.7.2 TWI: Software Reset

when a software reset is performed during a frame and when TWCK is low, it is impossible to initiate a new transfer in READ or WRITE mode.

Problem Fix/Workaround

None.

1.2.7.3 TWI: Disabling Does not Operate Correctly

Any transfer in progress is immediately frozen if the Control Register (TWI_CR) is written with the bit MSDIS at 1. Furthermore, the status bits TXCOMP and TXRDY in the Status Register (TWI_SR) are not reset.

Problem Fix/Workaround

The user must wait for the end of transfer before disabling the TWI. In addition, the interrupts must be disabled before disabling the TWI.

1.2.7.4 TWI: NACK Status Bit Lost

During a master frame, if TWI_SR is read between the Non Acknowledge condition detection and the TXCOMP bit rising in the TWI_SR, the NACK bit is not set.

Problem Fix/Workaround

The user must wait for the TXCOMP status bit by interrupt and must not read the TWI_SR as long as transmission is not completed.

TXCOMP and NACK fields are set simultaneously and the NACK field is reset after the read of the TWI_SR.

1.2.7.5 TWI: Possible Receive Holding Register Corruption

When loading the TWI_RHR, the transfer direction is ignored. The last data byte received in the TWI_RHR is corrupted at the end of the first subsequent transmit data byte. Neither RXRDY nor OVERRUN status bits are set if this occurs.

Problem Fix/Workaround

The user must be sure that received data is read before transmitting any new data.

1.2.8 Universal Synchronous Asynchronous Receiver Transmitter (USART)

1.2.8.1 USART: CTS in Hardware Handshaking

When Hardware Handshaking is used and if CTS goes low near the end of the starting bit, a character can be lost.

Problem Fix/Workaround

CTS must not go low during a time slot occurring between 2 Master Clock periods before the starting bit and 16 Master Clock periods after the rising edge of the starting bit.

1.2.8.2 USART: Hardware Handshaking – Two Characters Sent

If CTS switches from 0 to 1 during the TX of a character and if the holding register (US_THR) is not empty, the content of US_THR will also be transmitted.

Problem Fix/Workaround

Don't use the PDC in transmit mode and do not fill US_THR before TXEMPTY is set at 1.

1.2.8.3 USART: XOFF Character Bad Behavior

The XOFF character is sent only when the receive buffer is detected full. While the XOFF is being sent, the remote transmitter is still transmitting. As only one Holding register is available in the receiver, characters will be lost in reception. This makes the software handshaking functionality ineffective.

Problem Fix/Workaround

None.

1.2.9 Voltage Regulator

1.2.9.1 Voltage Regulator: Current Consumption in Deep Mode

Current consumption in Deep Mode is maximum 60 µA instead of 25 µA.

Due to current rejection from VDDIN to VDDCORE, the current consumption in Deep Mode cannot be guaranteed. Instead, 60 µA is guaranteed whatever the condition.

Problem Fix/Workaround

None.

1.2.9.2 *Voltage Regulator: Load Versus Temperature*

Maximum load is 50 mA at 85 °C (instead of 100 mA).

Maximum load is 100 mA at 70°C.

Problem Fix/Workaround

None.

1.3 AT91SAM7S128 Errata - Revision B Parts

Refer to Section 1.1 ”Marking”, on page 1.

Note: AT91SAM7S128 Revision B chip ID is: 0x270C 0741

1.3.1 Non Volatile Memory Bits (NVM Bits)

1.3.1.1 NVM Bits: Write/Erase Cycles Number

The maximum number of write/erase cycles for Non Volatile Memory bits is 100. This includes Lock Bits (LOCKx), General Purpose NVM bits (GPNVMx) and the Security Bit.

This maximum number of write/erase cycles is not applicable to 128 KB Flash memory, it remains at 10K for the Flash memory.

Problem Fix/Workaround

None.

1.3.2 Parallel Input/Output Controller (PIO)

1.3.2.1 PIO: Electrical Characteristics on NRST and PA0-PA16 and PA21-31

When NRST or PA0-PA16 or PA21-PA31 are set as digital inputs with pull-up enabled, the voltage of the I/O stabilizes at VPull-up.

Vpull-up

VPull-up Min	VPull-up Max
VDDIO - 0.65 V	VDDIO - 0.45 V

This condition causes a leakage through VDDIO. This leakage is 45 µA per pad in worst case at 3.3 V and 25 µA at 1.8V.

I Leakage

Parameter	Typ	Max
I Leakage at 3,3V	2.5 µA	45 µA
I Leakage at 1.8V	1 µA	25 µA

Problem Fix/Workaround

It is recommended to use an external pull-up if needed.

1.3.2.2 PIO: Drive Low NRST, PA0-PA16 and PA21-PA31

When NRST or PA0-PA16 and or PA21-PA31 are set as digital inputs with pull-up enabled, driving the I/O with an output impedance higher than 500 ohms may not drive the I/O to a logical zero.

Problem Fix/Workaround

Output impedance must be lower than 500 ohms.

1.3.3 Pulse Width Modulation Controller (PWM)

1.3.3.1 PWM: Update when PWM_CCNTx = 0 or 1

If the Channel Counter Register value is 0 or 1, the Channel Period Register or Channel Duty Cycle Register is directly modified when writing the Channel Update Register.

Problem Fix/Workaround

Check the Channel Counter Register before writing the update register.

1.3.3.2 PWM: Update when PWM_CPRDx = 0

When Channel Period Register equals 0, the period update is not operational.

Problem Fix/Workaround

Do not write 0 in the period register.

1.3.3.3 PWM: Counter Start Value

In left aligned mode, the first start value of the counter is 0. For the other periods, the counter starts at 1.

Problem Fix/Workaround

None.

1.3.3.4 PWM: Constraints on Duty Cycle Value

Setting Channel Duty Cycle Register (PWM_CDTYx) at 0 in center aligned mode or at 0 or 1 in left aligned mode may change the polarity of the signal.

Problem Fix/Workaround

Do not set PWM_CDTYx at 0 in center aligned mode.

Do not set PWM_CDTYx at 0 or 1 in left aligned mode.

1.3.3.5 PWM: Behavior of CHIDx Status Bits in the PWM_SR Register

Erratic behavior of the CHIDx status bit in the PWM_SR Register. When a channel is disabled by writing in the PWM_DIS Register just after enabling it (before completion of a Clock Period of the clock selected for the channel), the PWM line is internally disabled but the CHIDx status bit in the PWM_SR stays at 1.

Problem Fix/Workaround

Do not disable a channel before completion of one period of the selected clock.

1.3.4 Real Time Timer (RTT)

1.3.4.1 RTT: Possible Event Loss when Reading RTT_SR

If an event (RTTINC or ALMS) occurs within the same slow clock cycle during which the RTT_SR is read, the corresponding bit might be cleared. This can lead to the loss of this event.

Problem Fix/Workaround:

The software must handle the RTT event as an interrupt and should not poll RTT_SR.

1.3.5 Serial Peripheral Interface (SPI)

1.3.5.1 SPI: Bad tx_ready behavior when CSAAT = 1 and SCBR = 1

If the SPI is programmed with CSAAT = 1, SCBR(baudrate) = 1 and two transfers are performed consecutively on the same slave with an IDLE state between them, the tx_ready signal does not rise after the second data has been transferred in the shifter. This can imply for example, that the second data is sent twice.

Problem Fix/Workaround

Do not use the combination CSAAT = 1 and SCBR = 1.

1.3.5.2 SPI: LASTXFER (Last Transfer) behavior

In FIXED Mode, with CSAAT bit set, and in “PDC mode” the Chip Select can rise depending on the data written in the SPI_TDR when the TX_EMPTY flag is set. If for example, the PDC writes a “1” in the bit 24 (LASTXFER bit) of the SPI_TDR, the chip select will rise as soon as the TXEMPTY flag is set.

Problem Fix/Workaround

Use the CS in PIO mode when PDC mode is required and CS has to be maintained between transfers.

1.3.5.3 SPI: SPCK Behavior in Master Mode

SPCK pin can toggle out before the first transfer in Master Mode.

Problem Fix/Workaround

In Master Mode, MSTR bit must be set (in SPI_MR register) before configuring SPI_CSRx registers.

1.3.5.4 SPI: Chip Select and Fixed Mode

In fixed Mode, if a transfer is performed through a PDC on a Chip select different from the Chip select 0, the output spi_size sampled by the PDC will depend on the field, BITS (Bits per Transfer) of SPI_CSR0 register, whatever the selected Chip select is. For example, if SPI_CSR0 is configured for a 10-bit transfer whereas SPI_CSR1 is configured for an 8-bit transfer, when a transfer is performed in Fixed mode through the PDC, on Chip select 1, the transfer will be considered as a HalfWord transfer.

Problem Fix/Workaround

If a PDC transfer has to be performed in 8 bits, on a Chip select y (y as different from 0), the BITS field of the SPI_CSR0 must be configured in 8 bits, in the same way as the BITS field of the CSRy Register.

1.3.5.5 SPI: Baudrate Set to 1

When Baudrate is set at 1 (i.e. when serial clock frequency equals the system clock frequency) and when the BITS field of the SPI_CSR register (number of bits to be transmitted) equals an ODD value (in this case 9,11,13 or 15), an additional pulse will be generated on output SPCK.

Everything is OK if the BITS field equals 8,10,12,14 or 16 and Baudrate = 1.

Problem Fix/Workaround

None.

1.3.5.6 SPI: Disable In Slave Mode

The SPI disable is not possible in slave mode.

Problem Fix/Workaround

Read first the received data, then perform the software reset.

1.3.6 Synchronous Serial Controller (SSC)

1.3.6.1 SSC: Periodic Transmission Limitations in Master Mode

If the Least Significant Bit is sent first (MSBF = 0), the first TAG during the frame synchro is not sent.

Problem Fix/Workaround

None.

1.3.6.2 SSC: Transmitter Limitations in Slave Mode

If TK is programmed as output and TF is programmed as input, it is impossible to emit data when the start of edge (rising or falling) of synchro has a Start Delay equal to zero.

Problem Fix/Workaround

None.

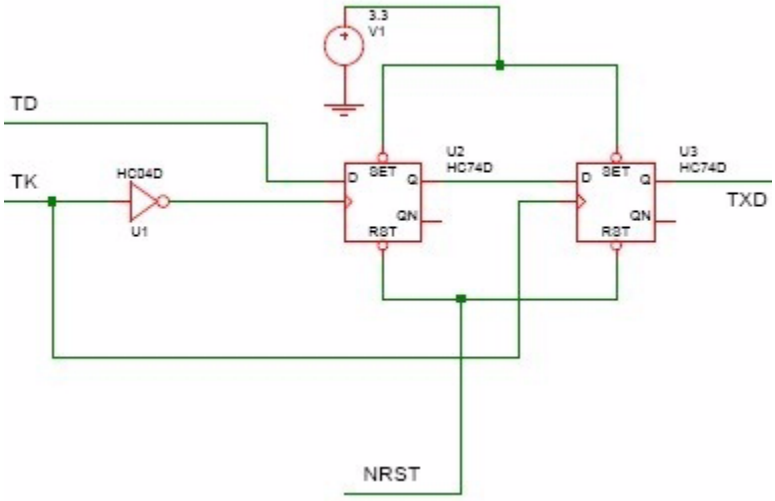
1.3.6.3 SSC: Transmitter Limitations in Slave Mode

If TK is programmed as an input and TF is programmed as an output and requested to be set to low/high during data emission, the Frame Synchro signal is generated one bit clock period after the data start and one data bit is lost. This problem does not exist when generating a periodic synchro.

Problem Fix/Workaround

The data need to be delayed for one bit clock period with an external assembly.

In the following schematic, TD, TK and NRST are AT91SAM7S signals, TXD is the delayed data to connect to the device.



1.3.7 Two-wire Interface (TWI)

1.3.7.1 TWI: Clock Divider

The value of CLDIV x 2^{CKDIV} must be less than or equal to 8191, the value of CHDIV x 2^{CKDIV} must be less than or equal to 8191·

Problem Fix/Workaround

None.

1.3.7.2 TWI: Software Reset

When a software reset is performed during a frame and when TWCK is low, it is impossible to initiate a new transfer in READ or WRITE mode.

Problem Fix/Workaround

None.

1.3.7.3 TWI: Disabling Does not Operate Correctly

Any transfer in progress is immediately frozen if the Control Register (TWI_CR) is written with the bit MSDIS at 1. Furthermore, the status bits TXCOMP and TXRDY in the Status Register (TWI_SR) are not reset.

Problem Fix/Workaround

The user must wait for the end of transfer before disabling the TWI. In addition, the interrupts must be disabled before disabling the TWI.

1.3.7.4 TWI: NACK Status Bit Lost

During a master frame, if TWI_SR is read between the Non Acknowledge condition detection and the TXCOMP bit rising in the TWI_SR, the NACK bit is not set.

Problem Fix/Workaround

The user must wait for the TXCOMP status bit by interrupt and must not read the TWI_SR as long as transmission is not completed.

TXCOMP and NACK fields are set simultaneously and the NACK field is reset after the read of the TWI_SR.

1.3.7.5 TWI: Possible Receive Holding Register Corruption

When loading the TWI_RHR, the transfer direction is ignored. The last data byte received in the TWI_RHR is corrupted at the end of the first subsequent transmit data byte. Neither RXRDY nor OVERRUN status bits are set if this occurs.

Problem Fix/Workaround

The user must be sure that received data is read before transmitting any new data.

1.3.8 USART: Universal Synchronous Asynchronous Receiver Transmitter

1.3.8.1 USART: CTS in Hardware Handshaking

When Hardware Handshaking is used and if CTS goes low near the end of the starting bit, a character can be lost.

Problem Fix/Workaround

CTS must not go low during a time slot occurring between 2 Master Clock periods before the starting bit and 16 Master Clock periods after the rising edge of the starting bit.

1.3.8.2 USART: Hardware Handshaking – Two Characters Sent

If CTS switches from 0 to 1 during the TX of a character and if the holding register (US_THR) is not empty, the content of US_THR will also be transmitted.

Problem Fix/Workaround

Don't use the PDC in transmit mode and do not fill US_THR before TXEMPTY is set at 1.

1.3.8.3 USART: XOFF Character Bad Behavior

The XOFF character is sent only when the receive buffer is detected full. While the XOFF is being sent, the remote transmitter is still transmitting. As only one Holding register is available in the receiver, characters will be lost in reception. This makes the software handshaking functionality ineffective.

Problem Fix/Workaround

None.

1.3.9 Voltage Regulator

1.3.9.1 Voltage Regulator: Current Consumption in Deep Mode

Current consumption in Deep Mode is maximum 60 µA instead of 25 µA.

Due to current rejection from VDDIN to VDDCORE, the current consumption in Deep Mode cannot be guaranteed. Instead, 60 µA is guaranteed whatever the condition.

Problem Fix/Workaround

None.

1.3.9.2 Voltage Regulator: Load Versus Temperature

Maximum load is 50 mA at 85 °C (instead of 100 mA).

Maximum load is 100 mA at 70°C.

Problem Fix/Workaround

None.