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AX88796BLF / AX88796BLI

Low-pin-count Non-PCI 8/16-bit 10/100M Fast Ethernet Controller

Features

Document No.: AX88796B_16/04/27/07

- High-performance non-PCI local bus
  - Support both 8 bit and 16 bit local CPU interfaces include MCS-51 series, 80186 series CPU and ISA bus
  - SRAM-like host interface, easily interfaced to most common embedded MCUs
  - Embed 8Kx16 bits SRAM for packet buffers
  - Support Slave-DMA to minimize CPU overhead
  - Support burst-mode read for highest performance applications
  - Interrupt pin with programmable Hold-off timer
- Single-chip Fast Ethernet controller
  - Compatible with IEEE802.3, 802.3u standards
  - Integrate Fast Ethernet MAC/PHY transceiver in one chip
  - Support 10Mbps and 100Mbps data rate
  - Support full and half duplex operations
  - Support 10/100Mbps N-way Auto-negotiation operation
  - Support twisted pair crossover detection and auto-correction (HP Auto-MDIX)
  - Support IEEE 802.3x flow control for full-duplex operation
  - Support back-pressure flow control for half-duplex operation
  - Support VLAN match filter
- Support Wake-on-LAN function to reduce power by following events
  - Detection of a change in the network link state
  - Receipt of a Magic Packet
  - Receipt of a MS wakeup frame
- NE2000 register level compatible instruction
  - Detection performance can be enhanced with only a minor host driver modification from original NE2000 driver
- Support EEPROM interface to store MAC address (Optional)
- Support up to 2 (out) /1 (in/out) General Purpose pins
- Support LED pins for various network activity indications
- Integrate voltage regulator and 25MHz crystal oscillator
- 0.18um CMOS process. 3.3V power supply with 5V tolerance I/O pins
- 64-pin LQFP , RoHS package
- Operate over 0 to +70 °C or -40 to +85 °C temperature range
- US patent approved (NO 6799231)

Product description

The AX88796B is a low-pin-count (64-pin LQFP) non-PCI Ethernet controller for the Embedded and Industrial Ethernet applications. The AX88796B supports 8/16-bit SRAM-like host interface, providing a glue-less connection to most common embedded MCUs. The AX88796B integrates on-chip Fast Ethernet MAC and PHY, which is IEEE802.3 10Base-T and IEEE802.3u 100Base-TX compatible, and 8Kx16 bits embedded SRAM for packet buffering to accommodate high bandwidth applications. The AX88796B has a wide array of features including support for Twisted Pair Crossover Detection and Auto-Correction, Wake-on-LAN power management, and IEEE 802.3x and back-pressure flow control. The AX88796B supports two operating temperature ranges, namely, commercial grade from 0 to 70 °C and industrial grade from –40 to 85 °C. The small form factor of 64-pin LQFP package helps reduce the overall PCB space. The programming of AX88796B is simple and compatible with NE2000, so the users don't need any modification and can easily port the software drivers to many embedded systems very quickly. Combining these features with ASIX's free TCP/IP software stack for 8-bit microcontrollers, AX88796B provides the best Ethernet solution for embedded networking applications.

System Block Diagram

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1.0 Introduction

1.1 General Description:

The AX88796B provides industrial standard NE2000 registers level compatible instruction set. Various drivers are easily acquired, maintained, and used and no much additional effort is required. Software is easily port to various embedded systems with no pain and tears. AX88796B also provides transmit queuing function to enhance standard NE2000 of transmitting performance.

The AX88796B Fast Ethernet Controller is a high performance and highly integrated local CPU bus Ethernet Controller with embedded 10/100Mbps PHY/Transceiver and 8K*16 bit SRAM. The AX88796B supports both 8/16-bit local CPU interfaces including MCS-51 series, 80186 series, ISA bus and high-performance SRAM-like interface. The simple host interface provides a glue-less connection to most common microprocessors and microcontrollers. The AX88796B provides both 10Mbps and 100Mbps Ethernet function based on IEEE802.3 / IEEE802.3u LAN standard.

1.2 AX88796B Block Diagram:

Fig - 1 AX88796B Block Diagram

1.3 AX88796B Pin Connection Diagram

The AX88796B is housed in the 64-pin plastic light quad flat pack. Fig - 2 shows the AX88796B pinout diagram.

Fig - 2 AX88796B Pin Out Diagram

2.0 Signal Description

The following abbreviations are used in AX88796B pinout:
All pin names with the "n" suffix are low-active signals.
The following abbreviations are used in following Tables.

I	**Input 1.8V**	**8m**	**8mA driving strength**
O	**Output 1.8V**	**S**	**Schmitt trigger**
I5	**Input 3.3V with 5V tolerant**	**PU**	**Internal Pull Up 75Kohm**
O5	**Output 3.3V with 5V tolerant**	**PD**	**Internal Pull Down 75kohm**
T5	**Tri-state with 5V tolerant**	**P**	**Power Pin**
B5	**Bi-directional I/O, 3.3V with 5V tolerant**	**A**	**Analog**
4m	**4mA driving strength**		

2.1 Local CPU Bus Interface Signals Group

Signal	Type	Pin No.	Description
SA[4:0]	I5	46, 47, 48, 49, 50	System Address: Signals SA[4:0] are address bus input lines. Used to select internal CSR's.
SA[5] or FIFO_SEL	I5/PD	45	System Address or FIFO Select: When driven high, all accesses to the AX88796B are to the RX or TX data buffer FIFO (DP). AX88796B supports two kinds of Data Port for receiving/transmitting packets from/to AX88796B. One is the PIO Data Port (offset 10h); the other one is the SRAM-like Data Port (e.g. offset 800h ~ FFFh for Samsung2440 processor as described in Appendix A4 of AX88796B datasheet). The SRAM-like Data Port address range depends on which address line of host processor is being connected to the address line SA5/FIFO_SEL of AX88796B. Software on host CPU can issue Single Data Read/Write command to both PIO Data Port and SRAM-like Data Port. However, to use Burst Data Read/Write commands, one has to use SRAM-like Data Port, which requires SA5/FIFO_SEL (pin 45) of AX88796B connecting to an upper address line of host CPU. Our reference schematic has SA5/FIFO_SEL pin connected to upper address line for supporting Burst Data Read/Write commands.
SD[15:0]	B5/8m	27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42	System Data Bus: Signals SD[15:0] constitute the bi-directional data bus.
IRQ	O5/T5/8m	23	Programmable Interrupt request. Programmable polarity, source and buffer types. Can be configure by EEPROM auto-loader or BTCR (offset 15h)
CSn	I5	52	Chip Select: Active low.
RDn	I5	53	Read: Active low strobe to indicate a read cycle.
WRn	I5	54	Write: Active low strobe to indicate a write cycle. This signal also used to wakeup the AX88796B when it is in reduced power state.
IOIS16n	T5/8m	55	16 Bit Port: For ISA bus used. The IOIS16n is asserted when the address at the range corresponds to an I/O address to which the chip responds, and the I/O port addressed is capable of 16-bit access.
AEN or PSEN	I5	51	Address Enable: When 186, ISA mode, this signal is active low to access AX88796B. PSEN: When 51 modes, this signal is active high to access AX88796B.

PME	O5/T5/8m	22	Wakeup Indicator: When programmed to do so, is asserted when the AX88696B detects a wake event and is requesting the system to wake up from the D1 sleep state. The polarity and buffer type of this signal is programmable by BTCR (offset 15h)

Tab - 1 Local CPU bus interface signals group

2.2 10/100Mbps Twisted-Pair Interface pins group

Signal	Type	Pin No.	Description
TPI+	AB	3	Twisted Pair Receive Input, Positive
TPI-	AB	4	Twisted Pair Receive Input, Negative
TPO+	AB	6	Twisted Pair Transmit Output, Positive
TPO-	AB	7	Twisted Pair Transmit Output, Negative
RSET_BG	AO	64	Off-chip resister. Must be connected 12.1K ohm ± 1% to ground.

Tab - 2 10/100Mbps Twisted-Pair Interfaces pins group

2.3 Built-in PHY LED indicator pins group

Signal	Type	Pin No.	Description
I_FULL/COL	O5/8m	16	Full-Duplex/Collision Status. If this signal is low, it indicates full-duplex link established, and if it is high, then the link is in half-duplex mode. When in half-duplex and collision occurrence, the output will be driven low for 80ms and driven high at minimum 80ms.
I_SPEED	O5/8m	15	Speed Status: If this signal is low, it indicates 100Mbps, and if it is high, then the speed is 10Mbps.
I_LK/ACT	O5/8m	14	Link Status/Active: If this signal is low, it indicates link, and if it is high, then the link is fail. When in link status and line activity occurrence, this signal is pulsed high (LED off) for 80ms whenever transmit or receive activity is detected. This signal is then driven low again for a minimum of 80ms, after which time it will repeat the process if TX or RX activity is detected.

Tab - 3 Built-in PHY LED indicator pins group

2.4 EEPROM Signals Group

Signal	Type	Pin No.	Description
EECS	B5/4m/PD	21	EEPROM Chip Select: EEPROM chip select signal.
EECK	B5/4m/PD	20	EEPROM Clock: Signal connected to EEPROM clock pin. EECS, EECK can load BUS type setting during power on reset cycle.

EECS	EECK	BUS TYPE
0	0	ISA BUS / SRAM-Like
0	1	80186
1	0	Reserved
1	1	MCS-51 (805X)

EEDIO	B5/4m/PU	19	EEPROM Data In/Out: Signal connected to EEPROM data input and data output pin.

Tab - 4 EEPROM bus interface signals group

2.5 Miscellaneous pins group

Signal	Type	Pin No.	Description
XTALIN	I	61	Crystal/Oscillator Input: A 25Mhz crystal, +/- 50 PPM can be connected across XTALIN and XTALOUT. CMOS Local Clock: A 25Mhz clock, +/- 50 PPM, 40%-60% duty cycle. Note that the pin does not support 3.3V or 5V voltage supply.
XTALOUT	O	62	Crystal/Oscillator Output: A 25Mhz crystal, +/- 50 PPM can be connected across XTALIN and XTALOUT. If a single-ended external clock (LCLK) is connected to XTALIN, the crystal output pin should be left floating.
RSTn	I5/S	17	Reset: Reset is active low then place AX88796B into reset mode. During the rising edge the AX88796B loads the power on setting data.
TCLK	I5/PD	56	Test Clock Pins: As a clock input for ASIC testing only No connection when normal operation
TCLK_EN	I5/PD/S	57	Enable TCLK in to ASIC as a main clock for test only. No connection when normal operation
TEST2	I5/S	12	TEST mode select Connect to ground when normal operation
TEST1	I5/S	13	TEST mode select Connect to ground when normal operation
VCC3A3	P	1	Power Supply for Analog Circuit: +3.3V DC.
GND3A3	P	2	Power Supply for Analog Circuit: +0V DC or Ground Power.
VCC18A	P	5, 60	Analog power for oscillator, PLL, and Ethernet PHY differential I/O pins, 1.8V
GND18A	P	8, 63	Analog ground for oscillator, PLL, and Ethernet PHY differential I/O pins.
V18F	P	9	On-chip 3.3V to 1.8V Regulator output +1.8V DC.
VCC3R3	P	10	On-chip 3.3V to 1.8V Regulator power supply: +3.3V DC.
GND3R3	P	11	On-chip 3.3V to 1.8V Regulator ground.
GND	P	18, 26, 58	Ground.
VCC3IO	P	25, 44	Power Supply for IO: +3.3V DC.
VCCK	P	24, 43, 59	Power Supply for core logic: +1.8V DC.

Tab - 5 miscellaneous pins group

3.0 Memory and CSR Mapping

1. EEPROM Memory Mapping
2. CSR Mapping
3. Local Memory Mapping

3.1 EEPROM Memory Mapping

EEPROM interface can access via CSR offset 14h SMI/EEPROM registers when auto load operation completed. The content of EEPROM data will be auto-loaded to internal memory from 0000h to 001Fh and from 0400h to 040Fh automatically when hardware reset. It is similar to NE2000 PROM store Ethernet address. The real MAC address must configured by PAR0 ~ PAR5 (CR page1 offset1 ~ offset6). The auto-loader only write to internal SRAM not write to PAR0 ~ PAR5. An example as below, if the desired Ethernet physical address is 10-32-54-76-98-BA
It is a programmed EEPROM if auto-load value is 5AA5h from EEPROM address 0h. After hardware reset the EEPROM loader will read first word and check pattern 5AA5h. If the first word value not equal to 5AA5h then the EEPROM loader proclaimed that no external EEPROM or external EEPROM is a non-programmed EEPROM.

Addr	Bits	D[15:8]	D[7:0]	Description
5h	[15:0]	BAh	98h	MAC address 6th, 5th
4h	[15:0]	76h	54h	MAC address 4th, 3rd
3h	[15:0]	32h	10h	MAC address 2nd, 1st (multicast bit is 1st of bit_0)
2h	[15:11]	No define		Always zero
	[10:8]	PHY_CONFIG		Configure internal PHY in different ways, such as 10BASE_T half-duplex mode. If EEPROM auto loader not found 5AA5h pattern in first word then internal PHY will be not been manual configuration. (Default is Auto-negotiation enable with all capabilities)
				[10:8] — Function
				000 — Auto-negotiation enable with all capabilities
				001 — Auto-negotiation with 100BASE-TX FDX / HDX ability
				010 — Auto-negotiation with 10BASE-T FDX / HDX ability
				011 — Reserved
				100 — Manual selection of 100BASE-TX FDX
				101 — Manual selection of 100BASE-TX HDX
				110 — Manual selection of 10BASE-T FDX
				111 — Manual selection of 10BASE-T HDX
	[7:6]		No define	Always zero
	[5]		IRQ_TYPE_EEP	This bit will logic OR with BTCR (15h) bit-5 and will been clear when host write BTCR. (Offset 15h)
	[4]		IRQ_POL_EEP	This bit will logic OR with BTCR (15h) bit-4 and will been clear when host write BTCR. (Offset 15h)
	[3]		No define	Always zero
	[2]		NE2000_PROM	When set, AX88796B internal memory map of 1Ch ~ 1Fh will be configured to 57h. An ASCII code “W”. Otherwise configured to 42h. An ASCII code “B”.
	[1:0]		No define	Always zero
1h	[15:0]	00h	06h	Indicates the total of word counts for auto loading
0h	[15:0]	5Ah	A5h	Programmed pattern

Tab - 6 EEPROM data format example

3.2 CSR Mapping

System I/O Offset	Function
0000H ~ 001FH	AX88796B Command Status Register

Tab - 7 CSR Address Mapping

3.3 Internal SRAM Memory Mapping

Offset	Function
0000H ~ 001FH	Load from EEPROM
0020H ~ 03FFH	Reserved
0400H ~ 040FH	Load from EEPROM
0410H ~ 3FFFH	Reserved
4000H ~ 7FFFH	NE2000 compatible mode 8K x 16 SRAM Buffer
8000H ~ FFFFH	Reserved

Tab - 8 Local Memory Mapping

SRAM Address	D[15:8]	D[7:0]
1EH	57H / 42H	57H / 42H
1CH	57H / 42H	57H / 42H
1AH ~ 10H	00H	00H
0AH	BAH	BAH (E'NET ADDRESS 5)
08H	98H	98H (E'NET ADDRESS 4)
06H	76H	76H (E'NET ADDRESS 3)
04H	54H	54H (E'NET ADDRESS 2)
02H	32H	32H (E'NET ADDRESS 1)
00H	10H	10H (E'NET ADDRESS 0)

Tab - 9 Internal SRAM Map 00H ~ 1FH

SRAM Address	D[15:8]	D[7:0]
40EH	57H	57H
0406H ~ 040DH	00H	00H
0404H	BAH (E'NET ADDRESS 5)	98H (E'NET ADDRESS 4)
0402H	76H (E'NET ADDRESS 3)	54H (E'NET ADDRESS 2)
0400H	32H (E'NET ADDRESS 1)	10H (E'NET ADDRESS 0)

Tab - 10 internal SRAM Map 0400H ~ 040FH

AX88796B internal memory address mapping

Fig - 3 Internal SRAM map

4.0 Basic Operation

4.1 Receiver Filtering

The address filtering logic compares the Destination Address Field (first 6 bytes of the received packet) to the Physical address registers stored in the Address Register Array. If any one of the six bytes does not match the pre-programmed physical address, the Protocol Control Logic rejects the packet. This is for unicast address filtering. All multicast destination addresses are filtered using a hashing algorithm. (See following description.) If the multicast address indexes a bit that has been set in the filter bit array of the Multicast Address Register Array the packet is accepted, otherwise the Protocol Control Logic rejects it. Each destination address is also checked for all 1's, which is the reserved broadcast address.

4.1.1 Unicast Address Match Filter

The physical address registers are used to compare the destination address of incoming packets for rejecting or accepting packets. Comparisons are performed on a byte wide basis. The bit assignment shown below relates the sequence in PAR0-PAR5 to the bit sequence of the received packet.

	D7	D6	D5	D4	D3	D2	D1	D0
PAR0	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
PAR1	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
PAR2	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16
PAR3	DA31	DA30	DA29	DA28	DA27	DA26	DA25	DA24
PAR4	DA39	DA38	DA37	DA36	DA35	DA34	DA33	DA32
PAR5	DA47	DA46	DA45	DA44	DA43	DA42	DA41	DA40

Note: The bit sequence of the received packet is DA0, DA1, … DA7, DA8 ….

4.1.2 Multicast Address Match Filter

The Multicast Address Registers provide filtering of multicast addresses hashed by the CRC logic. All destination addresses are fed through the 32 bits CRC generation logic and as the last bit of the destination address enters the CRC, the 6 most significant bits of the CRC generator are latched. These 6 bits are then decoded by a 1 of 64 decode to index a unique filter bit (FB0-63) in the Multicast Address Registers. If the filter bit selected is set, the multicast packet is accepted. The system designer would use a program to determine which filter bits to set in the multicast registers. All multicast filter bits that correspond to Multicast Address Registers accepted by the node are then set to one. To accept all multicast packets all of the registers are set to all ones.

	D7	D6	D5	D4	D3	D2	D1	D0
MAR0	FB7	FB6	FB5	FB4	FB3	FB2	FB1	FB0
MAR1	FB15	FB14	FB13	FB12	FB11	FB10	FB9	FB8
MAR2	FB23	FB22	FB21	FB20	FB19	FB18	FB17	FB16
MAR3	FB31	FB30	FB29	FB28	FB27	FB26	FB25	FB24
MAR4	FB39	FB38	FB37	FB36	FB35	FB34	FB33	FB32
MAR5	FB47	FB46	FB45	FB44	FB43	FB42	FB41	FB40
MAR6	FB55	FB54	FB53	FB52	FB51	FB50	FB49	FB48
MAR7	FB63	FB62	FB61	FB60	FB59	FB58	FB57	FB56

If address Y is found to hash to the value 32 (20H), then FB32 (ref. 4.1.2) in MAR2 should be initialized to ``1". This will cause the AX88796B to accept any multicast packet with the address Y.
Although the hashing algorithm does not guarantee perfect filtering of multicast address, it will perfectly filter up to 64 logical address filters if these addresses are chosen to map into unique locations in the multicast filter.

Note: The first bit of received packet sequence is 1's stands by Multicast Address.

4.1.3 Broadcast Address Match Filter

The Broadcast check logic compares the Destination Address Field (first 6 bytes of the received packet) to all 1's, which is the values are "FF FF FF FF FF FF FF" in Hex format. If any bit of the six bytes does not equal to 1's, the Protocol Control Logic rejects the packet.

4.1.4 VLAN Match Filter

AX88796B compares the thirteenth and fourteenth bytes of receive frames. If not match with VLAN_ID1, VLAN_ID_0 (offset 1dh, 1ch) then reject current frame. The VLAN filter will always accept VLAN_ID is zero of receive frames due to it is 802.1q (for priority purpose) frames. The maximum length of the good packet is thus change from 1518 bytes to 1522 bytes.

4.1.5 Aggregate Address Filter with Receive Configuration Setup

The final address filter decision depends on the destination address types, identified by the above 4 address match filters, and the setup of parameters of Receive Configuration Register.

Definitions of address match filter result are as following:

Signal	Value	Description
Phy	=1	Unicast Address Match
	=0	Unicast Address not Match
Mul	=1	Multicast Address Match
	=0	Multicast Address not Match
Bro	=1	Broadcast Address Match
	=0	Broadcast Address not Match
VID	=1	VLAN ID Match
	=0	VLAN ID not Match
AGG	=1	Aggregate Address Match
	=0	Aggregate Address not Match

The meaning of AB, AM and PRO signals, please refer to “Receive Configuration Register” RCR (offset 0Ch)
The meaning of VLANE signal, Please refer to “MAC Configure Register” MCR (offset 1Bh)

Aggregate Address Filter function will be:

4.2 Buffer Management Operation

There are four buffer memory access types used in AX88796B.

1. Packet Reception (Write data to memory from MAC)
2. Packet Transmission (Read data from memory to MAC)
3. Filling Packets to Transmit Buffer (Host fill data to memory)
4. Removing Packets from the Receive Buffer Ring (Host read data from memory)

The type 1 and 2 operations act as Local DMA. Type 1 does Local DMA write operation and type 2 does Local DMA read operation. The type 3 and 4 operations act as Remote DMA. Type 3 does Remote DMA write operation and type 4 does Remote DMA read operation.

4.2.1 Packet Reception

The Local DMA receives channel uses a Buffer Ring Structure comprised of a series of contiguous fixed length 256 byte (128 word) buffers for storage of received packets. The location of the Receive Buffer Ring is programmed in two registers, a Page Start and a Page Stop Register. Ethernet packets consist of minimum packet size (64 bytes) to maximum packet size (1522 bytes), the 256 byte buffer length provides a good compromise between short packets and longer packets to most efficiently use memory. In addition these buffers provide memory resources for storage of back-to-back packets in loaded networks. Buffer Management Logic in the AX88796B controls the assignment of buffers for storing packets. The Buffer Management Logic provides three basic functions: linking receive buffers for long packets, recovery of buffers when a packet is rejected, and recalculation of buffer pages that have been read by the host.

At initialization, a portion of the 16k byte (or 8k word) address space is reserved for the receiver buffer ring. Two eight bit registers, the Page Start Address Register (PSTART) and the Page Stop Address Register (PSTOP) define the physical boundaries of where the buffers reside. The AX88796B treats the list of buffers as a logical ring; whenever the DMA address reaches the Page Stop Address, the DMA is reset to the Page Start Address.

Fig - 4 Receive Buffer Ring

Initialization Of The Buffer Ring

Two static registers and two working registers control the operation of the Buffer Ring. These are the Page Start Register, Page Stop Register (both described previously), the Current Page Register and the Boundary Pointer Register. The Current Page Register points to the first buffer used to store a packet and is used to restore the DMA for writing status to the Buffer Ring or for restoring the DMA address in the event of a Runt packet, a CRC, or Frame Alignment error. The Boundary Register points to the first packet in the Ring not yet read by the host. If the local DMA address ever reaches the Boundary, reception is aborted. The Boundary Pointer is also used to initialize the Remote DMA for removing a packet and is advanced when a packet is removed. A simple analogy to remember the function of these registers is that the Current Page Register acts as a Write Pointer and the Boundary Pointer acts as a Read Pointer.

Fig - 5 Receive Buffer Ring At Initialization

Beginning Of Reception

When the first packet begins arriving the AX88796B and begins storing the packet at the location pointed to by the Current Page Register. An offset of 4 bytes is reserved in this first buffer to allow room for storing receives status corresponding to this packet.

Linking Receive Buffer Pages

If the length of the packet exhausts the first 256 bytes buffer, the DMA performs a forward link to the next buffer to store the remainder of the packet. For a maximal length packet the buffer logic will link six buffers to store the entire packet. Buffers cannot be skipped when linking; a packet will always be stored in contiguous buffers. Before the next buffer can be linked, the Buffer Management Logic performs two comparisons. The first comparison tests for equality between the DMA address of the next buffer and the contents of the Page Stop Register. If the buffer address equals the Page Stop Register, the buffer management logic will restore the DMA to the first buffer in the Receive Buffer Ring value programmed in the Page Start Address Register. The second of comparison test between the DMA address of the next buffer address and the contents of the Boundary Pointer Register. If the two values are equal the reception is aborted. The Boundary Pointer Register can be used to protect against overwriting any area in the receive buffer that has not yet been read. When linking buffers, buffer management will never cross this pointer, effectively avoiding any overwrites. If the buffer address does not match either the Boundary Pointer or Page Stop Address, the link to the next buffer is performed.

Linking Buffers

Before the DMA can enter the next contiguous 256 bytes buffer, the address is checked for equality to PSTOP and to the Boundary Pointer. If neither is reached, the DMA is allowed to use the next buffer.

Buffer Ring Overflow

If the Buffer Ring has been filled and the DMA reaches the Boundary Pointer Address, reception of the current incoming packet will be discard by the AX88796B. Thus, the packets previously received and still contained in the Ring will not be destroyed.

End Of Packet Operations

At the end of the packet the AX88796B determines whether the received packet is to be accepted or rejected. It either branch to a routine to store the or to another routine that recovers the buffers used to store the packet.
If current of packet is accepted then AX88796B write two words of buffer header on receive buffer.

Buffer Header	Description
NPR, Status	D[15:8]: Next Page Pointer D[7:6]: always zero D[5]: multicast or broadcast D[4]: runt packet D[3]: MII error D[2]: alignment error D[1]: CRC error D[0]: good packet
Length	D[15:11]: always zero D[10:0]: packet length

Successful Reception

If the packet is successfully received as shown, the DMA is restored to the first buffer used to store the packet (pointed to by the Current Page Register). The DMA then stores the Receive Status, a Pointer to where the next packet will be stored and the number of received bytes. Note that the remaining bytes in the last buffer are discarded and reception of the next packet begins on the next empty 256 byte buffer boundary. The Current Page Register is then initialized to the next available buffer in the Buffer Ring. (The location of the next buffer had been previously calculated and temporarily stored in an internal scratchpad register.)

Buffer Recovery For Rejected Packets

If the packet is a runt packet or contains CRC or Frame Alignment errors, it is rejected. The buffer management logic resets the DMA back to the first buffer page used to store the packet (pointed to by CPR), recovering all buffers that had been used to store the rejected packet. This operation will not be performed if the AX88796B is programmed to accept either runt packets or packets with CRC or Frame Alignment errors. The received CRC is always stored in buffer memory after the last byte of received data for the packet.

4.2.2 Packet Transmission

The Local DMA Read is also used during transmission of a packet. Three registers control the DMA transfer during transmission, a Transmit Page Start Address Register (TPSR) and the Transmit Byte Count Registers (TBCR0, 1). When the AX88796B receives a command to transmit the packet pointed to by these registers, buffer memory data will be moved into the FIFO as required during transmission. The AX88796B Controller will generate and append the preamble, synch and CRC fields. AX88796B supports options of transmit queue function to enhance transmit performance.

Original NE2000 Of Transmit Buffer

AX88796B remote DMA write default operation is continue to write next address even over transmit buffer area. Host can do whole memory read / write testing. And host must handle the transmit data do not overwrite receive buffer area when performing fill transmit data to transmit buffer.

Options Of Transmit Buffer As A Ring

When active Transmit Buffer Ring Enable (CR page3 of offset 0Dh). AX88796B remote DMA write operation will role over from last transmit page to first transmit page. Host no need reassign RSAR0, RSAR1 again to fill transmit data for first page.

Options Back-To-Back Transmission (TX Command Queue)

When active TX Queue Enable (offset 1Bh), Host can continue Writing TXP (bit 2 of CR register) to push TPSR and TBCR1, 0 into AX88796B TX command queue as long as Transmit buffer has enough vacancy and CTEPR (offset 1Ch) bit7 is ‘0’(Not full). After current packet transmitted completely, MAC TX will pop out next TPSR and TBCR1, 0 from TX Command Queue then transmit this packet following CSMA/CD protocol. It is recommended to enable this function to enhance TX performance.

AX88796B will report Current of Transmit End Page CTEPR (offset 1Ch) when every packet transmits completed.
Host can understand AX88796B current of transmitting buffer point by reading CTEPR.

Transmit Packet Assembly

The AX88796B requires a contiguous assembled packet with the format shown below. The transmit byte count includes the Destination Address, Source Address, Length Field and Data. It does not include preamble and CRC. When transmitting data smaller than 64 bytes, AX88796B can auto padding to a minimum length of 64 bytes Ethernet frame. The packets are placed in the buffer RAM by the system. System programs the AX88796B Core's Remote DMA to move the data from the system buffer RAM to internal transmit buffer RAM.

The data transfer must be 16-bits (1 word) when in 16-bit mode, and 8-bits when the AX88796B Controller is set in 8-bit mode. The data width is selected by setting the WTS bit in the Data Configuration Register.

Destination Address	6 Bytes
Source Address	6 Bytes
Length / Type	2 Bytes
Data (Pad if < 46 Bytes)	46 Bytes Min.

General Transmit Packet Format

Transmission

Prior to transmission, the TPSR (Transmit Page Start Register) and TBCR0, TBCR1 (Transmit Byte Count Registers) must be initialized. To initiate transmission of the packet the TXP bit in the Command Register is set. The Transmit Status Register (TSR) is cleared and the AX88796B begins to pre-fetch transmit data from memory. If the Inter-packet Gap (IPG) has timed out the AX88796B will begin transmission.

Conditions Required To Begin Transmission

In order to transmit a packet, the following three conditions must be met:
1. The Inter-packet Gap Timer has timed out
2. At least one byte has entered the FIFO.
3. If a collision had been detected then before transmission the packet back-off time must have timed out.

Collision Recovery

During transmission, the Buffer Management logic monitors the transmit circuitry to determine if a collision has occurred. If a collision is detected, the Buffer Management logic will reset the FIFO and restore the Transmit DMA pointers for retransmission of the packet. The COL bit will be set in the TSR and the NCR (Number of Collisions Register) will be incremented. If 15 retransmissions each result in a collision the transmission will be aborted and the ABT bit in the TSR will be set.

Transmit Packet Assembly Format

The following diagrams describe the format for how packets must be assembled prior to transmission for different byte ordering schemes. The various formats are selected in the Data Configuration Register.

D15 D8	D7 D0
D[15:8]	D[7:0]
Destination Address 1	Destination Address 0
Destination Address 3	Destination Address 2
Destination Address 5	Destination Address 4
Source Address 1	Source Address 0
Source Address 3	Source Address 2
Source Address 5	Source Address 4
Type / Length 1	Type / Length 0
Data 1	Data 0
…	…

WTS = 1 in Data Configuration Register.
This format is used with ISA or 80186 Mode.

D7 D0
Destination Address 0 (DA0)
Destination Address 1 (DA1)
Destination Address 2 (DA2)
Destination Address 3 (DA3)
Destination Address 4 (DA4)
Destination Address 5 (DA5)
Source Address 0 (SA0)
Source Address 1 (SA1)
Source Address 2 (SA2)
Source Address 3 (SA3)
Source Address 4 (SA4)
Source Address 5 (SA5)
Type / Length 0
Type / Length 1
Data 0
Data 1
…

WTS = 0 in Data Configuration Register.
This format is used with ISA or MCS-51 Mode.

Note: All examples above will result in a transmission of a packet in order of DA0 (Destination Address 0), DA1, DA2, DA3 and so on in byte. Bits within each byte will be transmitted least significant bit first.

4.2.3 Filling Packet to Transmit Buffer (Host fill data to memory)

The Remote DMA channel is used to both assembles packets for transmission, and to remove received packets from the Receive Buffer Ring. It may also be used as a general-purpose slave DMA channel for moving blocks of data or commands between host memory and local buffer memory. There are two modes of operation, Remote Write and Remote Read Packet.

Two register pairs are used to control the Remote DMA, a Remote Start Address (RSAR0, RSAR1) and a Remote Byte Count (RBCR0, RBCR1) register pair. The Start Address Register pair points to the beginning of the block to be moved while the Byte Count Register pair is used to indicate the number of bytes to be transferred. Full handshake logic is provided to move data between local buffer memory (Embedded Memory) and a bi-directional data port.

Remote Write

A Remote Write transfer is used to move a block of data from the host into local buffer memory. The Remote DMA will read data from the I/O port and sequentially write it to local buffer memory beginning at the Remote Start Address. The DMA Address will be incremented and the Byte Counter will be decremented after each transfer. The DMA is terminated when the Remote Byte Count Register reaches a count of zero.

4.2.4 Removing Packets from the Ring (Host read data from memory)

Remote Read

A Remote Read transfer is used to move a block of data from local buffer memory to the host. The Remote DMA will sequentially read data from the local buffer memory, beginning at the Remote Start Address, and write data to the I/O port. The DMA Address will be incremented and the Byte Counter will be decremented after each transfer. The DMA is terminated when the Remote Byte Count Register reaches zero.

Packets are removed from the ring using the Remote DMA or an external device. When using the Remote DMA. The Boundary Pointer can also be moved manually by programming the Boundary Register. Care should be taken to keep the Boundary Pointer at least one buffer behind the Current Page Pointer. The following is a suggested method for maintaining the Receive Buffer Ring pointers.

1. At initialization set up a software variable (next_pkt) to indicate where the next packet will be read. At the beginning of each Remote Read DMA operation, the value of next_pkt will be loaded into RSAR0 and RSAR1.
2. When initializing the AX88796B set:
   BNRY = PSTART
   CPR = PSTART + 1
   next_pkt = PSTART + 1
3. After a packet is DMAed from the Receive Buffer Ring, the Next Page Pointer (second byte in AX88796B receive packet buffer header) is used to update BNRY and next_pkt.
   next_pkt = Next Page Pointer
   BNRY = Next Page Pointer - 1
   If BNRY < PSTART then BNRY = PSTOP – 1

Note the size of the Receive Buffer Ring is reduced by one 256-byte buffer; this will not, however, impede the operation of the AX88796B. The advantage of this scheme is that it easily differentiates between buffer full and buffer empty.

It is full when BNRY = CPR.
It is empty when BNRY = CPR-1.

Storage Format For Received Packets

The following diagrams describe the format for how received packets are placed into memory by the local DMA channel. These modes are selected in the Data Configuration Register.

D15 D8	D7 D0
Next Packet Pointer	Receive Status
Receive Byte Count 1	Receive Byte Count 0
Destination Address 1	Destination Address 0
Destination Address 3	Destination Address 2
Destination Address 5	Destination Address 4
Source Address 1	Source Address 0
Source Address 3	Source Address 2
Source Address 5	Source Address 4
Type / Length 1	Type / Length 0
Data 1	Data 0
…	…

WTS = 1 in Data Configuration Register.
This format is used with ISA or 80186 Mode.

D7 D0
Receive Status
Next Packet Pointer
Receive Byte Count 0
Receive Byte Count 1
Destination Address 0
Destination Address 1
Destination Address 2
Destination Address 3
Destination Address 4
Destination Address 5
Source Address 0
Source Address 1
Source Address 2
Source Address 3
Source Address 4
Source Address 5
Type / Length 0
Type / Length 1
Data 0
Data 1
…

WTS = 0 in Data Configuration Register.
This format is used with ISA or MCS-51 Mode.

4.2.5 Other Useful Operations

Memory Diagnostics

Memory diagnostics can be achieved by Remote Write/Read DMA operations. The following is a suggested step for memory test and assume the AX88796B has been well initialized.

1. Issue the STOP command to the AX88796B. This is accomplished be setting the STP bit in the AX88796B's Command Register. Writing 21H to the Command Register will stop the AX88796B.
2. Wait for at least 1.5 ms. Since the AX88796B will complete any reception that is in progress, it is necessary to time out for the maximum possible duration of an Ethernet reception. This action prevents buffer memory from written data through Local DMA Write.
3. Write data pattern to MUT (memory under test) by Remote DMA write operation.
4. Read data pattern from MUT (memory under test) by Remote DMA read operation.
5. Compare the read data pattern with original write data pattern and check if it is equal.
6. Repeat step 3 to step 5 with various data pattern.

Loop-back Diagnostics

1. Issue the STOP command to the AX88796B. This is accomplished be setting the STP bit in the AX88796B's Command Register. Writing 21h to the Command Register will stop the AX88796B.
2. Wait for at least 1.5 ms. Since the AX88796B will complete any reception that is in progress, it is necessary to time out for the maximum possible duration of an Ethernet reception. This action prevents buffer memory from written data through Local DMA Write.
3. Place the AX88796B in mode 1 loop-back. (MAC internal loop-back) This can be accomplished by setting LB1 and LB0, of the Transmit Configuration Register to ``0,1".
4. Issue the START command to the AX88796B. This can be accomplished by writing 22h to the Command Register. This is necessary to activate the AX88796B's Remote DMA channel.
5. Write data that want to transmit to transmit buffer by Remote DMA write operation.
6. Issue the TXP command to the AX88796B. This can be accomplished by writing 26h to the Command Register.
7. Read data current receive buffer by Remote DMA read operation.
8. Compare the received data with original transmit data and check if it is equal.
9. Repeat step 5 to step 8 for more packets test.

4.3 Wake-up Detection

Setting wake up Control and Status WUCS (CR page3, offset 0Ah) and D1 power saving in Power Management Register PMR (CR page3, offset 0Bh), place the AX88796B in wake on LAN detection mode. In this mode, normal data reception is disabled. And detection logic within the MAC examines receive data for three kinds of WOL events.

- Examines receive data for the pre-programmed wake-up frame patterns
- Examines receive data for the Magic Packet frame patterns
- Examines PHY link status change

4.3.1 Wake-up frame

AX88796B supports four programmable filters that support many different receive packet patterns. If the remote wakeup mode is enable (in D1 sleep state). The remote wakeup function receives all frames and checks each frame against the enabled filter and recognizes the frame as a remote wake-up frame if it passes the MAC address filtering and CRC value match. In order to determine which bytes of the frames should be checked by the CRC-16 (x16 +x15 +x2 +1) module. AX88796B use a programmable byte mask and a programmable pattern offset for each of the four supported filters. AX88796B also provide last byte match check and options cascade four programmable filters. Make the four of detectors can operate simultaneously or sequentially.

The byte mask is a 32-bit field that specifies whether or not each of the 32 contiguous bytes within the frame, beginning in the pattern offset, should be checked. If bit j in the byte mask is set, the diction logic checks byte offset +j in the frame.

The pattern offset define on Offset 3 ~ 0 for each wake-up filter 3 ~ 0 and the real offset value equal to Offset register multiplied by 2. (For example, The real offset value equal to 12 if set 6 on Offset register field)

Last bytes 3 ~ 0 for each wake-up filter 3 ~ 0 also. The contents of Last Byte register must equal to the last of Byte Mask bit indicates of byte value. For example, if set Byte Mask [31:0] as 00C30003h then Byte Mask [23] is the last byte. Thus, The contents of Last byte register must equal to byte value of offset + 23.

In order to load the 32-bits of wake up control register host driver software must perform 4 writes for every 32 bit of registers.
The first write of 8-bit is located at [31:24]. The second write will also occupy [31:24] and shift the first write of data to [23:16]. The first write of data will be located at [7:0] after continue 4 times of write data.

3								2								1								0							
8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0

Byte Mask 0					
Byte Mask 1					
Byte Mask 2					
Byte Mask 3					
Wakeup Frame 1 CRC			Wakeup Frame 0 CRC		
Wakeup Frame 3 CRC			Wakeup Frame 2 CRC		
Offset 3	Offset 2		Offset 1	Offset 0	
Last Byte 3	Last Byte 2		Last Byte 1	Last Byte 0	
Reserved		Cascade Command [2:0]	Command 3	Command 2	Command 1	Command 0

Wake-Up frame Byte Mask Register Structure

.
For Example.
A Ping packet is configured as a Wakeup frame and AX88196B MAC address is 00 A0 0C C4 7D 69.

```
00 A0 0C C4 7D 69 00 0E C6 12 34 56 08 00 45 00
00 3C 01 8C 00 00 80 01 27 1E C0 09 C9 02 C0 09
C9 01 08 00 47 5C 05 00 01 00 61 62 63 64 65 66
67 68 69 6A 6B 6C 6D 6E 6F 70 71 72 73 74 75 76
77 61 62 63 64 65 66 67 68 69 CRC (4 bytes)
```

Host configure Wakeup frame registers sequences

// Go to gape3
Write CR(Offset 0h) C2h ; page3
// Set Byte Mask 0 = 00 40 08 07
Write WFBM0 (Page3, Offset 01H) 07h ; WFBM0 = **07** 00 00 00h
Write WFBM0 (Page3, Offset 01H) 08h ; WFBM0 = **08 07** 00 00h
Write WFBM0 (Page3, Offset 01H) 40h ; WFBM0 = **40 08 07** 00h
Write WFBM0 (Page3, Offset 01H) 00h ; WFBM0 = **00 40 08 07**h
// Set {Wakeup Frame 1 CRC, Wakeup Frame 0 CRC} = 00 00 **2B 42**h
Write WF10CRC (Offset 05H) 42h ; WF10CRC = **42** 00 00 00h
Write WF10CRC (Offset 05H) 2Bh ; WF10CRC = **2B 42** 00 00h
Write WF10CRC (Offset 05H) 00h ; WF10CRC = **00 2B 42** 00h
Write WF10CRC (Offset 05H) 00h ; WF10CRC = **00 00 2B 42**h
// Set {Offset 3 2 1 0} = 00 00 00 06h
Write WFOFST (Offset 07H) 06h ; WFOFST = **06** 00 00 00h
Write WFOFST (Offset 07H) 00h ; WFOFST = **00 06** 00 00h
Write WFOFST (Offset 07H) 00h ; WFOFST = **00 00 06** 00h
Write WFOFST (Offset 07H) 00h ; WFOFST = **00 00 00 06**h (Offset = 6*2 = 12)
// Set {Last Byte 3 2 1 0} = 00 00 00 08h
Write WFLB (Page3, Offset 08H) 08h ; {Last Byte 3 2 1 0} = **08** 00 00 00h
Write WFLB (Page3, Offset 08H) 00h ; {Last Byte 3 2 1 0} = **00 08** 00 00h
Write WFLB (Page3, Offset 08H) 00h ; {Last Byte 3 2 1 0} = **00 00 08** 00h
Write WFLB (Page3, Offset 08H) 00h ; {Last Byte 3 2 1 0} = **00 00 00 08**h
// Set {Cascade, Command 3 2 1 0} = 00 00 00 03h
Write WFCMD (Offset 09H) 03h ; WFCMD = **03** 00 00 00h
Write WFCMD (Offset 09H) 00h ; WFCMD = **00 03** 00 00h
Write WFCMD (Offset 09H) 00h ; WFCMD = **00 00 03** 00h
Write WFCMD (Offset 09H) 00h ; WFCMD = **00 00 00 03**h (enabled wake-up frame filter 0, and DA match is required)
// Set PME and IRQ pin I/O Buffer Type (Please Ref. Datasheet Offset 15 descriptions)
Write BTCR (Offset 15H) ;
// Host enables wakeup frame detection then enter D1 sleep
Write WUCSR (Page3, Offset 0AH) 02h ; (Wakeup frame enable)
Write PMR (Offset 0BH) 01h ; (Enter D1 Sleep mode)

4.3.2 Magic Packet frame

AX88796B checks frame for 16 repetitions of the MAC address without any breaks or interruptions. The 16 repetitions may be anywhere in the frame but must be preceded by the synchronization stream 48'hFF_FF_FF_FF_FF_FF pattern. If the MAC address of a node is 00h 11h 22h 33h 44h 55h, then AX88796B scans for the following data sequence in an Ethernet frame.

```
Destination Address (6 byte) Source Address (6 byte) . . . . . . . . . FF FF FF FF FF FF
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
. . . . . CRC (4 byte)
```

4.4 Flow Control

The AX88796B supports Full-duplex flow control using the pause control frame. It also supports half-duplex flow control using collision base of back-pressure method.

4.4.1 Full-Duplex Flow Control

The format of a PAUSE frame is illustrated below. It conforms to the standard Ethernet frame format but includes a unique type field and other parameters as follows:
The destination address of the frame may be set to either the unique DA of the station to be paused, or to the globally assigned multicast address 01-80-C2-00-00-01 (hex). The IEEE 802.3 standard for use in MAC control PAUSE frames has reserved this multicast address. The "Type" field of the PAUSE frame is set to 88-08 (hex) to indicate the frame is a MAC Control frame.
The MAC Control opcode field is set to 00-01 (hex) to indicate the type of MAC Control frame being used is a PAUSE frame. The PAUSE frame is the only type of MAC Control frame currently defined.
The MAC Control Parameters field contains a 16-bit value that specifies the duration of the PAUSE event in units of 512-bit times. Valid values are 00-00 to FF-FF (hex). If an additional PAUSE frame arrives before the current PAUSE time has expired, its parameter replaces the current PAUSE time, so a PAUSE frame with parameter zero allows traffic to resume immediately.
A 42-byte reserved field (transmitted as all zeros) is required to pad the length of the PAUSE frame to the minimum Ethernet frame size.

Preamble (7-bytes)	Start Frame Delimiter (1-byte)	Dest. MAC Address (6-bytes) **= (01-80-C2-00-00-01)**	Source MAC Address (6-bytes)	Length/Type (2-bytes) **= 802.3 MAC Control (88-08)**	**MAC Control Opcode (2-bytes) = PAUSE (00-01)**	**MAC Control Parameters (2-bytes) = (00-00 to FF-FF)**	**Reserved (42-bytes) = all zeros**	Frame Check Sequence (4-bytes)

AX88796B will inhibit transmit frames for a specified period of time if a PAUSE frame received and CRC is correct. If a PAUSE request is received while a transmit frame is in progress, then the pause will take effect after the transmitting is completed.

AX88796B base on “Rx Page Start Register” (CR page0 Offset 01h) and “Rx Page Stop Register”(CR page0 Offset 02h) to calculate and got the total of free page count can be used for store received packets. (One page equal to 256 bytes) The total of free page count will decrease when packets received. A programmable of high water free-page-count in “Flow Control Register” (Offset 1Ah) used to measure the water level of receive buffer. AX88796B use XOFF / XON flow-control method to avoid missing packet if receive buffer almost full. A XON transmitting when the total of free page count equal to or less then “high water free-page-count”. A XOFF transmitting when the total of free page count equal to or greater then (“high water free-page-count” + 6 pages).

Fig - 6 TX / RX Flow control

4.4.2 Half-Duplex Flow Control

Whenever the receive buffer becomes full crosses a certain threshold level, The MAC starts sending a Jam signal, which will result in a collision. After sensing the collision, the remote station will back off its transmit ion. AX88796B only generate this collision-based of back-pressure when it receives a new frame, in order to avoid any late collisions.

A programmable of “Back-pressure Jam Limit count” (Offset 17h) is used for avoid HUB port partition due to many continues of collisions. AX88796B will reset the “Back-pressure Jam Limit count” when either a transmitted or received frame without collision. A back-pressure leakage allow when senses continue of collisions count up to “Back-pressure Jam Limit count”, it will be no jamming one of receive frame even receive buffer is full.

4.5 Big- and Little-endian Support

AX88796B supports “Big-“ or “Little-endian” processor. To support big-endian processors, the hardware designer must explicitly invert the layout of the byte lanes. In addition, for a 16-bit interface, the big-endian register must be set correctly following the table below.

Additionally, please refer to Big-endian register (offset 1Eh), for additional information on status indication on big- or little-endian modes.

MODE OFOPERATION	AX88796B DATA PINS		DESCRIPTION
	SD[15:8]	SD[7:0]	
Mode 0 Big-endian register (offset 1Eh) not equal to 0x0000h			
Even access	Byte3	Byte2	This mode can be used by 32-bit processors operating with an external 16-bit bus.
Odd access	Byte1	Byte0	
Mode 0 Little-endian register (offset 1Eh) equal to 0x0000h (default)			
Even access	Byte1	Byte0	This mode can also be used by native 16-bit processors.
Odd access	Byte3	Byte2	

Tab - 11 Byte Lane Mapping

AX88796B’s 16-bit Data Port (DP) read/write like a FIFO not rely on address pin. The “Even access” means the first of access Data Port (DP) behind of remote read/write Command Register (CR). The second time access Data Port (DP) is “Odd access” and then next is “Even access”, and so on.

Host can read bit-7 in “Device Status Register” (Offset 17h) to know the current of big- or little-endian types. The default is Little-endian mode.

4.6 General Purpose Timer (GP Timer)

The programmable General Purpose Timer can be used to generate periodic host interrupts and the resolution of this timer is 100us.

The GP timer is a 16-bit of register. GPT1 (CR page3 offset 0Fh) and GPT0 (CR page3 offset 0Eh) to compost this 16-bit of General Purpose Timer. This GP timer field of default value is FFFFh. Once set the General Purpose Timer Enable (CR page3 Offset 0Dh) the GPT counts down until it reaches 0000h then update the a new pre-load value into GPT, and continues counting.

The GPT interrupt has no status indicate in Interrupt Status Register (CR page0 offset 07h). The interrupt event will keep active until host driver read Interrupt Status Register (CR page0 offset 07h) then clear GPT interrupt event.

4.7 EEPROM Interface

AX88796B can optionally load its MAC address from an external serial EEPROM. If a properly configured EEPROM is detected by AX88796B at power-up, hard reset or host set a reload EEPROM request (CR page3 offset 0Ch), the constants of EEPROM data will be auto loading to internal memory from 0000h to 001Fh and from 0400h to 040Fh automatically. It is similar NE2000 PROM store MAC address field. A detailed explanation of the EEPROM data format in section 3.1 “EEPROM Memory Mapping”. After auto load EEPROM completed not indicate AX88796B knew its MAC address. Host driver can get MAC address from internal memory (0000h ~ 001Fh) or (0400h ~ 040Fh) and write “Physical Address Registers” (CR page1 offset 01h ~ 06h).

The AX88796B EEPROM use 3 PIN to connect to a most “93C46” type EEPROM configured for x16-bit operation. A connect diagram as below

Fig - 7 EEPROM connections

After EEPROM loader has finished reading the MAC after power-on, hard reset or host set a reload EEPROM request (CR page3 offset 0Ch), the Host is free to perform EECS, EECK and EEDIO as General Purpose I/O pin.

4.8 Power management

AX88796B supports power-down modes to allow applications to minimize power consumption. There is one normal operation power state, D0 and there are two power saving states: D1, and D2. The “Power Management Register”(CR Page3 Offset 0Bh) controls those of power management modes. In D1 power saving state, AX88796B supports Wake on LAN function. In D2 power saving state, AX88796B will off all function block and clocks to minimize power consumption. After wakeup event, the “Power Management Register” will be cleared and state at normal operation power state. When AX88796B in either D1 or D2 power saving mode, host can write “Host Wake Up Register” (Offset 1Fh) return the AX88796B to the D0 state. Power is reduced to various modules by disabling the clocks as outlined in table as below.

AX88796B BLOCK	D0 (Normal operation)	D1 (WOL)	D2
Internal clock	On	On	Off
MAC and Host	On	Off	Off
MAC power management	On	Rx Block On	Off
PHY	On	On	Off

Tab - 12 Power Management Statuses

4.8.1 Power Management Event Indicators

The external PME signal can be setup as Push-Pull driver or open-drain buffer. And also can be set as active high or active low. When set the PME_IND bit to a '1', (offset 15h) the external PME signal will be driven active for 60ms upon detection of a wake-up event. When the PME_IND bit is cleared, the PME signal will be driven continuously upon detection of a wake-up event. Host can checks which kind of wake-up event activity by reads "Wake up Control and Status Register"(CR page3 offset 0Ah). Host can writing "Power Management Register"(CR page3 offset 0Bh) or writing a '1' to clear wake-up event activity flags on "Wake up Control and Status Register"(CR page3 offset 0Ah) to deactivated PME signal.

Fig - 8 PME and IRQ signal generation

4.9 Device Ready or Busy

There are three kinds of device ready indicator in "Device Status Register" (Offset 17h). Those are indicates AX88796B internal operation busy. In order to prevent the host access AX88796B in the busy stage, host can to check the "Device Status Register" before doing some key operations.

When a "0" at the bit-4 (D-RDY) in "Device Status Register" (Offset 17h), indicate the AX88796B in reset state or power saving state or EEPROM loading state or loop-back mode swapping.

When a "0" at the bit-5 (RD-RDY) in "Device Status Register" (Offset 17h), indicate the remote-DMA-read data not ready yet, host must not read data port (DP) in this period. The non-ready period only happen when host set a remote-read command on "Command Register"(CR), and it will be go to ready state when a valid data pop out for host to reading. Host driver can back-to-back read data port (DP) since checked the RD-RDY was ready. The maximum of remote-read non-ready period only spend 60ns. Host can ignore to check RD_RDY if host access time not faster then it.

When a "0" at the bit-6 (RDMA-RDY) in "Device Status Register" (Offset 17h), indicate the remote DMA not completed yet. This RDMA-RDY will be cleared when host write "Remote Byte Count 0" RBCR0 (CR page0 Offset 0Ah) or "Remote Byte Count 1" RBCR1 (CR page0 Offset 0Bh). The byte counter will down counting when every data port (DP) access. This RDMA-RDY will be set when byte counter count to zero.

5.0 Registers Operation

5.1 MAC Control and Status Registers (CSR)

All registers of MAC Core are 8-bit wide except data port (DP). Data Port is optional 8 or 16-bit wide by WTS (DCR). Offset 01h to 0Fh mapped into pages, which are selected by PS (Page Select) in the Command Register.

Offset	Page0	Page1	Page2	Page3
00H	Command Register (CR)			
01H	Page0 of registers	Page1 of registers	Page2 of registers	Page3 of registers
02H				
03H				
04H				
05H				
06H				
07H				
08H				
09H				
0AH				
0BH				
0CH				
0DH				
0EH				
0FH				
10H, 11H	Data Port (DP)			
12H	Inter-frame Gap Segment 1 (IFGS1)			
13H	Inter-frame Gap Segment 2 (IFGS2)			
14H	MII/EEPROM Access			
15H	Buffer Type Configure Register (BTCR)			
16H	Inter-frame Gap (IFG)			
17H	Device Status Register (DSR) / Back-pressure Jam Limit Count (BJLC)			
18H	Max Frame Size [7:0]			
19H	Max Frame Size [11:8]			
1AH	Flow Control Register (FCR)			
1BH	MAC Configure Register (MCR)			
1CH	Current TX End Page Register (CTEPR) / VLAN_ID_0			
1DH	Reserved / VLAN_ID_1			
1EH	Reserved / Big-Endian Register (BER)			
1FH	Software Reset / Host Wake up (HWAKE)			

PAGE 0 (PS1=0,PS0=0)

Offset	Read	Write
00H	Command Register (CR)	Command Register (CR)
01H	Rx Page Start Register (PSTART)	Page Start Register (PSTART)
02H	Rx Page Stop Register (PSTOP)	Page Stop Register (PSTOP)
03H	Boundary Pointer (BNRY)	Boundary Pointer (BNRY)
04H	Transmit Status Register (TSR)	Transmit Page Start Address (TPSR)
05H	Number of Collisions Register (NCR)	Transmit Byte Count Register 0 (TBCR0)
06H	Current Page Register (CPR)	Transmit Byte Count Register 1 (TBCR1)
07H	Interrupt Status Register (ISR)	Interrupt Status Register (ISR)
08H	Current Remote DMA Address 0 (CRDA0)	Remote Start Address Register 0 (RSAR0)
09H	Current Remote DMA Address 1 (CRDA1)	Remote Start Address Register 1 (RSAR1)
0AH	Reserved	Remote Byte Count 0 (RBCR0)
0BH	Reserved	Remote Byte Count 1 (RBCR1)
0CH	Receive Status Register (RSR)	Receive Configuration Register (RCR)
0DH	Frame Alignment Error Tally Register (CNTR0)	Transmit Configuration Register (TCR)
0EH	CRC Error Tally Register (CNTR1)	Data Configuration Register (DCR)
0FH	Frames Lost Tally Register (CNTR2)	Interrupt Mask Register (IMR)
11H, 10H	Data Port (DP)	Data Port (DP)
12H	Inter-frame Gap Segment 1 (IFGS1)	Inter-frame Gap Segment 1 (IFGS1)
13H	Inter-frame Gap Segment 2 (IFGS2)	Inter-frame Gap Segment 2 (IFGS2)
14H	MII/EEPROM Access	MII/EEPROM Access
15H	Buffer Type Configure Register (BTCR)	Buffer Type Configure Register (BTCR)
16H	Inter-frame Gap (IFG)	Inter-frame Gap (IFG)
17H	Device Status Register (DSR)	Back-pressure Jam Limit count (BJLC)
18H	Max Frame Size [7:0]	Max Frame Size [7:0]
19H	Max Frame Size [11:8]	Max Frame Size [11:8]
1AH	Flow Control Register (FCR)	Flow Control Register (FCR)
1BH	MAC Configure Register (MCR)	MAC Configure Register (MCR)
1CH	Current TX End Page Register (CTEPR)	VLAN_ID_0
1DH	Reserved	VLAN_ID_1
1EH	Reserved	Big-Endian Register (BER)
1FH	Software Reset	Host Wake up (HWAKE)

Tab - 13 Page 0 of MAC Core Registers Mapping

PAGE 1 (PS1=0,PS0=1)

Offset	Read	Write
01H	Physical Address Register 0 (PAR0)	Physical Address Register 0 (PAR0)
02H	Physical Address Register 1 (PAR1)	Physical Address Register 1 (PAR1)
03H	Physical Address Register 2 (PAR2)	Physical Address Register 2 (PAR2)
04H	Physical Address Register 3 (PAR3)	Physical Address Register 3 (PAR3)
05H	Physical Address Register 4 (PAR4)	Physical Address Register 4 (PAR4)
06H	Physical Address Register 5 (PAR5)	Physical Address Register 5 (PAR5)
07H	Current Page Register (CPR)	Current Page Register (CPR)
08H	Multicast Address Register 0 (MAR0)	Multicast Address Register 0 (MAR0)
09H	Multicast Address Register 1 (MAR1)	Multicast Address Register 1 (MAR1)
0AH	Multicast Address Register 2 (MAR2)	Multicast Address Register 2 (MAR2)
0BH	Multicast Address Register 3 (MAR3)	Multicast Address Register 3 (MAR3)
0CH	Multicast Address Register 4 (MAR4)	Multicast Address Register 4 (MAR4)
0DH	Multicast Address Register 5 (MAR5)	Multicast Address Register 5 (MAR5)
0EH	Multicast Address Register 6 (MAR6)	Multicast Address Register 6 (MAR6)
0FH	Multicast Address Register 7 (MAR7)	Multicast Address Register 7 (MAR7)

Tab - 14 Page 1 of MAC Core Registers Mapping

PAGE 2 (PS1=1,PS0=0)

Offset	Read	Write
01H	Reserved	Reserved
02H	Reserved	Reserved
03H	Reserved	Reserved
04H	Reserved	Reserved
05H	Reserved	Reserved
06H	Reserved	Reserved
07H	Reserved	Reserved
08H	Reserved	Reserved
09H	Reserved	Reserved
0AH	Total Receive Buffer Free Page (TFP)	Reserved
0BH	Chip version (00h)	Reserved
0CH	Receive Configuration Register (RCR)	Reserved
0DH	Transmit Configuration Register (TCR)	Reserved
0EH	Data Configuration Register (DCR)	Reserved
0FH	Interrupt Mask Register (IMR)	Reserved

Tab - 15 Page 2 of MAC Core Registers Mapping

PAGE 3 (PS1=1,PS0=1)

Offset	Read	Write
01H	WFBM0	WFBM0
02H	WFBM1	WFBM1
03H	WFBM2	WFBM2
04H	WFBM3	WFBM3
05H	WF10CRC	WF10CRC
06H	WF32CRC	WF32CRC
07H	WFOFST	WFOFST
08H	WFLB	WFLB
09H	WFCMD	WFCMD
0AH	WUCSR	WUCSR
0BH	PMR	PMR
0CH	Reserved	REER
0DH	MISC	MISC
0EH	GPT0	GPT0
0FH	GPT1	GPT1

Tab - 16 Page 3 of MAC Core Registers Mapping

5.1.1 Command Register (CR)

Offset 00H (Read/Write)

Field	Name	Description (Default = 21h)
7:6	PS1, PS0	PS1, PS0: Page Select The two bits select which register's page is to be accessed. It will be reset to default value when set PMR to D1 to D2 sleep state. PS1 PS0 0 0 page 0 (default) 0 1 page 1 1 0 page 2 1 1 page 3
5:3	RD2, RD1, RD0	RD2, RD1, RD0: Remote DMA Command These three encoded bits control operation of the Remote DMA channel. RD2 could be set to abort any Remote DMA command in process. RD2 is reset by AX88796B when a Remote DMA has been completed. The Remote Byte Count should be cleared when a Remote DMA has been aborted. The Remote Start Address is not restored to the starting address if the Remote DMA is aborted. It will be reset to default value when set PMR to D1 to D2 sleep state. RD2 RD1 RD0 0 0 0 Not allowed 0 0 1 Remote Read 0 1 0 Remote Write 0 1 1 Not allowed 1 X X Abort / Complete Remote DMA (default)
2	TXP	TXP: Transmit Packet This bit could be set to initiate transmission of a packet
1	START	START: This bit is used to active AX88796B operation. This bit always read high when Host set once. It only clear by hardware or software reset.
0	STOP	STOP: Stop AX88796B This bit is used to stop the AX88796B operation. It will be reset to default value when set PMR to D1 to D2 sleep state.

5.1.2 Rx Page Start Register (PSTART)

Page0 Offset 01H (Read/Write)

Field	Name	Description (Default = 00h)
7:0	PSTART	Receive Buffer Ring Page Start Register

5.1.3 Rx Page Stop Register (PSTOP)

Page0 Offset 02H (Read/Write)

Field	Name	Description (Default = 00h)
7:0	PSTOP	Receive Buffer Ring Page Stop Register

5.1.4 Boundary Pointer (BNRY)

Page0 Offset 03H (Read/Write)

Field	Name	Description (Default = 4Ch)
7:0	BNRY	Boundary Page Pointer

5.1.5 Transmit Page Start Address (TPSR)

Page0 Offset 04H (Write)

Field	Name	Description
7:0	TPSR	Transmit Page Start Address

5.1.6 Transmit Status Register (TSR)

Page0 Offset 04H (Read)

Field	Name	Description (Default = 00h)
7	OWC	Out of window collision
6:4	-	Reserved
3	ABT	Transmit Aborted Indicates the AX88796 aborted transmission because of excessive collision.
2	COL	Transmit Collided Indicates that the transmission collided at least once with another station on the network.
1	-	Reserved
0	PTX	Packet Transmitted Indicates transmission without error.

5.1.7 Transmit Byte Count Register (TBCR0)

Page0 Offset 05H (Write)

Field	Name	Description
7:0	TBCR0	Transmit Byte Count Register. The bit assignment is shown below

	7	6	5	4	3	2	1	0
TBCR1	L15	L14	L13	L12	L11	L10	L9	L8
	7	6	5	4	3	2	1	0
TBCR0	L7	L6	L5	L4	L3	L2	L1	L0

5.1.8 Number Of Collisions Register (NCR)

Page0 Offset 05H (Read)

Field	Name	Description (Default = 00h)
7:4	-	Always zero
3:0	NCR	If no collisions are experienced during a transmission attempt, the COL bit of the TSR will not be set and the contents of NCR will be zero. If there are excessive collisions, the ABT bit in the TSR will be set and the contents of NCR will be zero. The NCR is cleared after the TXP bit in the CR is set.

5.1.9 Transmit Byte Count Register (TBCR1)

Page0 Offset 06H (Write)

Field	Name	Description
7:0	TBCR1	Transmit Byte Count Register.

5.1.10 Current Page Register (CPR)

Page0 Offset 06H (Read)

Field	Name	Description (Default = 4Dh)
7:0	CPR	The Buffer Management Logic as a backup register for reception uses this register internally. CURR contains the address of the first buffer to be used for a packet reception and is used to restore DMA pointers in the event of receive errors. This register is initialized to the same value as PSTART and should not be written to again unless the controller is Reset. 7 6 5 4 3 2 1 0 CURR A15 A14 A13 A12 A11 A10 A9 A8

5.1.11 Interrupt Status Register (ISR)

Page0 Offset 07H (Read/Write)

Field	Name	Description (Default = 80h)
7	RST	Reset Status: Set when AX88796B enters reset state (or a wake-up event) and cleared when a start command is issued to the CR. Writing to this bit is no effect.
6	RDC	Remote DMA Complete Set when remote DMA operation has been completed. Write this bit to high then reset it.
5	CNT	Counter Overflow Set when MSB of one or more of the Tally Counters has been set. Write this bit to high then reset its.
4	OVW	OVERWRITE: Set when receive buffer ring storage resources have been exhausted. Write this bit to high then reset it.
3	TXE	Transmit Error Set when packet transmitted with one or more of the following errors Excessive collisions, Transmit over size and late collision. Write this bit to high then reset it.
2	RXE	Receive Error Indicates that a packet was received with one or more of the following errors CRC error Frame Alignment Error Missed Packet Write this bit to high then reset it.
1	PTX	Packet Transmitted Indicates packet transmitted with no error Write this bit to high then reset it.
0	PRX	Packet Received Indicates packet received with no error. Write this bit to high then reset it.

Remote DMA operations are programmed via the Remote Start Address (RSAR0, 1) and Remote Byte Count (RBCR0, 1) registers.

5.1.12 Remote Start Address Register (RSAR0)

Page0 Offset 08H (Write)

Field	Name	Description
7:0	RSAR0	The Remote Start Address is used to point to the start of the block of data to be transferred. 7 6 5 4 3 2 1 0 RSAR1 A15 A14 A13 A12 A11 A10 A9 A8 7 6 5 4 3 2 1 0 RSAR0 A7 A6 A5 A4 A3 A2 A1 A0

5.1.13 Remote Start Address Register (RSAR1)

Page0 Offset 09H (Write)

Field	Name	Description
7:0	RSAR1	The Remote Start Address is used to point to the start of the block of data to be transferred.

5.1.14 Remote Byte Count Register (RBCR0)

Page0 Offset 0AH (Write)

Field	Name	Description
7:0	RBCR0	The Remote Byte Count is used to indicate the length of the block (in bytes). 7 6 5 4 3 2 1 0 RBCR1 BC15 BC14 BC13 BC12 BC11 BC10 BC9 BC8 7 6 5 4 3 2 1 0 RBCR0 BC7 BC6 BC5 BC4 BC3 BC2 BC1 BC0

5.1.15 Remote Byte Count Register (RBCR1)

Page0 Offset 0BH (Write)

Field	Name	Description
7:0	RBCR1	The Remote Byte Count is used to indicate the length of the block (in bytes).

5.1.16 Current Remote DMA Address (CRDA0)

Page0 Offset 08H (Read)

Field	Name	Description (Default = 00h)
7:0	CRDA0	The Current Remote DMA Registers contain the current address of the Remote DMA. The bit assignment is shown below: 7 6 5 4 3 2 1 0 CRDA1 A15 A14 A13 A12 A11 A10 A9 A8 7 6 5 4 3 2 1 0 CRDA0 A7 A6 A5 A4 A3 A2 A1 A0

5.1.17 Current Remote DMA Address (CRDA1)

Page0 Offset 09H (Read)

Field	Name	Description (Default = 00h)
7:0	CRDA1	The Current Remote DMA Registers contain the current address of the Remote DMA. The bit assignment is shown below: 7 6 5 4 3 2 1 0 CRDA1 A15 A14 A13 A12 A11 A10 A9 A8 7 6 5 4 3 2 1 0 CRDA0 A7 A6 A5 A4 A3 A2 A1 A0

5.1.18 Receive Configuration Register (RCR)

Page0 Offset 0CH (Write)

Field	Name	Description
7	-	Reserved
6	-	Reserved
5	MON	Monitor Mode 0: Normal Operation. (Default) 1: Monitor Mode, the input packet will be checked on NODE ADDRESS and CRC but not buffered into memory.
4	PRO	PRO: Promiscuous Mode Enable the receiver to accept all packets with a physical address.
3	AM	AM: Accept Multicast Enable the receiver to accept packets with a multicast address. That multicast address must pass the hashing array.
2	AB	AB: Accept Broadcast Enable the receiver to accept broadcast packet.
1	AR	AR: Accept Runt Enable the receiver to accept runt packet.
0	SEP	SEP: Save Error Packet Enable the receiver to accept and save packets with error.

5.1.19 Receive Status Register (RSR)

Page0 Offset 0CH (Read)

Field	Name	Description (Default = 00h)
7	-	Reserved
6	DIS	Receiver Disabled
5	PHY	Multicast Address Received.
4	MPA	Missed Packet
3	-	Always Zero
2	FAE	Frame alignment error.
1	CR	CRC error.
0	PRX	Packet Received Intact

5.1.20 Transmit Configuration Register (TCR)

Page0 Offset 0DH (Write)

Field	Name	Description
7	FDU	Full Duplex This bit configure MAC media mode is Full Duplex or not. 0: Half duplex (Default) 1: Full duplex This duplex setting was wire or with MCR bit-7. Each one goes high then configures MAC as full-duplex. AX88796B will ignore this bit and MCR bit-7 when using internal PHY.
6	PD	Pad Disable 0: Pad will be added when packet length less than 60. (Default) 1: Pad will not be added when packet length less than 60.
5	RLO	Retry of late collision 0: Don't retransmit packet when late collision happens. (Default) 1: Retransmit packet when late collision happens.
4:3	-	Reserved
2:1	LB1, LB0	Encoded Loop-back Control These encoded configuration bits set the type of loop-back that is to be performed. LB1 LB0 Mode0 0 0 Normal operation (Default) Mode 1 0 1 Internal AX88796B loop-back Mode 2 1 0 PHY loop-back No Define 1 1 Reserved
0	CRC	Inhibit CRC 0: CRC appended by transmitter. (Default) 1: CRC inhibited by transmitter.

5.1.21 Frame Alignment Error Tally Register (CNTR0)

Page0 Offset 0DH (Read)

Field	Name	**Description** (Default = 00h)
7:0	CNTR0	This counter is incremented every time a packet is received with a Frame Alignment Error. The packet must have been recognized by the address recognition logic. The counter is cleared after the processor reads it.

5.1.22 Data Configuration Register (DCR)

Page0 Offset 0EH (Write)

Field	Name	Description
7:2	-	Reserved
1	-	Reserved
0	WTS	Word Transfer Select (Data Port Only) 0: Selects Data Port with byte-wide transfers. (Default) 1: Selects Data Port with word-wide transfers.

5.1.23 CRC Error Tally Register (CNTR1)

Page0 Offset 0EH (Read)

Field	Name	**Description** (Default = 00h)
7:0	CNTR1	This counter is incremented every time a packet is received with a CRC error. The packet must first be recognized by the address recognition logic. The counter is cleared after the processor reads it.

5.1.24 Interrupt mask register (IMR)

Page0 Offset 0FH (Write)

Field	Name	Description
7		Reserved
6	RDCE	DMA Complete Interrupt Enable. Default “low” disabled.
5	CNTE	Counter Overflow Interrupt Enable. Default “low” disabled.
4	OVWE	Overwrite Interrupt Enable. Default “low” disabled.
3	TXEE	Transmit Error Interrupt Enable. Default “low” disabled.
2	RXEE	Receive Error Interrupt Enable. Default “low” disabled.
1	PTXE	Packet Transmitted Interrupt Enable. Default “low” disabled.
0	PRXE	Packet Received Interrupt Enable. Default “low” disabled.

5.1.25 Frames Lost Tally Register (CNTR2)

Page0 Offset 0FH (Read)

Field	Name	Description (Default = 00h)
7:0	CNTR2	This counter is incremented if a packet cannot be received due to lack of buffer resources. In monitor mode, this counter will count the number of packets that pass the address recognition logic.

5.1.26 Physical Address Register 0 (PAR0)

Page1 Offset 01H (Read/Write)

Field	Name	Description (Default = 00h)
7:0	PAR0	Physical Address Register 0

5.1.27 Physical Address Register 1 (PAR1)

Page1 Offset 02H (Read/Write)

Field	Name	Description (Default = 00h)
7:0	PAR1	Physical Address Register 1

5.1.28 Physical Address Register 2 (PAR2)

Page1 Offset 03H (Read/Write)

Field	Name	Description (Default = 00h)
7:0	PAR2	Physical Address Register 2

5.1.29 Physical Address Register 3 (PAR3)

Page1 Offset 04H (Read/Write)

Field	Name	Description (Default = 00h)
7:0	PAR3	Physical Address Register 3

5.1.30 Physical Address Register 4 (PAR4)

Page1 Offset 05H (Read/Write)

Field	Name	Description (Default = 00h)
7:0	PAR4	Physical Address Register 4

5.1.31 Physical Address Register 5 (PAR5)

Page1 Offset 06H (Read/Write)

Field	Name	Description (Default = 00h)
7:0	PAR5	Physical Address Register 5

The physical address registers are used to compare the destination address of incoming packets for rejecting or accepting packets. Comparisons are performed on a byte wide basis. The bit assignment shown below relates the sequence in PAR0 ~ PAR5 to the bit sequence of the received packet.

	D7	D6	D5	D4	D3	D2	D1	D0
PAR0	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
PAR1	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
PAR2	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16
PAR3	DA31	DA30	DA29	DA28	DA27	DA26	DA25	DA24
PAR4	DA39	DA38	DA37	DA36	DA35	DA34	DA33	DA32
PAR5	DA47	DA46	DA45	DA44	DA43	DA42	DA41	DA40

Destination Address Source

P/S	DA0	DA1	DA2	DA3	.....	DA46	DA47	SA0	...

Note:
P/S = Preamble, Synch
DA0 = Physical/Multicast Bit

5.1.32 Current Page Register (CPR)

Page1 Offset 07H (Read/Write)

Field	Name	Description (Default = 4Dh)
7:0	CPR	The Buffer Management Logic as a backup register for reception uses this register internally. CURR contains the address of the first buffer to be used for a packet reception and is used to restore DMA pointers in the event of receive errors. This register is initialized to the same value as PSTART and should not be written to again unless the controller is Reset. 7 6 5 4 3 2 1 0 CURR A15 A14 A13 A12 A11 A10 A9 A8

5.1.33 Multicast Address Register 0 (MAR0)

Page1 Offset 08H (Read/Write)

Field	Name	Description (Default = 00h)
7:0	MAR0	Multicast Address Register 0

5.1.34 Multicast Address Register 1 (MAR1)

Page1 Offset 09H (Read/Write)

Field	Name	Description (Default = 00h)
7:0	MAR1	Multicast Address Register 1

5.1.35 Multicast Address Register 2 (MAR2)

Page1 Offset 0AH (Read/Write)

Field	Name	Description (Default = 00h)
7:0	MAR2	Multicast Address Register 2

5.1.36 Multicast Address Register 3 (MAR3)

Page1 Offset 0BH (Read/Write)

Field	Name	Description (Default = 00h)
7:0	MAR3	Multicast Address Register 3

5.1.37 Multicast Address Register 4 (MAR4)

Page1 Offset 0CH (Read/Write)

Field	Name	Description (Default = 00h)
7:0	MAR4	Multicast Address Register 4

5.1.38 Multicast Address Register 5 (MAR5)

Page1 Offset 0DH (Read/Write)

Field	Name	Description (Default = 00h)
7:0	MAR5	Multicast Address Register 5

5.1.39 Multicast Address Register 6 (MAR6)

Page1 Offset 0EH (Read/Write)

Field	Name	Description (Default = 00h)
7:0	MAR6	Multicast Address Register 6

5.1.40 Multicast Address Register 7 (MAR7)

Page1 Offset 0FH (Read/Write)

Field	Name	Description (Default = 00h)
7:0	MAR7	Multicast Address Register 7

5.1.41 Total Receive Buffer Free Page Register (TFP)

Page2 Offset 0AH (Read)

Field	Name	Description (Default = 7Fh)
7:0	TFP	Indicate total free page in receive buffer ring. A default value 7Fh after hardware / software reset. It will be update the real free page when every frame received.

5.1.42 Receive Configuration Register (RCR)

Page2 Offset 0CH (Read)

Field	Name	Description (Default = 00h)
7:0	RCR	Reference Page0 Offset 0CH for bits deifications.

5.1.43 Transmit Configuration Register (TCR)

Page2 Offset 0DH (Read)

Field	Name	Description (Default = 00h)
7:0	TCR	Reference Page0 Offset 0DH for bits deifications.

5.1.44 Data Configuration Register (DCR)

Page2 Offset 0EH (Read)

Field	Name	Description (Default = 00h)
7:0	DCR	Reference Page0 Offset 0EH for bits deifications.

5.1.45 Interrupt Mask Register (IMR)

Page2 Offset 0FH (Read)

Field	Name	Description (Default = 00h)
7:0	IMR	Reference Page0 Offset 0FH for bits deifications.

5.1.46 Wakeup Frame Byte Mask (WFBM0)

Page3 Offset 01H (Read/Write)

Field	Name	Description (Default = 00h)
31:0	WFBM0	Byte mask for wake-up frame filter 0. Host continue write 4 times to completed 32-bits of Byte Mask 0.

5.1.47 Wakeup Frame Byte Mask (WFBM1)

Page3 Offset 02H (Read/Write)

Field	Name	Description (Default = 00h)
31:0	WFBM1	Byte mask for wake-up frame filter 1. Host continue write 4 times to completed 32-bits of Byte Mask 1.

5.1.48 Wakeup Frame Byte Mask (WFBM2)

Page3 Offset 03H (Read/Write)

Field	Name	Description (Default = 00h)
31:0	WFBM2	Byte mask for wake-up frame filter 2. Host continue write 4 times to completed 32-bits of Byte Mask 2.

5.1.49 Wakeup Frame Byte Mask (WFBM3)

Page3 Offset 04H (Read/Write)

Field	Name	Description (Default = 00h)
31:0	WFBM3	Byte mask for wake-up frame filter 3. Host continue write 4 times to completed 32-bits of Byte Mask 3.

5.1.50 Wakeup Frame 1,0 CRC (WF10CRC)

Page3 Offset 05H (Read/Write)

Field	Name	Description (Default = 00h)
7:0	WF0_0CRC	Byte mask CRC for wake-up frame filter 0. Host continue write 4 times to completed 32-bits of Byte Mask 1 CRC and Byte Mask 0 CRC. CRC-16 Polynomials = X^16 + X^15 + X^2 + 1
15:8	WF0_1CRC	Byte mask CRC for wake-up frame filter 0.
23:16	WF1_0CRC	Byte mask CRC for wake-up frame filter 1.
31:24	WF1_1CRC	Byte mask CRC for wake-up frame filter 1.

5.1.51 Wakeup Frame 3,2 CRC (WF32CRC)

Page3 Offset 06H (Read/Write)

Field	Name	Description (Default = 00h)
7:0	WF2_0CRC	Byte mask CRC for wake-up frame filter 2. Host continue write 4 times to completed 32-bits of Byte Mask 3 CRC and Byte Mask 2 CRC. CRC-16 Polynomials = X^16 + X^15 + X^2 + 1
15:8	WF2_1CRC	Byte mask CRC for wake-up frame filter 2.
23:16	WF3_0CRC	Byte mask CRC for wake-up frame filter 3.
31:24	WF3_1CRC	Byte mask CRC for wake-up frame filter 3.

5.1.52 Wakeup Frame Offset (WFOFST)

Page3 Offset 07H (Read/Write)

Field	Name	Description (Default = 00h)
7:0	WF0OFST	Byte mask Offset for wake-up frame filter 0. Host continue write 4 times to completed 32-bits of Byte Mask 3, 2, 1, 0 Offset. The unit is 16-bit. (2bytes)
15:8	WF1OFST	Byte mask Offset for wake-up frame filter 1.
23:16	WF2OFST	Byte mask Offset for wake-up frame filter 2.
31:24	WF3OFST	Byte mask Offset for wake-up frame filter 3.

5.1.53 Wakeup Frame Last Byte (WFLB)

Page3 Offset 08H (Read/Write)

Field	Name	Description (Default = 00h)
7:0	WFLB0	Mask Last Byte for wake-up frame filter 0. Host continue write 4 times to completed 32-bits of Last Byte of 3, 2, 1, 0 filter.
15:8	WFLB1	Mask Last Byte for wake-up frame filter 1.
23:16	WFLB2	Mask Last Byte for wake-up frame filter 2.
31:24	WFLB3	Mask Last Byte for wake-up frame filter 3.

5.1.54 Wakeup Frame Command (WFCMD)

Page3 Offset 09H (Read/Write)

Field	Name	Description (Default = 00h)
3:0	WFCMD0	Byte Mask Command for wake-up frame filter 0. Host continue write 4 times to completed 32-bits of Byte Mask Command of 3, 2, 1, 0 filter and Mask cascade commend. Bit0: wake-up frame filter enable Bit1: destination match enable Bit2: Multicast match enable Bit3: Reserved
7:4	WFCMD1	Byte Mask Command for wake-up frame filter 1.
11:8	WFCMD2	Byte Mask Command for wake-up frame filter 2.
15:12	WFCMD3	Byte Mask Command for wake-up frame filter 3.
19:16	WFCSCD	Byte Mask Cascade Command for wake-up frame filter Bit-0: cascade wake-up filter 1 and 0 Bit-1: cascade wake-up filter 2 and 1 Bit-2: cascade wake-up filter 3 and 2
31:18	-	Reserved. Always zero.

5.1.55 Wakeup Control and Status Register (WUCSR)

Page3 Offset 0AH (Read/Write)

Field	Name	Description (Default = 00h)
7	-	Reserved
6	LSC	Link status change event flag. This bit will be clear when Host write PMR or set this bit.
5	WUFR	Wake-up Frame Received event flag. This bit will be clear when Host write PMR or set this bit.
4	MPR	Magic Packet Received event flag. This bit will be clear when Host write PMR or set this bit.
3	-	Reserved
2	LSCWE	Link status change wakeup enable 0: disable (Default) 1: enable
1	WUEN	Wake-up frame enable 0: disable (Default) 1: enable

0	MPEN	Magic Packet wake-up enables. 0: disable (Default) 1: enable

5.1.56 Power Management Register (PMR)

Page3 Offset 0BH (Read/Write)

Field	Name	Description (Default = 00h)
7:5	-	Reserved
4	REGSTB	0: Regulator in normal mode (Default) 1: Regulator in standby mode
3:2	-	Reserved
1:0	PMM	Power Management Mode, Self clear when wake-up 00: Normal Operation (Default) 01: D1 power saving. Supported Link status change, Wake-up and Magic frame for remote wake-up 10: D2 power saving. Only write host wake-up register (offset 1Fh) to leave D2 state. 11: Reserved. Do not set this mode.

5.1.57 Reload EEPROM Register (REER)

Page3 Offset 0CH (Write)

Field	Name	Description
7:1	-	Reserved
0	REER	Reload EEPROM Host set this bit to active reload EEPROM process. And it will auto clear by it self.

5.1.58 Misc. Control Register (MISC)

Page3 Offset 0DH (Write/Read)

Field	Name	Description (Default = 00h)
7:3	-	Reserved
2	GPTE	General Purpose Timer Enable 0: Disable (Default) 1: Enable
1	BCB1	Burst Cycle Base On SA1 or SA0 0: Base on SA0 (Default) 1: Base on SA1
0	TBR	Transmit Buffer Ring Enable 0: Remote DMA write can write any where of embedded memory. (Default) 1: Remote DMA write transmit buffer as a Ring from page 40h to PSTART –1.

5.1.59 General Purpose Timer0 Register (GPT0)

Page3 Offset 0EH (Write/Read)

Field	Name	Description (Default = FFh)
7:0	-	General Purpose Timer [7:0]

5.1.60 General Purpose Timer1 Register (GPT1)

Page3 Offset 0FH (Write/Read)

Field	Name	Description (Default = FFh)
7:0	-	General Purpose Timer [15:8]

5.1.61 Data Port (DP)

Offset 10H (Read/Write)

Field	Name	Description (Default = 00h)
15:8	DP	Data Port High byte
7:0	DP	Data Port Low byte

5.1.62 Inter-frame gap Segment 1(IFGS1)

Offset 12H (Read/Write)

Field	**Name**	**Description** (Default = 0Ch)
7	-	Reserved
6:0	IFGS1	Inter-frame Gap Segment 1.

5.1.63 Inter-frame gap Segment 2(IFGS2)

Offset 13H (Read/Write)

Field	**Name**	**Description** (Default = 12h)
7	-	Reserved
6:0	IFGS2	Inter-frame Gap Segment 2.

5.1.64 MII/EEPROM Management Register (MEMR)

Offset 14H (Read/Write)

Field	**Name**	**Description** (Default = 00h)
7	EECK	EECK EEPROM Clock. It output to Pin-20
6	EEO	EEO: (Read only) EEPROM Data Out value. It reflects Pin-19 EEDIO value.
5	EEI	EEI EEPROM Data In. It output to Pin-19 EEDIO as EEPROM data input value.
4	EECS	EECS EEPROM Chip Select. It output to Pin-21
3	MDO	MDO MII Data Out. It connects to internal PHY of MDO.
2	MDI	MDI (Read only) MII Data In. It connects to internal PHY of MDI.
1	DIR	Signal Direction: for both of SMI (MDIO) and EEPROM (EEDIO) 0: output direction, MDIO and EEDIO as push-pull drive out 1: input direction, MDIO and EEDIO as Z state for source from external signals
0	MDC	MDC MII Clock. It connect to internal PHY of MDC

5.1.65 I/O Buffer Type Configure Register (BTCR)

Offset 15H (Read/Write)

Field	**Name**	**Description** (Default = 00h)
7	-	Always write zero
6	PME_IQR_EN	PME interrupt enable 0: PME interrupt disable (Default) 1: PME interrupt enable
5	IRQ_TYPE	Interrupt I/O Buffer Type 0: Enable IRQ to function as an open-drain buffer for use in a wired-OR interrupt configuration. And ignored INTP field, the interrupt output is always active low. (Default) 1: IRQ output is a Push-Pull driver
4	IRQ_POL	Interrupt Polarity 0: Low active (Default) 1: High active
3	-	Reserved
2	PME_IND	PME indication 0: A static signal active when detect wake-up event. (Default) 1: A 60ms pulse active when detect wake-up event.
1	PME_TYPE	PME I/O Type. When cleared, PME_POL is ignored, and the output is always active low. 0: PME to function as an open-grain buffer for use in a wired-or configuration. (Default) 1: PME output is a Push-Pull driver.
0	PME_POL	PME Polarity. 0: PME active Low (Default) 1: PME active high (ignore when PME_TYPE is low)

5.1.66 Inter-frame gap (IFG)

Offset 16H (Read/Write)

Field	**Name**	**Description** (Default = 15h)	
7	-	Reserved, Always zero.	
6:0	IFG	Inter-frame Gap for Back-To-Back Transmission without collision	
		IFG	Bit-time of Frame gap
		15h – n	96 – (4*n)
		15h (default)	96
		15h + n	96 + (4*n)

5.1.67 Back-pressure Jam Limit Count (BJLC)

Offset 17H (Write)

Field	**Name**	**Description**
7:6	-	Reserved, Always zero.
5:0	BJLC	Back-pressure Jam Limit count, Default value is 19H.

5.1.68 Device Status Register (DSR)

Offset 17H (Read)

Field	**Name**	**Description**
7	B_ENDIAN	When set indicates big-endian mode. (The Big-endian Register's value not all zero)
6	RDMA_RDY	Remote DMA completed. It is same as ISR bit 6. When set, it indicates the remote DMA process was completed.
5	RD_RDY	Read Data Port Ready, When set, indicates data was ready from SRAM to data port for host reading.
4	D_RDY	Device Ready. When set, this bit indicates that AX88796B is ready to be accessed. This register can be read when AX88796B in any power management mode. When cleared, indicate AX88796B in reset, power saving or load EEPROM state.
3	-	Always zero
2	I_SPEED	PHY Link Speed: 0: indicate the link speed is 10Mb/s 1: indicate the link speed is 100Mb/s
1	I_DUPLEX	PHY Duplex mode: 0: half-duplex 1: full-duplex
0	I_LINK	Link Status: 0: Link off 1: Link up

5.1.69 MAX Frame Size Register (MFSR0)

Offset 18H (Read/Write)

Field	**Name**	**Description** (Default = 00h)
7:0	MFSR0	MAX Frame size [7:0], default {MFSR1, MFSR0} = 1536 bytes

5.1.70 MAX Frame Size Register (MFSR1)

Offset 19H (Read/Write)

Field	**Name**	**Description** (Default = 06h)
7:3	-	Reserved
2:0	MFSR1	MAX Frame size [10:8]

5.1.71 Flow Control Register (FCR)

Offset 1AH (Read/Write)

Field	**Name**	**Description** (Default = 07h)
7	FLWC	Flow-control 0: Flow-control disable (Default) 1: Flow-control enable
6	BPEN	Back Pressure in half-duplex flow-control (AX88796B will ignore this bit when running at full-duplex mode) 0: Back Pressure disable (Default) 1: Back Pressure enable
5:0	HWPC	High Water free Page Count. Default value is 7 (7 * 256 = 1792 bytes).

5.1.72 MAC Configure Register (MCR)

Offset 1BH (Read/Write)

Field	**Name**	**Description**
7	DUPX	MAC duplex mode setting When read, this bit is indicates the real duplex setting in MAC operation. 0: half-duplex 1: full-duplex When write, this duplex setting was wire or with TCR bit-7. Each one goes high then configures MAC as full-duplex mode. AX88796B will ignore this bit and TCR bit-7 when using internal PHY.
6	BPLE	Back-pressure leakage enable when continuous of collision N times. N number is reference register 17H of Back-pressure Jam Limit count. 0: Allow flow-control leakage to avoid HUB port going partition state due to too many of collision (Default) 1: No flow-control leakage
5	BBTC	Back-To-Back Transmission Control: 0: Disable (Default) 1: Enable Back-To-Back Transmission, Host can continue set TXP without check transmit completed Host can ignore Number of Collisions Register (NCR)
4	MPSEL	Media Select by Program 0: internal PHY is selected (Default) 1: external MII PHY is selected.
3	VLANE	VLAN enable 0: No supported VLAN frame tagged (Default) 1: Only accept Tag frames. AX88796 will reject packet if Tag x8100 and VID not match whit setting by host. Null VID (VID = 0) is acceptable.
2	CPTEFF	Capture effect. 0: always write low (Default) 1: for MAC test only. Force first collision of back off is 2 slot-time and second collision of back off is 0 slot time. Others as normal.
1	SPMAC	Super MAC. 0: always write low (Default) 1: for MAC test only. Back-off only 0 ~ 3 slot-time
0	ZEROBF	Zero Back Off Time. 0: always write low (Default) 1: for MAC test only. Back Off Time always zeros.

5.1.73 VLAN ID 0 Register (VIDR0)

Offset 1CH (Write)

Field	Name	Description
7:0	VIDR0	VLAN ID [7:0]

5.1.74 Current TX End Page Register (CTEPR)

Offset 1CH (Read)

Field	Name	Description (Default = 00h)
7	TXCQF	TX Command Queue full When set, indicate the TX Command queue was full. Host must check this status before queuing next transmit page and byte count.
6:0	CTEPR	AX88796B will update CTEPR (current TX end page) After every transmitting completed without collision. It is for Host to conform how many free page can reuse for next transmitting. The value is from 40h to 7Fh. It will be 00h when reset or STP.

5.1.75 VLAN ID 1 Register (VIDR1)

Offset 1DH (Write)

Field	Name	Description
7:5	PRI	Frame's priority
4	CFI	Canonical Address Frame Indicator
3:0	VIDR1	VLAN ID [11:8]

5.1.76 Big-Endian Register (BER)

Offset 1EH (Write)

Field	Name	Description (Default = 00h)
7:0	-	All zero, (Default): little-endian If not all zero means set data byte order as big-endian mode. Note: This mode can be used by 32-bit big-endian mode of processors operating with an external 16-bit bus only.

5.1.77 Host Wake Up Register (HWUR)

Offset 1FH (Write)

Field	Name	Description
7:1	-	Reserved
0	HWAKE (SC)	Host write one to wake up AX88796B from D2 power saving. It will be auto clear when wake up.

5.1.78 Software Reset

Offset 1FH (Read)

Field	Name	Description
7:0	-	Don't care this read value.

5.2 The Embedded PHY Registers

The MII management 16-bit register set implemented is as follows. And the following sub-section will describes each field of the registers.

Address	Name	Description	Default value
0	MR0	Control	3100H
1	MR1	Status	7809H
2	MR2	PHY Identifier 1	003BH
3	MR3	PHY Identifier 2	1841H
4	MR4	Autonegotiation Advertisement	01E1H
5	MR5	Autonegotiation Link Partner Ability	0000H
6	MR6	Autonegotiation Expansion	0000H

Tab - 17 The Embedded PHY Registers

Key to default:

Reset value
- 1: Bit set to logic one
- 0: Bit set to logic zero
- X: No set value

Access type
- RO: Read only
- RW: Read or write

Attribute
- SC: Self-clearing
- PS: Value is permanently set
- LL: Latch low
- LH: Latch high

5.2.1 MR0 -- Control Register Bit Descriptions

Field	Type	Description (Default = 3100h)
0.15 (SW_RESET)	0, RW / SC	1 = Software reset 0 = Normal operation
0.14 (LOOPBACK)	0, RW	1 = Loop-back enabled 0 = Normal operation
0.13(SPEED100)	1, RW	1 = 100Mbits/s 0 = 10Mbits/s
0.12 (NWAY_ENA)	1, RW	1 = Auto negotiation enabled. Bits 8 and 13 of this register are ignored when this bit is set. 0 = Auto negotiation disabled. Bits 8 and 13 of this register determine the link speed and mode.
0.11 (POWER DOWN)	0, RW	1 = Power down 0 = Normal operation
0.10 (ISOLATE)	0, R/W	1 = Isolate 0 = Normal operation
0.9 (REDONWAY)	0, RW / SC	Restart Autonegotiation. 1 = Restart auto negotiation 0 = Normal operation
0.8 (FULL_DUP)	1, RW	Duplex Mode. 1 = Full duplex operation 0 = Normal operation
0.7 (COLTST)	0, RW	Collision Test. 1 = Collision test enabled 0 = Normal operation
0.6:0 (RESERVED)	X, RO	Reserved. Write as 0, read as “don’t care”

5.2.2 MR1 -- Status Register Bit Descriptions

Field	Type	Description (Default = 7809h)
1.15 (T4ABLE)	0, RO / PS	**100Base-T4 Ability.** This bit will always be a 0. 0 = AX88796B is not able to perform in 100BASE-T4 mode
1.14 (TXFULDUP)	1, RO /PS	**100Base-TX Full-Duplex Ability.** 1 = AX88796B is able to perform in 100BASE-TX full duplex mode
1.13 (TXHAFDUP)	1, RO / PS	**100Base-TX Half-Duplex Ability.** 1 = AX88796B is able to perform in 100BASE-TX half duplex mode
1.12 (ENFULDUP)	1, RO / PS	**10Base-T Full-Duplex Ability.** 1 = AX88796B is able to perform in 10BASE-T full duplex mode
1.11 (ENHAFDUP)	1, RO / PS	**10Base-T Half-Duplex Ability.** 1 = AX88796B is able to perform in 10BASE-T half duplex mode
1.10:7 (RESERVED)	0, RO	**Reserved.** Write as 0, read as “don’t care”
1.6 (MF preamble suppression)	0, RO	**Management frame preamble suppression:** 0 = AX88796B will not accept management frames with preamble suppressed.
1.5 (NWAYDONE)	0, RO	**Autonegotiation Complete.** 1= Auto negotiation process complete 0 = Auto negotiation process not complete
1.4 (REM_FLT)	0, RO / LH	**Remote Fault.** 1 = Remote fault condition detected (cleared on read or by a chip reset) 0 = No remote fault condition detected
1.3 (NWAYABLE)	1, RO / PS	**Autonegotiation Ability.** 1 = AX88796B is able to perform auto-negotiation
1.2 (LSTAT_OK)	0, RO / LL	**Link Status.** 1 = Valid link established (100Mb/s or 10Mb/s operation) 0 = Link not established
1.1 (JABBER)	0, RO / LH	**Jabber Detect.** 1 = Jabber condition detected 0 = No Jabber condition detected
1.0 (EXT_ABLE)	1, RO / PS	**Extended Capability.** 1 = Extended register capable 0 = Basic register capable only

5.2.3 MR2 -- Identification 1 Registers

Field	Type	Description (Default = 003Bh)
2.15:0 (OUI[3:18])	RO	**Organizationally Unique Identifier.** The third through the twenty-fourth bit of the OUI assigned to the PHY manufacturer by the IEEE are to be placed in bits. 2.15:0 and 3.15:10.

5.2.3 MR3 – Identification 2 Registers

Field	Type	Description (Default = 1841h)
3.15:10 (OUI[19:24])	RO	**Organizationally Unique Identifier.** The remaining 6 bits of the OUI.
3.9:4 (MODEL[5:0])	RO	**Model Number.** 6-bit model number of the device.
3.3:0 (VERSION[3:0])	RO	**Revision Number.** The value of the present revision number

5.2.4 MR4 – Autonegotiation Advertisement Register

Field	Type	Description (Default = 01E1h)
4.15 (NEXT_PAGE)	0, RO / PS	**Next Page.** 0 = No next page available AX88796B does not support the next page function.
4.14 (ACK)	0, RO	**Acknowledge.** 1 = Link partner ability data reception acknowledged 0 = Not acknowledged
4.13 (REM_FAULT)	0, RW	**Remote Fault.** 1= Fault condition detected and advertised 0 = No fault detected
4.12:11 (RESERVED)	X, RW	**Reserved.** Write as 0, read as “don’t care”
4.10 (PAUSE)	0, RW	**Pause.** 1 = Pause operation is enabled for full-duplex links 0 = Pause operation is not enabled
4.9 (100BASET4)	0, RO / PS	**100Base-T4.** 0 = 100BASE-T4 is not supported
4.8 (100BASET_FD)	1, RW	**100Base-TX Full Duplex.** 1 = 100BASE-TX full-duplex is supported by this device 0 = 100BASE-TX full-duplex is not supported by this device
4.7 (100BASETX)	1, RW	**100Base-TX Half Duplex.** 1 = 100BASE-TX half-duplex is supported by this device 0 = 100BASE-TX half-duplex is not supported by this device
4.6 (10BASET_FD)	R/W	**10Base-T Full Duplex.** **1 = 10BASE-T full-duplex is supported by this PHY** **0 = 10BASE-T full-duplex is not supported by this PHY**
4.5 (10BASET)	R/W	**10Base-T Half Duplex.** 1 = 10BASE-T half-duplex is supported by this PHY 0 = 10BASE-T half-duplex is not supported by this PHY
4.4:0 (SELECT)	[0 0001], RW	**Selector Field**. Reset with the value 00001 for IEEE 802.3.

5.2.5 MR5 – Autonegotiation Link Partner Ability (Base Page) Register

Field	Type	Description (Default = 0000h)
5.15 (LP_NEXT_PAGE)	0, RO	**Link Partner Next Page.** 1 = Link partner is next page able 0 = Link partner is not next page able
5.14 (LP_ACK)	0, RO	**Link Partner Acknowledge.** 1 = Link partner reception of data word acknowledged 0 = Not acknowledged
5.13 (LP_REM_FAULT)	0, RO	**Remote Fault.** 1 = Remote fault indicated by link partner 0 = No remote fault indicated by link partner
5.12:11 (RESERVED)	X, RO	**Reserved.** Write as 0, read as “don’t care”
5.10 (LP_PAUSE)	0, RO	**Pause.** 1 = Pause operation is supported by link partner 0 = Pause operation is not supported by link partner
5.9 (LP_T4)	0, RO	**Link Partner 100BASE-T4 supports.** 1 = 100BASE-T4 is supported by link partner 0 = 100BASE-T4 is not supported by link partner
5.8 (LP_ TX_FD)	0, RO	**100BASE-TX full-duplex support.** 1 = 100BASE-TX full-duplex is supported by link partner 0 = 100BASE-TX full-duplex is not supported by link partner
5.7 (LP_ TX_HD)	0, RO	**100BASE-TX half-duplex support.** 1 = 100BASE-TX half-duplex is supported by link partner 0 = 100BASE-TX half-duplex is not supported by link partner
5.6 (LP_ 10_FD)	0, RO	**10BASE-T full-duplex support.** 1 = 10BASE-T full-duplex is supported by link partner 0 = 10BASE-T full-duplex is not supported by link partner
5.5 (LP_ 10_HD)	0, RO	**10BASE-T half-duplex support.** 1 = 10BASE-T half-duplex is supported by link partner 0 = 10BASE-T half-duplex is not supported by link partner
5.4:0 (LP_SELECT)	[0 0000], RO	**Selector Field.** Link partner’s binary encoded protocol selector

5.2.6 MR6 – Autonegotiation Expansion Register

Field	Type	Description (Default = 0000h)
6.15:5 (RESERVED)	0, RO	**Reserved**. Write as 0, read as “don’t care”
6.4 (PAR_DET_FAULT)	0, RO / LH	**Parallel Detection Fault.** 1 = Fault detected via the parallel detection function 0 = No fault detected
6.3 (LP_NEXT_PAGE_ABLE)	0, RO	**Link Partner Next Page Able.** 1 = Link partner is next page able 0 = Link partner is not next page able
6.2 (NEXT_PAGE_ABLE)	0, RO / PS	**Next Page Able.** 0 = PHY is not next page able
6.1 (PAGE_REC)	0, RO / LH	**Page Received**. 1 = New page received 0 = New page not received
6.0 (LP_NWAY_ABLE)	0, RO	**Link Partner Autonegotiation Capable.** 1 = Link partner auto-negotiation supported

6.0 CPU Read and Write Functions

6.1 ISA bus type access functions.

ISA bus Read function

Function Mode	CSn	AEN	A0	RDn	WRn	SD[15:8]	SD[7:0]
Standby Mode	H	X	X	X	X	High-Z	High-Z
Byte Access (For all of CSR except DP)	L L	L L	L H	L L	H H	Not Valid Not Valid	Even-Byte Odd-Byte
Word Access (Only for DP and WTS=1)	L	L	L	L	H	Odd-Byte	Even-Byte

ISA bus Write function

Function Mode	CSn	AEN	A0	RDn	WRn	SD[15:8]	SD[7:0]
Standby Mode	H	X	X	X	X	X	X
Byte Access (For all of CSR except DP)	L L	L L	L H	H H	L L	X X	Even-Byte Odd-Byte
Word Access (Only for DP and WTS=1)	L	L	L	H	L	Odd-Byte	Even-Byte

6.2 80186 CPU bus type access functions.

80186 CPU bus Read function

Function Mode	CSn	A0	RDn	WRn	SD[15:8]	SD[7:0]
Standby Mode	H	X	X	X	High-Z	High-Z
Byte Access (For all of CSR except DP)	L L	L H	L L	H H	Not Valid Odd-Byte	Even-Byte Not Valid
Word Access (Only for DP and WTS=1)	L	L	L	H	Odd-Byte	Even-Byte

80186 CPU bus Write function

Function Mode	CSn	A0	RDn	WRn	SD[15:8]	SD[7:0]
Standby Mode	H	X	X	X	X	X
Byte Access (For all of CSR except DP)	L L	L H	H H	L L	X Odd-Byte	Even-Byte X
Word Access (Only for DP and WTS=1)	L	L	H	L	Odd-Byte	Even-Byte

6.3 MCS-51 CPU bus type access functions.

8051 bus Read function

Function Mode	CSn	PSEN	SA0	RDn	WRn	SD[15:8]	SD[7:0]
Standby Mode	H	X	X	X	X	High-Z	High-Z
	X	L	X	X	X	High-Z	High-Z
Byte Access	L	H	L	L	H	Not Valid	Even-Byte
	L	H	H	L	H	Not Valid	Odd-Byte

8051 bus Write function

Function Mode	CSn	PSEN	SA0	RDn	WRn	SD[15:8]	SD[7:0]
Standby Mode	H	X	X	X	X	X	X
	X	L	X	X	X	X	X
Byte Access	L	H	L	H	L	X	Even-Byte
	L	H	H	H	L	X	Odd-Byte

6.5 CPU Access MII Serial Management Interface

Basic Operation

The primary function of station management is to transfer control and status information about the PHY to a management entity. This function is accomplished by the MDC clock input from MAC entity. The maximum frequency is 2.5 MHz.

The Internal PHY address is fixed to 10h and the equivalent circuit is shown as below:

Fig - 9 SMI connections

A specific set of registers and their contents (described in Tab - 19 MII Management Frames- field Description) defines the nature of the information transferred across the MDIO interface. Frames transmitted on the MII management interface will have the frame structure shown in Tab - 18 SMI Management Frame Format. The order of bit transmission is from left to right. Note that reading and writing the management register must be completed without interruption.

Read/Write (R/W)	**Pre**	**ST**	**OP**	**PHYAD**	**REGAD**	**TA**	**DATA**	**IDLE**
R	1. . .1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
W	1. . .1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Tab - 18 SMI Management Frame Format

Field	**Descriptions**
Pre	**Preamble**. The PHY will accept frames with no preamble. This is indicated by a 1 in MR1 1, bit 6.
ST	**Start of Frame.** The start of frame is indicated by a 01 pattern.
OP	**Operation Code**. The operation code for a read transaction is 10. The operation code for a write transaction is a 01.
PHYADD	**PHY Address**. The PHY address is 5 bits, allowing for 32 unique addresses. The first PHY address bit transmitted and received is the MSB of the address. A station management entity that is attached to multiple PHY entities must have prior knowledge of the appropriate PHY address for each entity.
REGAD	**Register Address.** The register address is 5 bits, allowing for 32 unique registers within each PHY. The first register address bit transmitted and received is the MSB of the address.
TA	**Turnaround**. The turnaround time is a 2-bit time spacing between the register address field, and the data field of a frame, to avoid drive contention on MDIO during a read transaction. During a write to the PHY, these bits is driven to 10 by the station. During a read, the MDIO is not driven during the first bit time and is driven to a 0 by the PHY during the second bit time.
DATA	**Data**. The data field is 16 bits. The first bit transmitted and received will be bit 15 of the register being addressed.
IDLE	**Idle Condition.** The IDLE condition on MDIO is a high-impedance state. All three state drivers will be disabled and the PHY's pull-up resistor will pull the MDIO line to logic 1.

Tab - 19 MII Management Frames- field Description

7.0 Electrical Specification and Timings

7.1 Absolute Maximum Ratings

Description	Rating	Units
VCCK (Core power supply)	-0.3 to 2.16	V
VCCIO (power supply for 3.3V I/O)	-0.3 to 4.0	V
VCCIO (Input voltage of 3.3V I/O with 5V tolerance)	-0.3 to 5.8	V
Storage Temperature	-65 to 150	°C
I_{IN} (DC input current)	20	mA
I_{OUT} (Output short circuit current)	20	mA

7.2 General Operation Conditions

Description	Symbol	Min	Typ	Max	Units
Operating Temperature	Ta	0		70	°C
		-40		85	
Junction Temperature	Tj	-40	+25	+125	°C
Supply Voltage for core (VCCK, VCC18A)	Vcc18	+1.62	+1.8	+1.98	V
Supply Voltage (VCC3A3, VCC3IO, VCC3R3)	Vcc3	+2.97	+3.30	+3.63	V

7.3 DC Characteristics

7.3.1 DC Characteristics of 3.3V with 5V Tolerance

Description		Symbol	Min	Typ	Max	Units
Low Input Voltage		Vil	-		0.8	V
High Input Voltage		Vih	2.0		-	V
Low Output Voltage		Vol	-		0.4	V
High Output Voltage		Voh	2.4		-	V
Switch threshold		Vt		1.5		V
Schmitt trigger negative going threshold voltage		Vt-	0.8	1.1		V
Schmitt trigger positive going threshold voltage		Vt+		1.6	2.0	V
Input pull-up resistance		Rpu	40	75	190	KΩ
Input pull-down resistance		Rpd	40	75	190	KΩ
Input Leakage Current		Iin	-10	±1	10	uA
	with pull-up resistance (Vin=0)		-15	-45	-85	uA
	with pull-down resistance(Vin=VCC3I)		15	45	85	uA
Tri-state Output Leakage Current		Ioz	-10	±1	10	uA

7.3.2 Power Consumption

- **Device only**

Power measurements base on 3.3V/25 °C condition.

Item	Symbol	Operating at 10BASE-T	Operating at 100BASE-TX	PHY power down	D2 power saving	Units
1	VCC3IO	10	10	8	0.04	mA
2	VCC3A3	20	20	16	0	mA
3	VCC3R3 (include VCCK, VCC18A)	20	88	17	0.08	mA
4	VCC3IO + VCC3A3 + VCC3R3	50	118	41	0.12	mA
		165	390	135	0.4	mW
5	ΘJC	13.47 (Thermal resistance of junction to case)				°C/W
6	ΘJA	45.28 (Thermal resistance of junction to ambient)				°C/W

- **Device and system components**

This is the total of Ethernet connectivity solution, which includes external components supporting the AX88796B Ethernet controller as shown in the schematic as below.
Power measurements base on 3.3V/25 °C condition.

Item	**Test Conditions**	Total Power (Typical)	**Units**
1	10BASE-T operation	462	mW
2	100BASE-TX operation	495	mW
3	Cable unplug and non power saving mode	587	mW
4	D1 power saving mode at 10BASE-T Link	448	mW
5	D1 power saving mode at 100BASE-TX Link	468	mW
6	PHY power down	140	mW
7	D2 power saving mode	0.66	mW

7.4 AC Timing Characteristics

7.4.1 Reset Timing

Symbol	Description	Min	Typ.	Max	Units
Trst	Reset pulse width	200	-	-	us
Is	Configuration input setup to RSTn rising	80			ns
Ih	Configuration input hold after RSTn rising	10			ns
Oen	Output driver after RSTn rising			80	ns

7.4.2 ISA Bus Access Timing

(1) Read cycle:

Symbol	Description	Min	Typ.	Max	Units
Tasu	ADDRESS SETUP TIME	0	-	-	ns
Tah	ADDRESS HOLD TIME	0	-	-	ns
Tonis16	IOIS16n VALID FROM SA[5:0], CSn AND AEN	-	-	11	ns
Toffis16	IOIS16n VALID FROM SA[5:0], CSn AND AEN	-	-	6	ns
Tdv	DATA VALID TIME FROM RDn	-	-	33*[1] 35*[2]	ns
Tdoh	DATA OUTPUT HOLD TIME	0	-	-	ns
Trdl	RDn LOW REQUIRE TIME	35	-	-	ns
Trdh	RDn HI REQUIRE TIME	13	-	-	ns
Tdon	DATA BUFFER TURN ON TIME	0			ns
Tdoff	DATA BUFFER TURN OFF TIME			7	ns
Tcycle	READ CYCLE TIME	48			ns

*[1] : Base on SD bus output load 25pF
*[2] : Base on SD bus output load 50pF

(2) Write cycle:

Symbol	Description	Min	Typ.	Max	Units
Tasu	ADDRESS SETUP TIME	0	-	-	ns
Tah	ADDRESS HOLD TIME	0			ns
Tonis16	IOIS16n VALID FROM SA[5:0], CSn AND AEN	-	-	11	ns
Toffis16	IOIS16n DISABLE FROM SA[5:0], CSn AND AEN	-	-	6	ns
Tds	DATA STABLE TIME	-	-	15	ns
Tdh	DATA HOLD TIME	0	-	-	ns
Twrl	WRn WIDTH TIME	45	-	-	ns
Twrh	WRn HI REQUIRE TIME	13	-	-	ns
Tcycle	WRITE CYCLE TIME	48	-	-	ns

7.4.3 80186 Type I/O Access Timing

(1) Read cycle:

Symbol	Description	Min	Typ.	Max	Units
Tasu	ADDRESS SETUP TIME	0	-	-	ns
Tah	ADDRESS HOLD TIME	0	-	-	ns
Tdv	DATA VALID TIME FROM RDn	-	-	33*[1] 35*[2]	ns
Tdoh	DATA OUTPUT HOLD TIME	0	-	-	ns
Trdl	RDn LOW REQUIRE TIME	35	-	-	ns
Trdh	RDn HI REQUIRE TIME	13	-	-	ns
Tdon	DATA BUFFER TURN ON TIME	0			ns
Tdoff	DATA BUFFER TURN OFF TIME			7	ns
Tcycle	READ CYCLE TIME	48			ns

*[1] : Base on SD bus output load 25pF
*[2] : Base on SD bus output load 50pF

(2) Write Cycle

Symbol	Description	Min	Typ.	Max	Units
Tasu	ADDRESS SETUP TIME	0	-	-	ns
Tah	ADDRESS HOLD TIME	0	-	-	ns
Tds	DATA STABLE TIME	-	-	15	ns
Tdh	DATA HOLD TIME	0	-	-	ns
Twrl	WRn WIDTH TIME	35	-	-	ns
Twrh	WRn HI REQUIRE TIME	13	-	-	ns
Tcycle	WRITE CYCLE TIME	48	-	-	ns

7.4.4 8051 Bus Access Timing

(1) Read cycle

Symbol	Description	Min	Typ.	Max	Units
Tasu	ADDRESS SETUP TIME	0	-	-	ns
Tah	ADDRESS HOLD TIME	0	-	-	ns
Tdv	DATA VALID TIME FROM RDn	-	-	33*[1] 35*[2]	ns
Tdoh	DATA OUTPUT HOLD TIME	0	-	-	ns
Trdl	RDn LOW REQUIRE TIME	35	-	-	ns
Trdh	RDn HI REQUIRE TIME	13	-	-	ns
Tdon	DATA BUFFER TURN ON TIME	0			ns
Tdoff	DATA BUFFER TURN OFF TIME			7	ns
Tcycle	READ CYCLE TIME	48			ns

*[1] : Base on SD bus output load 25pF
*[2] : Base on SD bus output load 50pF

(2) Write cycle

Symbol	Description	Min	Typ.	Max	Units
Tasu	ADDRESS SETUP TIME	0	-	-	ns
Tah	ADDRESS HOLD TIME	0	-	-	ns
Tds	DATA STABLE TIME	-	-	15	ns
Tdh	DATA HOLD TIME	0	-	-	ns
Twrl	WRn WIDTH TIME	35	-	-	ns
Twrh	WRn HI REQUIRE TIME	13	-	-	ns
Tcycle	WRITE CYCLE TIME	48	-	-	ns

7.4.5 Burst Reads Access Timing

Burst read access is enabled when set FIFO_SEL(SA5) is driven high during a read access. This is normally accomplished by connecting the FIFO_SEL(SA5) signal to a high-order address line. This mode is useful when the host processor must increment its address when accessing the AX88796B.

In this mode, performance is improved by allowing an unlimited number of back-to-back WORDS read cycles. AX88796B base on SA0 or SA1 address toggles to identify WORD access cycle time. Host can set burst cycle base on SA0 or SA1 toggle by BCB1 (CR page3 Offset 0Dh).

Symbol	Description	Min	Typ.	Max	Units
Tasu	ADDRESS SETUP TIME	0	-	-	ns
Tah	ADDRESS HOLD TIME	0	-	-	ns
Tdv	DATA VALID TIME FROM RDn	-	-	33*[1] 35*[2]	ns
Tadv	DATA VALID TIME FROM ADDRESS			33*[1] 35*[2]	ns
Tdoh	DATA OUTPUT HOLD TIME	0	-	-	ns
Trdh	RDn HI REQUIRE TIME	13	-	-	ns
Tacyc	READ CYCLE TIME	48			ns
Tdon	DATA BUFFER TURN ON	0			ns
Tdoff	DATA BUFFER TURN OFF			7	ns

*[1] : Base on SD bus output load 25pF
*[2] : Base on SD bus output load 50pF

8.0 Package Information

Symbol	Dimension (mm)		
	MIN.	TYP	MAX
A1	0.05		0.15
A2	1.35	1.40	1.45
A			1.60
b	0.13	0.18	0.23
D		7.00	
E		7.00	
e		0.40	
Hd		9.00	
He		9.00	
L	0.45	0.60	0.75
L1		1.00	
θ	0°	3.5°	7°

9.0 Ordering Information

Model NO	Description
AX88796BLF	64 PIN, LQFP Package, Commercial grade 0°C to +70 °C (Green, Lead-Free)
AX88796BLI	64 PIN, LQFP Package, Industrial grade -40°C to +85 °C (Green, Lead-Free)

Appendix A1: MCS51-like (8-bit)

An example, AX88796B's bus setting as MCS-51 mode. (Two external pull-up resister connect to EECS and EECK)

Read				Write			
Host Addr A[5:0]	SD[15:8]	SD[7:0]	AX88796B CSR Offset	Host Addr A[5:0]	SD[15:8]	SD[7:0]	AX88796B CSR Offset
0	Offset 1	Offset 0	0	0	no effect	To Offset 0	0
1	Offset 1	Offset 1	1	1	no effect	To Offset 1	1
2	Offset 3	Offset 2	2	2	no effect	To Offset 2	2
3	Offset 3	Offset 3	3	3	no effect	To Offset 3	3
4	Offset 5	Offset 4	4	4	no effect	To Offset 4	4
5	Offset 5	Offset 5	5	5	no effect	To Offset 5	5
6	Offset 7	Offset 6	6	6	no effect	To Offset 6	6
7	Offset 7	Offset 7	7	7	no effect	To Offset 7	7
8	Offset 9	Offset 8	8	8	no effect	To Offset 8	8
9	Offset 9	Offset 9	9	9	no effect	To Offset 9	9
A	Offset B	Offset A	A	A	no effect	To Offset A	A
B	Offset B	Offset B	B	B	no effect	To Offset B	B
C	Offset D	Offset C	C	C	no effect	To Offset C	C
D	Offset D	Offset D	D	D	no effect	To Offset D	D
E	Offset F	Offset E	E	E	no effect	To Offset E	E
F	Offset F	Offset F	F	F	no effect	To Offset F	F
10	(DP)	(DP)	(DP)	10	no effect	(DP)	(DP)
11	X	X	X	11	X	X	X
12	Offset 13	Offset 12	12	12	no effect	To Offset 12	12
13	Offset 13	Offset 13	13	13	no effect	To Offset 13	13
14	Offset 15	Offset 14	14	14	no effect	To Offset 14	14
15	Offset 15	Offset 15	15	15	no effect	To Offset 15	15
16	Offset 17	Offset 16	16	16	no effect	To Offset 16	16
17	Offset 17	Offset 17	17	17	no effect	To Offset 17	17
18	Offset 19	Offset 18	18	18	no effect	To Offset 18	18
19	Offset 19	Offset 19	19	19	no effect	To Offset 19	19
1A	Offset 1B	Offset 1A	1A	1A	no effect	To Offset 1A	1A
1B	Offset 1B	Offset 1B	1B	1B	no effect	To Offset 1B	1B
1C	Offset 1D	Offset 1C	1C	1C	no effect	To Offset 1C	1C
1D	Offset 1D	Offset 1D	1D	1D	no effect	To Offset 1D	1D
1E	No effect	Offset 1E	1E	1E	no effect	To Offset 1E	1E
1F	(Reset) *1	(Reset) *1	1F	1F	no effect	To Offset 1F	1F

*1 Read offset 1Fh register will reset AX88796B

Appendix A2: ISA-like (8/16-bit)

An example, AX88796B's bus setting as ISA mode. (No external resister connect to EECS and EECK)

CSR Read				CSR Write			
Host Addr A[5:0]	SD[15:8]	SD[7:0]	AX88796B CSR Offset	Host Addr A[5:0]	SD[15:8]	SD[7:0]	AX88796B CSR Offset
0	Offset 1	Offset 0	0	0	no effect	To Offset 0	0
1	Offset 1	Offset 1	1	1	no effect	To Offset 1	1
2	Offset 3	Offset 2	2	2	no effect	To Offset 2	2
3	Offset 3	Offset 3	3	3	no effect	To Offset 3	3
4	Offset 5	Offset 4	4	4	no effect	To Offset 4	4
5	Offset 5	Offset 5	5	5	no effect	To Offset 5	5
6	Offset 7	Offset 6	6	6	no effect	To Offset 6	6
7	Offset 7	Offset 7	7	7	no effect	To Offset 7	7
8	Offset 9	Offset 8	8	8	no effect	To Offset 8	8
9	Offset 9	Offset 9	9	9	no effect	To Offset 9	9
A	Offset B	Offset A	A	A	no effect	To Offset A	A
B	Offset B	Offset B	B	B	no effect	To Offset B	B
C	Offset D	Offset C	C	C	no effect	To Offset C	C
D	Offset D	Offset D	D	D	no effect	To Offset D	D
E	Offset F	Offset E	E	E	no effect	To Offset E	E
F	Offset F	Offset F	F	F	no effect	To Offset F	F
10	(DP)	(DP)	(DP)	10	(DP)	(DP)	(DP)
11	X	X	X	11	X	X	X
12	Offset 13	Offset 12	12	12	no effect	To Offset 12	12
13	Offset 13	Offset 13	13	13	no effect	To Offset 13	13
14	Offset 15	Offset 14	14	14	no effect	To Offset 14	14
15	Offset 15	Offset 15	15	15	no effect	To Offset 15	15
16	Offset 17	Offset 16	16	16	no effect	To Offset 16	16
17	Offset 17	Offset 17	17	17	no effect	To Offset 17	17
18	Offset 19	Offset 18	18	18	no effect	To Offset 18	18
19	Offset 19	Offset 19	19	19	no effect	To Offset 19	19
1A	Offset 1B	Offset 1A	1A	1A	no effect	To Offset 1A	1A
1B	Offset 1B	Offset 1B	1B	1B	no effect	To Offset 1B	1B
1C	Offset 1D	Offset 1C	1C	1C	no effect	To Offset 1C	1C
1D	Offset 1D	Offset 1D	1D	1D	no effect	To Offset 1D	1D
1E	No effect	Offset 1E	1E	1E	no effect	To Offset 1E	1E
1F	(Reset) *1	(Reset) *1	1F	1F	no effect	To Offset 1F	1F

*1 Read offset 1Fh register will reset AX88796B

Appendix A3: 186-like (16-bit)

An example, AX88796B's bus setting as 186 mode. (One external pull-up resister connect to EECK)

Read				Write			
Host Addr A[5:0]	SD[15:8]	SD[7:0]	AX88796B CSR Offset	Host Addr A[5:0]	SD[15:8]	SD[7:0]	AX88796B CSR Offset
0	Offset 1	Offset 0	0	0	no effect	To Offset 0	0
1	Offset 1	Offset 0	1	1	To Offset 1	no effect	1
2	Offset 3	Offset 2	2	2	no effect	To Offset 2	2
3	Offset 3	Offset 2	3	3	To Offset 3	no effect	3
4	Offset 5	Offset 4	4	4	no effect	To Offset 4	4
5	Offset 5	Offset 4	5	5	To Offset 5	no effect	5
6	Offset 7	Offset 6	6	6	no effect	To Offset 6	6
7	Offset 7	Offset 6	7	7	To Offset 7	no effect	7
8	Offset 9	Offset 8	8	8	no effect	To Offset 8	8
9	Offset 9	Offset 8	9	9	To Offset 9	no effect	9
A	Offset B	Offset A	A	A	no effect	To Offset A	A
B	Offset B	Offset A	B	B	To Offset B	no effect	B
C	Offset D	Offset C	C	C	no effect	To Offset C	C
D	Offset D	Offset C	D	D	To Offset D	no effect	D
E	Offset F	Offset E	E	E	no effect	To Offset E	E
F	Offset F	Offset E	F	F	To Offset F	no effect	F
10	(DP)	(DP)	(DP)	10	(DP)	(DP)	(DP)
11	X	X	X	11	X	X	X
12	Offset 13	Offset 12	12	12	no effect	To Offset 12	12
13	Offset 13	Offset 12	13	13	To Offset 13	no effect	13
14	Offset 15	Offset 14	14	14	no effect	To Offset 14	14
15	Offset 15	Offset 14	15	15	To Offset 15	no effect	15
16	Offset 17	Offset 16	16	16	no effect	To Offset 16	16
17	Offset 17	Offset 16	17	17	To Offset 17	no effect	17
18	Offset 19	Offset 18	18	18	no effect	To Offset 18	18
19	Offset 19	Offset 18	19	19	To Offset 19	no effect	19
1A	Offset 1B	Offset 1A	1A	1A	no effect	To Offset 1A	1A
1B	Offset 1B	Offset 1A	1B	1B	To Offset 1B	no effect	1B
1C	Offset 1D	Offset 1C	1C	1C	no effect	To Offset 1C	1C
1D	Offset 1D	Offset 1C	1D	1D	To Offset 1D	no effect	1D
1E	No effect	Offset 1E	1E	1E	no effect	To Offset 1E	1E
1F	(Reset) *1	(Reset) *1	1F	1F	To Offset 1F	no effect	1F

*1 Read offset 1Fh register will reset AX88796B

Appendix A4: co-work with 32-bit processor

An example, AX88796B co-work with Samsung 2440 processor. (32-bit processor with external 16-bit bus) AX88796B's bus setting as ISA mode. (Without external resister connect to EECS and EECK) Host can use burst read mode, it is useful host processor increment its address when moving AX88796B received data.

AX88796B supports two kinds of Data Port for receiving/transmitting packets from/to AX88796B. One is the PIO Data Port (offset 10h); the other one is the SRAM-like Data Port (e.g. offset 800h ~ FFFh for Samsung2440 processor as described in below figure). The SRAM-like Data Port address range depends on which address line of host processor is being connected to the address line SA5/FIFO_SEL of AX88796B.

Software on host CPU can issue Single Data Read/Write command to both PIO Data Port and SRAM-like Data Port. However, to use Burst Data Read/Write commands, one has to use SRAM-like Data Port, which requires SA5/FIFO_SEL (pin 45) of AX88796B connecting to an upper address line of host CPU. AX88796B with Samsung 2440 processor reference schematic has SA5/FIFO_SEL pin connected to upper address line (i.e. A11 of Samsung 2440) for supporting Burst Data Read/Write commands.

Read				Write			
Host Addr A[11:0]	SD[15:8]	SD[7:0]	AX88796B CSR Offset	Host Addr A[11:0]	SD[15:8]	SD[7:0]	AX88796B CSR Offset
0	Offset 1	Offset 0	0	0	no effect	To Offset 0	0
2	Offset 1	Offset 1	1	2	no effect	To Offset 1	1
4	Offset 3	Offset 2	2	4	no effect	To Offset 2	2
6	Offset 3	Offset 3	3	6	no effect	To Offset 3	3
8	Offset 5	Offset 4	4	8	no effect	To Offset 4	4
A	Offset 5	Offset 5	5	A	no effect	To Offset 5	5
C	Offset 7	Offset 6	6	C	no effect	To Offset 6	6
E	Offset 7	Offset 7	7	E	no effect	To Offset 7	7
10	Offset 9	Offset 8	8	10	no effect	To Offset 8	8
12	Offset 9	Offset 9	9	12	no effect	To Offset 9	9
14	Offset B	Offset A	A	14	no effect	To Offset A	A
16	Offset B	Offset B	B	16	no effect	To Offset B	B
18	Offset D	Offset C	C	18	no effect	To Offset C	C
1A	Offset D	Offset D	D	1A	no effect	To Offset D	D
1C	Offset F	Offset E	E	1C	no effect	To Offset E	E
1E	Offset F	Offset F	F	1E	no effect	To Offset F	F
20	10 (DP)	10 (DP)	10 (DP)	20	10 (DP)	10 (DP)	10 (DP)
22	X	X	X	22	X	X	X
24	Offset 13	Offset 12	12	24	no effect	To Offset 12	12
26	Offset 13	Offset 13	13	26	no effect	To Offset 13	13
28	Offset 15	Offset 14	14	28	no effect	To Offset 14	14
2A	Offset 15	Offset 15	15	2A	no effect	To Offset 15	15
2C	Offset 17	Offset 16	16	2C	no effect	To Offset 16	16
2E	Offset 17	Offset 17	17	2E	no effect	To Offset 17	17

30	Offset 19	Offset 18	18	30	no effect	To Offset 18	18
32	Offset 19	Offset 19	19	32	no effect	To Offset 19	19
34	Offset 1B	Offset 1A	1A	34	no effect	To Offset 1A	1A
36	Offset 1B	Offset 1B	1B	36	no effect	To Offset 1B	1B
38	Offset 1D	Offset 1C	1C	38	no effect	To Offset 1C	1C
3A	Offset 1D	Offset 1D	1D	3A	no effect	To Offset 1D	1D
3C	No effect	Offset 1E	1E	3C	no effect	To Offset 1E	1E
3E	(Reset) *1	(Reset) *1	1F	3E	no effect	To Offset 1F	1F
40 ~7FF	No used	No used	No used	40 ~7FF	No used	No used	No used
800 ~ FFF	(DP)	(DP)	10 (DP)	800 ~ FFF	(DP)	(DP)	10 (DP)

*1 Read offset 1Fh register will reset AX88796B

Appendix A5: big-endian processor of Data Byte Lands

An example, AX88796B co-work with big-endian processor like Renesas H8/SH2 MCU, etc.. (To support big-endian processors, the hardware designer must explicitly swap the connection of data byte lanes.)

Appendix B: Disable AX88796B voltage regulator

AX88796B integrates an on-chip 3.3V to 1.8V voltage regulator for single-power supply system design. If the system have 1.8V power source already, user may like to disable AX88796B voltage regulator and use the existing 1.8V power source (probably a higher efficiency version). In that case, user can connect VCC3R3 (pin-10) and GND3R3 (pin-11) to ground, keep V18F (pin-9) open, and set REGSTB bit of PMR register (see Page3 Offset 0BH bit-4 in section 5.1.56 Power Management Register (PMR)) to 0 (i.e. logic "low") to avoid the leakage current. Please refer to below picture for details.

Note: If user connects the VCC3R3 to 3.3V VCC and wants to disable the internal voltage regulator of AX88796B, the REGSTB bit of PMR register should be set to 1 to set the regulator in standby mode to reduce the leakage current.

Reversion History

Revision	Date	Comment
V1.0	2006/03/01	Initial Release.
V1.1	2006/03/31	1. Correct some typo errors. 2. Change page3 offset 0Dh register name from P30D to MISC. 3. Change the name of bit 5 of MCR register from TQCE to BBTC. 4. Define a short name “TXCQF” for bit 7 of CTEPR register. 5. Add the default values of PHY registers into Section 5.2.
V1.2	2006/09/08	1. Correct the pin descriptions of pin 60 and 63 in Figure 2 and Section 2-5. 2. Correct the Wakeup Frame registers configuration information in Section 4.3.1. 3. Update the reference schematics in Section 7.3.2, Appendix A1. 4. Remove Demonstration Circuit A, B, C reference schematics.
V1.3	2006/09/20	1. Modify the resistance value of pin 64 (RSET_BG) from 11.8 ± 1% K ohm to 12.1 ± 1% K ohm.
V1.4	2006/10/05	1. Add Thermal Resistance values (Θ_{Jc}, Θ_{JA}) of Junction in Section 7.3.2. 2. Correct the SD[7:0] values of Read cycle in Appendix A3 “186-like (16-bit)”. 3. Correct the SD[7:0] and SD[15:8] values of offset 1Fh register Read cycle in Appendix A1~A4.
V1.5	2007/3/19	1. Add US patent approved (NO 6799231) and VLAN in the Features page. 2. Change the product name in the Features page. 3. Correct the TPI+/TPI- pin name of AX88796B Pin Out Diagram in Section 1.3. 4. Modify some pin descriptions in Section 2.2 and 2.5. 5. Modify the Wake-up Configuration descriptions in Section 4.3.1 and 5.1.54. 6. Change the Storage Temperature to –56 to 150 °C in Section 7.1. 7. Add Appendix A5 to indicate the reference connection for big-endian processor. 8. Add Appendix B to indicate how to disable the internal regulator.
V1.6	2007/4/27	1. Modify the description of SA5/FIFO_SEL pin in Section 2.1 and Appendix A4. 2. Swapped the pin name of XTALIN and XTALOUT in Section 2.5 and Figure 2.

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