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10/100BASE 3-in-1 Local CPU Bus Fast Ethernet Controller with Embedded SRAM

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Features

- Highly integrated with embedded 10/100Mbps MAC, PHY and Transceiver
- Embedded 8K * 16 bit SRAM
- Compliant with IEEE 802.3/802.3u 100BASE-TX/FX specification
- NE2000 register level compatible instruction
- Single chip local CPU bus 10/100Mbps Fast Ethernet MAC Controller
- Support both 8 bit and 16 bit local CPU interfaces include MCS-51 series, 80186 series and MC68K series CPU
- Support both 10Mbps and 100Mbps data rate
- Support both full-duplex or half-duplex operation
- Provides an extra MII port for supporting other media. For example, Home LAN application
- Support EEPROM interface to store MAC address
- External and internal loop-back capability
- Support Standard Print Port for printer server application
- Support upto 3/1 General Purpose In/Out pins
- 128-pin LQFP low profile package
- Low Power Consumption, typical under 100mA
- 0.25 Micron low power CMOS process. 25MHz Operation, Pure 3.3V operation with 5V I/O tolerance.
- Non leed free part number is AX88796 L
- RoHS compliant part number is AX88796 LF

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Product description

The AX88796 Fast Ethernet Controller is a high performance and highly integrated local CPU bus Ethernet Controller with embedded 10/100Mbps PHY/Transceiver and 8K*16 bit SRAM. The AX88796 supports both 8 bit and 16 bit local CPU interfaces include MCS-51 series, 80186 series, MC68K series CPU and ISA bus. The AX88796 implements both 10Mbps and 100Mbps Ethernet function based on IEEE802.3 / IEEE802.3u LAN standard. The AX88796 also provides an extra IEEE802.3u compliant media-independent interface (MII) to support other media applications. Using MII interface, Home LAN PHY type media can be supported.
As well as, the chip also provides optional Standard Print Port (parallel port interface), can be used for printer server device or treat as simple general I/O port. The chip also support upto 3/1 additional General Purpose In/Out pins

System Block Diagram

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1.0 Introduction

1.1 General Description:

The AX88796 provides industrial standard NE2000 registers level compatible instruction set. Various drivers are easy acquired, maintenance and usage. No much additional effort to be paid. Software is easily port to various embedded systems with no pain and tears

The AX88796 Fast Ethernet Controller is a high performance and highly integrated local CPU bus Ethernet Controller with embedded 10/100Mbps PHY/Transceiver and 8K*16 bit SRAM. The AX88796 supports both 8 bit and 16 bit local CPU interfaces include MCS-51 series, 80186 series, MC68K series CPU and ISA bus. The AX88796 implements both 10Mbps and 100Mbps Ethernet function based on IEEE802.3 / IEEE802.3u LAN standard. The AX88796 also provides an extra IEEE802.3u compliant media-independent interface (MII) to support other media applications. Using MII interface, Home LAN PHY type media can be supported.

As well as, the chip also provides optional Standard Print Port (parallel port interface), can be used for printer server device or treat as simple general I/O port. The chip also support upto 3/1 additional General Purpose In/Out pins

The main difference between AX88796 and AX88195 are : 1) Embedded packet buffer memory 2) Built-in 10/100Mbps PHY/Transceiver 3) Replace memory I/F with PHY/Transceiver I/F. 4) Canceling SAX address decoding. 5) Fix interrupt status can't always clean up problem of AX88195. 6) Add upto 3/1 general Purpose In/Out pins.

AX88796 use 128-pin LQFP low profile package, 25MHz operation, and single 3.3V operation with 5V I/O tolerance. The ultra low power consumption is an outstanding feature and enlarges the application field. It is suitable for some power consumption sensitive product like small size embedded products, PDA (Personal Digital Assistant) and Palm size computer …etc.

1.2 AX88796 Block Diagram:

Fig - 1 AX88796 Block Diagram

1.3a AX88796 Pin Connection Diagram

The AX88796 is housed in the 128-pin plastic light quad flat pack. Fig - 2 shows the AX88796 pin connection diagram.

Fig - 2 AX88796 Pin Connection Diagram

1.3b AX88796 Pin Connection Diagram with SPP Port Option

Fig - 3 AX88796 Pin Connection Diagram with SPP Port Option

1.3.1 AX88796 Pin Connection Diagram for ISA Bus Mode

Fig - 4 AX88796 Pin Connection Diagram for ISA Bus Mode

1.3.2 AX88796 Pin Connection Diagram for 80x86 Mode

Fig - 5 AX88796 Pin Connection Diagram for 80x86 Mode

1.3.3 AX88796 Pin Connection Diagram for MC68K Mode

Fig - 6 AX88796 Pin Connection Diagram for MC68K Mode

1.3.4 AX88796 Pin Connection Diagram for MCS-51 Mode

Fig - 7 AX88796 Pin Connection Diagram for MCS-51 Mode

2.0 Signal Description

The following terms describe the AX88796 pin-out:
All pin names with the "/" suffix are asserted low.
The following abbreviations are used in following Tables.

I	**Input**	**PU**	**Internal Pull Up(200K)**
O	**Output**	**PD**	**Internal Pull Down(50K)**
I/O	**Input/Output**	**P**	**Power Pin**
TRI	**TRI-state**		

2.1 Local CPU Bus Interface Signals Group

SIGNAL	TYPE	PIN NO.	DESCRIPTION
SA[9:1], SA[0]/LDS	I	15, 12 – 4	System Address : Signals SA[9:0] are address bus input lines, which lower I/O spaces on chip. SA[0] also means Lower Data Strobe (/LDS) active low signal in 68K application mode.
/BHE or /UDS	I/PU	22	Bus High Enable or Upper Data Strobe : Bus High Enable is active low signal in some 16-bit application mode, which enable high bus (SD[15:8]) active. The signal also name as Upper Data Strobe (/UDS) for 68K application mode.
SD[15:0]	I/O/PD	23 – 26, 29 – 33, 35 – 39, 41 – 42	System Data Bus : Signals SD[15:0] constitute the bi-directional data bus.
IREQ/IREQ	O	16	Interrupt Request : When ISA BUS or 80186 CPU mode is select. IREQ is asserted high to indicate the host system that the chip requires host software service. When MC68K or MCS-51 CPU mode is select. /IREQ is asserted low to indicate the host system that the chip requires host software service.
RDY/DTACK	TRI/PU	2	Ready : This signal is set low to insert wait states during Remote DMA transfer. /Dtack : When Motorola CPU type is selected, the pin is active low inform CPU that data is accepted.
/CS	I/PU	128	Chip Select When the /CS signal is asserted, the chip is selected.
/IORD	I/PU	19	I/O Read :The host asserts /IORD to read data from AX88796 I/O space. When Motorola CPU type is select , the pin is useless.
/IOWR or R/W	I/PU	18	I/O Write :The host asserts /IOWR to write data into AX88796 I/O space. When Motorola CPU type is select, the pin is active high for read operation at the same time.
/IOCS16	TRI/PU	123	I/O is 16 Bit Port : The /IOIS16 is asserted when the address at the range corresponds to an I/O address to which the chip responds, and the I/O port addressed is capable of 16-bit access.
AEN or /PSEN	I/PD	1	Address Enable : The signal is asserted when the address bus is available for DMA cycle. When negated (low), AX88796 an I/O slave device may respond to addresses and I/O command. PSEN : This signal is active low for 8051 program access. For I/O device, AX88796, this signal is active high to access the chip. This signal is for 8051 bus application only.

Tab - 1 Local CPU bus interface signals group

2.2 10/100Mbps Twisted-Pair Interface pins group

SIGNAL	TYPE	PIN NO.	DESCRIPTION
TPI+	I	70	Received Data. Positive differential received 125M baud MLT3 or 10M baud Manchester data from magnetic.
TPI-	I	71	Received Data. Negative differential received 125M baud MLT3 or 10M baud Manchester data from magnetic.
TPO+	O	88	Transmit Data. Positive differential transmit 125M baud MLT3 or 10M baud Manchester data to magnetic.
TPO-	O	87	Transmit Data. Negative differential transmit 125M baud MLT3 or 10M baud Manchester data to magnetic.
REXT10	I	84	Current Setting 10Mbits/s. An external resistor 20k ohm is placed from this signal to ground to set the 10Mbits/s TP driver transmit output level.
REXT100	I	83	Current Setting 100Mbits/s. An external resistor 2.49k ohm is placed from this signal to ground to set the 100Mbits/s TP driver transmit output level.
REXTBS	I	74	External Bias Resistor. Band Gap Reference for the Receive Channel. Connect this signal to a 24.9k ohm +/- 1 percent resistor to ground. The parasitic load capacitance should be less than 15 pF.

Tab - 2 10/100Mbps Twisted-Pair Interfaces pins group

2.3 Built-in PHY LED indicator pins group

SIGNAL	TYPE	PIN NO.	DESCRIPTION
I_ACT or I_FULL/COL	O	62	Active Status : When I_OP is logic 1. If there is activity, transmit or receive, on the line occurred, the output will be driven low for 0.67 sec and then driven high at least 0.67 sec. Full-Duplex/Collision Status. When I_OP is logic 0. If this signal is low, it indicates full-duplex link established, and if it is high, then the link is in half-duplex mode. When in half-duplex and collision occurrence, the output will be driven low for 0.67 sec and driven high at least 0.67 sec. (Current sink capacity is 6mA)
I_SPEED	O	61	Speed Status : If this signal is low, it indicates 100Mbps, and if it is high, then the speed is 10Mbps. (Current sink capacity is 6mA)
I_LINK Or I_LK/ACT	O	60	Link Status : When I_OP is logic 1. If this signal is low, it indicates link, and if it is high, then the link is fail. Link Status/Active : When I_OP is logic 0. If this signal is low, it indicates link, and if it is high, then the link is fail. When in link status and line activity occurrence, the output will be driven low for 0.67 sec and driven high at least 0.67 sec. (Current sink capacity is 6mA)

Tab - 3 Built-in PHY LED indicator pins group

2.4 EEPROM Signals Group

SIGNAL	TYPE	PIN NO.	DESCRIPTION
EECS	O	51	EEPROM Chip Select : EEPROM chip select signal.
EECK	O/PD	50	EEPROM Clock : Signal connected to EEPROM clock pin.
EEDI	O	49	EEPROM Data In : Signal connected to EEPROM data input pin.
EEDO	I/PU	48	EEPROM Data Out : Signal connected to EEPROM data output pin.

Tab - 4 EEPROM bus interface signals group

2.5 MII interface signals group (Optional)

SIGNAL	TYPE	PIN NO.	DESCRIPTION
RXD[3:0]	I/PU	98 – 95	Receive Data : RXD[3:0] is driven by the PHY synchronously with respect to RX_CLK.
CRS	I/PD	100	Carrier Sense : Asynchronous signal CRS is asserted by the PHY when either the transmit or receive medium is non-idle.
RX_DV	I/PD	102	Receive Data Valid : RX_DV is driven by the PHY synchronously with respect to RX_CLK. Asserted high when valid data is present on RXD [3:0].
RX_ER	(Omit)	No Support	Receive Error : RX_ER ,is driven by PHY and synchronous to RX_CLK, is asserted for one or more RX_CLK periods to indicate to the port that an error has detected.
RX_CLK	I/PU	99	Receive Clock : RX_CLK is a continuous clock that provides the timing reference for the transfer of the RX_DV,RXD[3:0] and RX_ER signals from the PHY to the MII port of the repeater.
COL	I/PD	101	Collision : this signal is driven by PHY when collision is detected.
TX_EN	O	108	Transmit Enable : TX_EN is transition synchronously with respect to the rising edge of TX_CLK. TX_EN indicates that the port is presenting nibbles on TXD [3:0] for transmission.
TXD[3:0]	O	112 – 109	Transmit Data : TXD[3:0] is transition synchronously with respect to the rising edge of TX_CLK. For each TX_CLK period in which TX_EN is asserted, TXD[3:0] are accepted for transmission by the PHY.
TX_CLK	I/PU	107	Transmit Clock : TX_CLK is a continuous clock from PHY. It provides the timing reference for the transfer of the TX_EN and TXD[3:0] signals from the MII port to the PHY.
MDC	O/PU	67	Station Management Data Clock : The timing reference for MDIO. All data transfers on MDIO are synchronized to the rising edge of this clock. The signal output reflects MDC register value. About MDC register, please refer to MII/EEPROM Management register bit 0. MDC clock frequency is a 2.5MHz maximum accourding to IEEE 802.3u MII specification. Acturely, many PHYs are designed to accept higher frequency than 2.5MHz.
MDIO	I/O/PU	66	Station Management Data Input/Output :Serial data input/output transfers from/to the PHYs . The transfer protocol has to meet the IEEE 802.3u MII specification. For more information, please refer to section 6.5 CPU Access MII Station Management functions.

Tab - 5 MII interface signals group

2.6 Standard Printer Port (SPP) Interface pins group (Optional)

SIGNAL	TYPE	PIN NO.	DESCRIPTION
PD[7:5] PD[4:0]	I/O/PD I/O/PU	102 – 100 99 - 95	Parallel Data :The bi-directional parallel data bus is used to transfer information between CPU and peripherals. Default serve as input, using /DOE bit of register offset x1Ah to set the direction.
BUSY	I/PU	108	Busy : This is a status input from the printer, high indicating that the printer is not ready to receive new data.
/ACK	I/PU	107	Acknowledge : A low active input from the printer indicating that it has received the data and is ready to accept new data.
PE	I/PU	106	Paper Empty : A status input from the printer, high indicating that the printer is out of paper.
SLCT	I/PU	103	Slect: This high active input from the printer indicating that it has power on.
/ERR	I/PU	113	Error : A low active input from the printer indicating that there is an error condition at the printer.
/SLCTIN	O	112	Slect In: This active low output selects the printer.
/INIT	O	111	Init: This signal is used to initiate the printer when low.
/ATFD	O	110	Auto Feed :This output goes low to cause the printer to automatically feed one line after each line is printed.
/STRB	O	109	Strobe : A low active pulse on this output is used to strobe the print data into the printer.

Tab - 6 Standard Printer Port Interface pins group

2.7 General Purpose I/O pins group

Signal Name	Type	Pin No.	Description
GPI[2]/SPD	I/PU	113	Read register offset 17h bit 6 value reflects this input value.
GPI[1]/DPX	I/PU	106	When MII port is selected. Read register offset 17h bit 5 value reflects this input value. When SPP port is selected. The pin is defined as PE.
GPI[0]/LINK	I/PU	103	When MII port is selected. Read register offset 17h bit 4 value reflects this input value. When SPP port is selected. The pin is defined as SLCT.
GPO[0]	O	120	Default “1”. The pin reflects write register offset 17h bit 0 inverted value.

Tab - 7 General Purposes I/O pins group

2.8 Miscellaneous pins group

SIGNAL	TYPE	PIN NO.	DESCRIPTION
LCLK/XTALIN	I	79	CMOS Local Clock : A 25Mhz clock, +/- 100 PPM, 40%-60% duty cycle. The signal not supports 5 Volts tolerance. Crystal Oscillator Input : A 25Mhz crystal, +/- 30 PPM can be connected across XTALIN and XTALOUT.
XTALOUT	O	80	Crystal Oscillator Output : A 25Mhz crystal, +/- 30 PPM can be connected across XTALIN and XTALOUT. If a single-ended external clock (LCLK) is connected to XTALIN, the crystal output pin should be left floating.
CLKO25M	O	44	Clock Output : This clock is source from LCLK/XTALIN.
RESET	I/PU	3	Reset : Reset is active high then place AX88796 into reset mode immediately. During the falling edge the AX88796 loads the power on setting data.
CPU[1:0]	I/PU	59, 58	CPU type selection: CPU[1] CPU[0] CPU TYPE 0 0 ISA BUS 0 1 80186 1 0 MC68K 1 1 MCS-51 (805X)
IO_BASE[2:1] IO_BASE[0]	I/PU I/PD	119, 118, 117	I/O Base Address Selection: IO_BASE[2] IO_BASE[1] IO_BASE[0] IO_BASE 0 0 0 300h 0 0 1 320h 0 1 0 340h 0 1 1 360h 1 0 0 380h 1 0 1 3A0h 1 1 0 200h(default) 1 1 1 220h
I_OP	I/PU	116	LED Indicator Option : Selection of LED display mode. I_OP = 0: I_LK/ACT, I_SPEED and I_FULL/COL LED display mode. I_OP = 1: I_LINK, I_SPEED and I_ACT LED display mode. (default)
TEST[2:1]	I/PD	47, 65	Test Pins **:** Active high These pins are just for test mode setting purpose only. Must be pull down or keep no connection when normal operation.
IDDQ	I	46	For test only. Must be pulled down at normal operation.
BIST	I/PD	45	For test only. Must be pulled down or keep no connection when normal operation.
ZVREG	O	92	This sets the common mode voltage for 10Base-T and 100Base-TX modes. It should be connected to the center tap of the transmit side of the transformer
NC	N/A	17, 20, 21, 64, 122, 124, 125	No Connection : for manufacturing test only.
VDD	P	13, 27, 40, 53, 57, 104, 114, 126	Power Supply : +3.3V DC.
VSS	P	14, 28, 34, 43, 52, 54, 63, 94, 105,115, 127	Power Supply : +0V DC or Ground Power.
VDDA	P	56, 69,	Power Supply for Analog Circuit: +3.3V DC.

		73, 82	
VSSA	P	55, 68, 72, 75, 85,	Power Supply for Analog Circuit: +0V DC or Ground Power.
VDDM	P	76	Powers the analog block around the transmit/receive area. This should be connected to VDDA: +3.3V DC.
VSSM	P	77, 93	Powers the analog block around the transmit/receive area. This should be connected to VSSA: +0V DC or Ground Power.
VDDPD	P	78	The Phase Detector (or PLL) power. This should be isolated with other power: +3.3V DC.
VSSPD	P	81	The Phase Detector (or PLL) power. This should be isolated with other power: +0V DC or Ground.
VDDO	P	91	Power Supply for Transceiver Output Driver: +3.3V DC.
VSSO	P	86, 89, 90	Power Supply for Transceiver Output Driver: +0V DC or Ground.

Tab - 8 Miscellaneous pins group

2.9 Power on configuration setup signals cross reference table

Signal Name	Share with	Description
/SPP_SET	MDC	Standard Printer Port Selection: /SPP_SET = 0 : Standard Printer Port or GPIO is selected /SPP_SET = 1 : MII port is selected (default)

Tab - 9 Power on Configuration Setup Table

3.0 Memory and I/O Mapping

There are three memories or I/O mapping used in AX88796.

1. EEPROM Memory Mapping
2. I/O Mapping
3. Local Memory Mapping

3.1 EEPROM Memory Mapping

User can define by them and can access via I/O address offset 14H MII/EEPROM registers.
The contants of EEPROM will not be loading to any registers automaticlly.

3.2 I/O Mapping

SYSTEM I/O OFFSET	FUNCTION
0000H 001FH	MAC CORE REGISTER

Tab - 10 I/O Address Mapping

3.3 SRAM Memory Mapping

OFFSET	FUNCTION
0000H 3FFFH	RESERVED
4000H 7FFF	NE2000 COMPATABLE MODE 8K X 16 SRAM BUFFER
8000H FFFFH	RESERVED

Tab - 11 Local Memory Mapping

4.0 Basic Operation

4.1 Receiver Filtering

The address filtering logic compares the Destination Address Field (first 6 bytes of the received packet) to the Physical address registers stored in the Address Register Array. If any one of the six bytes does not match the pre-programmed physical address, the Protocol Control Logic rejects the packet. This is for unicast address filtering. All multicast destination addresses are filtered using a hashing algorithm. (See following description.) If the multicast address indexes a bit that has been set in the filter bit array of the Multicast Address Register Array the packet is accepted, otherwise it is rejected by the Protocol Control Logic. Each destination address is also checked for all 1's which is the reserved broadcast address.

4.1.1 Unicast Address Match Filter

The physical address registers are used to compare the destination address of incoming packets for rejecting or accepting packets. Comparisons are performed on a byte wide basis. The bit assignment shown below relates the sequence in PAR0-PAR5 to the bit sequence of the received packet.

	D7	D6	D5	D4	D3	D2	D1	D0
PAR0	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
PAR1	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
PAR2	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16
PAR3	DA31	DA30	DA29	DA28	DA27	DA26	DA25	DA24
PAR4	DA39	DA38	DA37	DA36	DA35	DA34	DA33	DA32
PAR5	DA47	DA46	DA45	DA44	DA43	DA42	DA41	DA40

Note: The bit sequence of the received packet is DA0, DA1, … DA7, DA8 ….

4.1.2 Multicast Address Match Filter

The Multicast Address Registers provide filtering of multicast addresses hashed by the CRC logic. All destination addresses are fed through the 32 bits CRC generation logic and as the last bit of the destination address enters the CRC, the 6 most significant bits of the CRC generator are latched. These 6 bits are then decoded by a 1 of 64 decode to index a unique filter bit (FB0-63) in the Multicast Address Registers. If the filter bit selected is set, the multicast packet is accepted. The system designer would use a program to determine which filter bits to set in the multicast registers. All multicast filter bits that correspond to Multicast Address Registers accepted by the node are then set to one. To accept all multicast packets all of the registers are set to all ones.

	D7	D6	D5	D4	D3	D2	D1	D0
MAR0	FB7	FB6	FB5	FB4	FB3	FB2	FB1	FB0
MAR1	FB15	FB14	FB13	FB12	FB11	FB10	FB9	FB8
MAR2	FB23	FB22	FB21	FB20	FB19	FB18	FB17	FB16
MAR3	FB31	FB30	FB29	FB28	FB27	FB26	FB25	FB24
MAR4	FB39	FB38	FB37	FB36	FB35	FB34	FB33	FB32
MAR5	FB47	FB46	FB45	FB44	FB43	FB42	FB41	FB40
MAR6	FB55	FB54	FB53	FB52	FB51	FB50	FB49	FB48
MAR7	FB63	FB62	FB61	FB60	FB59	FB58	FB57	FB56

If address Y is found to hash to the value 32 (20H), then FB32 in MAR2 should be initialized to ``1". This will cause the AX88796 to accept any multicast packet with the address Y.
Although the hashing algorithm does not guarantee perfect filtering of multicast address, it will perfectly filter up to 64 logical address filteres if these addresses are chosen to map into unique locations in the multicast filter.

Note: The first bit of received packet sequence is 1's stands by Multicast Address.

4.1.3 Broadcast Address Match Filter

The Broadcast check logic compares the Destination Address Field (first 6 bytes of the received packet) to all 1's, that is the values are "FF FF FF FF FF FF FF" in Hex format. If any bit of the six bytes does not equal to 1's, the Protocol Control Logic rejects the packet.

4.1.4 Aggregate Address Filter with Receive Configuration Setup

The final address filter decision depands on the destination address types, identified by the above 3 address match filters, and the setup of parameters of Receive Configuration Register.

Definitions of address match filter result are as following:

Signal	Value	Description
Phy	=1	Unicast Address Match
	=0	Unicast Address not Match
Mul	=1	Multicast Address Match
	=0	Multicast Address not Match
Bro	=1	Brocast Address Match
	=0	Brocast Address not Match
AGG	=1	Aggregate Address Match
	=0	Aggregate Address not Match

The meaning of AB, AM and PRO signals, please refer to "Receive Configuration Register"

Aggregate Address Filter function will be:

4.2 Buffer Management Operation

There are four buffer memory access types used in AX88796.

1. Packet Reception (Write data to memory from MAC)
2. Packet Transmision (Read data from memory to MAC)
3. Filling Packets to Transmit Buffer (Host fill data to memory)
4. Removing Packets from the Receive Buffer Ring (Host read data from memory)

The type 1 and 2 operations act as Local DMA. Type 1 does Local DMA write operation and type 2 does Local DMA read operation. The type 3 and 4 operations act as Remote DMA. Type 3 does Remote DMA write operation and type 4 does Remote DMA read operation.

4.2.1 Packet Reception

The Local DMA receive channel uses a Buffer Ring Structure comprised of a series of contiguous fixed length 256 byte (128 word) buffers for storage of received packets. The location of the Receive Buffer Ring is programmed in two registers, a Page Start and a Page Stop Register. Ethernet packets consist of minimum packet size (64 bytes) to maximum packet size (1522 bytes), the 256 byte buffer length provides a good compromise between short packets and longer packets to most efficiently use memory. In addition these buffers provide memory resources for storage of back-to-back packets in loaded networks. The assignment of buffers for storing packets is controlled by Buffer Management Logic in the AX88796. The Buffer Management Logic provides three basic functions: linking receive buffers for long packets, recovery of buffers when a packet is rejected, and recirculation of buffer pages that have been read by the host.

At initialization, a portion of the 16k byte (or 8k word) address space is reserved for the receiver buffer ring. Two eight bit registers, the Page Start Address Register (PSTART) and the Page Stop Address Register (PSTOP) define the physical boundaries of where the buffers reside. The AX88796 treats the list of buffers as a logical ring; whenever the DMA address reaches the Page Stop Address, the DMA is reset to the Page Start Address.

Fig - 8 Receive Buffer Ring

INITIALIZATION OF THE BUFFER RING

Two static registers and two working registers control the operation of the Buffer Ring. These are the Page Start Register, Page Stop Register (both described previously), the Current Page Register and the Boundary Pointer Register. The Current Page Register points to the first buffer used to store a packet and is used to restore the DMA for writing status to the Buffer Ring or for restoring the DMA address in the event of a Runt packet, a CRC, or Frame Alignment error. The Boundary Register points to the first packet in the Ring not yet read by the host. If the local DMA address ever reaches the Boundary, reception is aborted. The Boundary Pointer is also used to initialize the Remote DMA for removing a packet and is advanced when a packet is removed. A simple analogy to remember the function of these registers is that the Current Page Register acts as a Write Pointer and the Boundary Pointer acts as a Read Pointer.

Fig - 9 Receive Buffer Ring At Initialization

BEGINNING OF RECEPTION

When the first packet begins arriving the AX88796 and begins storing the packet at the location pointed to by the Current Page Register. An offset of 4 bytes is reserved in this first buffer to allow room for storing receive status corresponding to this packet.

LINKING RECEIVE BUFFER PAGES

If the length of the packet exhausts the first 256 bytes buffer, the DMA performs a forward link to the next buffer to store the remainder of the packet. For a maximal length packet the buffer logic will link six buffers to store the entire packet. Buffers cannot be skipped when linking, a packet will always be stored in contiguous buffers. Before the next buffer can be linked, the Buffer Management Logic performs two comparisons. The first comparison tests for equality between the DMA address of the next buffer and the contents of the Page Stop Register. If the buffer address equals the Page Stop Register, the buffer management logic will restore the DMA to the first buffer in the Receive Buffer Ring value programmed in the Page Start Address Register. The second comparison test for equality between the DMA address of the next buffer address and the contents of the Boundary Pointer Register. If the two values are equal the reception is aborted. The Boundary Pointer Register can be used to protect against overwriting any area in the receive buffer ring that has not yet been read. When linking buffers, buffer management will never cross this pointer, effectively avoiding any overwrites. If the buffer address does not match either the Boundary Pointer or Page Stop Address, the link to the next buffer is performed.

LINKING BUFFERS

Before the DMA can enter the next contiguous 256 bytes buffer, the address is checked for equality to PSTOP and to the Boundary Pointer. If neither are reached, the DMA is allowed to use the next buffer.

BUFFER RING OVERFLOW

If the Buffer Ring has been filled and the DMA reaches the Boundary Pointer Address, reception of the incoming packet will be aborted by the AX88796. Thus, the packets previously received and still contained in the Ring will not be destroyed. In a heavily loaded network environment the local DMA may be disabled, preventing the AX88796 from buffering packets from the network. To guarantee this will not happen, a software reset must be issued during all Receive Buffer Ring over flows (indicated by the OVW bit in the Interrupt Status Register). The following procedure is required to recover from a Receiver Buffer Ring Overflow. If this routine is not adhered to, the AX88796 may act in an unpredictable manner. It should also be noted that it is not permissible to service an overflow interrupt by continuing to empty packets from the receive buffer without implementing the prescribed overflow routine.

Note: It is necessary to define a variable in the driver, which will be called ``Resend".

1. Read and store the value of the TXP bit in the AX88796's Command Register.
2. Issue the STOP command to the AX88796. This is accomplished be setting the STP bit in the AX88796's Command Register. Writing 21H to the Command Register will stop the AX88796.
3. Wait for at least 1.5 ms. Since the AX88796 will complete any transmission or reception that is in progress, it is necessary to time out for the maximum possible duration of an Ethernet transmission or reception. By waiting 1.5 ms this is achieved with some guard band added. Previously, it was recommended that the RST bit of the Interrupt Status Register be polled to insure that the pending transmission or reception is completed. This bit is not a reliable indicator and subsequently should be ignored.
4. Clear the AX88796's Remote Byte Count registers (RBCR0 and RBCR1).
5. Read the stored value of the TXP bit from step 1, above. If this value is a 0, set the ``Resend" variable to a 0 and jump to step 6. If this value is a 1, read the AX88796's Interrupt Status Register. If either the Packet Transmitted bit (PTX) or Transmit Error bit (TXE) is set to a 1, set the ``Resend" variable to a 0 and jump to step 6. If neither of these bits is set, place a 1 in the ``Resend" variable and jump to step 6. This step determines if there was a transmission in progress when the stop command was issued in step 2. If there was a transmission in progress, the AX88796's ISR is read to determine whether or not the packet was recognized by the AX88796. If neither the PTX nor TXE bit was set, then the packet will essentially be lost and retransmitted only after a time-out takes place in the upper level software. By determining that the packet was lost at the driver level, a transmit command can be reissued to the AX88796 once the overflow routine is completed (as in step 11). Also, it is possible for the AX88796 to defer indefinitely, when it is stopped on a busy network. Step 5 also alleviates this problem. Step 5 is essential and should not be omitted

from the overflow routine, in order for the AX88796 to operate correctly.

6. Place the AX88796 in mode 1 loopback. This can be accomplished by setting bits D2 and D1, of the Transmit Configuration Register to ``0,1''.
7. Issue the START command to the AX88796. This can be accomplished by writing 22H to the Command Register. This is necessary to activate the AX88796's Remote DMA channel.
8. Remove one or more packets from the receive bufferring.
9. Reset the overwrite warning (OVW, overflow) bit in the Interrupt Status Register.
10. Take the AX88796 out of loopback. This is done by writing the Transmit Configuration Register with the value it contains during normal operation. (Bits D2 and D1 should both be programmed to 0.)
11. If the ``Resend'' variable is set to a 1, reset the ``Resend'' variable and reissue the transmit command. This is done by writing a value of 26H to the Command Register. If the ``Resend'' variable is 0, nothing needs to bedone.

END OF PACKET OPERATIONS

At the end of the packet the AX88796 determines whether the received packet is to be accepted or rejected. It either branches to a routine to store the Buffer Header or to another routine that recovers the buffers used to store the packet.

SUCCESSFUL RECEPTION

If the packet is successfully received as shown, the DMA is restored to the first buffer used to store the packet (pointed to by the Current Page Register). The DMA then stores the Receive Status, a Pointer to where the next packet will be stored and the number of received bytes. Note that the remaining bytes in the last buffer are discarded and reception of the next packet begins on the next empty 256 byte buffer boundary. The Current Page Register is then initialized to the next available buffer in the Buffer Ring. (The location of the next buffer had been previously calculated and temporarily stored in an internal scratchpad register.)

BUFFER RECOVERY FOR REJECTED PACKETS

If the packet is a runt packet or contains CRC or Frame Alignment errors, it is rejected. The buffer management logic resets the DMA back to the first buffer page used to store the packet (pointed to by CPR), recovering all buffers that had been used to store the rejected packet. This operation will not be performed if the AX88796 is programmed to accept either runt packets or packets with CRC or Frame Alignment errors. The received CRC is always stored in buffer memory after the last byte of received data for the packet.

Error Recovery

If the packet is rejected as shown, the DMA is restored by the AX88796 by reprogramming the DMA starting address pointed to by the Current Page Register.

4.2.2 Packet Transmision

The Local DMA Read is also used during transmission of a packet. Three registers control the DMA transfer during transmission, a Transmit Page Start Address Register (TPSR) and the Transmit Byte Count Registers (TBCR0,1). When the AX88796 receives a command to transmit the packet pointed to by these registers, buffer memory data will be moved into the FIFO as required during transmission. The AX88796 Controller will generate and append the preamble, synch and CRC fields.

TRANSMIT PACKET ASSEMBLY

The AX88796 requires a contiguous assembled packet with the format shown. The transmit byte count includes the Destination Address, Source Address, Length Field and Data. It does not include preamble and CRC. When transmitting data smaller than 46 bytes, the packet must be padded to a minimum size of 64 bytes. The programmer is responsible for adding and stripping pad bytes. The packets are placed in the buffer RAM by the system. System programs the AX88796 Core's Remote DMA to move the data from the data port to the RAM handshaking with system transfers loading the I/O data port.

The data transfer must be 16 bits (1 word) when in 16-bit mode, and 8 bits when the AX88796 Controller is set in 8-bit mode. The data width is selected by setting the WTS bit in the Data Configuration Register and setting the CPU[1:0] pins for ISA, 80186 or MC68K mode.

Destination Address	6 Bytes
Source Address	6 Bytes
Length / Type	2 Bytes
Data (Pad if < 46 Bytes)	46 Bytes Min.

General Transmit Packet Format

TRANSMISSION

Prior to transmission, the TPSR (Transmit Page Start Register) and TBCR0, TBCR1 (Transmit Byte Count Registers) must be initialized. To initiate transmission of the packet the TXP bit in the Command Register is set. The Transmit Status Register (TSR) is cleared and the AX88796 begins to prefetch transmit data from memory. If the Interpacket Gap (IPG) has timed out the AX88796 will begin transmission.

CONDITIONS REQUIRED TO BEGIN TRANSMISSION

In order to transmit a packet, the following three conditions must be met:
1. The Interpacket Gap Timer has timed out
2. At least one byte has entered the FIFO. (This indicates that the burst transfer has been started)
3. If a collision had been detected then before transmission the packet backoff time must have timed out.

COLLISION RECOVERY

During transmission, the Buffer Management logic monitors the transmit circuitry to determine if a collision has occurred. If a collision is detected, the Buffer Management logic will reset the FIFO and restore the Transmit DMA pointers for retransmission of the packet. The COL bit will be set in the TSR and the NCR (Number of Collisions Register) will be incremented. If 15 retransmissions each result in a collision the transmission will be aborted and the ABT bit in the TSR will be set.

Transmit Packet Assembly Format

The following diagrams describe the format for how packets must be assembled prior to transmission for different byte ordering schemes. The various formats are selected in the Data Configuration Register and setting the CPU[1:0] pins for ISA, 80186, MC68K or MCS-51 mode.

D15 D8	D7 D0
Destination Address 1	Destination Address 0
Destination Address 3	Destination Address 2
Destination Address 5	Destination Address 4

Source Address 1	Source Address 0
Source Address 3	Source Address 2
Source Address 5	Source Address 4
Type / Length 1	Type / Length 0
Data 1	Data 0
…	…

BOS = 0, WTS = 1 in Data Configuration Register.
This format is used with ISA or 80186 Mode.

D15 D8	D7 D0
Destination Address 0	Destination Address 1
Destination Address 2	Destination Address 3
Destination Address 4	Destination Address 5
Source Address 0	Source Address 1
Source Address 2	Source Address 3
Source Address 4	Source Address 5
Type / Length 0	Type / Length 1
Data 0	Data 1
…	…

BOS = 1, WTS = 1 in Data Configuration Register.
This format is used with MC68K Mode.

D7 D0
Destination Address 0 (DA0)
Destination Address 1 (DA1)
Destination Address 2 (DA2)
Destination Address 3 (DA3)
Destination Address 4 (DA4)
Destination Address 5 (DA5)
Source Address 0 (SA0)
Source Address 1 (SA1)
Source Address 2 (SA2)
Source Address 3 (SA3)
Source Address 4 (SA4)
Source Address 5 (SA5)
Type / Length 0
Type / Length 1
Data 0
Data 1
…

BOS = 0, WTS = 0 in Data Configuration Register.
This format is used with ISA, 80186 or MCS-51 Mode.

Note: All examples above will result in a transmission of a packet in order of DA0 (Destination Address 0), DA1, DA2, DA3 . . . in byte. Bits within each byte will be transmitted least significant bit first.

4.2.3 Filling Packet to Transmit Buffer (Host fill data to memory)

The Remote DMA channel is used to both assemble packets for transmission, and to remove received packets from the Receive Buffer Ring. It may also be used as a general purpose slave DMA channel for moving blocks

of data or commands between host memory and local buffer memory. There are two modes of operation, Remote Write and Remote Read Packet.

Two register pairs are used to control the Remote DMA, a Remote Start Address (RSAR0, RSAR1) and a Remote Byte Count (RBCR0, RBCR1) register pair. The Start Address Register pair points to the beginning of the block to be moved while the Byte Count Register pair is used to indicate the number of bytes to be transferred. Full handshake logic is provided to move data between local buffer memory (Embedded Memory) and a bidirectional I/O port.

REMOTE WRITE

A Remote Write transfer is used to move a block of data from the host into local buffer memory. The Remote DMA will read data from the I/O port and sequentially write it to local buffer memory beginning at the Remote Start Address. The DMA Address will be incremented and the Byte Counter will be decremented after each transfer. The DMA is terminated when the Remote Byte Count Register reaches a count of zero.

4.2.4 Removing Packets from the Ring (Host read data from memory)

REMOTE READ

A Remote Read transfer is used to move a block of data from local buffer memory to the host. The Remote DMA will sequentially read data from the local buffer memory, beginning at the Remote Start Address, and write data to the I/O port. The DMA Address will be incremented and the Byte Counter will be decremented after each transfer. The DMA is terminated when the Remote Byte Count Register reaches zero.

Packets are removed from the ring using the Remote DMA or an external device. When using the Remote DMA. The Boundary Pointer can also be moved manually by programming the Boundary Register. Care should be taken to keep the Boundary Pointer at least one buffer behind the Current Page Pointer. The following is a suggested method for maintaining the Receive Buffer Ring pointers.

1. At initialization, set up a software variable (next_pkt) to indicate where the next packet will be read. At the beginning of each Remote Read DMA operation, the value of next_pkt will be loaded into RSAR0 and RSAR1.
2. When initializing the AX88796 set:
   BNRY = PSTART
   CPR = PSTART + 1
   Next_pkt = PSTART + 1
3. After a packet is DMAed from the Receive Buffer Ring, the Next Page Pointer (second byte in AX88796 receive packet buffer header) is used to update BNRY and next_pkt.
   Next_pkt = Next Page Pointer
   BNRY = Next Page Pointer - 1
   If BNRY < PSTART then BNRY = PSTOP – 1

Note the size of the Receive Buffer Ring is reduced by one 256-byte buffer; this will not, however, impede the operation of the AX88796. The advantage of this scheme is that it easily differentiates between buffer full and buffer empty: it is full if BNRY = CPR; empty when BNRY = CPR-1.

STORAGE FORMAT FOR RECEIVED PACKETS

The following diagrams describe the format for how received packets are placed into memory by the local DMA channel. These modes are selected in the Data Configuration Register and setting the CPU[1:0] pins for ISA, 80186, MC68K or MCS-51 mode.

D15 D8	D7 D0
Next Packet Pointer	Receive Status
Receive Byte Count 1	Receive Byte Count 0
Destination Address 1	Destination Address 0
Destination Address 3	Destination Address 2
Destination Address 5	Destination Address 4
Source Address 1	Source Address 0
Source Address 3	Source Address 2
Source Address 5	Source Address 4
Type / Length 1	Type / Length 0
Data 1	Data 0
…	…

BOS = 0, WTS = 1 in Data Configuration Register.
This format is used with ISA or 80186 Mode.

D15 D8	D7 D0
Receive Status	Next Packet Pointer
Receive Byte Count 0	Receive Byte Count 1
Destination Address 0	Destination Address 1
Destination Address 2	Destination Address 3
Destination Address 4	Destination Address 5
Source Address 0	Source Address 1
Source Address 2	Source Address 3
Source Address 4	Source Address 5
Type / Length 0	Type / Length 1
Data 0	Data 1
…	…

BOS = 1, WTS = 1 in Data Configuration Register.
This format is used with MC68K Mode.

D7 D0
Receive Status
Next Packet Pointer
Receive Byte Count 0
Receive Byte Count 1
Destination Address 0
Destination Address 1
Destination Address 2
Destination Address 3
Destination Address 4
Destination Address 5
Source Address 0
Source Address 1
Source Address 2
Source Address 3
Source Address 4
Source Address 5
Type / Length 0
Type / Length 1
Data 0
Data 1
…

BOS = 0, WTS = 0 in Data Configuration Register.
This format is used with ISA, 80186 or MCS-51 Mode.

4.2.5 Other Useful Operations

MEMORY DIAGNOSTICS

Memory diagnostics can be achieved by Remote Write/Read DMA operations. The following is a suggested step for memory test and assume the AX88796 has been well initilized.

1. Issue the STOP command to the AX88796. This is accomplished be setting the STP bit in the AX88796's Command Register. Writing 21H to the Command Register will stop the AX88796.
2. Wait for at least 1.5 ms. Since the AX88796 will complete any reception that is in progress, it is necessary to time out for the maximum possible duration of an Ethernet reception. This action prevents buffer memory from written data through Local DMA Write.
3. Write data pattern to MUT (memory under test) by Remote DMA write operation.
4. Read data pattern from MUT (memory under test) by Remote DMA read operation.
5. Compare the read data pattern with original write data pattern and check if it is equal.
6. Repeat step 3 to step 5 with various data pattern.

LOOPBACK DIAGNOSTICS

1. Issue the STOP command to the AX88796. This is accomplished be setting the STP bit in the AX88796's Command Register. Writing 21H to the Command Register will stop the AX88796.
2. Wait for at least 1.5 ms. Since the AX88796 will complete any reception that is in progress, it is necessary to time out for the maximum possible duration of an Ethernet reception. This action prevents buffer memory from written data through Local DMA Write.
3. Place the AX88796 in mode 1 loopback. (MAC internal loopback) This can be accomplished by setting bits D2 and D1, of the Transmit Configuration Register to ``0,1".
4. Issue the START command to the AX88796. This can be accomplished by writing 22H to the Command Register. This is necessary to activate the AX88796's Remote DMA channel.
5. Write data that want to transmit to transmit buffer by Remote DMA write operation.
6. Issue the TXP command to the AX88796. This can be accomplished by writing 26H to the Command Register.
7. Read data current receive buffer by Remote DMA read operation.
8. Compare the received data with original transmit data and check if it is equal.
9. Repeat step 5 to step 8 for more packets test.

5.0 Registers Operation

5.1 MAC Core Registers

All registers of MAC Core are 8-bit wide and mapped into pages which are selected by PS (Page Select) in the Command Register.

PAGE 0 (PS1=0,PS0=0)

OFFSET	READ	WRITE
00H	Command Register (CR)	Command Register (CR)
01H	Page Start Register (PSTART)	Page Start Register (PSTART)
02H	Page Stop Register (PSTOP)	Page Stop Register (PSTOP)
03H	Boundary Pointer (BNRY)	Boundary Pointer (BNRY)
04H	Transmit Status Register (TSR)	Transmit Page Start Address (TPSR)
05H	Number of Collisions Register (NCR)	Transmit Byte Count Register 0 (TBCR0)
06H	Current Page Register (CPR)	Transmit Byte Count Register 1 (TBCR1)
07H	Interrupt Status Register (ISR)	Interrupt Status Register (ISR)
08H	Current Remote DMA Address 0 (CRDA0)	Remote Start Address Register 0 (RSAR0)
09H	Current Remote DMA Address 1 (CRDA1)	Remote Start Address Register 1 (RSAR1)
0AH	Reserved	Remote Byte Count 0 (RBCR0)
0BH	Reserved	Remote Byte Count 1 (RBCR1)
0CH	Receive Status Register (RSR)	Receive Configuration Register (RCR)
0DH	Reserved	Transmit Configuration Register (TCR)
0EH	Reserved	Data Configuration Register (DCR)
0FH	Reserved	Interrupt Mask Register (IMR)
10H, 11H	Data Port	Data Port
12H	IFGS1	IFGS1
13H	IFGS2	IFGS2
14H	MII/EEPROM Access	MII/EEPROM Access
15H	Test Register	Test Register
16H	Inter-frame Gap (IFG)	Inter-frame Gap (IFG)
17H	GPI	GPOC
18H - 1AH	Standard Printer Port (SPP)	Standard Printer Port (SPP)
1BH - 1EH	Reserved	Reserved
1FH	Reset	Reserved

Tab - 12 Page 0 of MAC Core Registers Mapping

PAGE 1 (PS1=0,PS0=1)

OFFSET	READ	WRITE
00H	Command Register (CR)	Command Register (CR)
01H	Physical Address Register 0 (PARA0)	Physical Address Register 0 (PAR0)
02H	Physical Address Register 1 (PARA1)	Physical Address Register 1 (PAR1)
03H	Physical Address Register 2 (PARA2)	Physical Address Register 2 (PAR2)
04H	Physical Address Register 3 (PARA3)	Physical Address Register 3 (PAR3)
05H	Physical Address Register 4 (PARA4)	Physical Address Register 4 (PAR4)
06H	Physical Address Register 5 (PARA5)	Physical Address Register 5 (PAR5)
07H	Current Page Register (CPR)	Current Page Register (CPR)
08H	Multicast Address Register 0 (MAR0)	Multicast Address Register 0 (MAR0)
09H	Multicast Address Register 1 (MAR1)	Multicast Address Register 1 (MAR1)
0AH	Multicast Address Register 2 (MAR2)	Multicast Address Register 2 (MAR2)
0BH	Multicast Address Register 3 (MAR3)	Multicast Address Register 3 (MAR3)
0CH	Multicast Address Register 4 (MAR4)	Multicast Address Register 4 (MAR4)
0DH	Multicast Address Register 5 (MAR5)	Multicast Address Register 5 (MAR5)
0EH	Multicast Address Register 6 (MAR6)	Multicast Address Register 6 (MAR6)
0FH	Multicast Address Register 7 (MAR7)	Multicast Address Register 7 (MAR7)
10H, 11H	Data Port	Data Port
12H	Inter-frame Gap Segment 1 IFGS1	Inter-frame Gap Segment 1 IFGS1
13H	Inter-frame Gap Segment 2 IFGS2	Inter-frame Gap Segment 2 IFGS2
14H	MII/EEPROM Access	MII/EEPROM Access
15H	Test Register	Test Register
16H	Inter-frame Gap (IFG)	Inter-frame Gap (IFG)
17H	GPI	GPOC
18H - 1AH	Standard Printer Port (SPP)	Standard Printer Port (SPP)
1BH - 1EH	Reserved	Reserved
1FH	Reset	Reserved

Tab - 13 Page 1 of MAC Core Registers Mapping

5.1.1 Command Register (CR) Offset 00H (Read/Write)

FIELD	NAME	DESCRIPTION
7:6	PS1,PS0	PS1,PS0 : Page Select The two bits selects which register page is to be accessed. PS1 PS0 0 0 page 0 0 1 page 1
5:3	RD2,RD1,RD0	RD2,RD1,RD0 : Remote DMA Command These three encoded bits control operation of the Remote DMA channel. RD2 could be set to abort any Remote DMA command in process. RD2 is reset by AX88796 when a Remote DMA has been completed. The Remote Byte Count should be cleared when a Remote DMA has been aborted. The Remote Start Address is not restored to the starting address if the Remote DMA is aborted. RD2 RD1 RD0 0 0 0 Not allowed 0 0 1 Remote Read 0 1 0 Remote Write 0 1 1 Not allowed 1 X X Abort / Complete Remote DMA
2	TXP	TXP : Transmit Packet This bit could be set to initiate transmission of a packet
1	START	START : This bit is used to active AX88796 operation.
0	STOP	STOP : Stop AX88796 This bit is used to stop the AX88796 operation.

5.1.2 Interrupt Status Register (ISR) Offset 07H (Read/Write)

FIELD	NAME	DESCRIPTION
7	RST	Reset Status : Set when AX88796 enters reset state and cleared when a start command is issued to the CR. NOTE: This bit does not generate an interrupt, it is merely a status indicator.
6	RDC	Remote DMA Complete Set when remote DMA operation has been completed This bit is cleared by writing a “1”.
5	CNT	Counter Overflow Set when MSB of one or more of the Tally Counters has been set. This bit is cleared by writing a “1”.
4	OVW	OVERWRITE : Set when receive buffer ring storage resources have been exhausted. This bit is cleared by writing a “1”.
3	TXE	Transmit Error Set when packet transmitted with one or more of the following errors ■ Excessive collisions ■ FIFO Underrun This bit is cleared by writing a “1”.
2	RXE	Receive Error Indicates that a packet was received with one or more of the following errors CRC error Frame Alignment Error FIFO Overrun Missed Packet This bit is cleared by writing a “1”.
1	PTX	Packet Transmitted Indicates packet transmitted with no error This bit is cleared by writing a “1”.
0	PRX	Packet Received Indicates packet received with no error. This bit is cleared by writing a “1”.

5.1.3 Interrupt mask register (IMR) Offset 0FH (Write)

FIELD	NAME	DESCRIPTION
7	-	Reserved
6	RDCE	DMA Complete Interrupt Enable. Default “low” disabled.
5	CNTE	Counter Overflow Interrupt Enable. Default “low” disabled.
4	OVWE	Overwrite Interrupt Enable. Default “low” disabled.
3	TXEE	Transmit Error Interrupt Enable. Default “low” disabled.
2	RXEE	Receive Error Interrupt Enable. Default “low” disabled.
1	PTXE	Packet Transmitted Interrupt Enable. Default “low” disabled.
0	PRXE	Packet Received Interrupt Enable. Default “low” disabled.

5.1.4 Data Configuration Register (DCR) Offset 0EH (Write)

FIELD	NAME	DESCRIPTION
7	RDCR	Remote DMA always completed
6:2	-	Reserved
1	-	Reserved
0	WTS	Word Transfer Select 0 : Selects byte-wide DMA transfers. 1 : Selects word-wide DMA transfers.

5.1.5 Transmit Configuration Register (TCR) Offset 0DH (Write)

FIELD	NAME	DESCRIPTION
7	FDU	Full Duplex : This bit indicates the current media mode is Full Duplex or not. 0 : Half duplex 1 : Full duplex
6	PD	Pad Disable 0 : Pad will be added when packet length less than 60. 1 : Pad will not be added when packet length less than 60.
5	RLO	Retry of late collision 0 : Don’t retransmit packet when late collision happens. 1 : Retransmit packet when late collision happens.
4:3	-	Reserved
2:1	LB1,LB0	Encoded Loop-back Control These encoded configuration bits set the type of loop-back that is to be performed. LB1 LB0 Mode 0 0 0 Normal operation Mode 1 0 1 Internal AX88796 loop-back Mode 2 1 0 PHYcevisor loop-back
0	CRC	Inhibit CRC 0 : CRC appended by transmitter. 1 : CRC inhibited by transmitter.

5.1.6 Transmit Status Register (TSR) Offset 04H (Read)

FIELD	NAME	DESCRIPTION
7	OWC	Out of window collision
6:4	-	Reserved
3	ABT	Transmit Aborted Indicates the AX88796 aborted transmission because of excessive collision.
2	COL	Transmit Collided Indicates that the transmission collided at least once with another station on the network.
1	-	Reserved
0	PTX	Packet Transmitted Indicates transmission without error.

5.1.7 Receive Configuration (RCR) Offset 0CH (Write)

FIELD	NAME	DESCRIPTION
7	-	Reserved
6	INTT	Interrupt Trigger Mode for ISA and 80186 modes 0 : Low active 1 : High active (default) Interrupt Trigger Mode for MCS-51 and MC68K modes 0 : High active 1 : Low active (default)
5	MON	Monitor Mode 0 : Normal Operation 1 : Monitor Mode, the input packet will be checked on NODE ADDRESS and CRC but not buffered into memory.
4	PRO	PRO : Promiscuous Mode Enable the receiver to accept all packets with a physical address.
3	AM	AM : Accept Multicast Enable the receiver to accept packets with a multicast address. That multicast address must pass the hashing array.
2	AB	AB : Accept Broadcast Enable the receiver to accept broadcast packet.
1	AR	AR : Accept Runt Enable the receiver to accept runt packet.
0	SEP	SEP : Save Error Packet Enable the receiver to accept and save packets with error.

5.1.8 Receive Status Register (RSR) Offset 0CH (Read)

FIELD	NAME	DESCRIPTION
7	-	Reserved
6	DIS	Receiver Disabled
5	PHY	Multicast Address Received.
4	MPA	Missed Packet
3	FO	FIFO Overrun
2	FAE	Frame alignment error.
1	CR	CRC error.
0	PRX	Packet Received Intact

5.1.9 Inter-frame gap (IFG) Offset 16H (Read/Write)

FIELD	NAME	DESCRIPTION
7	-	Reserved
6:0	IFG	Inter-frame Gap. Default value 15H.

5.1.10 Inter-frame gap Segment 1(IFGS1) Offset 12H (Read/Write)

FIELD	NAME	DESCRIPTION
7	-	Reserved
6:0	IFG	Inter-frame Gap Segment 1. Default value 0cH.

5.1.11 Inter-frame gap Segment 2(IFGS2) Offset 13H (Read/Write)

FIELD	NAME	DESCRIPTION
7	-	Reserved
6:0	IFG	Inter-frame Gap Segment 2. Default value 12H.

5.1.12 MII/EEPROM Management Register (MEMR) Offset 14H (Read/Write)

FIELD	NAME	DESCRIPTION
7	EECLK	EECLK: EEPROM Clock
6	EEO	EEO : (Read only) EEPROM Data Out value. That reflects Pin-48 EEDO value.
5	EEI	EEI EEPROM Data In. That output to Pin-49 EEDI as EEPROM data input value.
4	EECS	EECS EEPROM Chip Select
3	MDO	MDO MII Data Out. The value reflects to Pin-66 MDIO when MDIR=0.
2	MDI	MDI: (Read only) MII Data In. That reflects Pin-66 MDIO value.
1	MDIR	MII STA MDIO signal Direction MII Read Control Bit, asserts this bit let MDIO signal as the input signal. Deassert this bit let MDIO as output signal.
0	MDC	MDC MII Clock. This value reflects to Pin-67 MDC.

5.1.13 Test Register (TR) Offset 15H (Write)

FIELD	NAME	DESCRIPTION
7:5	-	Reserved
4	TF16T	Test for Collision, default value is logic 0 (User always keep the default value unchanged)
3	TPE	Test pin Enable, default value is logic 0 (User always keep the default value unchanged)
2:0	IFG	Select Test Pins Output, default value is logic 0 (User always keep the default value unchanged)

5.1.14 Test Register (TR) Offset 15H (Read)

FIELD	NAME	DESCRIPTION
7:4	-	Reserved
3	RST_TXB	100BASE-TX in Reset : This signal indicates that 100BASE-TX logic of internal PHY is in reset.
2	RST_10B	10BASE-T in Reset : This signal indicates that 10BASE-T logic of internal PHY is in reset.
1	RST_B	Reset Busy : This signal indicates that internal PHY is in reset.
0	AUTOD	Autonegotiation Done : This signal goes high whenever internal PHY autonegotiation has completed. It will go low if autonegotiation has to restart.

5.1.15 General Purpose Input Register (GPI) Offset 17H (Read)

FIELD	NAME	DESCRIPTION
7	-	Reserved
6	GPI2	This register reflects GPI[2] input value. May connect to external PHY speed status.
5	GPI1	This register reflects GPI[1] input value. May connect to external PHY duplex status.
4	GPI0	This register reflects GPI[0] input value. May connect to external PHY link status.
3	-	Reserved
2	I_SPD	This register reflects internal PHY speed status value. Logic one means 100Mbps
1	I_DPX	This register reflects internal PHY duplex status value. Logic one means full duplex.
0	I_LINK	This register reflects internal PHY link status value. Logic one means link ok.

5.1.16 GPO and Control (GPOC) Offset 17H (Write)

FIELD	NAME	DESCRIPTION
7	-	Reserved
6	PPDSET	Internal PHY Power Down Setting: Default “0”, Internal PHY is in normal operation mode Write PPDSET to “1” force Internal PHY into power down mode and MAC will also power down.
5	MPSET	Media Set by Program : The signal is valid only when MPSEL is set to high. When MPSET is logic 0 , internal PHY is selected. When MPSET is logic 1 , external MII PHY is selected.
4	MPSEL	Media Priority Select : MPSEL I_LINK GPI0 Media Selected 0 1 0 Internal PHY 0 1 1 Internal PHY 0 0 0 External MII PHY 0 0 1 Internal PHY 1 X X Depend on MPSET bit
3:1	-	Reserved
0	/GPO0	Default “0”. The register reflects to GPO[0] pin with inverted value.

5.1.17 SPP Data Port Register (SPP_DPR) Offset 18H (Read/Write)

FIELD	NAME	DESCRIPTION
7:0	DP	Printer Data Port. Default is in input mode. Write /DOE of SPP_CPR register to logic "0" to enable print data output to printer as bi-directional mode.

5.1.18 SPP Status Port Register (SPP_SPR) Offset 19H (Read)

FIELD	NAME	DESCRIPTION
7	/BUSY	Reading a '0' indicates that the printer is not ready to receive new data. The register reflects the **inverted** value of BUSY pin.
6	/ACK	Reading a '0' indicates that the printer has received the data and is ready to accept new data. The register reflects the value of /ACK pin.
5	PE	Reading a '1' indicates that the printer is out of paper. The register reflects the value of PE pin.
4	SLCT	Reading a '1' indicates that the printer has power on. The register reflects the value of SLCT pin.
3	/ERR	Reading a '0' indicates that there is an error condition at the printer. The register reflects the value of /ERR pin.
2:0	-	Reserved

5.1.19 SPP Command Port Register (SPP_CPR) Offset 1AH (Read/Write)

FIELD	NAME	DESCRIPTION
7:6	-	Reserved
5	/DOE	Setting to '0' enables print data output to printer. **Default sets to '1'.**
4	IRQEN	IRQ enable : printer port interrupt is **not supported**.
3	SLCTIN	Setting to '1' selects the printer. /SLIN pin reflects the **inverted** value of this signal.
2	/INIT	Setting to '0' initiates the printer /INIT pin reflects the value of this signal.
1	ATFD	Setting to '1' causes the printer to automatically feed one line after each line is printed. /ATFD pin reflects the **inverted** value of this signal.
0	STRB	Setting a low-high-low pulse on this register is used to strobe the print data into the printer. /STRB pin reflects the **inverted** value of this signal.

5.2 The Embedded PHY Registers

The MII management 16-bit register set implemented is as follows. And the following sub-section will describes each field of the registers. The format for the “FIELD” descriptions is as follows: the first number is the register number, the second number is the bit position in the register and the name of the instantiated pad is in capital letters. The format for the “TYPE” descriptions is as follows: R = read, W = write, LH = latch high, NA = not applicable.

ADDRESS	NAME	DESCRIPTION	DEFAULT(Hex Code)
0	MR0	Control	3000h
1	MR1	Status	7849h
2	MR2	PHY Identifier 1	0180h
3	MR3	PHY Identifier 2	BB10h
4	MR4	Autonegotiation Advertisement	01E1h
5	MR5	Autonegotiation Link Partner Ability	0000
6	MR6	Autonegotiation Expansion	0000
7	MR7	Next Page Transmit	0000
8 - 15	MR8 -15	(Reserved)	-
16	MR16	PCS Control Register	0000
17	MR17	Autonegotiation (read register A)	0000
18	MR18	Autonegotiation (read register B)	0000
19	MR19	Analog Test Register	-
20	MR20	User-defined Register	-
21	MR21	RXER Counter	0000
22 - 24	MR22 -24	Analog Test Registers	-
25 - 27	MR25 -27	Analog Test (tuner) Registers	-
28	MR28	Device Specific 1	-
29	MR29	Device Specific 2	2080
30	MR30	Device Specific 3	0000
31	MR31	Quick Status Register	-

Tab - 14 The Embedded PHY Registers

5.2.1 MR0 -- Control Register Bit Descriptions

FIELD	TYPE	DESCRIPTION
0.15 (SW_RESET)	R/W	**Reset.** Setting this bit to a 1 will reset the PHY. All registers will be set to their default state. This bit is self-clearing. The default is 0.
0.14 (LOOPBACK)	R/W	**Loopback.** When this bit is set to 1, no data transmission will take place on the media. Any receive data will be ignored. The loopback signal path will contain all circuitry up to, but not including, the PMD. The default value is a 0.
0.13(SPEED100)	R/W	**Speed Selection.** The value of this bit reflects the current speed of operation (1 = 100Mbits/s; 0 = 10Mbits/s). This bit will only affect operating speed when the autonegotiation enable bit (register 0, bit 12) is disabled (0). This bit is ignored when autonegotiation is enabled (register 0, bit 12). This bit is ANDed with the SPEED_PIN signal.
0.12 (NWAY_ENA)	R/W	**Autonegotiation Enable.** The autonegotiation process will be enabled by set-ting this bit to a 1. The default state is a 1.
0.11 (PWRDN)	R/W	**Powerdown.** The PHY may be placed in a low-power state by setting this bit to a 1, both the 10Mbits/s transceiver and the 100Mbits/s transceiver will be powered down. While in the power down state, the PHY will respond to management transactions. The default state is a 0.
0.10 (ISOLATE)	R/W	**Isolate.** When this bit is set to a 1, the MII outputs will be brought to the high-impedance state. The default state is a 0.
0.9 (REDONWAY)	R/W	**Restart Autonegotiation.** Normally, the autonegotiation process is started at powerup. The process may be restarted by setting this bit to a 1. The default state is a 0. The NWAYDONE bit (register 1, bit 5) is reset when this bit goes to a 1. This bit is self-cleared when autonegotiation restarts.
0.8 (FULL_DUP)	R/W	**Duplex Mode.** This bit reflects the mode of operation (1 = full duplex; 0 = half duplex). This bit is ignored when the autonegotiation enable bit (register 0, bit 12) is enabled. The default state is a 0. This bit is ORed with the F_DUP pin.
0.7 (COLTST)	R/W	**Collision Test.** When this bit is set to a 1, the PHY will assert the MCOL signal in response to MTX_EN.
0.6:0 (RESERVED)	NA	**Reserved.** All bits will read 0.

5.2.2 MR1 -- Status Register Bit Descriptions

FIELD	TYPE	DESCRIPTION
1.15 (T4ABLE)	R	**100Base-T4 Ability.** This bit will always be a 0. 0: Not able. 1: Able.
1.14 (TXFULDUP)	R	**100Base-TX Full-Duplex Ability.** This bit will always be a 1. 0: Not able. 1: Able.
1.13 (TXHAFDUP)	R	**100Base-TX Half-Duplex Ability.** This bit will always be a 1. 0: Not able. 1: Able.
1.12 (ENFULDUP)	R	**10Base-T Full-Duplex Ability.** This bit will always be a 1. 0: Not able. 1: Able.
1.11 (ENHAFDUP)	R	**10Base-T Half-Duplex Ability.** This bit will always be a 1. 0: Not able. 1: Able.
1.10:7 (RESERVED)	R	**Reserved.** All bits will read as a 0.
1.6 (NO_PA_OK)	R	**Suppress Preamble.** When this bit is set to a 1, it indicates that the PHY accepts management frames with the preamble suppressed.
1.5 (NWAYDONE)	R	**Autonegotiation Complete.** When this bit is a 1, it indicates the autonegotiation process has been completed. The contents of registers MR4, MR5, MR6, and MR7 are now valid. The default value is a 0. This bit is reset when autonegotiation is started.
1.4 (REM_FLT)	R	**Remote Fault.** When this bit is a 1, it indicates a remote fault has been detected. This bit will remain set until cleared by reading the register. The default is a 0.
1.3 (NWAYABLE)	R	**Autonegotiation Ability.** When this bit is a 1, it indicates the ability to perform autonegotiation. The value of this bit is always a 1.
1.2 (LSTAT_OK)	R	**Link Status.** When this bit is a 1, it indicates a valid link has been established. This bit has a latching function: a link failure will cause the bit to clear and stay cleared until it has been read via the management interface.
1.1 (JABBER)	R	**Jabber Detect.** This bit will be a 1 whenever a jabber condition is detected. It will remain set until it is read, and the jabber condition no longer exists.
1.0 (EXT_ABLE)	R	**Extended Capability.** This bit indicates that the PHY supports the extended register set (MR2 and beyond). It will always read a 1.

5.2.3 MR2, MR3 -- Identification Registers (1 and 2) Bit Descriptions

FIELD	TYPE	DESCRIPTION
2.15:0 (OUI[3:18])	R	**Organizationally Unique Identifier.** The third through the twenty-fourth bit of the OUI assigned to the PHY manufacturer by the IEEE are to be placed in bits. 2.15:0 and 3.15:10. This value is programmable.
3.15:10 (OUI[19:24])	R	**Organizationally Unique Identifier.** The remaining 6 bits of the OUI. The value for bits 24:19 is programmable.
3.9:4 (MODEL[5:0])	R	**Model Number.** 6-bit model number of the device. The model number is programmable.
3.3:0 (VERSION[3:0])	R	**Revision Number.** The value of the present revision number. The version number is programmable.

5.2.4 MR4 – Autonegotiation Advertisement Registers Bit Descriptions

FIELD	TYPE	DESCRIPTION
4.15 (NEXT_PAGE)	R/W	**Next Page.** The next page function is activated by setting this bit to a 1. This will allow the exchange of additional data. Data is carried by optional next pages of information.
4.14 (ACK)	R/W	**Acknowledge.** This bit is the acknowledge bit from the link code word.
4.13 (REM_FAULT)	R/W	**Remote Fault.** When set to 1, the PHY indicates to the link partner a remote fault condition.
4.12:10 (PAUSE)	R/W	**Pause.** When set to a 1, it indicates that the PHY wishes to exchange flow control information with its link partner.
4.9 (100BASET4)	R/W	**100Base-T4.** This bit should always be set to 0.
4.8 (100BASET_FD)	R/W	**100Base-TX Full Duplex.** If written to 1, autonegotiation will advertise that the PHY is capable of 100Base-TX full-duplex operation.
4.7 (100BASETX)	R/W	**100Base-TX.** If written to 1, autonegotiation will advertise that the PHY is capable of 100Base-TX operation.
4.6 (10BASET_FD)	R/W	**10Base-T Full Duplex.** If written to 1, autonegotiation will advertise that the PHY is capable of 10Base-T full-duplex operation.
4.5 (10BASET)	R/W	**10Base-T.** If written to 1, autonegotiation will advertise that the PHY is capable of 10Base-T operation.
4.4:0 (SELECT)	R/W	**Selector Field**. Reset with the value 00001 for IEEE 802.3.

5.2.5 MR5 – Autonegotiation Link Partner Ability (Base Page) Register Bit Descriptions

FIELD	TYPE	DESCRIPTION
5.15 (LP_NEXT_PAGE)	R	**Link Partner Next Page.** When this bit is set to 1, it indicates that the link partner wishes to engage in next page exchange.
5.14 (LP_ACK)	R	**Link Partner Acknowledge.** When this bit is set to 1, it indicates that the link partner has successfully received at least three consecutive and consistent FLP bursts.
5.13 (LP_REM_FAULT)	R	**Remote Fault.** When this bit is set to 1, it indicates that the link partner has a fault.
5.12:5 (LP_TECH_ABILITY)	R	**Technology Ability Field.** This field contains the technology ability of the link partner. These bits are similar to the bits defined for the MR4 register (see Table 16).
5.4:0 (LP_SELECT)	R	**Selector Field.** This field contains the type of message sent by the link partner. For IEEE 802.3 compliant link partners, this field should read 00001.

5.2.6 MR5 –Autonegotiation Link Partner(LP)Ability Register (Next Page)Bit Descriptions

FIELD	TYPE	DESCRIPTION
5.15 (LP_NEXT_PAGE)	R	**Next Page**. When this bit is set to logic 0, it indicates that this is the last page to be transmitted. Logic 1 indicates that additional pages will follow.
5.14 (LP_ACK)	R	**Acknowledge.** When this bit is set to a logic 1, it indicates that the link partner has successfully received its partner's link code word.
5.13 (LP__MES_PAGE)	R	**Message Page.** This bit is used by the NEXT _PAGE function to differentiate a message page (logic 1) from an unformatted page (logic 0).
5.12 (LP_ACK2)	R	**Acknowledge 2.** This bit is used by the NEXT_PAGE function to indicate that a device has the ability to comply with the message (logic 1) or not (logic 0).
5.11 (LP_TOGGLE)	R	**Toggle**. This bit is used by the arbitration function to ensure synchronization with the link partner during next page exchange. Logic 0 indicates that the previous value of the transmitted link code word was logic 1. Logic 1 indicates that the previous value of the transmitted link code word was logic 0.
5.10:0 (MCF)	R	**Message/Unformatted Code Field**. With these 11 bits, there are 2048 possible messages. Message code field definitions are described in annex 28C of the IEEE 802.3u standard.

5.2.7 MR6 – Autonegotiation Expansion Register Bit Descriptions

FIELD	TYPE	DESCRIPTION
6.15:5 (RESERVED)	R	**Reserved**.
6.4 (PAR_DET_FAULT)	R/LH	**Parallel Detection Fault.** When this bit is set to 1, it indicates that a fault has been detected in the parallel detection function. This fault is due to more than one technology detecting concurrent link conditions. This bit can only be cleared by reading this register.
6.3 (LP_NEXT_PAGE_ABLE)	R	**Link Partner Next Page Able.** When this bit is set to 1, it indicates that the link partner supports the next page function.
6.2 (NEXT_PAGE_ABLE)	R	**Next Page Able.** This bit is set to 1, indicating that this device supports the NEXT_PAGE function.
6.1 (PAGE_REC)	R/LH	**Page Received**. When this bit is set to 1, it indicates that a NEXT_PAGE has been received.
6.0 (LP_NWAY_ABLE)	R	**Link Partner Autonegotiation Capable.** When this bit is set to 1, it indicates that the link partner is autonegotiation capable.

5.2.8 MR7 –Next Page Transmit Register Bit Descriptions

FIELD	TYPE	DESCRIPTION
7.15 (NEXT_PAGE)	R/W	**Next Page.** This bit indicates whether or not this is the last next page to be transmitted. When this bit is 0, it indicates that this is the last page. When this bit is 1, it indicates there is an additional next page.
7.14 (ACK)	R	**Acknowledge.** This bit is the acknowledge bit from the link code word.
7.13 (MESSAGE)	R/W	**Message Page.** This bit is used to differentiate a message page from an unformatted page. When this bit is 0, it indicates an unformatted page. When this bit is 1, it indicates a formatted page.
7.12 (ACK2)	R/W	**Acknowledge 2.** This bit is used by the next page function to indicate that a device has the ability to comply with the message. It is set as follows: When this bit is 0, it indicates the device cannot comply with the message. When this bit is 1, it indicates the device will comply with the message.
7.11 (TOGGLE)	R	**Toggle.** This bit is used by the arbitration function to ensure synchronization with the link partner during next page exchange. This bit will always take the opposite value of the toggle bit in the previously exchanged link code word: If the bit is logic 0, the previous value of the transmitted link code word was logic 1. If the bit is a 1, the previous value of the transmitted link code word was a 0. The initial value of the toggle bit in the first next page transmitted is the inverse of the value of bit 11 in the base link code word, and may assume a value of 1 or 0.
7.10:0 (MCF)	R/W	**Message/Unformatted Code Field.** With these 11 bits, there are 2048 possible messages. Message code field definitions are described in annex 28C of the IEEE 802.3u standard.

5.2.9 MR16 – PCS Control Register Bit Descriptions

FIELD	TYPE	DESCRIPTION
16.15 (LOCKED)	R	**Locked.** Locked pin from descrambler block.
16.14-12 (UNUSED)	R	**Unused.** Will always be read back as 0.
16.11-4 (TESTBITS)	R/W	**Generic Test Bits.** These bits have no effect on the PCS block. They are for external use only. A 0 should be written to these bits.
16.3 (LOOPBACK)	R/W	**Loopback Configure.** When this bit is high, the entire loopback is performed in the PCS macro. When this bit is low, only the collision pin is disabled in loopback.
16.2 (SCAN)	R/W	**Scan Test Mode**.
16.1 (FORCE LOOPBACK)	R/W	**Force Loopback.** Force a loopback without forcing idle on the transmit side or disabling the collision pin.
16.0 (SPEEDUP COUNTERS)	R/W	**Speedup Counters.** Reduce link monitor counter to 10 us from 620 us. (Same as FASTTEST = 1.)

5.2.10 MR17 –Autonegotiation Register A Bit Descriptions

FIELD	TYPE	DESCRIPTION
17.15-13	R	**Reserved. Always 0.**
17.12	R	**Next Page Wait.**
17.11	R	**Wait Link_Fail_Inhibit_Wait_Timer (Link Status Check).**
17.10	R	**Wait Autoneg_Wait_Timer (Link Status Check).**
17.9	R	**Wait Break_Link_Timer (Transmit Disable).**
17.8	R	**Parallel Detection Fault.**
17.7	R	**Autonegotiation Enable.**
17.6	R	**FLP Link Good Check.**
17.5	R	**Complete Acknowledge.**
17.4	R	**Acknowledge Detect.**
17.3	R	**FLP Link Good.**
17.2	R	**Link Status Check.**
17.1	R	**Ability Detect.**
17.0	R	**Transmit Disable.**

5.2.11 MR18 –Autonegotiation Register B Bit Descriptions

FIELD	TYPE	DESCRIPTION
18.15	R	**Receiving FLPs**. Any of FLP Capture, Clock, Data_0, or Data_1 (FLP Rcv).
18.14	R	**FLP Pass** (FLP Rcv).
18.13	R	**Link Pulse Count** (FLP Rcv).
18.12	R	**Link Pulse Detect** (FLP Rcv).
18.11	R	**Test Pass** (NLP Rcv).
18.10	R	**Test Fail Count** (NLP Rcv).
18.9	R	**Test Fail Extend** (NLP Rcv).
18.8	R	**Wait Max Timer Ack** (NLP Rcv).
18.7	R	**Detect Freeze** (NLP Rcv).
18.6	R	**Test Fail** (NLP Rcv).
18.5	R	**Transmit Count Ack** (FLP Xmit).
18.4	R	**Transmit Data Bit** (FLP Xmit).
18.3	R	**Transmit Clock Bit** (FLP Xmit).
18.2	R	**Transmit ability** (FLP Xmit).
18.1	R	**Transmit Remaining Acknowledge** (FLP Xmit).
18.0	R	**Idle** (FLP Xmit).

5.2.12 MR20 –User Defined Register Bit Descriptions

FIELD	TYPE	DESCRIPTION
20.[15:0]	R/W	The data written into this user-defined register appears on the REG20_OUT[15:0] bus.

5.2.13 MR21 –RXER Counter Register Bit Descriptions

FIELD	TYPE	DESCRIPTION
21.0	W	This bit, when 0 puts this register in 16-bit counter mode. When 1, it puts this register in 8-bit counter mode. This bit is reset to a 0 and cannot be read.
21.15:0	R	When in 16-bit counter mode, these maintain a count of RXERs. It is reset on a read operation.
21.7:0	R	When in 8-bit counter mode, these maintain a count of RXERs. It is reset on a read operation
21.11:8	R	When in 8-bit mode, these contain a count of false carrier events (802.3 section 27.3.1.5.1). It is reset on a read operation.
21.15:12	R	When in 8-bit mode, these contain a count of disconnect events (Link Unstable 6, 802.3 section 27.3.1.5.1). It is reset on a read operation.

5.2.14 MR28 –Device-Specific Register 1 (Status Register) Bit Descriptions

FIELD	TYPE	DESCRIPTION
28.15:9 (UNUSED)	R	**Unused.** Read as 0.
28.8 (BAD_FRM)	R/LH	**Bad Frame.** If this bit is a 1, it indicates a packet has been received without an SFD. This bit is only valid in 10Mbits/s mode. This bit is latching high and will only clear after it has been read or the device has been reset.
28.7 (CODE)	R/LH	**Code Violation.** When this bit is a 1, it indicates a Manchester code violation has occurred. The error code will be output on the MRXD lines. Refer to Table 1 for a detailed description of the MRXD pin error codes. This bit is only valid in 10Mbits/s mode. This bit is latching high and will only clear after it has been read or the device has been reset.
28.6 (APS)	R	**Autopolarity Status.** When register 30, bit 3 is set and this bit is a 1, it indicates the PHY has detected and corrected a polarity reversal on the twisted pair. If the APF_EN bit (register 30, bit 3) is set, the reversal will be corrected inside the PHY. This bit is not valid in 100Mbits/s operation.
28.5 (DISCON)	R/LH	**Disconnect.** If this bit is a 1, it indicates a disconnect. This bit will latch high until read. This bit is only valid in 100Mbits/s mode.
28.4 (UNLOCKED)	R/LH	**Unlocked.** Indicates that the TX scrambler lost lock. This bit will latch high until read. This bit is only valid in 100Mbits/s mode.
28.3 (RXERR_ST)	R/LH	**RX Error Status.** Indicates a false carrier. This bit will latch high until read. This bit is only valid in 100Mbits/s mode.
28.2 (FRC_JAM)	R/LH	**Force Jam.** This bit will latch high until read. This bit is only valid in 100Mbits/s mode.
28.1 (LNK100UP)	R	**Link Up 100.** This bit, when set to a 1, indicates a 100Mbits/s transceiver is up and operational.
28.0 (LNK10UP)	R	**Link Up 10.** This bit, when set to a 1, indicates a 10Mbits/s transceiver is up and operational.

5.2.15 MR29 –Device-Specific Register 2 (100Mbps Control) Bit Descriptions

FIELD	TYPE	DESCRIPTION
29.15 (LOCALRST)	R/W	**Management Reset.** This is the local management reset bit. Writing logic 1 to this bit will cause the lower 16 registers and registers 28 and 29 to be reset to their default values. This bit is self-clearing.
29.14 (RST1)	R/W	**Generic Reset 1.** This register is used for manufacture test only.
29.13 (RST2)	R/W	**Generic Reset 2.** This register is used for manufacture test only.
29.12 (100_OFF)	R/W	**100Mbits/s Transmitter Off.** When this bit is set to 0, it forces TPI low and TPIN- high. This bit defaults to 1.
29.11 (LED_BLINK)	R/W	**LED Blinking.** This register, when 1, enables LED blinking. This is ORed with LED_BLINK_EN. Default is 0.
29.10 (CRS_SEL)	R/W	**Carrier Sense Select.** MCRS will be asserted on receive only when this bit is set to a 1. If this bit is set to logic 0, MCRS will by asserted on receive or transmit. This bit is ORed with the CRS_SEL pin.
29.9 (LINK_ERR)	R/W	**Link Error Indication.** When this bit is a 1, a link error code will be reported on MRXD[3:0] of the PHY when MRX_ER is asserted on the MII. The specific error codes are listed in the MRXD pin description. If it is 0, it will disable this function.
29.8 (PKT_ERR)	R/W	**Packet Error Indication Enable.** When this bit is a 1, a packet error code, which indicates that the scrambler is not locked, will be reported on MRXD[3:0] of the PHY when MRX_ER is asserted on the MII. When this bit is 0, it will disable this function.
29.7 (PULSE_STR)	R/W	**Pulse Stretching.** When this bit is set to 1, the CS, XS, and RS output signals will be stretched between approximately 42 ms - 84 ms. If this bit is 0, it will disable this feature. Default state is 0.
29.6 (EDB)	R/W	**Encoder/Decoder Bypass.** When this bit is set to 1, the 4B/5B-encoder and 5B/4B-decoder function will be disabled. This bit is ORed with the EDBT pin.
29.5 (SAB)	R/W	**Symbol Aligner Bypass.** When this bit is set to 1, the aligner function will be disabled.
29.4 (SDB)	R/W	**Scrambler/Descrambler Bypass.** When this bit is set to 1, the scrambling/ descrambling functions will be disabled. This bit is ORed with the SDBT pin.
29.3 (CARIN_EN)	R/W	**Carrier Integrity Enable.** When this bit is set to a 1, carrier integrity is enabled. This bit is ORed with the CARIN_EN pin.
29.2 (JAM_COL)	R/W	**Jam Enable.** When this bit is a 1, it enables JAM associated with carrier integrity to be ORed with MCOLMCRS.
29.1 (FEF-EN)	R/W	**Far-End Fault Enable**. This bit is used to enable the far-end fault detection and transmission capability. This capability may only be used if autonegotiation is disabled. This capability is to be used only with media which does not support autonegotiation. Setting this bit to 1 enables far-end fault detection, and logic 0 will disable the function. Default state is 0.
29.0 (FX)	R/W	**Fiber-Optic Mode.** When this bit is a 1, the PHY is in fiber-optic mode. This bit is ORed with FX_MODE.

5.2.16 MR30 –Device-Specific Register 3 (10Mbps Control) Bit Descriptions

FIELD	TYPE	DESCRIPTION
30.15 (Test10TX)	R/W	When high and 10Base-T is powered up, a continuous 10 MHz signal (1111) will be transmitted. This is only meant for testing. Default 0.
30.14 (RxPLLEn)	R/W	When high, all 10Base-T logic will be powered up when the link is up. Otherwise, portions of the logic will be powered down when no data is being received to conserve power. Default is 0.
30.13 (JAB_DIS)	R/W	**Jabber Disable.** When this bit is 1, disables the jabber function of the 10Base-T receive. Default is 0.
30.12:7 (UNUSED)	R/W	**Unused.** Read as 0.
30.6 (LITF_ENH)	R/W	**Enhanced Link Integrity Test Function.** When high, function is enabled. This is ORed with the LITF_ENH input. Default is 0.
30.5 (HBT_EN)	R/W	**Heartbeat Enable.** When this bit is a 1, the heartbeat function will be enabled. Valid in 10Mbits/s mode only.
30.4 (ELL_EN)	R/W	**Extended Line Length Enable.** When this bit is a 1, the receive squelch levels are reduced from a nominal 435 mV to 350 mV, allowing reception of signals with a lower amplitude. Valid in 10Mbits/s mode only.
30.3 (APF_EN)	R/W	**Autopolarity Function Disable.** When this bit is a 0 and the PHY is in 10 Mbits/s mode, the autopolarity function will determine if the TP link is wired with a polarity reversal. If there is a polarity reversal, the PHY will assert the APS bit (register 28, bit 6) and correct the polarity reversal. If this bit is a 1 and the device is in 10 Mbits/s mode, the reversal will not be corrected.
30.2 (RESERVED)	R/W	**Reserved**.
30.1 (SERIAL _SEL)	R/W	**Serial Select.** When this bit is set to a 1, 10Mbits/s serial mode will be selected. When the PHY is in 100Mbits/s mode, this bit will be ignored.
30.0 (ENA_NO_LP)	R/W	**No Link Pulse Mode.** Setting this bit to a 1 will allow 10Mbits/s operation with link pulses disabled. If the PHY is configured for 100Mbits/s operation, setting this bit will not affect operation.

5.2.17 MR31 –Device-Specific Register 4 (Quick Status) Bit Descriptions

FIELD	TYPE	DESCRIPTION
31.15 (ERROR)	R	**Receiver Error.** When this bit is a 1, it indicates that a receive error has been detected. This bit is valid in 100Mbits/s only. This bit will remain set until cleared by reading the register. Default is a 0.
31.14 (RXERR_ST)/(LINK_STAT_CHANGE)	R	**False Carrier.** When bit [31.7] is set to 0 and this bit is a 1, it indicates that the carrier detect state machine has found a false carrier. This bit is valid in 100Mbits/s only. This bit will remain set until cleared by reading the register. Default is 0. **Link Status Change.** When bit [31.7] is set to a 1, this bit is redefined to become the LINK_STAT_CHANGE bit and goes high whenever there is a change in link status (bit [31.11] changes state)
31.13 (REM_FLT)	R	**Remote Fault.** When this bit is a 1, it indicates a remote fault has been detected. This bit will remain set until cleared by reading the register. Default is a 0.
31.12 (UNLOCKED)/(JABBER)	R	**Unlocked/Jabber.** If this bit is set when operating in 100Mbits/s mode, it indicates that the TX descrambler has lost lock. If this bit is set when operating in 10Mbits/s mode, it indicates a jabber condition has been detected. This bit will remain set until cleared by reading the register.
31.11 (LSTAT_OK)	R	**Link Status.** When this bit is a 1, it indicates a valid link has been established. This bit has a latching low function: a link failure will cause the bit to clear and stay cleared until it has been read via the management interface.
31.10 (PAUSE)	R	**Link Partner Pause.** When this bit is set to a 1, it indicates that the LU3X54FTL wishes to exchange flow control information.
31.9 (SPEED100)	R	**Link Speed.** When this bit is set to a 1, it indicates that the link has negotiated to 100Mbits/s. When this bit is a 0, it indicates that the link is operating at 10Mbits/s.
31.8 (FULL_DUP)	R	**Duplex Mode.** When this bit is set to a 1, it indicates that the link has negotiated to full-duplex mode. When this bit is a 0, it indicates that the link has negotiated to half-duplex mode.
31.7 (INT_CONF)	R/W	**Interrupt Configuration.** When this bit is set to a 0, it defines bit [31.14] to be the RXERR_ST bit and the interrupt pin (MASK_STAT_INT) goes high whenever any of bits [31.15:12] go high, or bit [31.11] goes low. When this bit is set high, it redefines bit [31.14] to become the LINK_STAT_CHANGE bit, and the interrupt pin (MASK_STAT_INT) goes high only when the link status changes (bit [31.14] goes high). This bit defaults to 0.
31.6 (INT_MASK)	R/W	**Interrupt Mask.** When set high, no interrupt is generated by this channel under any condition. When set low, interrupts are generated according to bit [31.7].
31.5:3 (LOW_AUTO__STATE)	R	**Lowest Autonegotiation State.** These 3 bits report the state of the lowest autonegotiation state reached since the last register read, in the priority order defined below: 000: Autonegotiation enable. 001: Transmit disables or ability detects. 010: Link status check. 011: Acknowledge detects. 100: Complete acknowledges. 101: FLP link good check. 110: Next page wait. 111: FLP link good.
31.2:0 (HI_AUTO_STATE)	R	**Highest Autonegotiation State.** These 3 bits report the state of the highest autonegotiation state reached since the last register read, as defined above for bit [31.5:3].

6.0 CPU I/O Read and Write Functions

6.1 ISA bus type access functions.

ISA bus I/O Read function

Function Mode	/CS	/BHE	A0	/IORD	/IOWR	SD[15:8]	SD[7:0]
Standby Mode	H	X	X	X	X	High-Z	High-Z
Byte Access	L	H	L	L	H	Not Valid	Even-Byte
	L	H	H	L	H	Not Valid	Odd-Byte
Word Access	L	L	L	L	H	Odd-Byte	Even-Byte

ISA bus I/O Write function

Function Mode	/CS	/BHE	A0	/IORD	/IOWR	SD[15:8]	SD[7:0]
Standby Mode	H	X	X	X	X	X	X
Byte Access	L	H	L	H	L	X	Even-Byte
	L	H	H	H	L	X	Odd-Byte
Word Access	L	L	L	H	L	Odd-Byte	Even-Byte

6.2 80186 CPU bus type access functions.

80186 CPU bus I/O Read function

Function Mode	/CS	/BHE	A0	/IORD	/IOWR	SD[15:8]	SD[7:0]
Standby Mode	H	X	X	X	X	High-Z	High-Z
Byte Access	L	H	L	L	H	Not Valid	Even-Byte
	L	L	H	L	H	Odd-Byte	Not Valid
Word Access	L	L	L	L	H	Odd-Byte	Even-Byte

80186 CPU bus I/O Write function

Function Mode	/CS	/BHE	A0	/IORD	/IOWR	SD[15:8]	SD[7:0]
Standby Mode	H	X	X	X	X	X	X
Byte Access	L	H	L	H	L	X	Even-Byte
	L	L	H	H	L	Odd-Byte	X
Word Access	L	L	L	H	L	Odd-Byte	Even-Byte

6.3 MC68K CPU bus type access functions.

68K bus I/O Read function

Function Mode	/CS	/UDS	/LDS	R/W	SD[15:8]	SD[7:0]
Standby Mode	H	X	X	X	High-Z	High-Z
Byte Access	L	H	L	H	Not Valid	Odd-Byte
	L	L	H	H	Even-Byte	Not Valid
Word Access	L	L	L	H	Even-Byte	Odd-Byte

68K bus I/O Write function

Function Mode	/CS	/UDS	/LDS	R/W	SD[15:8]	SD[7:0]
Standby Mode	H	X	X	X	X	X
Byte Access	L	H	L	L	X	Odd-Byte
	L	L	H	L	Even-Byte	X
Word Access	L	L	L	L	Even-Byte	Odd-Byte

6.4 MCS-51 CPU bus type access functions.

8051 bus I/O Read function

Function Mode	/CS	/PSEN	SA0	/IORD	/IOWR	SD[15:8]	SD[7:0]
Standby Mode	H	X	X	X	X	High-Z	High-Z
	X	L	X	X	X	High-Z	High-Z
Byte Access	L	H	L	L	H	Not Valid	Even-Byte
	L	H	H	L	H	Not Valid	Odd-Byte

8051 bus I/O Write function

Function Mode	/CS	/PSEN	SA0	/IORD	/IOWR	SD[15:8]	SD[7:0]
Standby Mode	H	X	X	X	X	X	X
	X	L	X	X	X	X	X
Byte Access	L	H	L	H	L	X	Even-Byte
	L	H	H	H	L	X	Odd-Byte

6.5 CPU Access MII Station Management functions.

Basic Operation

The primary function of station management is to transfer control and status information about the PHY to a management entity. This function is accomplished by the MDC clock input from MAC entity, which has a maximum frequency of 12.5 MHz (for internal PHY only, as to external PHY please refer to the relevant specification), along with the MDIO signal.

The Internal PHY address is fixed to 10h and the equivalent circuit is shown as below:

A specific set of registers and their contents (described in Tab - 16 MII Management Frames- field Description) defines the nature of the information transferred across the MDIO interface. Frames transmitted on the MII management interface will have the frame structure shown in Tab - 15 MII Management Frame Format. The order of bit transmission is from left to right. Note that reading and writing the management register must be completed without interruption.

Read/Write (R/W)	Pre	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
R	1. . .1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
W	1. . .1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Tab - 15 MII Management Frame Format

Field	Descriptions
Pre	**Preamble**. The PHY will accept frames with no preamble. This is indicated by a 1 in register 1, bit 6.
ST	**Start of Frame.** The start of frame is indicated by a 01 pattern.
OP	**Operation Code**. The operation code for a read transaction is 10. The operation code for a write transaction is a 01.
PHYADD	**PHY Address**. The PHY address is 5 bits, allowing for 32 unique addresses. The first PHY address bit transmitted and received is the MSB of the address. A station management entity that is attached to multiple PHY entities must have prior knowledge of the appropriate PHY address for each entity.
REGAD	**Register Address.** The register address is 5 bits, allowing for 32 unique registers within each PHY. The first register address bit transmitted and received is the MSB of the address.
TA	**Turnaround**. The turnaround time is a 2-bit time spacing between the register address field, and the data field of a frame, to avoid drive contention on MDIO during a read transaction. During a write to the PHY, these bits is driven to 10 by the station. During a read, the MDIO is not driven during the first bit time and is driven to a 0 by the PHY during the second bit time.
DATA	**Data**. The data field is 16 bits. The first bit transmitted and received will be bit 15 of the register being addressed.
IDLE	**Idle Condition.** The IDLE condition on MDIO is a high-impedance state. All three state drivers will be disabled and the PHY's pull-up resistor will pull the MDIO line to logic 1.

Tab - 16 MII Management Frames- field Description

7.0 Electrical Specification and Timings

7.1 Absolute Maximum Ratings

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+85	°C
Storage Temperature	Ts	-55	+150	°C
Supply Voltage	Vdd	-0.3	+4.6	V
Input Voltage	Vin	-0.3	5.5*	V
Output Voltage	Vout	-0.3	Vdd+0.5	V
Lead Temperature (soldering 10 seconds maximum)	Tl	-55	+220	°C

Note : Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for extended period, adversely affect device life and reliability.
Note: * All digital input signals can sustain 5 Volts input voltage except pin-79 LCLK/XTALIN

7.2 General Operation Conditions

Description	SYM	Min	Tpy	Max	Units
Operating Temperature	Ta	0	25	+75	°C
Supply Voltage	Vdd	+3.14	+3.30	+3.46	V

7.3 DC Characteristics

(Vdd=3.0V to 3.6V, Vss=0V, Ta=0°C to 75°C)

Description	SYM	Min	Tpy	Max	Units
Low Input Voltage	Vil	-		0.8	V
High Input Voltage	Vih	1.9		-	V
Low Output Voltage	Vol	-		0.4	V
High Output Voltage	Voh	Vdd-0.4		-	V
Input Leakage Current	Iil	-1		+1	uA
Output Leakage Current	Iol	-1		+1	uA

Description	SYM	Min	Tpy	Max	Units
Power Consumption (3.3V)	SPt3v		94	120	mA

7.4 A.C. Timing Characteristics

7.4.1 XTAL / CLOCK

Symbol	Description	Min	Typ.	Max	Units
Tcyc	CYCLE TIME		40		ns
Thigh	CLK HIGH TIME	16	20	24	ns
Tlow	CLK LOW TIME	16	20	24	ns
Tr/Tf	CLK SLEW RATE	1	-	4	ns
Tod	LCLK/XTALIN TO CLKO OUT DELAY		10		

7.4.2 Reset Timing

Symbol	Description	Min	Typ.	Max	Units
Trst	Reset pulse width	100	-	-	LClk

7.4.3 ISA Bus Access Timing

(1) Read cycle:

Symbol	Description	Min	Typ.	Max	Units
Tsu(AEN)	AEN SETUP TIME	0	-	-	ns
Th(AEN)	AEN HOLD TIME	5	-	-	ns
Tsu(A)	ADDRESS SETUP TIME	0	-	-	ns
Th(A)	ADDRESS HOLD TIME	5	-	-	ns
Tv(CS16-A)	/IOCS16 VALID FROM SA[9:0], /CS, /BHE AND AEN	-	-	20	ns
Tdis(CS16-A)	/IOCS16 DISABLE FROM SA[9:0], /CS, /BHE AND AEN	-	-	6	ns
Tv(RDY)	RDY VALID FROM SA[9:0]=310 VALID, /CS,/BHE AND AEN	-	-	20	ns
Tdis(RDY)	RDY DISABLE FROM /IORD	0	-	-	ns
Ten(RD)	OUTPUT ENABLE TIME FROM /IORD	-	-	25	ns
Tdis(RD)	OUTPUT DISABLE TIME FROM /IORD	0.5	-	4	ns
T iord	IORD LOW REQUIRE TIME	60	-	-	ns
T idle	IORD HI REQUIRE TIME FOR REGISTER IORD HI REQUIRE TIME FOR DATA PORT	60 100	-	-	ns

*1: If /RDY did not connect, a minumin delay 280 ns must wait between Remote DMA read command ready and 1st date valid

(2) Write cycle:

Symbol	Description	Min	Typ.	Max	Units
Tsu(A)	ADDRESS SETUP TIME	1.5	-	-	ns
Th(A)	ADDRESS HOLD TIME	5			ns
Tsu(AEN)	AEN SETUP TIME	1.5	-	-	ns
Th(AEN)	AEN HOLD TIME	5	-	-	ns
Tv(CS16-A)	/IOCS16 VALID FROM SA[9:0], /CS, /BHE AND AEN	-	-	20	ns
Tdis(CS16-A)	/IOCS16 DISABLE FROM SA[9:0], /CS, /BHE AND AEN	-	-	6	ns
Tsu(WR)	DATA SETUP TIME	5	-	-	ns
Th(WR)	DATA HOLD TIME	5	-	-	ns
T iowr	IOW WIDTH TIME	60	-	-	ns
T cycle	CYCLE TIME FOR EVEREY DATA PORT WRITE	160	-	-	ns

7.4.4 80186 Type I/O Access Timing

(1) Read cycle:

Symbol	Description	Min	Typ.	Max	Units
Tsu(A)	ADDRESS SETUP TIME	0	-	-	ns
Th(A)	ADDRESS HOLD TIME	5	-	-	ns
Tv(RDY)	RDY VALID FROM SA,/CS AND /BHE	-	-	20	ns
Tdis(RDY)	RDY DISABLE FROM SA[9:0]=310 VALID, /CS AND /BHE	0	-	-	ns
Ten(RD)	OUTPUT ENABLE TIME FROM /IORD	-	-	25	ns
Tdis(RD)	OUTPUT DISABLE TIME FROM /IORD	0.5	-	4	ns
Tiord	IORD LOW WIDTH TIME	60	-	-	ns
Tidle	IORD HI REQUIRE TIME FOR REGISTER IORD HI REQUIRE TIME FOR DATA PORT	60 100	-	-	ns

*1: If /RDY did not connect, a minumin delay 280 ns must wait between Remote DMA read command ready and 1st date valid

(2) Write Cycle

Symbol	Description	Min	Typ.	Max	Units
Tsu(A)	ADDRESS SETUP TIME	1.5	-	-	ns
Th(A)	ADDRESS HOLD TIME	5	-	-	ns
Tsu(WR)	DATA SETUP TIME	5	-	-	ns
Th(WR)	DATA HOLD TIME	5	-	-	ns
Tiorw	/IOWR WIDTH TIME	60	-	-	ns
Tcycle	CYCYLE TIME FOR EVERY DATA PORT WRITE	160	-	-	ns

7.4.5 68K Type I/O Access Timing

(1) Read cycle

Symbol	Description	Min	Typ.	Max	Units
Tsu(A)	ADDRESS SETUP TIME	0	-	-	ns
Th(A)	ADDRESS HOLD TIME	5	-	-	ns
Tv(DTACK)	DACK VALID FROM /UDS OR /LDS	-	-	20	ns
Tdis(DTACK)	DACK DISABLE FROM /UDS OR /LDS	0	-	-	ns
Ten(DS)	OUTPUT ENABLE TIME FROM /UDS OR /LDS	-	-	25	ns
Tdis(DS)	OUTPUT DISABLE TIME FROM /UDS OR /LDS	0.5	-	4	ns
Tw(DS)	/UDS OR /LDS WIDTH TIME	60	-	-	ns
Tidle	IORD HI REQUIRE TIME FOR REGISTER IORD HI REQUIRE TIME FOR DATA PORT	60 100	-	-	ns

(2) Write cycle

Symbol	Description	Min	Typ.	Max	Units
Tsu(A)	ADDRESS SETUP TIME	1.5	-	-	ns
Th(A)	ADDRESS HOLD TIME	5	-	-	ns
Tv(DS-WR)	/UDS OR /LDS VALID FROM /UDS OR /LDS	0	-	-	ns
Tdis(WR-DS)	/W DISABLE FROM /UDS OR /LDS	5	-	-	ns
Tv(DTACK)	DACK VALID FROM /UDS OR /LDS	-	-	20	ns
Tdis(DTACK)	DACK DISABLE FROM /UDS OR /LDS	0	-	-	ns
Tdis(DS)	OUTPUT DISABLE TIME FROM /UDS OR /LDS	0.5	-	4	ns
Tsu(DS)	DATA SETUP TIME	5	-	-	ns
Th(DS)	DATA HOLD TIME	5	-	-	ns
Tw(DS)	/UDS,/LDS LOW WIDTH	60	-	-	ns
Tcycle	CYCYLE TIME FOR EVERY DATA PORT WRITE	160	-	-	ns

7.4.6 8051 Bus Access Timing

(1) Read cycle

Symbol	Description	Min	Typ.	Max	Units
Tsu(A)	ADDRESS SETUP TIME	0	-	-	ns
Th(A)	ADDRESS HOLD TIME	5	-	-	ns
Tsu(PSEN)	/PSEN SETUP TIME	0	-	-	ns
Th(PSEN)	/PSEN HOLD TIME	5	-	-	ns
Ten(RD)	OUTPUT ENABLE TIME FROM /IORD	-	-	25	ns
Tdis(RD)	OUTPUT DISABLE TIME FROM /IORD	0.5	-	4	ns
Tiord	IORD LOW WIDTH TIME	60	-	-	ns
Tidle	IORD HI REQUIRE TIME FOR REGISTER IORD HI REQUIRE TIME FOR DATA PORT	60 100	-	-	ns
Tv (RDY)	RDY VALID FROM IORD	20	-	-	ns

*1: If /RDY did not connect, a minumin delay 280 ns must wait between Remote DMA read command ready and 1st date valid

(2) Write cycle

Symbol	Description	Min	Typ.	Max	Units
Tsu(A)	ADDRESS SETUP TIME	1.5	-	-	ns
Th(A)	ADDRESS HOLD TIME	5	-	-	ns
Tsu(PSEN)	/PSEN SETUP TIME	1.5	-	-	ns
Th(PSEN)	/PSEN HOLD TIME	5	-	-	ns
Tsu(WR)	DATA SETUP TIME	5	-	-	ns
Th(WR)	DATA HOLD TIME	5	-	-	ns
Tiowr	IOWR WIDTH	60			ns
Tcycle	I/O CYCLE WIDTH TIME	160			ns

7.4.7 MII Timing

Symbol	Description	Min	Typ.	Max	Units
Ttclk	Cycle time(100Mbps)	-	40	-	ns
Ttclk	Cycle time(10Mbps)	-	400	-	ns
Ttch	high time(100Mbps)	14	-	26	ns
Ttch	high time(10Mbps)	140	-	260	ns
Trch	low time(100Mbps)	14	-	26	ns
Trch	low time(10Mbps)	140	-	260	ns
Ttv	Clock to data valid	-	-	20	ns
Tth	Data output hold time	5	-	-	ns
Trclk	Cycle time(100Mbps)	-	40	-	ns
Trclk	Cycle time(10Mbps)	-	400	-	ns
Trch	high time(100Mbps)	14	-	26	ns
Trch	high time(10Mbps)	140	-	260	ns
Trcl	low time(100Mbps)	14	-	26	ns
Trcl	low time(10Mbps)	140	-	260	ns
Trs	data setup time	6	-	-	ns
Trh	data hold time	10	-	-	ns
Trs1	RXER data setup time	10	-	-	ns

8.0 Package Information

SYMBOL	MILIMETER		
	MIN.	NOM	MAX
A1	0.05	0.1	0.15
A2	1.35	1.40	1.45
A			1.6
b	0.17	0.22	0.27
D	13.90	14.00	14.10
E	19.90	20.00	20.10
e		0.5	
Hd	15.60	16.00	16.40
He	21.00	22.00	23.00
L	0.45	0.60	0.75
L1		1.00	
θ	0°		7°

9.0 Ordering Information

AX88796	**L**	**F**
Product name	**Package LQFP**	**F: Lead Free**

Appendix A: Application Note 1

A.1 Using Crystal 25MHz

Note : The capacitors (33pf) may be various depend on the specification of crystal. While designing, please refer to the suggest circuit provided by crystal supplier.

A.2 Using Oscillator 25MHz

Appendix B: Power Consumption Reference Data

The following reference data of power consumption are measured base on prime application, that is AX88796 + EEPROM, at 3.3V/25 °C room temperature.

Item	Test Conditions	Typical Value	Units
1	Power save mode (Power Down register bit set to “1” asserted)	0	mA
2	Idel without Link	22	mA
3	Idel with 10M Link	30	mA
4	Idel with 100M Link	91	mA
5	Full traffic with 10Mbps at half-duplex mode	48 – 80	mA
6	Full traffic with 10Mbps at full-duplex mode	48 – 80	mA
7	Full traffic with 100Mbps at half-duplex mode	88 – 94	mA
8	Full traffic with 100Mbps at full-duplex mode	88 – 94	mA
9	Power save mode (Power Down register bit set to “1” asserted) no LED drive	0	mA
10	Idel without Link, no LED drive	22	mA
11	Idel with 10M Link, no LED drive	25	mA
12	Idel with 100M Link, no LED drive	84	mA
13	Full traffic with 10Mbps at half-duplex mode, no LED drive	46 – 66	mA
14	Full traffic with 10Mbps at full-duplex mode, no LED drive	46 – 66	mA
15	Full traffic with 100Mbps at half-duplex mode, no LED drive	83	mA
16	Full traffic with 100Mbps at full-duplex mode, no LED drive	83	mA

Errata of AX88796

1. MII Station Management functions have some difference from previous target specification.

Description: The target specification is using station management can access both internal PHY registers and external PHY registers when the PHY address is matched as describe in section 5.5. Anyway, this version can only access the current selected PHY's registers. How do you know which is the selected media or PHY? Please refer to section 4.1.16 GPO and Control (GPOC) register.

Solution: The defect will not affect single media application that is using embedded PHY. When using MII interface connects to external media (for example HomePNA) to come out with combo solution. Care must be taken, be sure which media is the current selected when you access PHY registers.

2. AX88796 can't support 68K CPU with byte mode

Solution: Please using word mode for high performance. MC68008 has only 8-bit bus, so AX88796 can't support this CPU.

3. When AX88796 transmit a packet and the packet is collided for 16 times. The packet will be reported as as PTX bit asserted rather than TXE asserted.

Solution: Packet collided 16 times and aborted is normal way, even that is rare happen in live network, in very heavy traffic. While the upper protocol layer will handle the situation and cover the packet loss.

4. Some chips may need long power down for successful PHY auto negotiation

Description: The PHY inside of AX88796 has a special request due to the semiconductor's process. Namely, it needs a very long power down for successful Auto Negotiation for some chips. We made a test in lab and found it would be no problem if the PHY's initial time kept for 2 sec for all chips. If the power down is less then this number, some of the PHY's Auto Negotiation will not be complete and there will be potential to cause the link fail. If the auto negotiation time is not long enough, uncertain numbers of chip may not work properly.

Countermeasure:

Following actions will fix the problem of long auto negotiation.

1. **Set the PHY register MR0 with 0x800h (1000,0000,0000) -- bit 11 of MR0 to '1' (Power down Mode).**
2. **Wait for 2.5 sec**
3. **Set the PHY register MR0 with 0x1200h(0001,0010,0000,0000) -- bit 12,9 of MR0 to '1' (auto negotiation enable and restart auto negotiation)**

5. Listed limitations (as following table) must consider when connecting with CPU's IO cycle is less then 160 ns.

Description: There are 4 limitations in AX88796 must not excess when using AX88796

	write	read	Note
Limitation_a : 60/60ns (min)	needed	needed	For all registers Except data port Active time = 60ns(min.) Idle time = 60ns.(min.)
Limitation_b : 60/100ns(min)	No needed	needed	For read data port access only Active time = 60ns(min.) Idle time = 100ns.(min.)
Limitation_c : 160ns(min)	needed	No needed	For write data port access only Active time + idle time = 160ns.(min.)
Limitation_d : 280ns(min)	No needed	Every 1'st data port of remote DMA read access	For data port read only

All limitations timing information has marked in corresponding timing diagram

6. When /RDY not connect, following steps must include in driver when "READ" data port

Step-1: write remote start address 0
Step-2: write remote start address 1
Step-3: write remote byte count 0
Step-4: write remote byte count 1
Step-5: write remote read command
Step-6: delay time for 280 ns
Step-7: read data port

7. AX88796 embedded PHY may "link fail" when quick plug/unplug RJ45 (4~5 times/sec)

Description: A watch dog timer rountine can kick the embedded PHY from hanged state to re-autonegotiation state. Watchdog Timer Routine will be called every 2 seconds, the PowerDownFlag is a software flag and should be set to FALSE on initialization.

```
-----------------------------------------------------------------------------------------------------------------------
  IF PowerDownFlag is TRUE
   {
        *Set PowerDownFlag to FALSE
        *Write MII Register 0 with 0x3100  (Power up AX88796's PHY).
         Exit watch dog timer routine
   }

  Read MII Register 1 (Status Register)
  IF Bit 2 (Link Status) is ONE (link up) , Exit the watchdog timer routine
  IF Bit 2 (Link Status) is ZERO (link down), Read MII Register 1 again.

  IF Bit 2 (Link Status) is ONE (link up), Exit the watchdog timer routine
  IF Bit 2 (Link Status) is still ZERO (link down)

{
        * Write MII Register 0 with 0x3900   (Power down AX88796's PHY)
        * Set the PowerDownFlag to TRUE

}
  Exit the watchdog timer routine
-----------------------------------------------------------------------------------------------
```

Demonstration Circuit (A) : AX88796 with ISA Bus + HomePNA 1M8 PHY

AX88796 10BASE-T/100BASE-TX & 1M HomePNA Application with NS83851 PHYceiver. (reference only)(ISA Mode)

ASIX ELECTRONIC CORPORATION			
Title	ISA BUS		
Size A4	Document Number 796NS3A.SCH		Rev 2.0
Date: Thursday, April 19, 2001	Sheet 1 of 4		

U3
AX88796
LQFP
P1
DB-25F
U4
25MHZ OSC
Y1
25MHZ
XIN
XOUT
U2
93C56R
JP1
6PIN JUMP
L1
L2
L3
L5
F.B.
SMD 1206
4.7uF/16V
SMD 1206
3.3V
3.3VD
3.3VA
GND
R5
0
R49 10K *1
R46 10K
R20 20 PCLK
R48 10K *2
R25 10K
R26 10K *3
R27 10K *3
R6 10K *4
R1 10K *5
R2 10K *5
R3 10K *5
R23 24.9K 1%
R22 2.49K 1%
R21 20K 1%
R9 330
R8 330
R7 330
D3 LED
D2 LED
D1 LED
LINK_LED LINK/ACT_LED
SPEEDLED
ACT_LED FULL/COL_LED
PPD_SET
STROB#
ATFD#
PD0
ERR
PD1
INIT#
PD2
SLIN#
PD3
PD4
PD5
PD6
PD7
ACK
BUSY
PE
SLCT
SA[0..9]
SD[0..15]
BHE#
IORD#
IOWR#
AEN
RESET
IRQ
RDY
IOIS16#
RXER
RXDV
COL
CRS
RXCK
RXD0
RXD1
RXD2
RXD3
TXCK
TXEN
TXD0
TXD1
TXD2
TXD3
MDC
MDIO
PCLK
TPIP
TPIN
ZVREG
TPOP
TPON
*6 Use Crystal or Oscillator.
Link LED
Speed LED
FULL LED
*3 CPU Type select
CPU1 CPU0 MODE
OFF OFF 8051
OFF ON MC68K
ON OFF 80186
ON ON ISA BUS
*5 IOBASE Select
IOBASE2 IOBASE1 IOBASE0 IO BASE
OFF OFF OFF 200h default
OFF OFF ON 220h
OFF ON OFF 380h
OFF ON ON 3A0h
ON OFF OFF 340H
ON OFF ON 360h
ON ON OFF 300h
ON ON ON 320h
*1 Pin 67 SPP_SET# = 0 : Select printer interface.
Pin 67 SPP_SET# = 1 : Select MII interface.(Default)
*2 Pin 50 PPD_SET = 0 : Internal PHY in normal mode.(default)
Pin 50 PPD_SET = 1 : Internal PHY in power down mode.(match up CIS)
*4 Pin 116 I_OP = 0 : LNK/ACT & FULL/COL LED Display be used.
Pin 116 I_OP = 1 : LNK & ACT LED Display be used.
ASIX ELECTRONICS CORPORATION
Title
AX88796
Size A3
Document Number
796NS3A1.SCH
Rev 2.0
Date: Thursday, April 19, 2001
Sheet 2 of 4

ASIX ELECTRONICS CORPORATION		
Title DP83851C		
Size A4	Document Number 796NS3A2.SCH	Rev 2.0
Date: Thursday, April 19, 2001	Sheet 3 of 4	

ASIX ELECTRONIC CO.		
Title RJ45 & RJ11		
Size A4	Document Number 796NS3A3.SCH	Rev 2.0
Date: Wednesday, May 22, 2002	Sheet 4 of 4	

Revision	Date(M/D/Y)	Comment
V 1.7	01/24//02	1 Remove Tally counter at MAC register list 2 Modify RDY timing diagram in ISA and 186 mode 3 Remove BOS bit in DCR register 4 Include LED current sink value
V1.8	06/18/02	Schematic change for hi-voltage Cap, change from 0.01u to 1000PF
V1.9	08/19/03	1. Add Tio (DS) timing information to all modes
V2.0	09/19/03	1. Improve the readability of timing diagram 2. Add limitiations in timing diagram for hi-speed CPU's application and note when RDY not connect
V2.1	10/30/03	Modify Errata and add following: 1 Long AN issue 2 Limitations information 3 WDY routine
V2.2	02/18/05	1. Add Ordering Information (Section 9.0) 2. Describe the abbreviations of PU & PD more detailly (Section 2.0) 3. Take out one of the "power on configuration setup signals cross reference table" (Section 2.9) 4. Modify the trace and description (Section 6.5)
V2.3	09/12/05	1. Add non leed free and RoHS part number in the features 2. Add description (Section 5.1.2) 3. Add description at PPDSET pin (Section 5.1.16)

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