SONET/SDH TIMING CARD SYNCHRONIZER **ZL30116**

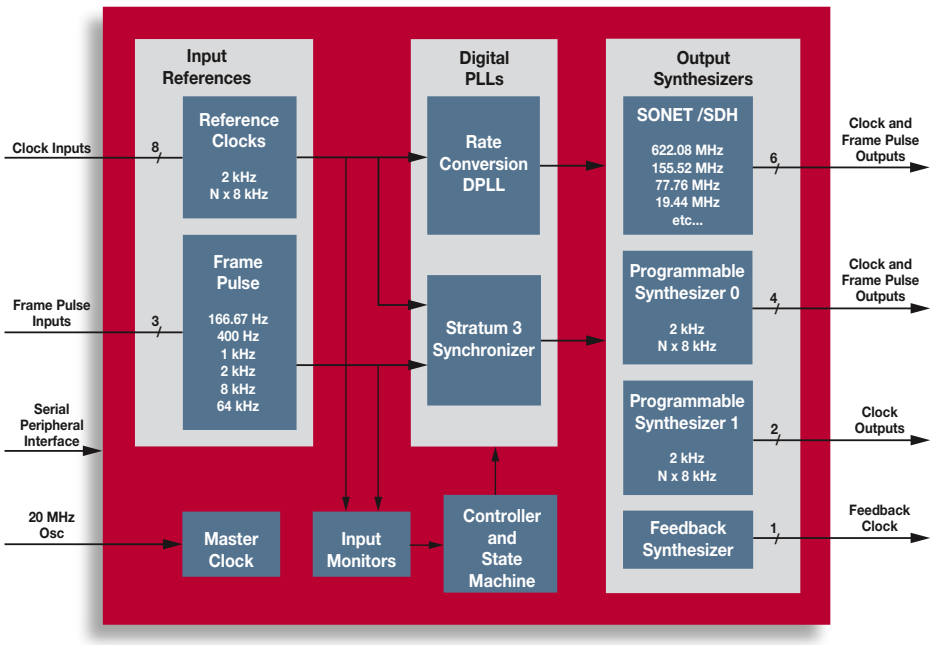
PRODUCT PREVIEW

Zarlink's ZL30116 chip is a SONET Stratum 3/G.813 compliant system clock management device for multi-service provisioning and edge platforms operating at up to OC-48/STM-16 speeds.

A highly integrated, compact device, the ZL30116 PLL combines the network synchronization capabilities of a digital PLL with the jitter performance of an analog PLL. The ZL30116 PLL delivers all of the clocks and clock formatting required to allow existing SONET/SDH infrastructures to carry new Ethernet, VoIP and Fiber Channel services.

The ZL30116 PLL integrates SONET Stratum 3/G.813 capabilities including an integrated rate conversion PLL, master/slave redundancy functions, ultra-low jitter SONET/SDH clock synthesis, programmable clock synthesis and clock formatting in a single chip measuring just 9 x 9 mm.

ZL30116 Simplified Block Diagram



Applications

- AdvancedTCA™ systems
- Multi-Service Edge Switches and Routers
- Multi-Service Provisioning Platforms
- Add-Drop Multiplexers
- Wireless base stations
- DSLAM & next-generation DLCs
- Core routers

Integrated Chip for SONET/SDH Timing Cards

- Single-chip integrates network synchronization functions of a DPLL with jitter generation of an APLL
- Meets GR-253-CORE SONET Stratum 3 and ITU-T G.813 requirements
- Jitter attenuation under 1 ps (less than 25% of jitter budget for OC-48/STM-16 interfaces)
- Provides two independently configurable DPLLs:
  - DPLL1 provides all features for generating SONET/SDH compliant clocks
  - DPLL2 generates independent, general purpose clocks
- Supports master/slave clock redundancy configurations
- Programmable phase delay adjustment compensates for static delays
- Optional external feedback path provides dynamic delay compensation
- Operates in free-run, normal and holdover modes and provides automatic hitless reference switching
- Eight reference inputs supporting clock frequencies in any multiple of 8 kHz up to 77.76 MHz and 2 kHz
- Selectable output clocks (6.48 MHz, 19.44 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz) eliminate need for external dividers & clock multiplying DPLLs
- Programmable output synthesizers generate clock frequencies from any multiple of 8 kHz up to 77.76 MHz in addition to 2 kHz
- Programmable frame pulse formatter replaces CPLD or FPGA gates

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ZL30116 SONET/SDH TIMING CARD SYNCHRONIZER APPLICATION

SONET/SDH Timing Card Synchronization

Zarlink's ZL30116 is a compact, highly integrated SONET Stratum 3/G.813 compliant system synchronizer and clock management device for next-generation multi-service provisioning and edge products. Incorporating digital and analog PLLs, the single chip manages SONET/SDH network synchronization functions at OC-48/STM-16 speeds. Competing two-chip or module approaches are more than twice the size of the ZL30116 and require external devices to manage high-speed network timing.

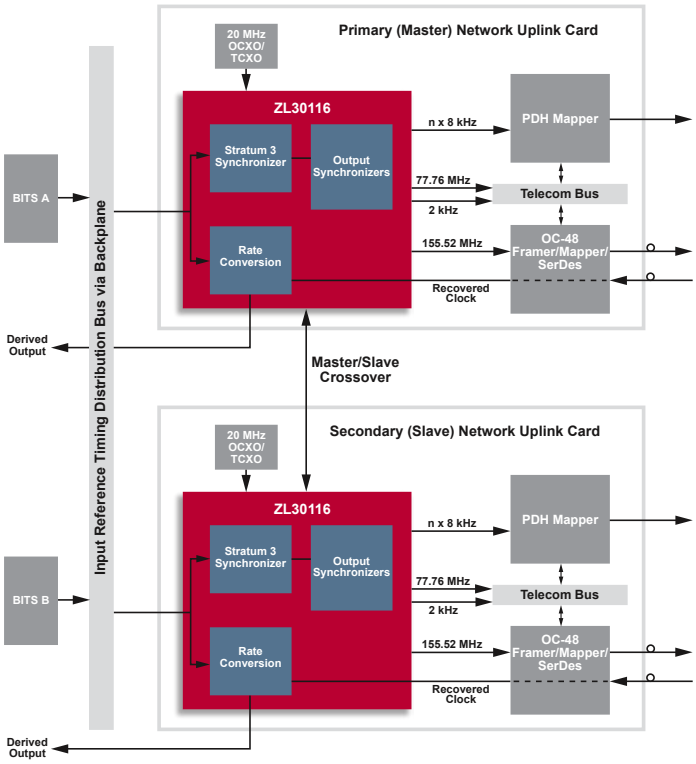
As illustrated below, the ZL30116 can be used as the sole timing device for a network uplink card operating at speeds up to OC-48/STM-16. The ZL30116 provides the network synchronization functions necessary to comply with SONET Stratum 3/G.813 and the clocks and jitter performance to time OC-48/STM-16 uplinks.

The chip simultaneously accepts and monitors up to eight input references and three frame pulse (sync) inputs for frequency accuracy, phase irregularity and loss of clock. The ZL30116 can be configured to manually or automatically switch between valid input references upon reference failure. When automatic reference switching is used, reference selection criteria is based on input priority. An optional revertive feature ensures the highest priority valid reference is always selected. When no valid references are available, the device automatically enters holdover mode and generates output clocks based on historical reference frequency data.

Two ZL30116 devices can be connected in a redundant (master/slave) configuration. A dedicated crossover link, combined with programmable phase delay adjustment, allows for very close phase alignment between master and slave output clocks.

The ZL30116 can simultaneously generate 13 output clocks from three independent clock frequency families. Common SONET/SDH clock frequencies, programmable n x 8 kHz clock frequencies and programmable frame pulses can be generated simultaneously. CMOS and differential LVPECL outputs are provided. Ultra-low jitter SONET/SDH outputs up to 622.08 MHz can directly drive OC-48/STM-16 framers.

With leading integration, flexibility, programmability and performance, the device's network synchronization functionality and ultra-low jitter SONET/SDH output clocks deliver a complete single-chip timing solution.



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