28234-ERR-001-I
August 26, 2005

RS8234

Product and Documentation Errata

Documentation Affected: **RS8234 Data Sheet (28234-DSH-001-B)**
Product Affected: **RS8234EBGD (28234-15), RS8234EBGC (28234-13), RS8234EBGB (28234-12), and RS8234EBG (28234-11)**

1 Product Errata

1.1 ACR Notification when Seg Status Queue is full

Description

There is a potential buffer leakage problem when a segmentation status queue is in a full condition, and the SAR writes an ACR notification status queue entry.

By writing an ACR notification in a status queue full condition, the SAR might overwrite the first status queue entry in the queue. Therefore, the buffers linked to this first status queue entry are not returned.

Workaround

This problem only occurs when transmitting ABR traffic with the ACR Notification mechanism enabled.

If operating in such a mode, then a status queue full condition is avoided by selecting a large enough status queue size. If a segmentation status queue is full, no cells belonging to this status queue are segmented, and therefore the cell transmission is interrupted.

Status queue full interrupt generation should be enabled. Once a status queue full condition is reached, the host gives the status queue read process a high priority.

In order to decrease the probability of a buffer leakage, the host might decrease the internally used status queue size by one or two entries. Therefore, the difference between the read and the read update pointer in the host would be at least one or two entries.

1.2 RxEn* is too Fast in Slave Utopia Mode

Description

When operating in slave Utopia mode, RxEn* is an input to the SAR. The specified hold time for RxEn* is violated by 500 ps.

Workaround

If operating in slave Utopia mode, RxEn* should be slowed on the board to provide an additional 500 ps of hold time beyond the specification.

1.3 RSM Status Queue Overflow on DMA FIFO Full Status

Description

If a PDU is received when the DMA FIFO is full (such that a FIFO full packet discard RSM Status entry is written), the RSM Status entry is written even if the status queue is full. This results in an overwritten valid RSM Status entry.

Note that in an operational system, if the DMA FIFO is overflowing, the status queue is overflowing, or both, there are some serious system issues.

Workaround

There is no workaround. Avoid the RSM Status Queue full with the DMA FIFO full condition.

1.4 PCI Base Address Restrictions

Description

Through EEPROM loading of the MEMORY_SIZE_MASK field of the PCI Configuration Special Status register, the SAR's memory space may be mapped to 8MB. A bug prevents this feature from working. Setting bit 23 of the PCI Base Address register results in the bug.

Workaround

The PCI Base Address should always be set as if the SAR is setup to use its full default memory space of 16MB. The MEMORY_SIZE_MASK field of the PCI Configuration Special Status register must be set to 0b00000000 (0x00).

1.5 Firewall Leak on FBQ Empty Condition

Description

When firewalling is enabled in the RSM coprocessor and an FBQ empty (underflow) condition is encountered, the RX_COUNTER field in the VCC table(s) still decrements each time the VCC receives a BOM cell. The RX_COUNTER should not be decremented when the FBQ is empty.

Workaround

There is no workaround. Avoid FBQ empty conditions when firewalling is enabled.

1.6 PCI Write With No Byte Enables

Description

A PCI write to SAR address space 0x0004 ---> 0x17FC with no byte enables, results in a write. This is in violation of the PCI specification. This problem was observed with a 64 bit processor (Verde) operating on a 32 bit PCI bus. When the processor writes to an address not on a 64 bit boundary, the PCI address is aligned to a 64 bit boundary where the first 32 bit write is generated with no byte enables.

Workaround

The problem is avoided by always doing writes to addresses on a 64 bit boundary in the SAR address range of 0x0004 ---> 0x17FC. This should be easy to accomplish since there are very few writes to the SAR's internal address space during run-time applications.

1.7 Slave PCI Disconnect Error

Description

Periodically, the PCI slave performs a disconnect with data, but does not write the data into the FIFO. This is evident in that a local memory access is not performed for the errored data. This error condition occurs when the FIFO is full. This was determined by looking at the difference between the PCI address and the local memory address at the time of the error condition. The error condition always occurs on the first data word after the address cycle. At this point, only a retry should occur because a disconnect will occur only after 8 wait states. The only difference between a retry and disconnect with data is that the HTRDY signal is active for a disconnect.

The problem is caused when both the almost full and full go inactive at the same time. This can be due to two reads occurring within the timeframe of one PCI clock. This can happen if the SYSCLK is running a little faster than the PCI clock.

Workaround

By performing a dummy read after 5 consecutive writes, the slave FIFO is prevented from filling and therefore possibly triggering this error condition.

1.8 EPD Auto-Recovery Does Not Work in AAL0 Mode

Description

When the SAR encounters an FBQ under-flow error or a RSM status queue over-flow error, the EPD bit is set in the RSM VCC table. The SAR will discard cells until the EPD event is cleared. The SAR should automatically recover from the EPD event by resetting the EPD bit once the error condition(s) have been cleared. The SAR does not reset the EPD bit and continues to discard cells even after the error condition(s) have been cleared.

Workaround

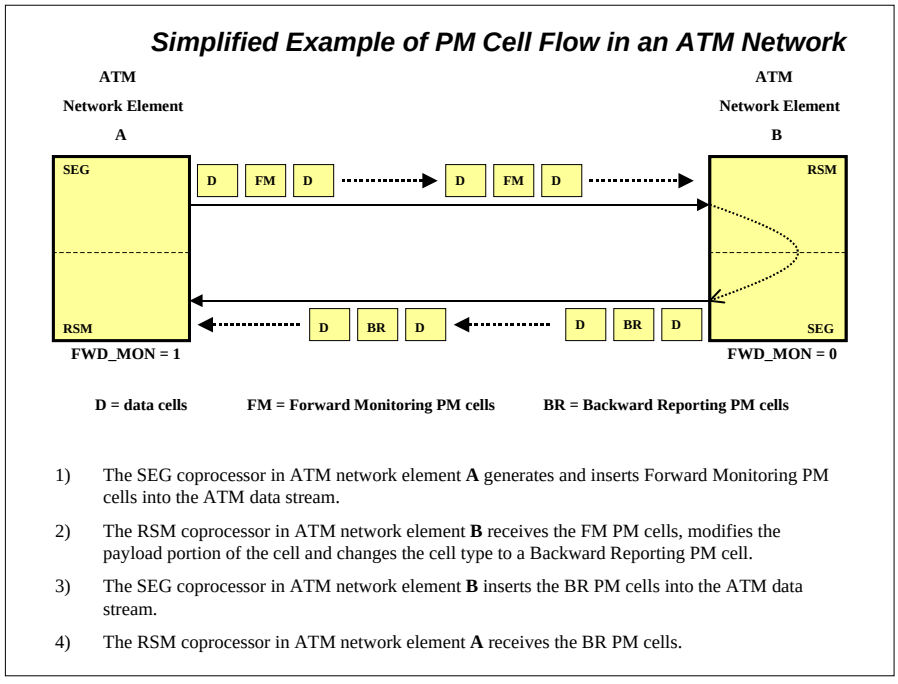
After the error condition(s) is cleared, the EPD bit must be written to 0 in order to resume AAL0 processing on the VCC.

1.9 Possible Erroneous Backward Reporting (BR) PM Cell Generation

Description:

When the PM function is "re-enabled" on an active VCC with Forward Monitoring enabled, the SAR may generate an erroneous BR PM cell. The following figure and subsequent steps, show the test scenario in which this problem was uncovered.

Figure 1-10. *2 ATM Network Elements (NE) Connected Full Duplex; NE A & NE B*



1) The SEG coprocessor in ATM network element **A** generates and inserts Forward Monitoring PM cells into the ATM data stream.

2) The RSM coprocessor in ATM network element **B** receives the FM PM cells, modifies the payload portion of the cell and changes the cell type to a Backward Reporting PM cell.

3) The SEG coprocessor in ATM network element **B** inserts the BR PM cells into the ATM data stream.

4) The RSM coprocessor in ATM network element **A** receives the BR PM cells.

1. NE A: Initialized with PM “on”, ready to send and receive on one AAL0 VCC, FWD_MON = 1
2. NE B: Initialized with PM “on”, ready to send and receive on same VCC, FWD_MON = 0
3. Write Tx Q in NE A, a packet is transmitted from NE A to NE B
4. Check cell counters in both NE A and NE B
   - NE A: Tx = AC (packet length + one FM PM cell), Rx = 1 (one BR PM cell)
   - NE B: Tx = 1 (one BR PM cell), Rx = AC (packet length + one FM PM cell)
5. Turn PM “off ” on both NE A and NE B
6. Write Tx Q in NE B, a packet is transmitted from NE B to NE A
7. Check cell counters in both NE A and NE B
   - NE A: Tx = AC (unchanged), Rx = AC (+ packet length)
   - NE B: Tx = AC (+ packet length), Rx = AC (unchanged)
8. NE A: Clear SEG and RSM PM structures, turn “on” PM and set FWD_MON = 0
9. NE B: Clear SEG and RSM PM structures, turn “on” PM and set FWD_MON = 1
10. Write Tx Q in NE B, a packet is transmitted from NE B to NE A
11. Check cell counters in both NE A and NE B
    - NE A: Tx = AD (+ one BR PM cell), Rx = 159 (should be 158; + packet length and one FM PM cell)
    - NE B: Tx = 159 (should be 158; + packet length and one FM PM cell), Rx = AD (+ one BR PM cell)

The generation of the erroneous BR PM cell occurs in operation number 10 above. NE B was previously enabled for PM activity and had received a Forward Monitoring (FM) PM cell during operation number 3. Also during operation number 3, NE B turned around the received FM PM cell and sourced a BR PM cell to NE A. As part of the FM PM to BR PM cell processing in NE B, the SAR had set two state variables (ACK_PM & BCK_PM) in the SEG VCC table. When NE B sources a packet in operation number 6, with PM turned off, the SAR resets the ACK_PM bit, but does not reset the BCK_PM bit. When PM is re-enabled on NE B the FM PM to BR PM mechanism in the SAR is out of synchronization. The next packet segmented by NE B results in an erroneous BR PM cell being sent before the first data cell of the packet. After the generation of the erroneous BR PM cell in NE B, the SAR FM PM to BR PM cell processing mechanism is resynchronized. In this scenario NE A would receive an unexpected BR PM cell.

Workaround:

Two possible workarounds are available for this errata item. The first workaround accepts the possibility of an erroneous BR PM cell generation with S/W awareness. The second workaround eliminates the generation of the erroneous BR PM cell by setting two state variable bits in the SEG VCC table to an initialization state.

1. An awareness of this anomaly needs to be built into the application/driver S/W. All of the expected FM PM and BR PM cells are sent and received and the contents and Status indications are correct. The generation of the erroneous BR PM cell does not cause any corruption within the normal PM cell processing, it merely shows up as an unexpected BR PM cell at the receiving ATM Network Element. When this happens simply discard this cell.

2. The SEG VCC needs to be in an idle state (not actively segmenting) when performing writes to the SEG VCC Table in order to avoid potential coherency problems within bytes lanes. The ACK_PM (bit 23 of word 0) and the BCK_PM (bit 30 of word 6) control bits in the SEG VCC Table need to be set to zero when re-enabling the PM function on the VCC with Forward Monitoring. This will eliminate the possible generation of an erroneous BR PM cell .

1.11 Incoming DMA FIFO full condition may cause subsequent bad PCI transactions

Description

The bug occurs when inc_dma state machine is in the idle state and checks the number of words in the incoming DMA FIFO to start a write transaction. If the word count is 252 and a word write is still pending from the previous transaction, the state machine will write a burst of data and attempt a write after the FIFO becomes full. The result is that a word will be dropped and when the PCI reads command words from the incoming FIFO, it will read a data word which it interprets as a command word. The behavior of the PCI becomes unpredictable at this point and could become locked up. The bug is not dependent upon large versus small FIFO size, Endianism, or 32/64 PCI mode.

Workaround

The condition which causes the bug can be avoided by never allowing the FIFO to approach the full condition. This can be achieved by making sure the FF_DSC bit is always set in configured VCCs (word 0, bit20, of the VCC table). This will enable the reassembler to gracefully discard packets when the FIFO become almost full. In addition to setting the FF_DSC bit, it is also advised to set the OAM_FF_DSC (bit 12) in Reassembly Control Register 1.

2 Documentation Errata

Documentation Affected: RS8234 Data Sheet (28234-DSH-001-B)

2.1 Remove References to QFC in Data Sheet

Description

a. The first paragraph of section 5.4.11.3 should read as follows:

The user returns credit, at the same time the buffer is recovered to the free buffer queue, by writing the third word of the free buffer queue. The VCC_INDEX is written to the channel to which credit is returned. The FWD_VLD bit is set to a logic high. The RSM coprocessor increments the RX_COUNTER[15:0] of the applicable channel. For proper operation of the update interval function, buffers must be returned at the same time as credits are returned.

b. Replace QFC with ABR in the Description/Function for ABR_CTRL Field Name in Table 5-15.

2.2 Incorrect Value Listed for OOR_INT Field

Description

Table 14-4 Table of Values for Scheduler Control Register Initialization lists the OOR_INT (12-bit) field Initialized Value as 0x1C9D. The correct value should read 0xC9D.

2.3 Remove References to MAX_BURST_LEN Field

Description

All references to the MAX_BURST_LEN field should be removed from the Data Sheet. The following changes should be made on page 8-1.

8.2 DMA Read

For outgoing messages, DMA read cycles move data from host memory to the segmentation coprocessor using a gather DMA method. The maximum burst size is thirteen 32-bit words, which correspond to one cell.

8.3 DMA Write

For incoming messages, DMA write cycles move data from the reassembly coprocessor to host memory using a scatter DMA method. The maximum burst size is fourteen 32-bit words, which correspond to one ATM cell and a status word appended to PM cells.

2.4 PCI Configuration in EEPROM

Description

The first sentence in Section 11.9.1 incorrectly states: ‘The first 32 bytes of the EEPROM are used to store PCI Configuration information,’. In addition, the second to last sentence in this section incorrectly states: ‘Bytes above address offset 0x20 can be used by application software or device drivers as needed’.

Section 11.9.1 should be changed to read as follows:

> The first 11 bytes of the 128-byte EEPROM are used to store PCI configuration information, loaded into the PCI Configuration space at reset. Unless otherwise specified, all unused bytes are reserved and should be programmed to 0x00. Bytes above address offset 0x0A can be used by application software or device drivers as needed.