AVR082: Replacing ATmega161 by ATmega162

8-bit AVR® Microcontroller

Application Note

Features

- **ATmega161 Errata Corrected in ATmega162**
- **Improvements to Timer/Counters**
- **Improvements to External Memory Interface**
- **Improvements to UART**
- **Changes in EEPROM Write Timing**
- **Changes in Programming Interface**
- **Fuse Settings**
- **Oscillators and Selecting Start-up Delays**
- **Changes to Watchdog Timer**
- **JTAG Interface**
- **Self-Programming**
- **Other Concerns**
- **Features not Available in ATmega161 Compatibility Mode**

Introduction

This application note is a guide to assist current ATmega161 users in converting existing designs to the ATmega162. The ATmega162 has two operating modes selected through the fuse settings. The M161C Fuse selects whether the ATmega161 compatibility mode should be used or not. By default, the M161C Fuse is unprogrammed and the ATmega162 operates in Normal mode. When the compatibility mode is used, only non-conflicting enhancements make the part different from the ATmega161. Additionally, the electrical characteristics of the ATmega162 are different including an increase in operating frequency because of a change in process technology. Check the data sheet for detailed information. When the M161C Fuse is unprogrammed, all new features are supported, but porting the code may require more work.

ATmega161 Errata Corrected in ATmega162

The following items from the Errata Sheets of the ATmega161 do not apply to the ATmega162. Refer to the ATmega161 Errata Sheet for a more detailed description of the Errata.

PWM not Phase Correct

All Timers in ATmega162 have been redesigned to generate phase correct PWM.

Increased Interrupt Latency

In ATmega162, all instructions are interruptable, and no dead-lock situation exists if a loop is followed by a two-word instruction for the purpose of looping until an interrupt goes active.

Rev. 2516B–AVR–11/02

Interrupt Return Fails when Stack Pointer Addresses the External Memory

In ATmega162, the Stack Pointer can be placed freely within the Data Memory Address Space, even in external memory.

Writing UBBRH Affects Both UART0 and UART1

In ATmega162, each USART has their own UBRRH Register.

Store Program Memory Instruction May Fail

The SPM instruction in ATmega162 works as expected for all frequencies and voltages within the specification.

Changes to Names

The following control bits have changed names, but have the same functionality and placement when accessed as in ATmega161:

Table 1. Changed Bit Names[1]

Bit Name in ATmega161	Bit Name in ATmega162	I/O Register (ATmega161)	Comments
PWMn(0)	WGMn0	TCCRn(A)	“A” and “0” in 16-bit timers only
PWMn1	WGMn1	TCCRnA	
CTCn	WGMn2	TCCRn(B)	“B” in16-bit timers only
PSR10	PSR310	SFIOR	
WDTOE	WDCE	WDTCR	See “Changes to Watchdog Timer” on page 5.
CHR9n	UCSZn2	USCRnB	
ORn	DORn	UCSRnA	

Note: 1. The Register Summary in ATmega161 names the AS0 bit AS02. It is called AS0 elsewhere in that data sheet, as well as everywhere in ATmega162.

The following bits have changed locations, but have the same functionality when accessed as in ATmega161:

Table 2. Changed Bit Locations

Bit Name	Register	Location in ATmega161	Location in ATmega162
TOIE2	TIMSK	Bit 4	Bit 2
OCIE2	TIMSK	Bit 2	Bit 4
TOV2	TIFR	Bit 4	Bit 2
OCF2	TIFR	Bit 2	Bit 4

The following I/O Registers have changed names, but include the same functionality and placement when accessed as in ATmega161:

Table 3. Changed Register Names

Register name in ATmega161	Register name in ATmega162	Comments
GIMSK	GICR	
MCUSR	MCUCSR	
UBRRHI	UBRR0H and UBRR1H	Shared register split into two registers. See “Improvements to UART” on page 3.
UBRR0	UBRR0L	
UBRR1	UBRR1L	

Improvements to Timer/Counters

For details about the improved and additional features, please refer to the data sheet. The following features have been added:

- Variable top value in PWM mode.
- Timer/Counter0 extended with compare function and PWM.
- For Timer/Counter1, Phase and Frequency Correct PWM mode in addition to the Phase Correct PWM mode.

Updating of OCR in PWM Mode (Applies to all Timer/Counters)

In PWM mode, the value written to the Output Compare Register is not physically used as compare value until the Timer/Counter reaches the value TOP. The interpretation of this point of time differs between ATmega161 and ATmega162. In ATmega161, the new OCR value is used in the cycle where the Timer/Counter has the value TOP. In ATmega162, the counter value TOP is used to update the compare value, i.e., it is first active in the cycle where the Timer/Counter has the value TOP-1 down-counting.

Improvements to External Memory Interface

Refer to the ATmega162 data sheet for details on the changed timing.

Improvements to UART

The UART in ATmega161 has been replaced by a USART in ATmega162. The ATmega162 USART is compatible with the ATmega161 UART with one exception: The two-level Receive Register acts as a FIFO. The FIFO is disabled when the M161C Fuse is programmed. Still the following must be kept in mind when the M161C Fuse is programmed:

- The UDR must only be read once for each incoming data.
- The Error Flags (FE and DOR) and the ninth data bit (RXB8) are buffered with the data in the receive buffer. Therefore the status bits must always be read before the UDR Register is read. Otherwise, the error status will be lost.

ATmega161 contains the baud-rate high-bytes for both UARTs in a common register – UBRRHI. ATmega162 has separate registers for the high-bytes of the two USARTs; UBRR0H and UBRR1H, implying a modification to the code when porting the design to ATmega162

Another minor difference is the initial value of RXB8, which is “1” in the UART in ATmega161 and “0” in the USART in ATmega162.

Changes to EEPROM Write Timing

In ATmega161, the EEPROM write time takes 2,048 cycles of the calibrated RC Oscillator. In ATmega162, the EEPROM write time takes 8,448 cycles of the calibrated RC Oscillator. This is in both devices regardless of the clock source and frequency of the system clock. The calibrated RC Oscillator is assumed to be calibrated to 1.0 MHz in both devices.

Note: Changing the value in the OSCCAL Register affects the frequency of the calibrated RC Oscillator and hence the EEPROM write time.

Programming Interface

The Parallel Programming algorithm is changed. In Parallel mode, the ATmega162 supports page programming of the EEPROM. The timing requirements for Parallel Programming have been changed. See the ATmega162 data sheet for details.

The STK500 supports both In-System Programming and Parallel Programming of the ATmega162.

Fuse Settings

ATmega162 contains more fuses than ATmega161. Table 4 shows the ATmega161 compatible fuse settings. Some of the fuses are described further in the following sections.

Table 4. Comparing Fuses in ATmega161 and ATmega162(1)

Fuse	Default ATmega161 Setting	Default ATmega162 Setting	ATmega161 Compatible Setting
M161C	–	1	0
BODLEVEL2	–	1	1
BODLEVEL1	–	1	0
BODLEVEL0(2)	1	1	1
OCDEN	–	1	1
JTAGEN	–	0	1(3)
SPIEN	0	0	0
WDTON	–	1	1
EESAVE	–	1	1
BOOTSZ1	–	0	0
BOOTSZ0	–	0	1
BOOTRST	1	1	1
CKDIV16	–	0	1
CKOUT	–	1	1
SUT1	–	1	See note (4)
SUT0	–	0	See note (4)
CKSEL3	–	0	See note (4)
CKSEL2	0	0	See note (4)
CKSEL1	1	1	See note (4)
CKSEL0	0	0	See note (4)

Notes: 1. A dash indicates that the fuse is not present in ATmega161.
2. ATmega161 has only one BODLEVEL Fuse. Here, this one is called BODLEVEL0

3. See “JTAG Interface” on page 5.
4. The CKSEL Fuses are available in both ATmega161 and ATmega162. However, the SUT and CKSEL setting should be reconsidered when moving to ATmega162. See “Oscillators and Selecting Start-up Delays” on page 5.

Oscillators and Selecting Start-up Delays

In ATmega161, the CKSEL Fuses selects both which Oscillator is active, and the duration of the start-up delay. In ATmega162, the active Oscillator and its frequency range is selected by the CKSEL Fuses, while the SUT Fuses selects start-up delay for the given Oscillator. Hence, the CKSEL Fuse setting from ATmega161 must be reconsidered when moving to ATmega162. Follow the guidelines from the section “System Clock and Clock Options” in the ATmega162 data sheet to find appropriate start-up values.

Changes to Watchdog Timer

The Watchdog Timer in ATmega162 is improved compared to the one in ATmega161. In ATmega161, the Watchdog Timer is either enabled or disabled, while ATmega162 supports two safety levels selected by the WDTON Fuse. See description in ATmega162 data sheet for further information.

The combination of programming the M161C Fuse and having the WDTON Fuse unprogrammed makes the Watchdog Timer behave exactly as in ATmega161.

The frequency of the Watchdog Oscillator in ATmega162 is close to 1.0 MHz for all supply voltages. The typical frequency of the Watchdog Oscillator in ATmega161 is close to 1.0 MHz at 5V, but the Time-out period increases with decreasing V_{CC}. This means that the selection of Time-out period for the Watchdog Timer (in terms of number of WDT Oscillator cycles) must be reconsidered when porting the design to ATmega162. Refer to the data sheet for ATmega162 for further information.

JTAG Interface

The ATmega162 provides a JTAG interface, which can be used for programming, boundary-scan, and On-chip debug. Refer to data sheet for details. The device is shipped with the JTAGEN Fuse programmed in order to allow programming through the JTAG interface. This fuse must be erased to be ATmega161 compatible (If not, four pins are dedicated to the Test Access Port – TAP instead of being I/O pins). The M161C Fuse does *not* override the JTAGEN Fuse.

Self-Programming

Both ATmega162 and ATmega161 supports Self-Programming. In ATmega161 the CPU is halted both during Page Erase and during Page Write. In ATmega162, the CPU is only halted when programming the No-Read-While-Write – NRWW – section of the Flash memory. The SPMEN bit in the SPMCR Register will be auto-cleared in both devices. This means that a Boot-loader for ATmega161 can be written without polling for completion of the erase or the write operation. If this is the case, porting the code to ATmega162 requires rewriting the code to poll for SPMEN to go low before starting a new Page Erase, Page Write or writing the Lock bits command.

However, the data sheet for ATmega161 recommends this polling operation for compatibility with future devices, so as long as this recommendation is followed, the Boot Loader can be used in ATmega162 without modification.

Other Concerns

The ATmega162 has a signature byte different from the one used in ATmega161. Make sure you are using the signature byte of ATmega162 when porting the design.

As stated in the data sheet for ATmega161, the user should write unused bits to zero if they are accessed (for compatibility to future devices). If not, new features in ATmega162 may be triggered when ATmega161 designs are ported to ATmega162. In particular, the MCUSR Register in ATmega161 is replaced by the MCUCSR Register in ATmega162. If these status bits were cleared by writing 0xFF to the register in ATmega161, this may trigger incorrect behavior when ported to ATmega162, since the new control bits will be set.

Features not Available in ATmega161 Compatibility Mode

The M161C Fuse makes the ATmega162 compatible to ATmega161. However, with the M161C Fuse programmed, some of the new features in ATmega162 become unavailable. The following features are not supported when the ATmega162 is used in the ATmega161 compatibility mode:

- The FIFO operation of the USART.
- Timer/Counter3 (16-bit Timer/Counter identical to Timer/Counter1).
- Access to the System Clock Prescaler. (Note that the fuse CKDIV16 still determines the initial state of the prescaler).
- Pin Change Interrupts on Port A and Port C.
- A timed sequence to change Watchdog Timer prescaler settings by software.
- As shown in “Interrupt Vectors in ATmega162” in the data sheet, the M161C Fuse remaps the Interrupt Vectors to be equal to those in ATmega161. This means that the following six Interrupt Vectors disappears, and vectors from number 11 to 28 moved up to become vectors number 5 to 22.

Table 5.

Vector No.	Program Address	Source	Interrupt Definition
5	$008	PCINT0	Pin Change Interrupt Request 0
6	$00A	PCINT1	Pin Change Interrupt Request 1
7	$00C	TIMER3 CAPT	Timer/Counter3 Capture Event
8	$00E	TIMER3 COMPA	Timer/Counter3 Compare Match A
9	$010	TIMER3 COMPB	Timer/Counter3 Compare Match B
10	$012	TIMER3 OVF	Timer/Counter3 Overflow

If any of the features above are needed or wanted and the M161C Fuse is unprogrammed, this introduces several differences between ATmega162 and ATmega161 which do not exist as long as the compatibility fuse is programmed:

- Address space 0x0060-0x00FF is dedicated extended I/O, not internal SRAM.
- Address space 0x0100-0x04FF is dedicated internal SRAM, thus the external memory starts at address 0x500 (external memory on ATmega161 starts at address 0x460).
- A timed sequence must be followed to change Watchdog Timer prescaler settings by software.
- The UART will have an extra input buffer which allows one more data byte to be received before the Data OverRun Flag (DOR) is set.
- The Interrupt Vectors differ, since the six additional Interrupt Vectors outlined above are present as vectors number 5 to 10.

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