Network Connectivity

TIMING MODULE
ZL30462

ZL30462 Simplified Block Diagram

The ZL™30462 is a compact, off-the-shelf timing module ideal for high-speed network access equipment. The module integrates digital and analog phase locked loop (DPLL and APLL) technology, a 20MHz master oscillator, and all of the support circuitry required for a high-performance system clock in a single small outline package.

Zarlink's ZL30462 supports the industry's widest range of clock frequencies, and features flexible, independent dual inputs and high-speed jitter attenuated outputs. These clock frequencies meet the requirements of a new generation of linecard needing TDM and high speed SONET/SDH clocks. The ZL30462 also ensures reliable network synchronization with fast lock, time interval error correction and automatic holdover.

The combination of Zarlink's industry-leading integration and reliability features translates to substantial savings in cost, board space and time-to-market.

Applications

- SDH Add/Drop Multiplexers
- SDH STM1 Uplinks
- Integrated Access Devices
- ATM Edge Switch
- SONET Linecard

At a Glance

- **Package:** 40-pin SMT DIL
- **Volume production:** April 2003

High Performance

- High speed 19.44MHz CMOS and 155.52MHz LVPECL output clocks surpass OC3 jitter performance.
- Four selectable input frequencies (8kHz, 1.544MHz, 2.048MHz and 19.44MHz) with impairment monitoring.
- Fast lock and automatic holdover modes ensure synchronization when the timing source is interrupted.
- Provides Time Interval Error (TIE) correction to allow hitless reference switching.

Flexible for Multiple System Requirements

- Supports free-run, normal (locked) or holdover modes.
- Accepts reference inputs from two independent sources.
- Provides two low jitter clocks, three additional support clocks (2.048MHz, 8.192MHz, 16.384MHz) and two frame pulse outputs.

Simplifies Design

- Internal 20MHz master oscillator
- Easy-to-use hardware control functions
- Small size 2.54cm x 2.54cm Surface Mount Technology (SMT)

Standards Compliant

- Telcordia GR-1244-CORE for Stratum 4 and 4E
- ITU-T G.813 option 1 (see Data Sheet for exceptions)

Complimentary Products

- TDM switches
- TDM to Packet processors (IP/ATM)

Customer Support

The ZL30462 is supported by a customer evaluation board as well as with extended in-house support.

ZARLINK SEMICONDUCTOR

Network Connectivity

Applications

The complexity of network timing is quickly increasing, as more and more network elements are added to support the rising traffic densities at the network edge. The timing and synchronization of these elements is critical in determining network performance.

The ZL30462 provides an ideal solution to the complex timing requirements of today's networks. As shown in the diagram below, the module can be used throughout a system where transmit data must be synchronized to a master system reference clock.

The ZL30462 accepts reference signals from one or two independent sources, and locks the input to one of four frequencies: 8kHz, 1.544MHz, 2.048MHz and 19.44MHz. The device then produces a low-jitter output at 19.44MHz CMOS or 155.52MHz LVPECL, the most commonly used logic levels for framers and mappers.

The compact, easy-to-implement module integrates all of the components and support circuitry required for high-performance timing solution. The ZL30462 replaces the components typically required for a network clock, thereby providing a board savings of up to 50% while reducing system cost and complexity. Measuring only 2.54cm x 2.54cm, the module has the smallest footprint in its class. This is a substantial savings compared to alternative solutions, which generally require external TDM clocks as well as external logic translation circuits for LVPECL.

Zarlink's timing module is based on proven reliability features including fast lock, time interval error correction and automatic holdover. Holdover mode allows the device to ensure accurate timing, even when the reference source is lost.

The combination of integration and reliability features makes the ZL30462 the most efficient solution in its class.

Application Diagram

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