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KS8995M Integrated 5-Port 10/100 Managed Switch

Overview

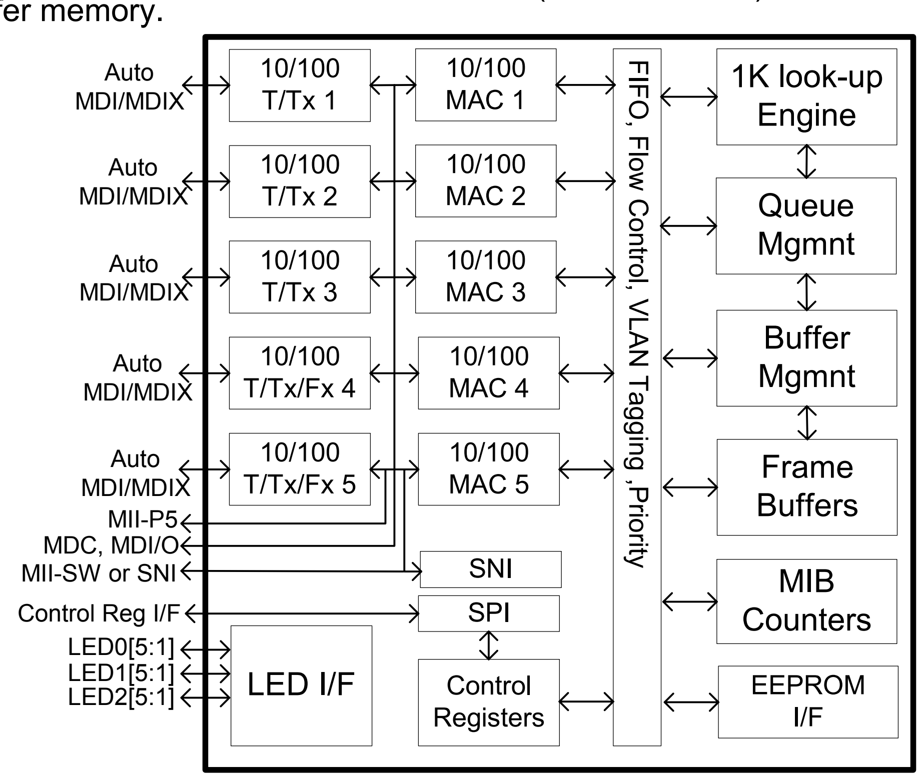
The KS8995M is a highly integrated layer-2 managed switch with optimized BOM (Bill-Of-Materials) cost for low port count, cost-sensitive 10/100Mbps switch systems. It also provides an extensive feature set such as tag/port-based VLAN, QoS priority, management, MIB counters, dual MII interface and CPU control/data interfaces to effectively address both current and emerging Fast Ethernet applications.

The KS8995M contains five 10/100 transceivers with patented mixed-signal low-power technology, five MAC (Media Access Control) units, a high-speed non-blocking switch fabric, a dedicated address lookup engine, and an on-chip frame buffer memory.

All PHY units support 10Base-T and 100Base-Tx. In addition, two of the PHY units support 100Base-Fx (Ports 4 & 5).

Feature Highlights

- Integrated switch with 5 MACs and 5 Fast Ethernet transceivers fully compliant to IEEE 802.3u standard
- Shared memory based switch fabric with fully non-blocking configuration
- 1.4Gbps high performance memory bandwidth
- 10Base-T, 100Base-TX and 100Base-FX modes (Fx in Ports 4 & 5)
- Dual MII configuration: MII-Switch (MAC or PHY mode MII) and MII-P5 (PHY mode MII)



KS8995M

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Feature Highlights (Cont'd)

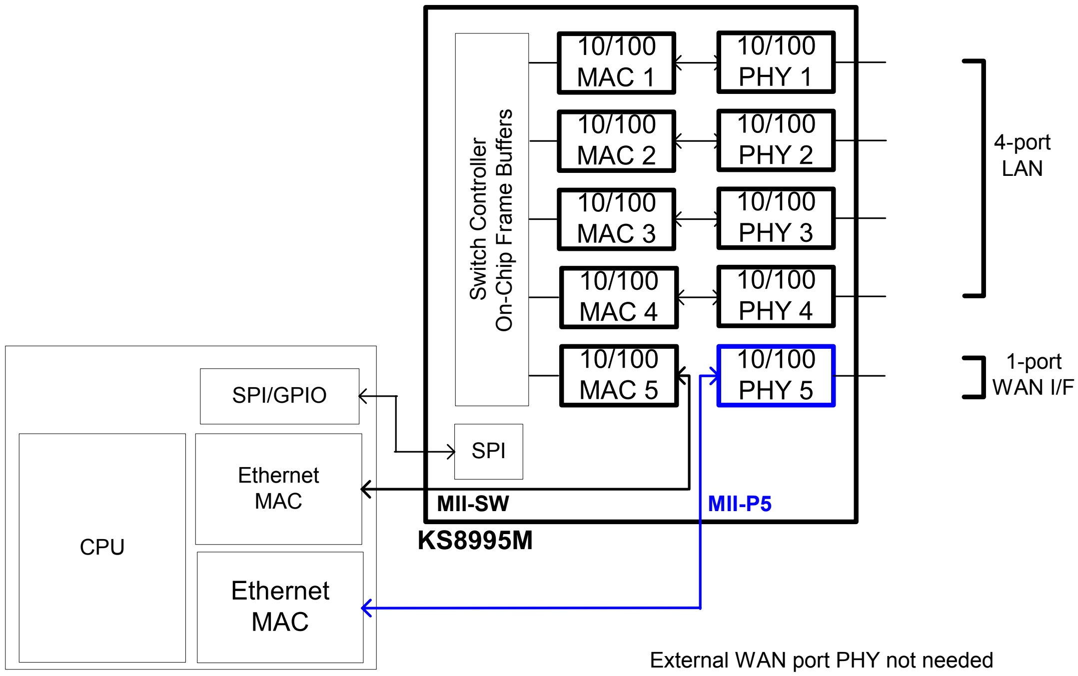
- IEEE 802.1Q tag-based VLAN (16 VLANs, full-range VID) for DMZ port, WAN/LAN separation or inter-VLAN switch links
- VLAN ID tag/untag options, per-port basis
- Programmable rate limiting 0 to 100Mbps, ingress & egress port, rate options for high & low priority, per port basis
- Flow control or drop packet rate limiting (ingress port)
- Integrated MIB counters for fully compliant statistics gathering, 34 MIB counters per port
- Enable/Disable option for huge frame size up to 1916 bytes per frame
- IGMP v1/v2 Snooping for multicast packet filtering
- Special tagging mode to send CPU info on ingress packet's port value
- SPI slave (complete) and MDIO (MII PHY only) serial management interface for control of register configuration
- MAC-id based security lock option
- Control registers configurable on-the-fly (port-priority, 802.1P/D/Q, AN…)
- CPU read access to MAC forwarding table entries
- 802.1D Spanning Tree Protocol
- Port mirroring / monitoring / sniffing: ingress and/or egress traffic to any port or MII
- Broadcast storm protection with % control - global & per-port basis
- Optimization for fiber-to-copper media conversion
- Full-chip hardware power-down support (register configuration not saved)
- Per-port based software power-save on PHY (idle link detection, register configuration preserved)
- QoS / CoS packets prioritization supports: per port, 802.1P and DiffServ based.
- 802.1p/q tag insertion or removal on a per port basis (egress)
- MDC & MDI/O interface support to access the MII PHY control registers (not all control registers)
- MII local loopback support
- On-chip 64Kbyte memory for frame buffering (not shared with 1K unicast address table)
- Wire speed reception and transmission
- Integrated look-up engine with dedicated 1 K MAC addresses
- Full duplex IEEE 802.3x & half-duplex back pressure flow control
- Comprehensive LED support
- 7-wire SNI support for legacy MAC interface
- Automatic MDI / MDI-X crossover for plug-and-play
- Disable Automatic MDI/MDI-X option
- Low power core: 1.8V
- I/O: 2.5V or 3.3V
- 0.18um CMOS technology
- 128 pin PQFP package

Applications

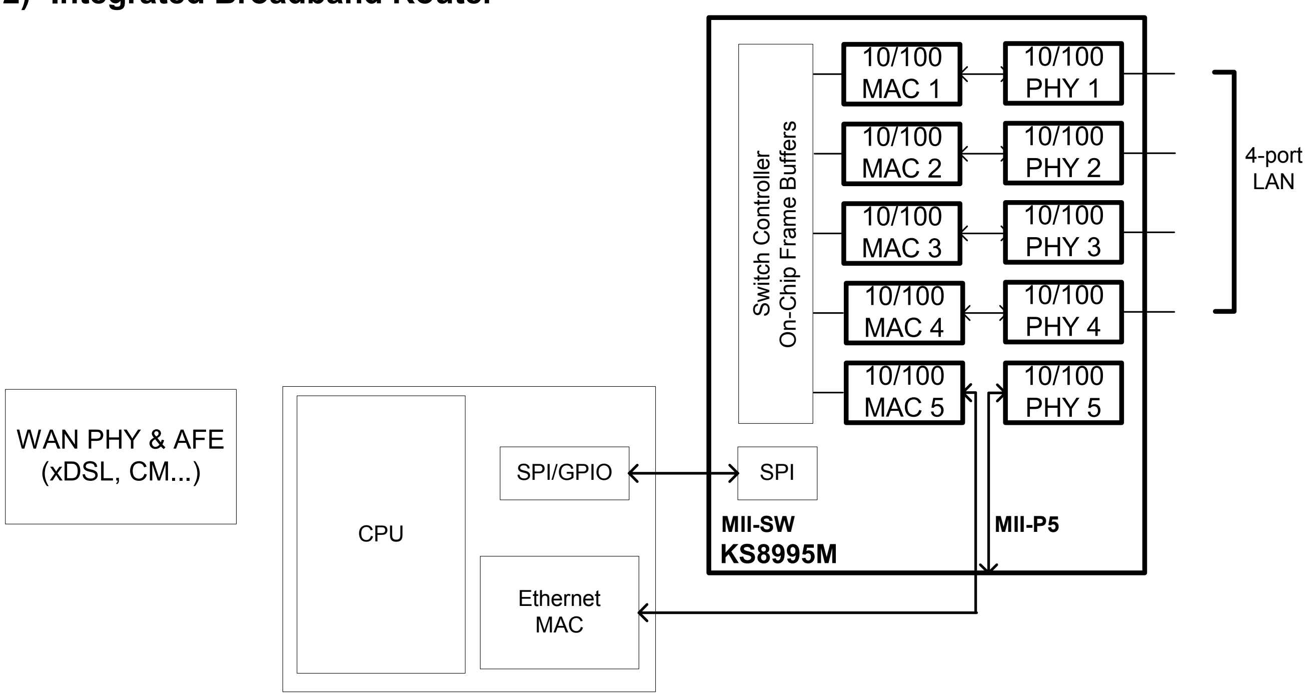
- Broadband gateway / firewall / VPN
- Integrated DSL or cable modem multi-port router
- Wireless LAN access point + gateway
- Home networking expansion
- Standalone 10/100 switch
- Hotel / Campus / MxU gateway
- Enterprise VoIP Gateway / Phone
- FTTx customer premise equipment
- Managed Media converter

System Level Configurations:

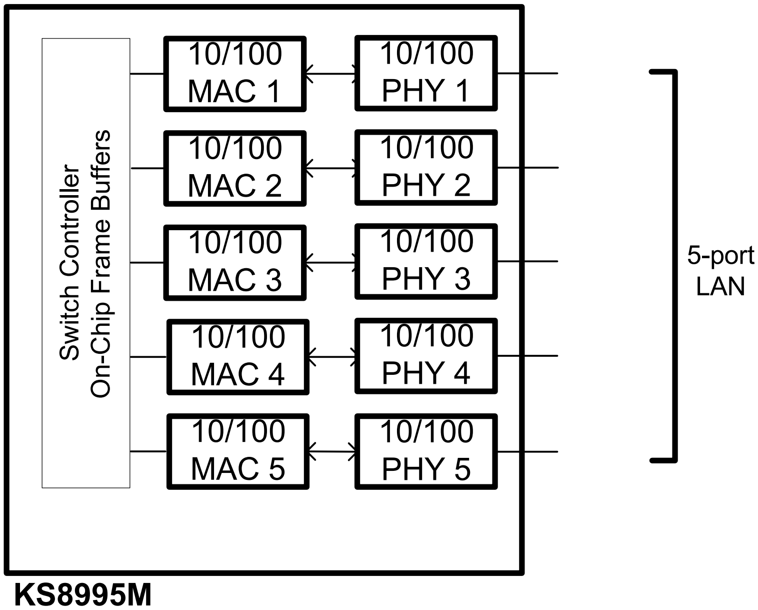
1) Broadband Gateway



2) Integrated Broadband Router



3) Standalone switch



Revision History

Revision	Date	Summary of Changes
1.00	11/05/01	Created
1.01	11/09/01	Pinout Mux1/2, DVCC-IO 2.5/3.3V, feature list, register spec 11-09
1.02	12/03/01	Editorial changes, added new register and MIB descriptions. Added paragraph describing TOS registers. Imported functional descriptions. Formatting.
1.03	12/12/01	Incorporate changes per engineering feedback as well as updating functional descriptions and adding new timing information.
1.04	12/13/01	Changed Rev. and For. Modes to PHY and MAC modes respectively. Added MIIM clarification in 4.8. Reformatted section sequence. Added hex register addresses. Added advertisement ability descriptions.
1.05	12/18/01	Inserted switch forwarding flow charts.
1.06	12/20/01	Added new KS8995M block diagram, editorial changes, register descriptions changes and cross-references from functional descriptions to register and strap in options.
1.07	1/22/01	Changed FXSD pins to inputs, added new descriptions to section 4.7 for configuration interfaces. Edited pin descriptions.
1.08	3/1/02	Editorial changes in 5.3.35 and 5.3.36. Updated figure 2 flowchart. Updated table 2 for MAC mode connections. Separate static MAC bit assignments for read and write. Edited read and write examples to MAC tables and MIB counters. Changed Table 3 KS8995M signals to "S" suffix. Changed aging description in register 2, bit 0. Changed Section 5.2 to Port Registers and listed all port register addresses. Changed port control 11 description for bits [7:5]. Changed MIB counter descriptions in 5.3.36.
1.09	5/17/02	Sec. 6.0 Changed MII setting descriptions. Changed pu/pd descriptions for SMRXD2. Sec. 5.2.3, changed pu/pd description for forced flow control. Sec. 3.7.3, Edited large packet sizes back in. Sec. 8.0 Added in typical supply current numbers for 100 Base TX and 10 Base TX operation. 5.2.3 Added in note for illegal half-duplex, force flow control. 6.0 Added extra X1 clock input description. 8.0 Updated to chip only current numbers. Added Section 9.4 SPI Timing. Feature Highlights
1.10	7/29/02	Sec. 6.0, changed SMRXC and SMTXC to I/O. Input in MAC mode, output in PHY mode MII. Sec. 8.0 modified current consumption to chip only numbers. Sec. 3.7.5 Added

		description for no dropped packets in half duplex mode. Added recommended operating conditions Sec. 7.1 Added Idle mode current consumption in Sec. 8.0 Added Sec. 11.0 Added 3.01 kOhm resistor instructions for ISET section 6.0 Changed Polarity of transmit pairs in section 6.0. Changed description for register 2, bit 1, in section 5.0 Added section 9.5 reset timing.
1.11	12/17/02	5.1.4 changed 802.1x to 802.3x. 5.1.7, changed default column to disable flow control for pull down, and enable flow control for pull up. 5.2.14 and 5.4.1 indicate loop back is at the PHY. Added description to register 4 bit 2 to indicate that STPID packets from CPU to normal ports are not allowed as 1522 byte tag packets. Fixed dynamic MAC address example errors in 5.3.35. Changed definition of forced MDI, MDIX in section 5.2.14, 5.2.15 and 5.4.1. Added Section 12.0 Part Ordering Information. Added Ambient operating temperature for KS8995Mi
1.12	3/10/03	Changed Pin 120 description to NC. Changed SPIQ pin description to Otri. Changed logo. Changed contact information.
1.13	4/29/03	Changed Register 1, revision ID from 0x0 to 0x2 Added Register 11, bit 3 for PHY power save mode Changed Register 29, 45, 61, 77, 93 bit0 from Loop back to MAC Loop back Changed Register 31, 47, 63, 79, 95 from Status 1 to Control 14. Added register 31, 47, 63, 79, 95 Bit 3 = force link, Bit 4 = soft reset, bit 5 = PHY isolate Bit 6 = remote Loop back Bit 7 = PHY Loop back Changed VCCAT voltage from 2.5v to 2.5v or 3.3v Changed Pin #1 description to MDIXDIS: disable auto MDI/MDIX feature Changed order number to KS8995M A

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LIST OF TABLES AND FIGURES

1.0 Introduction

The KS8995M contains five 10/100 physical layer transceivers and five MAC (Media Access Control) units with an integrated layer 2 managed switch. The device runs in three modes. The first mode is as a five-port integrated switch. The second is as a five-port switch with the fifth port decoupled from the physical port. In this mode access to the fifth MAC is provided through an MII (Media Independent Interface). This is useful for implementing an integrated broadband router. The third mode uses the dual MII feature to recover the use of the fifth PHY. This allows the additional broadband gateway configuration, where the fifth PHY may be accessed through the MII-P5 port.

The KS8995M has the flexibility to reside in a managed or unmanaged design. In a managed design, a host processor has complete control of the KS8995M via the SPI bus, or partial control via the MDC/MDIO interface. An unmanaged design is achieved through I/O strapping or EEPROM programming at system reset time.

On the media side, the KS8995M supports IEEE 802.3 10BaseT, 100BaseTX on all ports, and 100BaseFX on ports 4 and 5. The KS8995M can be used as two separate media converters.

Physical signal transmission and reception are enhanced through the use of patented analog circuitry that makes the design more efficient and allows for lower power consumption and smaller chip die size.

The major enhancements from the KS8995E to the KS8995M are support for host processor management, a dual MII interface, tag as well as port based VLAN, spanning tree protocol support, IGMP snooping support, port mirroring support and rate limiting functionality.

2.0 Functional Overview: Physical Layer Transceiver

2.1 100BaseTX Transmit

The 100BaseTX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ to NRZI conversion, MLT3 encoding and transmission. The circuit starts with a parallel to serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding followed by a scrambler. The serialized data is further converted from NRZ to NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 3.01 KΩ resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot and timing jitter. The wave-shaped 10BaseT output is also incorporated into the 100BaseTX transmitter.

2.2 100BaseTX Receive

The 100BaseTX receiver function performs adaptive equalization, DC restoration, MLT3 to NRZI conversion, data and clock recovery, NRZI to NRZ conversion, de-scrambling, 4B/5B decoding and serial to parallel conversion. The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristics to optimize the performance. In this design, the variable equalizer will make an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then it tunes itself for optimization. This is an ongoing process and can self adjust against environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of base line wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. The signal is then sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

2.3 PLL Clock Synthesizer

The KS8995M generates 125 MHz, 42 MHz, 25 MHz and 10 MHz clocks for system timing. Internal clocks are generated from an external 25 MHz crystal or oscillator.

2.4 Scrambler/De-scrambler (100BaseTX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander. The data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). This can generate a 2047-bit non-repetitive sequence. The receiver will then de-scramble the incoming data stream with the same sequence at the transmitter.

2.5 100BaseFX operation

100BaseFX operation is very similar to 100BaseTX operation with the differences being that the scrambler / de-scrambler and MLT3 encoder / decoder are bypassed on transmission and reception. In this mode the auto negotiation feature is bypassed since there is no standard that supports fiber auto negotiation.

2.6 100BaseFX Signal Detection

The physical port runs in 100BaseFX mode if FXSDx >.6V for ports 4 and 5 only. This signal is internally referenced to 1.25V. The fiber module interface should be set by a voltage divider such that FXSDx ‘H’ is above this 1.25V reference, indicating signal detect, and FXSDx ‘L’ is below the 1.25V reference to indicate no signal. When FXSDx is below .6V then 100BaseFX mode is disabled. Since there is no auto-negotiation for 100BaseFX mode, ports 4 and 5 must be forced to either full or half duplex. Note that strap in options exist to set duplex mode for port 4, but not for port 5.

2.7 100BaseFX Far End Fault

Far end fault occurs when the signal detection is logically false from the receive fiber module. When this occurs, the transmission side signals the other end of the link by sending 84 1’s followed by a zero in the idle period between frames. The far end fault may be disabled through register settings.

2.8 10BaseT Transmit

The output 10BaseT driver is incorporated into the 100BaseT driver to allow transmission with the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3 V amplitude. The harmonic contents are at least 27 dB below the fundamental when driven by an all-ones Manchester-encoded signal.

2.9 10BaseT Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths in order to prevent noises at the RXP or RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KS8995M decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

2.10 Power Management

The KS8995M features a per port power down mode. To save power the user can power down ports that are not in use by setting port control registers or MII control registers. In addition, it also supports full chip power down mode. When activated, the entire chip will be shut down.

2.11 MDI / MDI-X auto crossover

The KS8995M supports MDI / MDI-X auto crossover. This facilitates the use of either a straight connection CAT-5 cable or a crossover CAT-5 cable. The auto-sense function will detect remote transmit and receive pairs, and correctly assign the transmit and receive pairs from the Micrel device. This can be highly useful when end users are unaware of cable types and can also save on an additional uplink configuration connection. The auto crossover feature may be disabled through the port control registers.

2.12 Auto Negotiation

The KS8995M conforms to the auto negotiation protocol as described by the 802.3 committee. Auto negotiation allows UTP (Unshielded Twisted Pair) link partners to select the best common mode of operation. In auto negotiation the link partners advertise capabilities across the link to each other. If auto negotiation is not supported or the link partner to the KS8995M is forced to bypass auto negotiation, then the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The flow for the link set up is depicted in Figure 1.

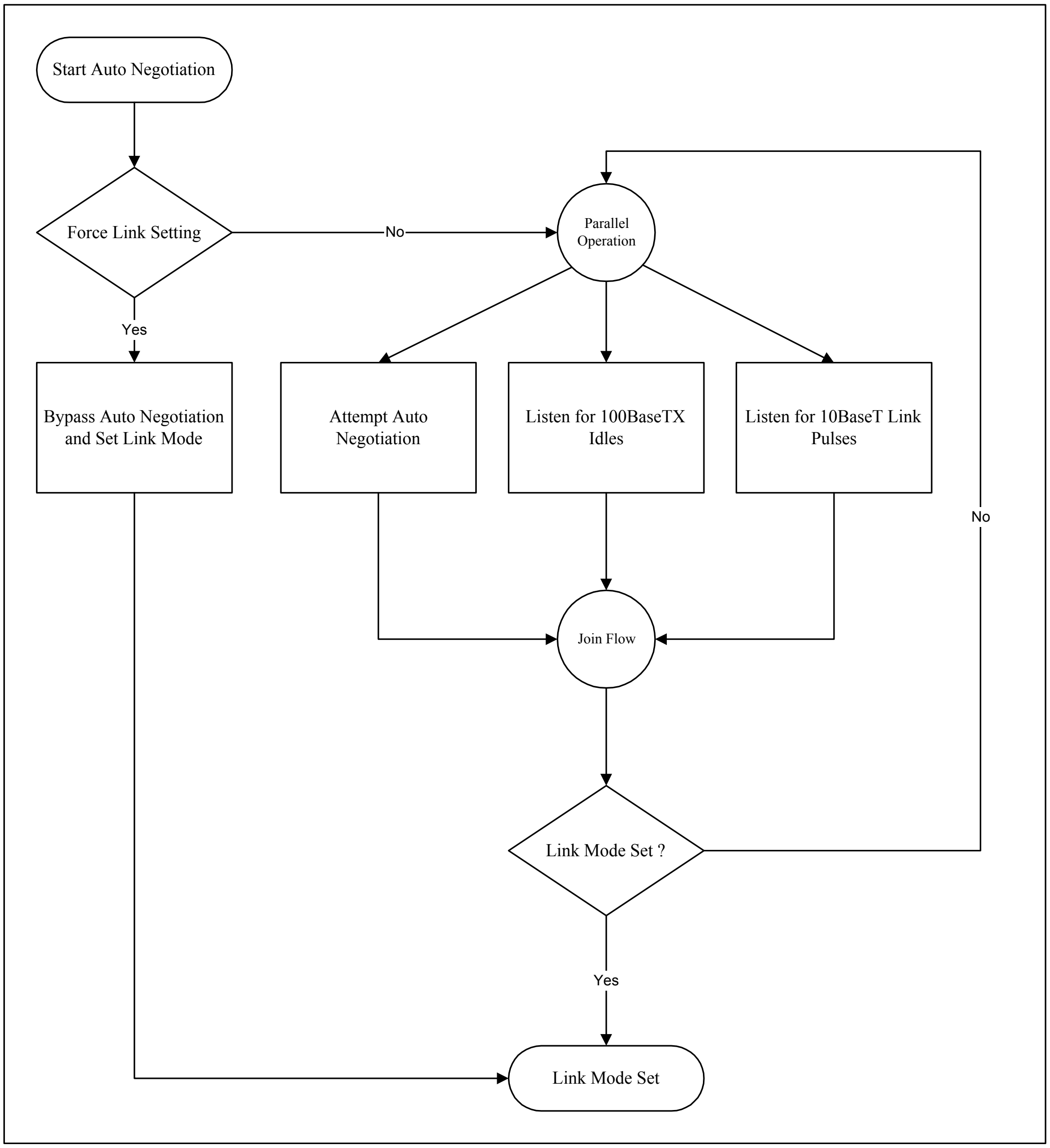


Figure 1-Auto Negotiation

3.0 Functional Overview: Switch Core

3.1 Address Look Up

The internal look up table stores MAC addresses and their associated information. It contains a 1K unicast address table plus switching information. The KS8995M is guaranteed to learn 1K addresses and distinguishes itself from hash-based look up tables which, depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

3.2 Learning

The internal look up engine will update its table with a new entry if the following conditions are met:

(1). The received packet's SA does not exist in the look up table.
(2). The received packet is good; the packet has no receiving errors, and is of legal length.

The look up engine will insert the qualified SA into the table, along with the port number and time stamp. If the table is full, the last entry of the table will be deleted to make room for the new entry.

3.3 Migration

The internal look up engine also monitors whether a station has moved. If so, it will update the table accordingly. Migration happens when the following conditions are met:

(1). The received packet's SA is in the table but the associated source port information is different.
(2). The received packet is good; the packet has no receiving errors, and is of legal length.

The look up engine will update the existing record in the table with the new source port information.

3.4 Aging

The look up engine will update the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the look up engine will remove the record from the table. The look up engine constantly performs the aging process and will continuously remove aging records. The aging period is 300 $\pm$ 75 seconds. This feature can be enabled or disabled through register 3 or by external pull-up or pull-down resistors on LED[5][2] (See section 5.1.4).

3.5 Forwarding

The KS8995M will forward packets using an algorithm that is depicted in the following flowcharts. Figure 2 shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and comes up with “port to forward 1” (PTF1). PTF1 is then further modified by the Spanning Tree, IGMP snooping, port mirroring, and port VLAN processes to come up with “port to forward 2” (PTF2) as shown in Figure 3. This is where the packet will be sent.

Figure 2 DA look up flowchart, stage 1

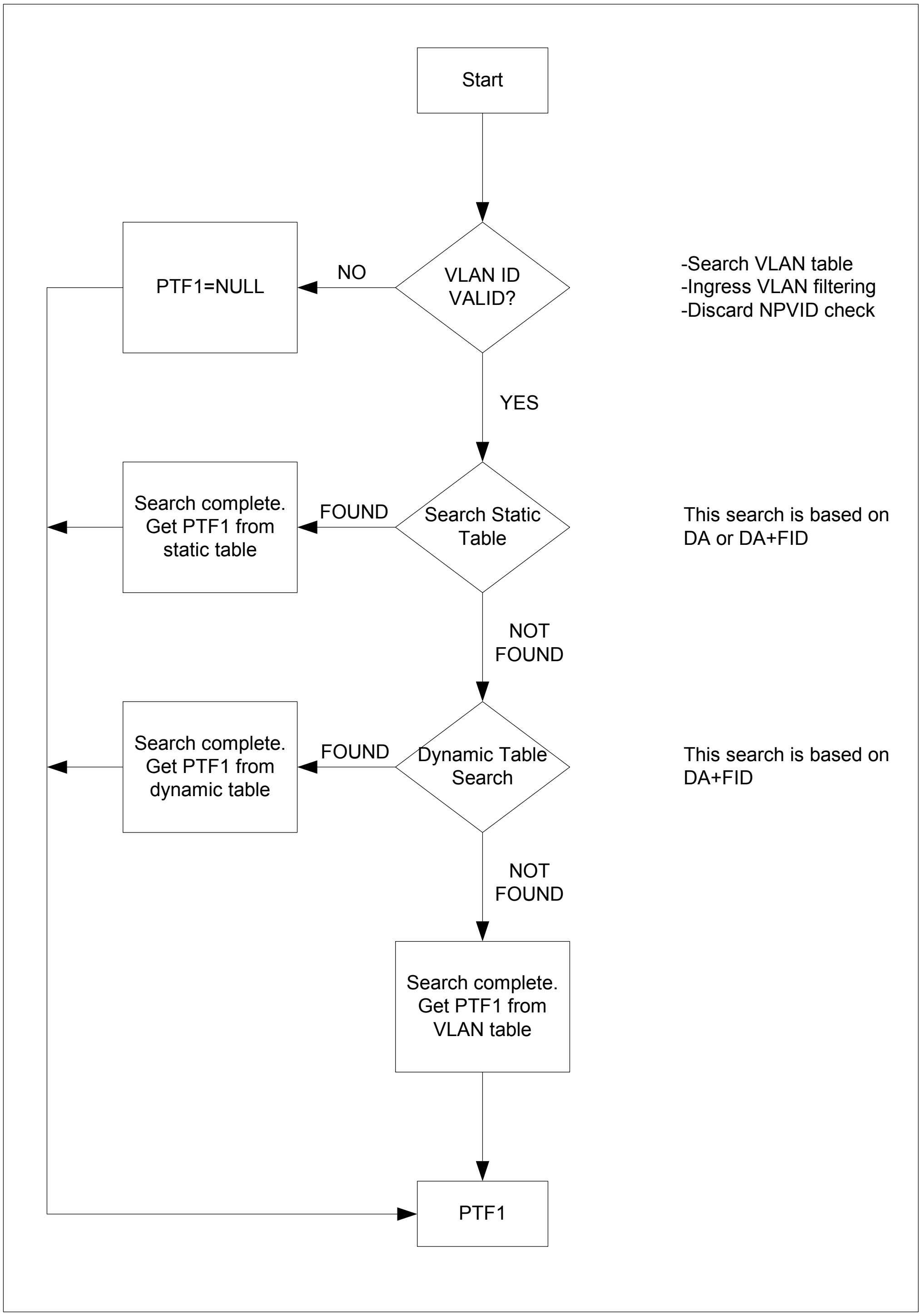
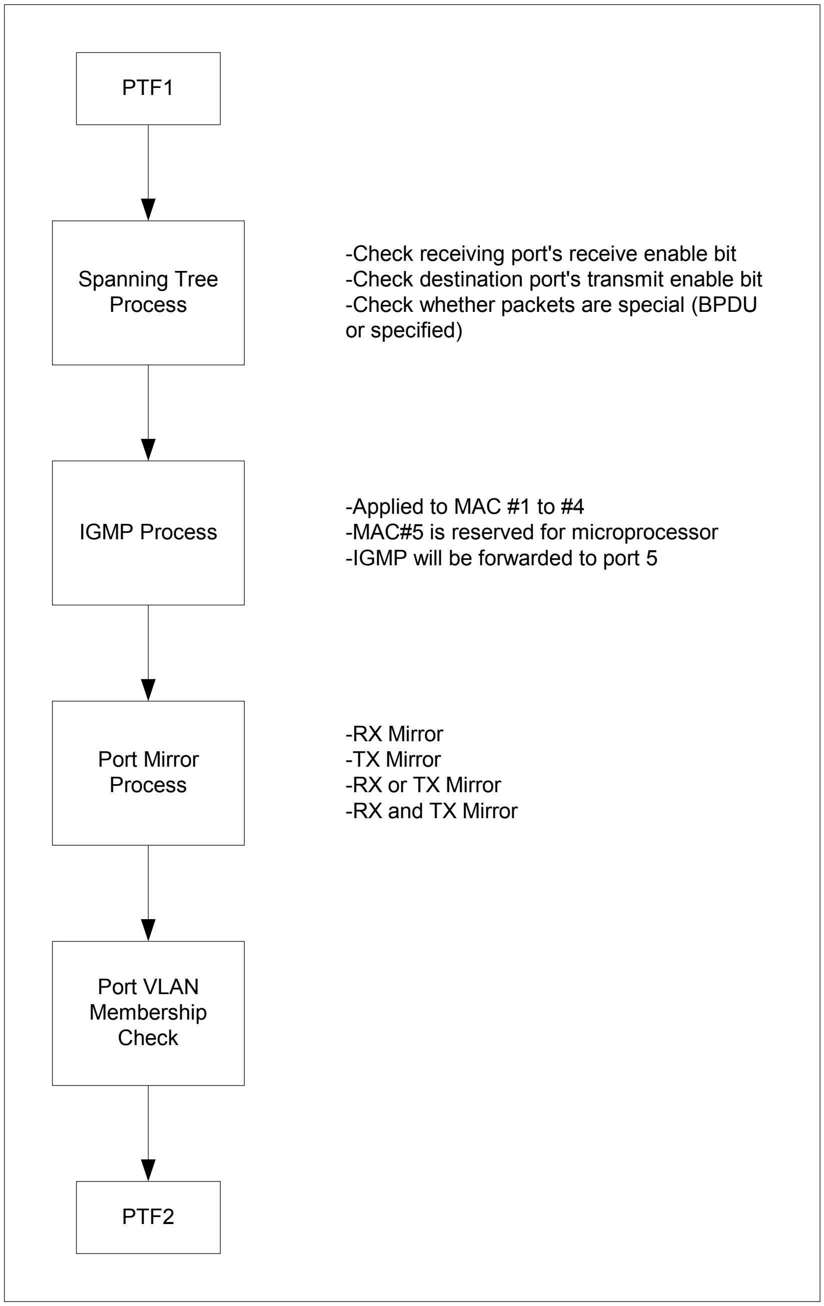


Figure 3 DA resolution flowchart, stage 2



The KS8995M will not forward the following packets:

(1). Error packets. These include framing errors, FCS errors, alignment errors, and illegal size packet errors.
(2). 802.3x pause frames. The KS8995M will intercept these packets and perform the appropriate actions.
(3). "Local" packets. Based on destination address (DA) look up. If the destination port from the look up table matches the port where the packet was from, the packet is defined as "local".

3.6 Switching Engine

The KS8995M features a high performance switching engine to move data to and from the MAC's, packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency.

The KS8995M has a 64kB internal frame buffer. This resource is shared between all five ports. The buffer sharing mode can be programmed through register 2 (See section 5.1.3). In one mode, ports are allowed to use any free buffers in the buffer pool. In the second mode, each port is only allowed to use 1/5 of the total buffer pool. There are a total of 512 buffers available. Each buffer sized at 128B.

3.7 MAC operation

The KS8995M strictly abides by IEEE 802.3 standards to maximize compatibility.

Inter Packet Gap (IPG)

If a frame is successfully transmitted, the 96 bit time IPG is measured between the two consecutive MTXEN. If the current packet is experiencing collision, the 96 bit time IPG is measured from MCRS and the next MTXEN.

3.7.1 Backoff Algorithm

The KS8995M implements the IEEE Std 802.3 binary exponential back-off algorithm, and optional "aggressive mode" back off. After 16 collisions, the packet will be optionally dropped depending on the chip configuration in register 3. (See section 5.1.4)

3.7.2 Late Collision

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet will be dropped.

3.7.3 Illegal Frames

The KS8995M discards frames less than 64 bytes and can be programmed to accept frames up to 1536 bytes in register 4. For special applications, the KS8995M can also be programmed to accept frames up to 1916 bytes in register 4. Since the KS8995M supports VLAN tags, the maximum sizing is adjusted when these tags are present. See the EEPROM section for programming options.

3.7.4 Flow Control

The KS8995M supports standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KS8995M receives a pause control frame, the KS8995M will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (being flow controlled), only flow control packets from the KS8995M will be transmitted.

On the transmit side, the KS8995M has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues and available receive queues.

The KS8995M will flow control a port, which just received a packet, if the destination port resource is being used up. The KS8995M will issue a flow control frame (XOFF), containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the KS8995M will send out the other flow control frame (XON) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being activated and deactivated too many times.

The KS8995M will flow control all ports if the receive queue becomes full.

3.7.5 Half Duplex Back Pressure

A half duplex back pressure option (Note: not in 802.3 standards) is also provided. The activation and deactivation conditions are the same as the above in full duplex mode. If back pressure is required, the KS8995M will send preambles to defer the other stations' transmission (carrier sense deference). To avoid jabber and excessive deference defined in 802.3 standard, after a certain time it will discontinue the carrier sense but it will raise the carrier sense quickly. This short silent time (no carrier sense) is to prevent other stations from sending out packets and keeps other stations in carrier sense deferred state. If the port has packets to send during a back pressure situation, the carrier sense type back pressure will be interrupted and those packets will be transmitted instead. If there are no more packets to send, carrier sense type back pressure will be active again until switch resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, reducing the chance of further colliding and maintaining carrier sense to prevent reception of packets.

To ensure no packet loss in 10 Base T or 100 Base TX half duplex modes, the user must enable the following:

1. Aggressive Backoff (register 3, bit 0)
2. No Excessive collision drop (register 4, bit 3)
3. Back Pressure (register 4, bit 5)

These bits are not set as the default because this is not the IEEE standard.

3.7.6 Broadcast Storm Protection

The KS8995M has an intelligent option to protect the switch system from receiving too many broadcast packets. Broadcast packets will be forwarded to all ports except the source port, and thus use too many switch resources (bandwidth and available space in transmit queues). The KS8995M has the option to include "multicast packets" for storm control. The broadcast storm rate parameters are programmed globally, and can be enabled or disabled on a per port basis. The rate is based on a 50ms interval for 100BT and a 500 ms interval for 10BT. At the beginning of each interval, the counter is cleared to zero, and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in register 6 and register 7. The default setting for registers 6 and 7 is 0x4A, which is 74 decimal. This is equal to a rate of 1 %, calculated as follows:

148,800 frames/sec * 50 ms/interval * 1% = 74 frames/interval (approx.) = 0x4A

3.8 MII Interface Operation

The MII (Media Independent Interface) is specified by the IEEE 802.3 committee and provides a common interface between physical layer and MAC layer devices. The KS8995M provides two such interfaces. The MII-P5 interface is used to connect to the fifth PHY, whereas the MII-SW interface is used to connect to the fifth MAC. Each of these MII interfaces contains two distinct groups of signals, one being for transmission and the other for receiving. The table below describes the signals used in the MII-P5 interface.

Table 1 – MII-P5 Signals (PHY Mode)

MII signal	Description	KS8995M signal
MTXEN	Transmit enable	PMTXEN
MTXER	Transmit error	PMTXER
MTXD3	Transmit data bit 3	PMTXD[3]
MTXD2	Transmit data bit 2	PMTXD[2]
MTXD1	Transmit data bit 1	PMTXD[1]
MTXD0	Transmit data bit 0	PMTXD[0]
MTXC	Transmit clock	PMTXC
MCOL	Collision detection	PCOL
MCRS	Carrier sense	PCRS
MRXDV	Receive data valid	PMRXDV
MRXER	Receive error	PMRXER
MRXD3	Receive data bit 3	PMRXD[3]
MRXD2	Receive data bit 2	PMRXD[2]
MRXD1	Receive data bit 1	PMRXD[1]
MRXD0	Receive data bit 0	PMRXD[0]
MRXC	Receive clock	PMRXC
MDC	Management Data Clock	MDC
MDIO	Management Data I/O	MDIO

Table 2 - MII-SW Signals

PHY mode connections			**MAC mode connections**	
External MAC	KS8995M signal	Description	External PHY	KS8995M signal
MTXEN	SMTXEN	Transmit enable	MTXEN	SMRXDV
MTXER	SMTXER	Transmit error	MTXER	Not used
MTXD3	SMTXD[3]	Transmit data bit 3	MTXD3	SMRXD[3]
MTXD2	SMTXD[2]	Transmit data bit 2	MTXD2	SMRXD[2]
MTXD1	SMTXD[1]	Transmit data bit 1	MTXD1	SMRXD[1]
MTXD0	SMTXD[0]	Transmit data bit 0	MTXD0	SMRXD[0]
MTXC	SMTXC	Transmit clock	MTXC	SMRXC
MCOL	SCOL	Collision detection	MCOL	SCOL
MCRS	SCRS	Carrier sense	MCRS	SCRS
MRXDV	SMRXDV	Receive data valid	MRXDV	SMTXEN
MRXER	Not used	Receive error	MRXER	SMTXER
MRXD3	SMRXD[3]	Receive data bit 3	MRXD3	SMTXD[3]
MRXD2	SMRXD[2]	Receive data bit 2	MRXD2	SMTXD[2]
MRXD1	SMRXD[1]	Receive data bit 1	MRXD1	SMTXD[1]
MRXD0	SMRXD[0]	Receive data bit 0	MRXD0	SMTXD[0]
MRXC	SMRXC	Receive clock	MRXC	SMTXC

The MII-P5 interface operates in PHY mode only, while the MII-SW interface operates in either MAC mode or PHY mode. These interfaces are nibble wide data interfaces and therefore run at ¼ the network bit rate (not encoded). Additional signals on the transmit side indicate when data is valid or when an error occurs during transmission. Likewise, the receive side has indicators that convey when the data is valid and without physical layer errors. For half duplex operation there is a signal that indicates a collision has occurred during transmission.

Note that the signal MRXER is not provided on the MII-SW interface for PHY mode operation and the signal MTXER is not provided on the MII-SW interface for MAC mode operation. Normally MRXER would indicate a receive error coming from the physical layer device. MTXER would indicate a transmit error from the MAC device. These signals are not appropriate for this configuration. For PHY mode operation, if the device interfacing with the KS8995M has an MRXER pin, it should be tied low. For MAC mode operation, if the device interfacing with the KS8995M has an MTXER pin, it should be tied low.

3.9 SNI Interface Operation

The SNI (Serial Network Interface) is compatible with some controllers used for network layer protocol processing. This interface can be directly connected to these types of devices. The signals are divided into two groups, one being for transmission and the other for reception. The signals involved are described in the table below.

Table 3-SNI Signals

SNI signal	Description	KS8995M signal
TXEN	Transmit enable	SMTXEN
TXD	Serial transmit data	SMTXD[0]
TXC	Transmit clock	SMTXC
COL	Collision detection	SCOL
CRS	Carrier sense	SMRXDV
RXD	Serial receive data	SMRXD[0]
RXC	Receive clock	SMRXC

This interface is a bit wide data interface and therefore runs at the network bit rate (not encoded). An additional signal on the transmit side indicates when data is valid. Likewise, the receive side has an indicator that conveys when the data is valid.

For half duplex operation there is a signal that indicates a collision has occurred during transmission.

4.0 KS8995M Advanced Functionality

4.1 Spanning Tree Support:

To support spanning tree, port 5 is the designated port for the processor.

The other ports (port 1 – port 4) can be configured in one of the five spanning tree states via "transmit enable", "receive enable" and "learning disable" register settings in registers 18, 34, 50, and 66 for ports 1, 2, 3 and 4 respectively. The following description shows the port setting and software actions taken for each of the five spanning tree states.

Disable state: The port should not forward or receive any packets. Learning is disabled.
Port setting: "transmit enable = 0, receive enable = 0, learning disable =1"
Software action: the processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the static table with "overriding bit" set) and the processor should discard those packets. Note: processor is connected to port 5 via MII interface. Address learning is disabled on the port in this state.

Blocking state: only packets to the processor are forwarded. Learning is disabled.
Port setting: "transmit enable = 0, receive enable = 0, learning disable =1"
Software action: the processor should not send any packets to the port(s) in this state. The processor should program the "Static Mac table" with the entries that it needs to receive (e.g. BPDU packets). The "overriding" bit should also be set so that the switch will forward those specific packets to the processor. Address learning is disabled on the port in this state.

Listening state: only packets to and from the processor are forwarded. Learning is disabled.
Port setting: "transmit enable = 0, receive enable = 0, learning disable =1"
Software action: The processor should program the "Static MAC table" with the entries that it needs to receive (e.g. BPDU packets). The "overriding" bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state, see "special tagging" mode (section 4.2) for details. Address learning is disabled on the port in this state.

Learning state: only packets to and from the processor are forwarded. Learning is enabled
Port setting: "transmit enable = 0, receive enable = 0, learning disable = 0"
Software action: The processor should program the "Static MAC table" with the entries that it needs to receive (e.g. BPDU packets). The "overriding" bit should be set so that the switch will forward those specific packets to the processor.

The processor may send packets to the port(s) in this state, see “special tagging” mode for details. Address learning is enabled on the port in this state.

Forwarding state: packets are forwarded and received normally. Learning is enabled.
Port setting: “transmit enable = 1, receive enable = 1, learning disable = 0”
Software action: The processor should program the “Static MAC table” with the entries that it needs to receive (e.g. BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state, see “special tagging” mode for details. Address learning is enabled on the port in this state.

4.2 Special Tagging Mode

The special tagging mode is designed for Spanning Tree protocol IGMP snooping and is flexible for use in other applications. The special tagging mode, similar to 802.1Q, requires software to change network drivers to insert/modify/strip/interpret the special tag. This mode is enabled by setting both register 11 bit 0 and register 80 bit 2.

Table 4-Special Tagging Mode Format

802.1Q tag format	Special tag format
TPID (tag protocol identifier, 0x8100) + TCI.	STPID(special tag identifier, 0x810 + 4 bit for “port mask”) + TCI

The STPID will only be seen and used on the port 5 interface, which should be connected to a processor. Packets from the processor to the switch should be tagged with STPID and the port mask defined as below:
“0001”, packet to port 1 only.
“0010”, packet to port 2 only
“0100”, packet to port 3 only
“1000”, packet to port 4 only
“0011”, packet broadcast to port 1 and port 2.
…..
“1111” packet broadcast to port 1, 2, 3 and 4.
“0000” normal tag, will use KS8995M internal look up result. Normal packets should use this setting. If packets from the processors do not have a tag, the KS8995M will treat them as normal packets and an internal look up will be performed.

The KS8995M uses a non-zero “port mask” to bypass the look up result and override any port setting, regardless of port states (blocking, disable, listening, learning). The table below shows the egress rules when dealing with STPID.

Table 5-STPID Egress Rules (Processor to Switch Port 5)

Ingress tag field	Tx port "tag insertion"	Tx port "tag removal"	Egress Action to tag field
(0x810+ port mask)	0	0	-Modify tag field to 0x8100 -recalculate CRC -no change to TCI if not null VID -replace VID with ingress (port 5) port VID if null VID
(0x810+ port mask)	0	1	-(STPID + TCI) will be removed. -padding to 64 bytes if necessary -recalculate CRC
(0x810+ port mask)	1	0	-Modify tag field to 0x8100 -recalculate CRC -no change to TCI if not null VID -replace VID with ingress (port 5) port VID if null VID
(0x810+ port mask)	1	1	-Modify tag field to 0x8100 -recalculate CRC -no change to TCI if not null VID -replace VID with ingress (port 5) port VID if null VID
Not Tagged	Don't care	Don't care	Determined by the dynamic MAC address table.

For packets from regular ports (port 1 – port 4) to port 5, the port mask is used to tell the processor which port the packet was received on, defined as
"0001" from port 1,
"0010" from port 2,
"0100" from port 3,
"1000" from port 4.

No values other than the previous four defined should be received in this direction in the special mode. The egress rule for this direction is defined as,

Table 6-STPID Egress Rules (Switch to Processor)

Ingress packets	Egress Action to tag field
Tagged with 0x8100 + TCI	-Modify TPID to 0x810 + "port mask", which indicates source port. -no change to TCI, if VID is not Null -replace Null VID with ingress port VID. -recalculate CRC
Not tagged.	-Insert TPID to 0x810 + "port mask", which indicates source port. –Insert TCI with ingress port VID -recalculate CRC

4.3 IGMP Support

There are two parts involved to support IGMP in layer 2. The first part is "IGMP" snooping. The switch will trap IGMP packets and forward them only to the processor port. The IGMP packets are identified as IP packets (either Ethernet IP packets or IEEE 802.3 SNAP IP packets) AND IP version = 0x4 AND protocol number = 0x2. The second part is "multicast address insertion" in the static MAC table. Once the multicast address is programmed in the static MAC table, the multicast session will be trimmed to the subscribed ports, instead of broadcasting to all ports. To enable this feature, set register 5 bit 6 to 1. Also "special tag mode" needs to be enabled, so that the processor knows which port the IGMP packet was received on. Enable "special tag mode" by setting both register 11 bit 0 and register 80 bit 2.

4.4 Port Mirroring Support

KS8995M supports "port mirror" comprehensively as:

(1), "receive only" mirror on a port. All the packets received on the port will be mirrored on the sniffer port. For example, port 1 is programmed to be "rx sniff", and port 5 is programmed to be the "sniffer port". A packet, received on port 1, is destined to port 4 after the internal look up. The KS8995M will forward the packet to both port 4 and port 5. KS8995M can optionally forward even "bad" received packets to port 5.

(2), "transmit only" mirror on a port. All the packets transmitted on the port will be mirrored on the sniffer port. For example, port 1 is programmed to be "tx sniff", and port 5 is programmed to be the "sniffer port". A packet, received on any of the ports, is destined to port 1 after the internal look up. The KS8995M will forward the packet to both port 1 and port 5.

(3), “receive and transmit” mirror on two ports. All the packets received on port A AND transmitted on port B will be mirrored on the sniffer port. To turn on the “AND” feature, set register 5 bit 0 to 1. For example, port 1 is programmed to be “rx sniff”, port 2 is programmed to be “transmit sniff” and port 5 is programmed to be the “sniffer port”. A packet, received on port 1, is destined to port 4 after the internal look up. The KS8995M will forward the packet to port 4 only, since it does not meet the “AND” condition. A packet, received on port 1, is destined to port 2 after the internal look up. The KS8995M will forward the packet to both port 2 and port 5.

Multiple ports can be selected to be “rx sniffed” or “tx sniffed”. And any port can be selected to be the “sniffer port”. All these per port features can be selected through register 17.

4.5 VLAN support

KS8995M supports 16 active VLANs out of 4096 possible VLANs specified in IEEE 802.1Q. KS8995M provides a 16-entry VLAN table, which converts VID (12 bits) to FID (4bits) for address look up. If a non-tagged or null-VID-tagged packet is received, the ingress port VID is used for look up. In the VLAN mode, the look up process starts with VLAN table look up to determine whether the VID is valid. If the VID is not valid, the packet will be dropped and its address will not be learned. If the VID is valid, FID is retrieved for further look up. FID+DA is used to determine the destination port. FID+SA is used for learning purposes.

Table 7-FID+DA look up in the VLAN mode

DA found in Static MAC table	USE FID flag?	FID match?	DA+FID found in dynamic MAC table	Action
No	Don’t care	Don’t care	No	Broadcast to the membership ports defined in the VLAN table bit [20:16]
No	Don’t care	Don’t care	Yes	Send to the destination port defined in the dynamic MAC table bit[54:52]
Yes	0	Don’t care	Don’t care	Send to the destination port(s) defined in the static MAC table bit[52:48]
Yes	1	No	No	Broadcast to the membership ports defined in the VLAN

				table bit [20:16]
Yes	1	No	Yes	Send to the destination port defined in the dynamic MAC table bit[54:52]
Yes	1	Yes	Don't care	Send to the destination port(s) defined in the static MAC table bit[52:48]

Table 8-FID+SA look up in the VLAN mode

SA+FID found in dynamic MAC table	Action
No	The SA+FID will be learned into the dynamic table.
Yes	Time stamp will be updated.

Advanced VLAN features are also supported in KS8995M, such as "VLAN ingress filtering" and "discard non PVID" defined in register 18 bit 6 and bit 5. These features can be controlled on a port basis.

4.6 Rate Limit Support

KS8995M supports hardware rate limiting on "receive" and "transmit" independently on a per port basis. It also supports rate limiting in a priority or non-priority environment. The rate limit starts from 0 kbps and goes up to the line rate in steps of 32 kbps. The KS8995M uses one second as an interval. At the beginning of each interval, the counter is cleared to zero, and the rate limit mechanism starts to count the number of bytes during this interval.

For receive, if the number of bytes exceeds the programmed limit, the switch will stop receiving packets on the port until the "one second" interval expires. There is an option provided for flow control to prevent packet loss. If the rate limit is programmed greater than or equal to 128kbps and the byte counter is 8Kbytes below the limit, the flow control will be triggered. If the rate limit is programmed lower than 128kbps and the byte counter is 2Kbytes below the limit, the flow control will be triggered.

For transmit, if the number of bytes exceeds the programmed limit, the switch will stop transmitting packets on the port until the "one second" interval expires.

If priority is enabled, the KS8995M can support different rate controls for both high priority and low priority packets. This can be programmed through registers 21 – 27.

4.7 Configuration Interface

The KS8995M can function as a managed switch or unmanaged switch. If no EEPROM or micro-controller exists, the KS8995M will operate from its default setting. Some default settings are configured via strap in options as indicated in the table below.

Table 9 Strap-In Pin Summary

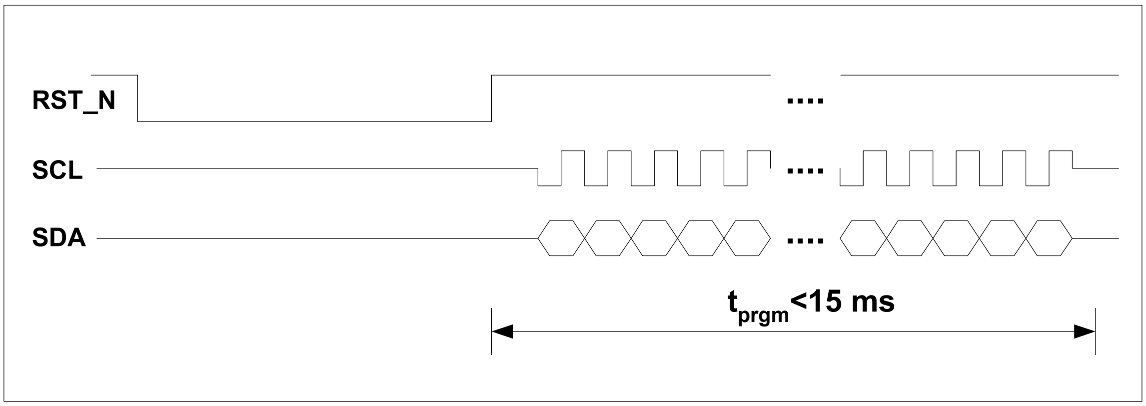
<table>
<tr><th>Pin #</th><th>Pin Name</th><th>PU/PD</th><th>Description</th></tr>
<tr><td>1</td><td>TEST1</td><td></td><td>NC for normal operation. Factory test pin.</td></tr>
<tr><td>45</td><td>MUX1</td><td>NC</td><td rowspan="2">MUX1 and MUX2 should be left unconnected for normal operation. They are factory test pins.
<table>
<tr><td>Mode</td><td>Mux1</td><td>Mux2</td></tr>
<tr><td>Normal Operation</td><td>NC</td><td>NC</td></tr>
<tr><td>Remote analog loopback mode for testing only</td><td>0</td><td>1</td></tr>
<tr><td>Reserved</td><td>1</td><td>0</td></tr>
<tr><td>power save mode for testing only</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>46</td><td>MUX2</td><td>NC</td></tr>
<tr><td>62</td><td>PMRXD3</td><td>Ipd / O</td><td>PHY[5] MII receive bit 3. Strap option: PD (default) = enable flow control; PU = disable flow control</td></tr>
<tr><td>63</td><td>PMRXD2</td><td>Ipd / O</td><td>PHY[5] MII receive bit 2. Strap option: PD (default) = disable back pressure; PU = enable back pressure</td></tr>
<tr><td>64</td><td>PMRXD1</td><td>Ipd / O</td><td>PHY[5] MII receive bit 1. Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets</td></tr>
<tr><td>65</td><td>PMRXD0</td><td>Ipd / O</td><td>PHY[5] MII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement</td></tr>
<tr><td>66</td><td>PMRXER</td><td>Ipd / O</td><td>PHY[5] MII receive error. Strap option: PD = 1522/1518 bytes; PU (default) = packet size up to 1536 bytes</td></tr>
<tr><td>67</td><td>PCRS</td><td>Ipd / O</td><td>PHY[5] MII carrier sense/Force duplex mode (See section 5.2.13) For port 4 only. PD (default) = Force half duplex if auto-negotiation is disabled or fails. PU = Force full duplex if auto-negotiation is disabled or fails.</td></tr>
<tr><td>68</td><td>PCOL</td><td>Ipd / O</td><td>PHY[5] MII collision detect/ Force flow control (See section 5.2.3) For port 4 only. PD (default) = No force flow control. PU = Force flow control.</td></tr>
<tr><td>80</td><td>SMRXD3</td><td>Ipd / O</td><td>Switch MII receive bit 3. Strap option: PD (default) = Disable Switch MII full-duplex flow control; PU = Enable Switch MII full-duplex flow control</td></tr>
<tr><td>81</td><td>SMRXD2</td><td>Ipd / O</td><td>Switch MII receive bit 2. Strap option: PD (default) = Switch MII in full duplex mode; PU = Switch MII in half-duplex mode.</td></tr>
<tr><td>82</td><td>SMRXD1</td><td>Ipd / O</td><td>Switch MII receive bit 1. Strap option: PD (default) = Switch MII in 100Mbps mode; PU = Switch MII in 10Mbps mode</td></tr>
<tr><td>83</td><td>SMRXD0</td><td>Ipd / O</td><td>Switch MII receive bit 0; Strap option: LED Mode
PD (default) = Mode 0; PU = Mode 1. See also register 11.</td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td>
<table>
<tr><td></td><td>Mode 0</td><td>Mode 1</td></tr>
<tr><td>LEDX_2</td><td>Lnk/Act</td><td>100Lnk/act</td></tr>
<tr><td>LEDX_1</td><td>Fulld/Col</td><td>10Lnk/act</td></tr>
<tr><td>LEDX_0</td><td>Speed</td><td>Fulld</td></tr>
</table>
</td></tr>
<tr><td>86</td><td>SCONF1</td><td>Ipd</td><td>Dual MII configuration pin.
<table>
<tr><td>Pin# (91,86,87):</td><td>Switch MII</td><td>PHY[5] MII</td></tr>
<tr><td>000</td><td>Disable, Otri</td><td>disable, Otri</td></tr>
<tr><td>001</td><td>phy mode MII</td><td>disable, Otri</td></tr>
<tr><td>010</td><td>mac mode MII</td><td>disable, Otri</td></tr>
<tr><td>011</td><td>phy mode SNI</td><td>disable, Otri</td></tr>
<tr><td>100</td><td>Disable</td><td>Disable</td></tr>
<tr><td>101</td><td>phy mode MII</td><td>phy mode MII</td></tr>
<tr><td>110</td><td>mac mode MII</td><td>phy mode MII</td></tr>
<tr><td>111</td><td>phy mode SNI</td><td>phy mode MII</td></tr>
</table>
</td></tr>
<tr><td>87</td><td>SCONF0</td><td>Ipd</td><td>Dual MII configuration pin</td></tr>
<tr><td>90</td><td>LED5-2</td><td>Ipu / O</td><td>LED indicator 2. Strap option: Aging setup. See section 3.4 PU (default) = Aging Enable; PD = Aging disable.</td></tr>
<tr><td>91</td><td>LED5-1</td><td>Ipu / O</td><td>LED indicator 1. Strap option: PU (default): enable PHY MII I/F. PD: tristate all PHY MII output. See pin#86 SCONF1.</td></tr>
<tr><td>113</td><td>PS1</td><td>Ipd</td><td>Serial bus configuration pin
If EEPROM is not present, the KS8995M will start itself with chip default (00)..
<table>
<tr><td>Pin Config</td><td>Serial bus configuration</td></tr>
<tr><td>PS[1:0]=00</td><td>I2C master mode for EEPROM</td></tr>
<tr><td>PS[1:0]=01</td><td>Reserved</td></tr>
<tr><td>PS[1:0]=10</td><td>SPI slave mode for CPU interface</td></tr>
<tr><td>PS[1:0]=11</td><td>Factory test mode (BIST)</td></tr>
</table>
</td></tr>
<tr><td>114</td><td>PS0</td><td>Ipd</td><td>Serial bus configuration pin. See pin#113 description</td></tr>
<tr><td>128</td><td>TEST2</td><td>NC</td><td>NC for normal operation. Factory test pin.</td></tr>
</table>

4.7.1 I2C Master Serial bus configuration

If a 2-wire EEPROM exists, the KS8995M can perform more advanced features like “broadcast storm protection”, “rate control”, etc. The EEPROM should have the entire valid configuration data from register 0 to register 109 defined in the memory map, except the status registers. After reset, the KS8995M will start to read all 110 registers sequentially from the EEPROM. The configuration access time (t_{prgm}) is less than 15ms as shown in figure Figure 4.

Figure 4 KS8995M EEPROM Configuration Timing Diagram



To configure the KS8995M with a pre-configured EEPROM use the following steps:

1. At the board level, connect pin 110 on the KS8995M to the SCL pin on the EEPROM. Connect pin 111 on the KS8995M to the SDA pin on the EEPROM.
2. Set the input signals PS[1:0] (pins 113 and 114 respectively) to “00”. This puts the KS8995M serial bus configuration into I2C master mode.
3. Be sure the board level reset signal is connected to the KS8995M reset signal on pin 115 (RST_N).
4. Program the contents of the EEPROM before placing it on the board with the desired configuration data. Note that the first byte in the EEPROM must be “95” for the loading to occur properly. If this value is not correct, all other data will be ignored.
5. Place EEPROM on the board and power up the board. Assert the active-low board level reset to RST_N on the KS8995M. After the reset is deasserted, the KS8995M will begin reading configuration data from the EEPROM. The configuration access time (t_{prgm}) is less than 15ms.

Note: For proper operation, make sure that pin 47 (PWRDN_N) is not asserted during the reset operation.

4.7.2 SPI Slave Serial Bus Configuration

The KS8995M can also act as an SPI slave device. Through the SPI, the entire feature set can be enabled, including "VLAN", "IGMP snooping", " MIB counters" etc. The external master device can access any register from register 0 to register 127 randomly. The system should configure all the desired settings before enabling the switch in the KS8995M. To enable the switch, write a one to register 1 bit 0.

Two standard SPI commands are supported (00000011 for "READ DATA", and 00000010 for "WRITE DATA"). To speed configuration time, the KS8995M also supports multiple reads or writes. After a byte is written to or read from the KS8995M, the internal address counter automatically increments if the SPI Slave Select signal (SPIS_N) continues to be driven low. If SPIS_N is kept low after the first byte is read, the next byte at the next address will be shifted out on SPIQ. If SPIS_N is kept low after the first byte is written, bits on the Master Out Slave Input (SPID) line will be written to the next address. Asserting SPIS_N high terminates a read or write operation. This means that the SPIS_N signal must be asserted high and then low again before issuing another command and address. The address counter wraps back to zero once it reaches the highest address. Therefore the entire register set can be written to or read from by issuing a single command and address.

The KS8995M is able to support a 5MHz SPI bus. A high performance SPI master is recommended to prevent internal counter overflow.

To use the KS8995M SPI:

1. At the board level, connect KS8995M pins as follows:

Table 10 KS8995M SPI Connections

KS8995M Pin No.	KS8995M Signal Name	Microprocessor Signal Description
112	SPIS_N	SPI Slave Select
110	SPIC	SPI Clock
111	SPID	Master Out Slave Input
109	SPIQ	Master In Slave Output

2. Set the input signals PS[1:0] (pins 113 and 114 respectively) to "10" to set the serial configuration to SPI slave mode.
3. Power up the board and assert a reset signal. After reset, the start switch bit in register 1 will be set to '0'. Configure the desired settings in the KS8995M before setting the start register to '1'.

4. Write configuration to registers using a typical SPI write data cycle as shown in Figure 5 or SPI multiple write as shown in Figure 7. Note that data input on SPID is registered on the rising edge of SPIC.
5. Registers can be read and configuration can be verified with a typical SPI read data cycle as shown in Figure 6 or a multiple read as shown in Figure 8. Note that read data is registered out of SPIQ on the falling edge of SPIC.
6. After configuration is written and verified, write a '1' to register 1 bit 0 to begin KS8995M operation.

Figure 5 SPI Write Data Cycle

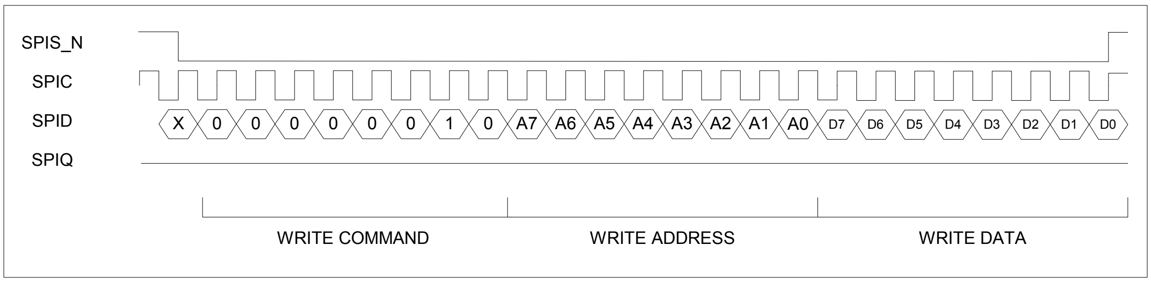


Figure 6 SPI Read Data Cycle

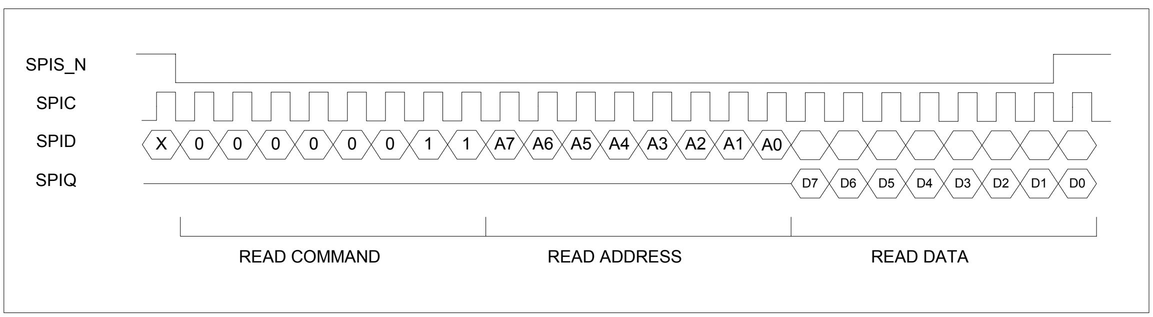


Figure 7 SPI Multiple Write

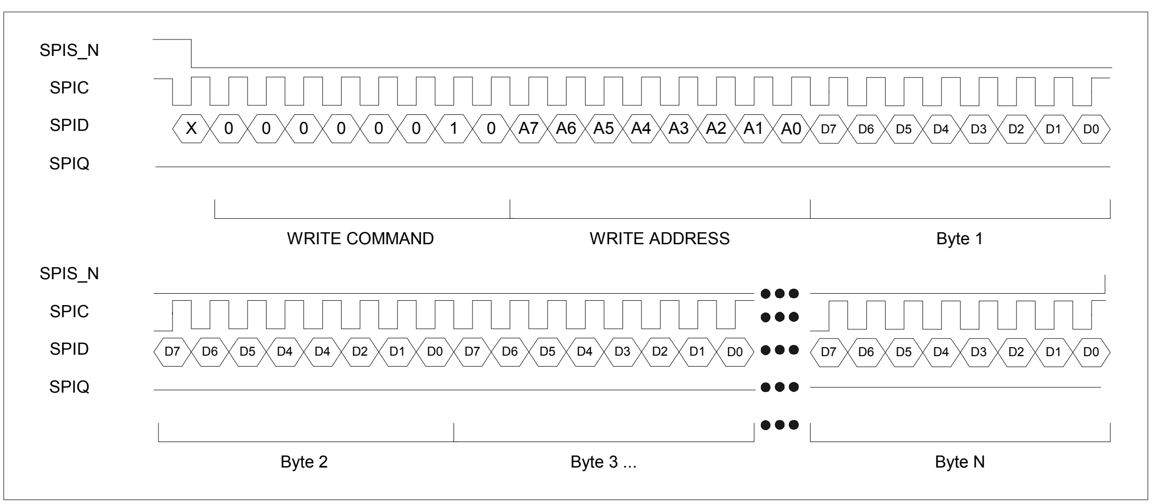
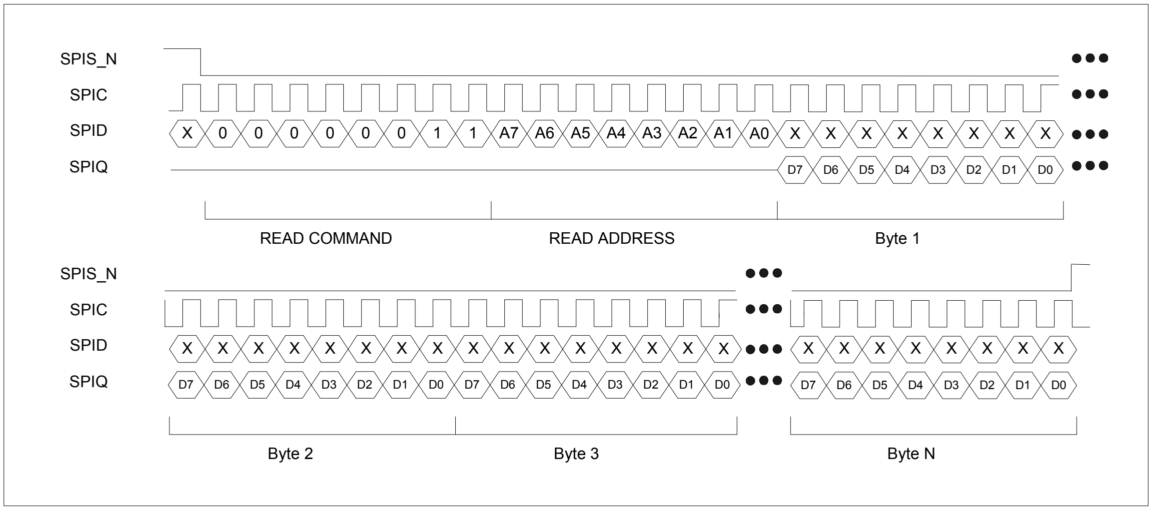


Figure 8 SPI Multiple Read



4.8 MII Management Interface (MIIM)

A standard MIIM interface is provided for all five PHY devices in the KS8995M. An external device with MDC/MDIO capability is able to read PHY status or to configure PHY settings. For details on the MIIM interface standard please reference the IEEE 802.3 specification section 22.2.4.5. The MIIM interface does not have access to all the configuration registers in the KS8995M. It can only access the standard MII registers. (See section 5.4). The SPI interface, on the other hand, can be used to access the entire KS8995M feature set.

5.0 Register Description

Table 11-Master Register Map

Offset		
Decimal	**Hex**	**Description**
0-1	0x00-0x01	Chip ID Registers
2-11	0x02-0x0B	Global Control Registers
12-15	0x0C-0x0F	Reserved
16-29	0x10-0x1D	Port 1 Control Registers
30-31	0x1E-0x2F	Port 1 Status Registers
32-45	0x20-0x2D	Port 2 Control Registers
46-47	0x2E-0x2F	Port 2 Status Registers
48-61	0x30-0x3D	Port 3 Control Registers
62-63	0x3E-0x3F	Port 3 Status Registers
64-77	0x40-0x4D	Port 4 Control Registers
78-79	0x4E-0x4F	Port 4 Status Registers
80-93	0x50-0x5D	Port 5 Control Registers
94-95	0x5E-0x5F	Port 5 Status Registers
96-103	0x60-0x67	TOS Priority Control Registers
104-109	0x68-0x6D	MAC Address Registers
110-111	0x6E-0x6F	Indirect Access Control Registers
112-120	0x70-0x78	Indirect Data Registers
121-122	0x79-0x7A	Digital Testing Status Registers
123-124	0x7B-0x7C	Digital Testing Control Registers
125-126	0x7D-0x7E	Analog Testing Control Registers
127	0x7F	Analog Testing Status Register

5.1 Global Registers

5.1.1 Register 0 (0x00): Chip ID0

Bit	Name	R/W	Description	Default
7-0	Family ID	RO	Chip family	0x95

5.1.2 Register 1 (0x01): Chip ID1 / Start Switch

Bit	Name	R/W	Description	Default
7-4	Chip ID	RO	0x0 is assigned to M series. (95M)	0x0
3-1	Revision ID	RO	Revision ID	0x2
0	Start Switch	RW	=1, start the chip when external pins (PS1, PS0) = (1,0) or (0,1) Note : in (PS1,PS0) = (0,0) mode, the chip will start automatically, after trying to read the external EEPROM. If EEPROM does not exist, the chip will use default values for all internal registers. If EEPROM is present,	-

			the contents in the EEPROM will be checked. The switch will check: (1) Register 0 = 0x95, (2) Register 1 [7:4] = 0x0. If this check is OK, the contents in the EEPROM will override chip register default values. =0, chip will not start when external pins (PS1, PS0) = (1,0) or (0,1) Note: (PS1, PS0) = (1,1) for factory test only.	

5.1.3 Register 2 (0x02): Global Control 0

Bit	Name	R/W	Description	Default
7	Reserved	R/W	Reserved	0x0
6-4	802.1p base priority	R/W	Used to classify priority for incoming 802.1Q packets. “user priority” is compared against this value. >= : classified as high priority < : classified as low priority	0x4
3	Enable PHY MII	R/W	=1, enable PHY MII interface (note: if not enabled, the switch will tri-state all outputs)	Pin LED[5][1] strap option. Pull down(0): isolate Pull up(1): Enable Note: LED[5][1] has internal pull up.
2	Buffer share mode	R/W	=1, buffer pool is shared by all ports. A port can use more buffer when other ports are not busy. =0, a port is only allowed to use 1/5 of the buffer pool	0x1
1	UNH mode	R/W	=1 the switch will drop packets with 0x8808 in T/L filed, or DA=01-80-C2-00-00-01 =0, the switch will drop packets qualified as “flow control” packets.	0
0	Link change age	R/W	=1, link change from “link” to “no link” will cause fast aging (<800us) to age address table faster. After an age cycle is complete, the age logic will return to normal (300 ± 75 seconds). Note: If any port is unplugged, all addresses will be automatically aged out.	0

5.1.4 Register 3 (0x03): Global Control 1

Bit	Name	R/W	Description	Default
7	Pass all frames	R/W	=1, switch all packets including bad ones. Used solely for debugging purpose. Works in conjunction with Sniffer mode.	0
6	Reserved	R/W	Reserved	0
5	IEEE 802.3x Transmit flow control	R/W	=0, will enable transmit flow control based on AN result. =1, will not enable transmit flow control no	Pin PMRXD3 strap option. Pull down(0):

	disable		matter what AN result is	Enable tx flow control Pull up(1): Disable tx/rx flow control Note: PMRXD3 has internal pull down
4	IEEE 802.3x Receive flow control disable	R/W	=0, will enable receive flow control based on AN result. =1, will not enable receive flow control no matter what AN result is Note: Bit 5 and bit 4 default values are controlled by the same pin, but they can be programmed independently.	Pin PMRXD3 strap option. Pull down(0): Enable rx flow control Pull up(1): Disable tx/rx flow control Note: PMRXD3 has internal pull down
3	Frame Length field check	R/W	1=Will check frame length field in the IEEE packets. If the actual length does not match, the packet will be dropped. (for L/T < 1500)	0
2	Aging enable	R/W	=1, Enable age function in the chip =0, Disable aging function	Pin LED[5][2] strap option. Pull down(0): Aging disable Pull up(1): Aging Enable Note: LED[5][2] has internal pull up.
1	Fast age enable	R/W	1=Turn on fast age (800us)	0
0	Aggressive back off enable	R/W	1=Enable more aggressive back off algorithm in half duplex mode to enhance performance. This is not an IEEE standard	Pin PMRXD0 strap option. Pull down(0): Disable aggressive back off Pull up(1): Aggressive back off Note: PMRXD0 has internal pull down

5.1.5 Register 4 (0x04): Global Control 2

Bit	Name	R/W	Description	Default
7	Unicast port-VLAN mismatch discard	R/W	This feature is used for port-VLAN (described in reg17, reg33..) =1, all packets can not cross VLAN boundary =0, unicast packets (excluding unkown/mutlicast/broadcast) can cross VLAN boundary	1
6	Multicast Storm protection Disable	R/W	=1, "Broadcast Storm Protection" does not include multicast packets. Only DA=FFFFFFFFFFFF packets will be regulated. =0, "Broadcast Storm Protection" includes DA =FFFFFFFFFFFF and DA[40] = 1 packets.	1
5	Back pressure mode	R/W	=1, carrier sense based backpressure is selected. =0, collision based backpressure is selected.	1
4	Flow control and back pressure fair mode	R/W	=1, fair mode is selected. In this mode, if a flow control port and a non-flow control port talk to the same destination port, packets from the non-flow control port may be dropped. This is to prevent the flow control port from being flow controlled for an extended period of time. =0, in this mode, if a flow control port and a non-flow control port talk to the same destination port, the flow control port will be flow controlled. This may not be "fair" to the flow control port.	1
3	No excessive collision drop	R/W	=1, the switch will not drop packets when 16 or more collisions occur. =0, the switch will drop packets when 16 or more collisions occur.	Pin PMRXD1 strap option. Pull down(0): Drop excessive collision packets Pull up(1): Don't drop excessive collision packets Note: PMRXD1 has internal pull down
2	Huge packet support	R/W	=1, will accept packet sizes up to 1916 bytes (inclusive). This bit setting will override setting from bit 1 of the same register. =0, the max packet size will be determined	0

			by bit 1 of this register.	
1	Legal Maximum Packet size check disable	R/W	=1, will accept packet sizes up to 1536 bytes (inclusive). =0, 1522 bytes for tagged packets (not including packets with STPID from CPU to ports 1-4), 1518 bytes for untagged packets. Any packets larger than the specified value will be dropped.	Pin PMRXER strap option. Pull down(0): 1518/1522 byte packets Pull up(1): 1536 byte packets Note: PMRXER has internal pull down
0	Priority Buffer reserve	R/W	=1, Each output queue is pre-allocated 48 buffers, used exclusively for high priority packets. It is recommended to enable this when priority queue feature is turned on. =0, No reserved buffers for high priority packets.	0

5.1.6 Register 5 (0x05): Global Control 3

Bit	Name	R/W	Description	Default
7	802.1Q VLAN enable	R/W	=1, 802.1Q VLAN mode is turned on. VLAN table needs to set up before the operation. =0, 802.1Q VLAN is disabled	0
6	IGMP snoop enable on Switch MII interface	R/W	=1, IGMP snoop enabled. All the IGMP packets will be forwarded to Switch MII port. =0, IGMP snoop disabled.	0
5	Enable direct mode on Switch MII interface	R/W	=1, direct mode on port 5. This is a special mode for the Switch MII interface. Using preamble before MRXDV to direct switch to forward packets, bypassing internal look up. =0, normal operation	0
4	Enable pre tag on Switch MII interface	R/W	=1, packets forwarded to Switch MII interface will be pre-tagged with the source port number. (preamble before MRXDV) =0, normal operation	0
3-2	Priority Scheme select	R/W	00 = always deliver high priority packets first 01 = deliver high/low packets at ratio 10/1 10 = deliver high/low packets at ratio 5/1 11 = deliver high/low packets at ratio 2/1	00
1	Enable “tag” mask	R/W	=1, the last 5 digits in the VID field are used as a mask to determine which port(s) the packet should be forwarded to. =0, no tag masks.	0
0	Sniff mode select	R./W	=1, will do rx AND tx sniff (both source port and destination port need to match) =0, will do rx OR tx sniff (Either source port or destination port needs to match). This is the mode used to implement rx only sniff.	0

5.1.7 Register 6 (0x06): Global Control 4

Bit	Name	R/W	Description	Default
7	Switch MII backpressure enable	R/W	=1, enable half duplex back pressure on Switch MII interface. =0, disable back pressure on switch MII interface	0
6	Switch MII half duplex mode	R/W	=1, enable MII interface half duplex mode. =0, enable MII interface full duplex mode.	Pin SMRXD2 strap option. Pull down(0): Full duplex mode Pull up(1): Half duplex mode Note: SMRXD2 has internal pull down
5	Switch MII flow control enable	R/W	=1, enable full duplex flow control on Switch MII interface. =0, disable full duplex flow control on Switch MII interface.	Pin SMRXD3 strap option. Pull down(0): disable flow control Pull up(1): enable flow control Note: SMRXD3 has internal pull down
4	Switch MII 10BT	R/W	=1, the switch interface is in 10Mbps mode =0, the switch interface is in 100Mbps mode	Pin SMRXD1 strap option. Pull down(0): Enable 100Mbps Pull up(1): Enable 10Mpbs Note: SMRXD1 has internal pull down
3	Null VID replacement	R/W	=1, will replace NULL VID with port VID(12 bits) =0, no replacement for NULL VID	0
2-0	Broadcast storm protection rate Bit [10:8]	R/W	This along with the next register determines how many “64 byte blocks” of packet data allowed on an input port in a preset period. The period is 50ms for 100BT or 500ms for 10BT. The default is 1%.	000

5.1.8 Register 7 (0x07): Global Control 5

Bit	Name	R/W	Description	Default
7-0	Broadcast storm protection rate Bit [7:0]	R/W	This along with the previous register determines how many "64 byte blocks" of packet data are allowed on an input port in a preset period. The period is 50ms for 100BT or 500ms for 10BT. The default is 1%.	0x4A

148,800 frames/sec * 50 ms/interval * 1% = 74 frames/interval (approx.) = 0x4A

5.1.9 Register 8 (0x08): Global Control 6

Bit	Name	R/W	Description	Default
7-0	Factory testing	R/W	Reserved	0x24

5.1.10 Register 9 (0x09): Global Control 7

Bit	Name	R/W	Description	Default
7-0	Factory testing	R/W	Reserved	0x24

5.1.11 Register 10 (0x0A): Global Control 8

Bit	Name	R/W	Description	Default
7-0	Factory testing	R/W	Reserved	0x24

5.1.12 Register 11 (0x0B): Global Control 9

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Description</th><th>Default</th></tr>
<tr><td>7-3</td><td>Reserved</td><td></td><td>N/A</td><td>0</td></tr>
<tr><td>3</td><td>PHY power Save</td><td>R/W</td><td>0 = disable PHY power save mode
1 = enable PHY power save mode</td><td>0</td></tr>
<tr><td>2</td><td>Factory setting</td><td>R/W</td><td>Reserved</td><td>0</td></tr>
<tr><td>1</td><td>LED mode</td><td>R/W</td><td>0 = led mode 0
1 = led mode 1
<table><tr><th></th><th>Mode 0</th><th>Mode 1</th></tr><tr><td>LEDX_2</td><td>Lnk/Act</td><td>100Lnk/act</td></tr><tr><td>LEDX_1</td><td>Fulld/Col</td><td>10Lnk/act</td></tr><tr><td>LEDX_0</td><td>Speed</td><td>Fulld</td></tr></table></td><td>Pin SMRXD0 strap option.
Pull down(0): Enable led mode 0
Pull up(1): Enable led mode 1
Note: SMRXD0 has internal pull down 0</td></tr>
<tr><td>0</td><td>Special TPID mode</td><td>R/W</td><td>Used for direct mode forwarding from port 5. See description in "spanning tree" functional description.</td><td>0</td></tr>
</table>

5.2 Port Registers

The following registers are used to enable features that are assigned on a per port basis. The register bit assignments are the same for all ports, but the address for each port is different, as indicated.

5.2.1 Register 16 (0x10): Port 1 Control 0
Register 32 (0x20): Port 2 Control 0
Register 48 (0x30): Port 3 Control 0
Register 64 (0x40): Port 4 Control 0
Register 80 (0x50): Port 5 Control 0

Bit	Name	R/W	Description	Default
7	Broadcast storm protection enable	R/W	=1, enable broadcast storm protection for ingress packets on the port =0, disable broadcast storm protection	0
6	Diffserv priority classification enable	R/W	=1, enable diffserv priority classification for ingress packets on port =0, disable diffserv function	0
5	802.1p priority classification enable	R/W	=1, enable 802.1p priority classification for ingress packets on port =0, disable 802.1p	0
4	Port based priority classification enable	R/W	=1, ingress packets on the port will be classified as high priority if “Diffserv” or “802.1p” classification is not enabled or fails to classify. =0, ingress packets on port will be classified as low priority if “Diffserv” or “802.1p” classification is not enabled or fails to classify. Note: “Diffserv”, “802.1p” and port priority can be enabled at the same time. The or’ed result of 802.1p and DSCP overwrites the port priority.	0
3	reserved	R/W	reserved	0
2	Tag insertion	R/W	=1, when packets are output on the port, the switch will add 802.1Q tags to packets without 802.1Q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port’s “port VID”. =0, disable tag insertion	0
1	Tag removal	R/W	=1, when packets are output on the port, the switch will remove 802.1Q tags from packets with 802.1Q tags when received. The switch will not modify packets received without tags. =0, disable tag removal	0
0	Priority Enable	R/W	=1, the port output queue is split into high and low priority queues. =0, single output queue on the port. There is no priority differentiation even though	0

			packets are classified into high or low priority.	

5.2.2 Register 17 (0x11): Port 1 Control 1 Register 33 (0x21): Port 2 Control 1 Register 49 (0x31): Port 3 Control 1 Register 65 (0x41): Port 4 Control 1 Register 81 (0x51): Port 5 Control 1

Bit	Name	R/W	Description	Default
7	Sniffer port	R/W	=1, Port is designated as sniffer port and will transmit packets that are monitored. =0, Port is a normal port	0
6	Receive sniff	R/W	=1, All the packets received on the port will be marked as "monitored packets" and forwarded to the designated "sniffer port" =0, no receive monitoring	0
5	Transmit sniff	R/W	=1, All the packets transmitted on the port will be marked as "monitored packets" and forwarded to the designated "sniffer port" =0, no transmit monitoring	0
4-0	Port VLAN membership	R/W	Define the port's " Port VLAN membership. Bit 4 stands for port 5, bit 3 for port 4… bit 0 for port 1. The Port can only communicate within the membership. A '1' includes a port in the membership, a '0' excludes a port from membership.	0x1f

5.2.3 Register 18 (0x12): Port 1 Control 2 Register 34 (0x22): Port 2 Control 2 Register 50 (0x32): Port 3 Control 2 Register 66 (0x42): Port 4 Control 2 Register 82 (0x52): Port 5 Control 2

Bit	Name	R/W	Description	Default
7	Reserved		reserved	0x0
6	Ingress VLAN filtering	R/W	=1, the switch will discard packets whose VID port membership in VLAN table bit[20:16] does not include the ingress port. =0, no ingress VLAN filtering	0
5	Discard Non PVID packets	R/W	=1, the switch will discard packets whose VID does not match ingress port default VID. =0, no packets will be discarded	0
4	Force flow control	R/W	=1, will always enable rx and tx flow control on the port, regardless of AN result. =0, the flow control is enabled based on AN result. Note: Setting a port for both half duplex and forced flow control is an illegal configuration. For half duplex enable back pressure.	0 (For port 4 only, there is a special configuration pin to set the default, Pin PCOL strap option.

				Pull down(0): No Force flow control Pull up(1): Force flow control Note: PCOL has internal pull down)
3	Back pressure enable	R/W	=1, enable port's half duplex back pressure =0, disable port's half duplex back pressure.	Pin PMRXD2 strap option. Pull down(0): disable back pressure Pull up(1): enable back pressure Note: PMRXD2 has internal pull down
2	Transmit enable	R/W	=1, enable packet transmission on the port =0, disable packet transmission on the port	1
1	Receive enable	R/W	=1, enable packet reception on the port =0, disable packet reception on the port	1
0	Learning disable	R/W	=1, disable switch address learning capability =0, enable switch address learning	0

(Note : bits 2-0 are used for spanning tree support. See Section 4.1 Spanning Tree Support)

5.2.4 Register 19 (0x13): Port 1 Control 3
Register 35 (0x23): Port 2 Control 3
Register 51 (0x33): Port 3 Control 3
Register 67 (0x43): Port 4 Control 3
Register 83 (0x53): Port 5 Control 3

Bit	Name	R/W	Description	Default
7-0	Default tag [15:8]	R/W	Port's default tag, containing 7-5: user priority bits 4: CFI bit 3-0 : VID[11:8]	0

5.2.5 Register 20 (0x14): Port 1 Control 4
Register 36 (0x24): Port 2 Control 4
Register 52 (0x34): Port 3 Control 4
Register 68 (0x44): Port 4 Control 4
Register 84 (0x54): Port 5 Control 4

Bit	Name	R/W	Description	Default
7-0	Default tag [7:0]	R/W	Default port 1's tag, containing 7-0: VID[7:0]	1

Note: Registers 19 and 20 (and those corresponding to other ports) serve two purposes:

(1). Associated with the ingress untagged packets, and used for egress tagging.
(2). Default VID for the ingress untagged or null-VID-tagged packets, and used for address look up.

5.2.6 Register 21 (0x15): Port 1 Control 5
Register 37 (0x25): Port 2 Control 5
Register 53 (0x35): Port 3 Control 5
Register 69 (0x45): Port 4 Control 5
Register 85 (0x55): Port 5 Control 5

Bit	Name	R/W	Description	Default
7-0	Transmit high priority rate control [7:0]	R/W	This along with port control 7, bits [3:0] form a 12-bit field to determine how many “32Kbps” high priority blocks can be transmitted. (in a unit of 4K bytes in a one second period)	0

5.2.7 Register 22 (0x16): Port 1 Control 6
Register 38 (0x26): Port 2 Control 6
Register 54 (0x36): Port 3 Control 6
Register 70 (0x46): Port 4 Control 6
Register 86 (0x56): Port 5 Control 6

Bit	Name	R/W	Description	Default
7-0	Transmit low priority rate control [7:0]	R/W	This along with port control 7, bits [7:4] form a 12-bit field to determine how many “32Kbps” low priority blocks can be transmitted. (in a unit of 4K bytes in a one second period)	0

5.2.8 Register 23 (0x17): Port 1 Control 7
Register 39 (0x27): Port 2 Control 7
Register 55 (0x37): Port 3 Control 7
Register 71 (0x47): Port 4 Control 7
Register 87 (0x57): Port 5 Control 7

Bit	Name	R/W	Description	Default
7-4	Transmit low priority rate control [11:8]	R/W	This along with port control 6, bits [7:0] form a 12 bit field to determine how many “32Kbps” low priority blocks can be transmitted. (in a unit of 4K bytes in a one second period)	0
3-0	Transmit high priority rate control [11:8]	R/W	This along with port control 5, bits [7:0] form a 12 bit field to determine how many “32Kbps” high priority blocks can be transmitted. (in unit of 4K bytes in a one second period)	0

5.2.9 Register 24 (0x18): Port 1 Control 8
Register 40 (0x28): Port 2 Control 8
Register 56 (0x38): Port 3 Control 8
Register 72 (0x48): Port 4 Control 8
Register 88 (0x58): Port 5 Control 8

Bit	Name		Description	Default
7-0	Receive high priority rate control [7:0]	R/W	This along with port control 10, bits [3:0] form a 12 bit field to determine how many "32Kbps" high priority blocks can be received. (in a unit of 4K bytes in a one second period)	0

5.2.10 Register 25 (0x19): Port 1 Control 9
Register 41 (0x29): Port 2 Control 9
Register 57 (0x39): Port 3 Control 9
Register 73 (0x49): Port 4 Control 9
Register 89 (0x59): Port 5 Control 9

Bit	Name		Description	Default
7-0	Receive low priority rate control [7:0]	R/W	This along with port control 10, bits [7:4] form a 12 bit field to determine how many "32Kbps" low priority blocks can be received. (in a unit of 4K bytes in a one second period).	0

5.2.11 Register 26 (0x1A): Port 1 Control 10
Register 42 (0x2A): Port 2 Control 10
Register 58 (0x3A): Port 3 Control 10
Register 74 (0x4A): Port 4 Control 10
Register 90 (0x5A): Port 5 Control 10

Bit	Name	R/W	Description	Default
7-4	Receive low priority rate control [11:8]	R/W	This along with port control 9, bits [7:0] form a 12 bit field to determine how many "32Kbps" low priority blocks can be received. (in a unit of 4K bytes in a one second period)	0
3-0	Receive high priority rate control [11:8]	R/W	This along with port control 8, bits [7:0] form a 12 bit field to determine how many "32Kbps" high priority blocks can be received. (in a unit of 4K bytes in a one second period)	0

5.2.12 Register 27 (0x1B): Port 1 Control 11
Register 43 (0x2B): Port 2 Control 11
Register 59 (0x3B): Port 3 Control 11
Register 75 (0x4B): Port 4 Control 11
Register 91 (0x5B): Port 5 Control 11

Bit	Name	R/W	Description	Default
7	Receive differential priority rate control	R/W	=1, If bit 6 is also '1' this will enable receive rate control for this port on low priority packets at the low priority rate. If bit 5 is also '1', this will enable receive rate control on high priority packets at the high priority rate. =0, receive rate control will be based on the low priority rate for all packets on this port.	0

6	Low priority receive rate control enable	R/W	=1, enable port's low priority receive rate control feature =0, disable port's low priority receive rate control.	0
5	High priority receive rate control enable	R/W	=1, If bit 7 is also '1' this will enable the port's high priority receive rate control feature. If bit 7 is a '0' and bit 6 is a '1', all receive packets on this port will be rate controlled at the low priority rate. =0, disable port's high priority receive rate control feature	0
4	Low priority receive rate flow control enable	R/W	=1, flow control may be asserted if the port's low priority receive rate is exceeded. =0, flow control is not asserted if the port's low priority receive rate is exceeded.	0
3	High priority receive rate flow control enable	R/W	=1, flow control may be asserted if the port's high priority receive rate is exceeded. (to use this, differential receive rate control must be on) =0, flow control is not asserted if the port's high priority receive rate is exceeded.	0
2	Transmit differential priority rate control	R/W	=1, will do transmit rate control on both high and low priority packets based on the rate counters defined by the high and low priority packets respectively. =0, will do transmit rate control on any packets. The rate counters defined in low priority will be used.	0
1	Low priority transmit rate control enable	R/W	=1, enable the port's low priority transmit rate control feature =0, disable the port's low priority transmit rate control feature	
0	High priority transmit rate control enable	R/W	=1, enable the port's high priority transmit rate control feature =0, disable the port's high priority transmit rate control feature	0

5.2.13 Register 28 (0x1C): Port 1 Control 12
Register 44 (0x2C): Port 2 Control 12
Register 60 (0x3C): Port 3 Control 12
Register 76 (0x4C): Port 4 Control 12
Register 92 (0x5C): Port 5 Control 12

NOTE: Port Control 12 and 13, and Port Status 0 contents can be accessed by MIIM (MDC/MDIO) interface via the standard MIIM register definition.

Bit	Name	R/W	Description	Default
7	Disable auto negotiation	R/W	=1, disable auto negotiation, speed and duplex are decided by bit 6 and 5 of the same register. =0, auto negotiation is on	0
6	Forced Speed	R/W	=1, forced 100BT if AN is disabled (bit 7) =0, forced 10BT if AN is disabled (bit 7)	1

5	Forced duplex	R/W	=1, forced full duplex if (1) AN is disabled or (2) AN is enabled but failed. =0, forced half duplex if (1) AN is disabled or (2) AN is enabled but failed.	0 (For port 4 only, there is a special configure pin to set the default, Pin PCRS strap option. Pull down(0): Force half duplex Pull up(1): Force full duplex Note: PCRS has internal pull down)
4	Advertised flow control capability	R/W	=1, advertise flow control capability =0, suppress flow control capability from transmission to link partner	1
3	Advertised 100BT Full duplex capability	R/W	=1, advertise 100BT Full duplex capability =0, suppress 100BT Full duplex capability from transmission to link partner	1
2	Advertised 100BT half duplex capability	R/W	=1, advertise 100BT half duplex capability =0, suppress 100BT half duplex capability from transmission to link partner	1
1	Advertised 10BT Full duplex capability	R/W	=1, advertise 10BT Full duplex capability =0, suppress 10BT Full duplex capability from transmission to link partner	1
0	Advertised 10BT half duplex capability	R/W	=1, advertise 10BT half duplex capability =0, suppress 10BT half duplex capability from transmission to link partner	1

5.2.14 Register 29 (0x1D): Port 1 Control 13
Register 45 (0x2D): Port 2 Control 13
Register 61 (0x3D): Port 3 Control 13
Register 77 (0x4D): Port 4 Control 13
Register 93 (0x5D): Port 5 Control 13

Bit	Name	R/W	Description	Default
7	LED off	R/W	=1, Turn off all port's LEDs (LEDx_2, LEDx_1, LEDx_0, where "x" is the port number). These pins will be driven high if this bit is set to one. =0, normal operation	0
6	Txids	R/W	=1, disable port's transmitter =0, normal operation	0

5	Restart AN	R/W	=1, restart auto-negotiation =0, normal operation	0
4	Disable Far end fault	R/W	=1, disable far end fault detection & pattern transmission. =0, enable far end fault detection & pattern transmission	0
3	Power down	R/W	=1, power down =0, normal operation	0
2	Disable auto MDI/MDIX	R/W	=1, disable auto MDI/MDIX function =0, enable auto MDI/MDIX function	0
1	Forced MDI	R/W	=1, If auto MDI/MDIX is disabled, force PHY into MDI mode =0, Do not force PHY into MDI mode	0
0	MAC Loopback	R/W	=1, Perform MAC loopback =0, normal operation	0

5.2.15 Register 30 (0x1E): Port 1 Status 0
Register 46 (0x2E): Port 2 Status 0
Register 62 (0x3E): Port 3 Status 0
Register 78 (0x4E): Port 4 Status 0
Register 94 (0x5E): Port 5 Status 0

Bit	Name	R/W	Description	Default
7	MDIX status	RO	=1, MDI =0, MDIX	0
6	AN done	RO	=1, AN done =0, AN not done	0
5	Link good	RO	=1, Link good =0, Link not good	0
4	Partner flow control capability	RO	=1, link partner flow control capable =0, link partner not flow control capable	0
3	Partner 100BT full duplex capability	RO	=1, link partner 100BT full duplex capable =0, link partner not 100BT full duplex capable	0
2	Partner 100BT half duplex capability	RO	=1, link partner 100BT half duplex capable =0, link partner not 100BT half duplex capable	0
1	Partner 10BT full duplex capability	RO	=1, link partner 10BT full duplex capable =0, link partner not 10BT full duplex capable	0
0	Partner 10BT half duplex capability	RO	=1, link partner 10BT half duplex capable =0, link partner not 10BT half duplex capable	0

5.2.16 Register 31 (0x1F): Port 1 Control 14
Register 47 (0x2F): Port 2 Control 14
Register 63 (0x3F): Port 3 Control 14
Register 79 (0x4F): Port 4 Control 14
Register 95 (0x5F): Port 5 Control 14

Bit	Name	R/W	Description	Default

7	PHY loopback	R/W	=1, perform PHY loopback, i.e. loopback MAC's TX back to RX =0, normal operation	0
6	Remote Loopback	R/W	=1, perform remote loopback, i.e. loopback PHY's Rx back to Tx =0, normal operation	0
5	PHY isolate	R/W	=1, electrical isolation of PHY from MII and TX+/Tx- =0, normal operation	0
4	Soft Reset	R/W	=1, PHY soft reset =0, normal operation	0
3	Force Link	R/W	=1, Force link in the PHY =0, normal operation	0
2-1	reserved	RO	N/A	
0	Far end fault	RO	=1, Far end fault status detected. =0, no far end fault status detected.	0

5.3 Advanced Control registers

The IPv4 TOS priority control registers implement a fully decoded 64 bit DSCP (Differentiated Services Code Point) register used to determine priority from the 6 bit TOS field in the IP header. The most significant 6 bits of the TOS field are fully decoded into 64 possibilities, and the singular code that results is compared against the corresponding bit in the DSCP register. If the register bit is a 1, the priority is high; if it is a 0, the priority is low.

5.3.1 Register 96 (0x60): TOS priority control register 0

Bit	Name	R/W	Description	Default
7-0	DSCP[63:56]	R/W		00000000

5.3.2 Register 97 (0x61): TOS priority control register 1

Bit	Name	R/W	Description	Default
7-0	DSCP[55:48]	R/W		00000000

5.3.3 Register 98 (0x62): TOS priority control register 2

Bit	Name	R/W	Description	Default
7-0	DSCP[47:40]	R/W		00000000

5.3.4 Register 99 (0x63): TOS priority control register 3

Bit	Name	R/W	Description	Default
7-0	DSCP[39:32]	R/W		00000000

5.3.5 Register 100 (0x64): TOS priority control register 4

Bit	Name	R/W	Description	Default
7-0	DSCP[31:24]	R/W		00000000

5.3.6 Register 101 (0x65): TOS priority control register 5

Bit	Name	R/W	Description	Default
7-0	DSCP[23:16]	R/W		00000000

5.3.7 Register 102 (0x66): TOS priority control register 6

Bit	Name	R/W	Description	Default
7-0	DSCP[15:8]	R/W		00000000

5.3.8 Register 103 (0x67): TOS priority control register 7

Bit	Name	R/W	Description	Default
7-0	DSCP[7:0]	R/W		00000000

Registers 104 to 109 define the switching engine’s MAC address. This 48-bit address is used as the source address in MAC pause control frames.

5.3.9 Register 104 (0x68): MAC address register 0

Bit	Name	R/W	Description	Default
7-0	MACA[47:40]	R/W		0x00

5.3.10 Register 105 (0x69): MAC address register 1

Bit	Name	R/W	Description	Default
7-0	MACA[39:32]	R/W		0x10

5.3.11 Register 106 (0x6A): MAC address register 2

Bit	Name	R/W	Description	Default
7-0	MACA[31:24]	R/W		0xA1

5.3.12 Register 107 (0x6B): MAC address register 3

Bit	Name	R/W	Description	Default
7-0	MACA[23:16]	R/W		0xff

5.3.13 Register 108 (0x6C): MAC address register 4

Bit	Name	R/W	Description	Default
7-0	MACA[15:8]	R/W		0xff

5.3.14 Register 109 (0X6D): MAC address register 5

Bit	Name	R/W	Description	Default
7-0	MACA[7:0]	R/W		0xff

Use registers 110 and 111 to read or write data to the static MAC address table, VLAN table, dynamic address table, or the MIB counters.

5.3.15 Register 110 (0x6E): Indirect Access Control 0

Bit	Name	R/W	Description	Default
7-5	Reserved	R/W	Reserved	000
4	Read High Write Low	R/W	=1, read cycle =0, write cycle	0
3-2	Table select	R/W	00 = static mac address table selected 01 = VLAN table selected 10 = dynamic address table selected 11 = MIB counter selected	0
1-0	Indirect address high	R/W	Bit 9-8 of indirect address	00

5.3.16 Register 111 (0x6F): Indirect Access Control 1

Bit	Name	R/W	Description	Default
7-0	Indirect address low	R/W	Bit 7-0 of indirect address	00000000

Note : (1) write to register 111 will actually trigger a command. Read or write access will be decided by bit 4 of reg110.

5.3.17 Register 112 (0x70): Indirect Data register 8

Bit	Name	R/W	Description	Default
68-64	Indirect data	R/W	Bit 68-64 of indirect data	00000

5.3.18 Register 113 (0x71): Indirect Data register 7

Bit	Name	R/W	Description	Default
63-56	Indirect data	R/W	Bit 63-56 of indirect data	00000000

5.3.19 Register 114 (0x72): Indirect Data register 6

Bit	Name	R/W	Description	Default
55-48	Indirect data	R/W	Bit 55-48 of indirect data	00000000

5.3.20 Register 115 (0x73): Indirect Data register 5

Bit	Name	R/W	Description	Default
47-40	Indirect data	R/W	Bit 47-40 of indirect data	00000000

5.3.21 Register 116 (0x74): Indirect Data register 4

Bit	Name	R/W	Description	Default
39-32	Indirect data	R/W	Bit 39-32 of indirect data	00000000

5.3.22 Register 117 (0x75): Indirect Data register 3

Bit	Name	R/W	Description	Default
31-24	Indirect data	R/W	Bit of 31-24 of indirect data	00000000

5.3.23 Register 118 (0x76): Indirect Data register 2

Bit	Name	R/W	Description	Default
23-16	Indirect data	R/W	Bit 23-16 of indirect data	00000000

5.3.24 Register 119 (0x77): Indirect Data register 1

Bit	Name	R/W	Description	Default
15-8	Indirect data	R/W	Bit 15-8 of indirect data	00000000

5.3.25 Register 120 (0x78): Indirect Data register 0

Bit	Name	R/W	Description	Default
7-0	Indirect data	R/W	Bit 7-0 of indirect data	00000000

DO NOT WRITE OR READ TO/FROM REGISTERS 121 TO 127.
DOING SO MAY PREVENT PROPER OPERATION.
MICREL INTERNAL TESTING ONLY

5.3.26 Register 121 (0x79): Digital Testing Status 0

Bit	Name	R/W	Description	Default
7-0	Factory testing	RO	Reserved Qm_split status	0x0

5.3.27 Register 122 (0x7A): Digital Testing Status 1

Bit	Name	R/W	Description	Default
7-0	Factory testing	RO	Reserved Dbg[7:0]	0x0

5.3.28 Register 123 (0x7B): Digital Testing Control 0

Bit	Name	R/W	Description	Default
7-0	Factory testing	R/W	Reserved Dbg[12:8]	0x0

5.3.29 Register 124 (0x7C): Digital Testing Control 1

Bit	Name	R/W	Description	Default
7-0	Factory testing	R/W	Reserved	0x0

5.3.30 Register 125 (0x7D): Analog Testing Control 0

Bit	Name	R/W	Description	Default
7-0	Factory testing	R/W	Reserved	0x0

5.3.31 Register 126 (0x7E): Analog Testing Control 1

Bit	Name	R/W	Description	Default
7-0	Factory testing	R/W	Reserved	0x0

5.3.32 Register 127 (0x7F): Analog Testing Status

Bit	Name	R/W	Description	Default
7-0	Factory testing	RO	Reserved	0x0

5.3.33 Static MAC address table

KS8995M has a static and a dynamic address table. When a DA look up is requested, both tables will be searched to make a packet forwarding decision. When an SA look up is requested, only the dynamic table is searched for aging, migration and learning purposes. The static DA look up result will have precedence over the dynamic DA look up result. If there are DA matches in both tables, the result from the static table will be used. The static table can only be accessed and controlled by an external SPI master (usually a processor). The entries in the static table will not be aged out by KS8995M. An external device does all addition, modification and deletion.

Note: Register bit assignments are different for static MAC table reads and static MAC table write as shown in the two tables below.

Format of static MAC table for reads (8 entries)

Bit	Name	R/W	Description	Default
60-57	FID	RO	Filter VLAN ID, representing one of the 16 active VLANs.	0000
56	Use FID	RO	=1, use (FID+MAC) to look up in static table =0, use MAC only to look up in static table	0

55	Reserved		Reserved	N/A
54	override	RO	=1, override spanning tree "transmit enable=0" or "receive enable=0" setting. This bit is used for spanning tree implementation =0, no override	0
53	valid	RO	=1, this entry is valid, the look up result will be used =0, this entry is not valid	0
52-48	Forwarding ports	RO	The 5 bits control the forward ports, ex 00001, forward to port 1 00010, forward to port 2 ….. 10000, forward to port 5 00110, forward to port 2 and port 3 11111, broadcasting (excluding the ingress port)	00000
47-0	MAC address	RO	48 bit mac address	0x0

Format of static MAC table for writes (8 entries)

Bit	Name	R/W	Description	Default
59-56	FID	W	Filter VLAN ID, representing one of the 16 active VLANs.	0000
55	Use FID	W	=1, use (FID+MAC) to look up in static table =0, use MAC only to look up in static table	0
54	override	W	=1, override spanning tree "transmit enable=0" or "receive enable=0" setting. This bit is used for spanning tree implementation =0, no override	0
53	valid	W	=1, this entry is valid, the look up result will be used =0, this entry is not valid	0
52-48	Forwarding ports	W	The 5 bits control the forward ports, ex 00001, forward to port 1 00010, forward to port 2 ….. 10000, forward to port 5 00110, forward to port 2 and port 3 11111, broadcasting (excluding the ingress port)	00000
47-0	MAC address	W	48 bit mac address	0x0

Examples:
(1), Static Address Table Read (read the 2nd entry)
 Write to reg110 with 0x10 (read static table selected)
 Write to reg111 with 0x1 (trigger the read operation)
 Then
 Read reg113 (60-56)
 Read reg114 (55-48)
 Read reg115 (47-40)
 Read reg116 (39-32)
 Read reg117 (31-24)
 Read reg118 (23-16)

Read reg119 (15-8)
Read reg120 (7-0)
(2), Static Address Table Write (write the 8th entry)
Write reg113 (59-56)
Write reg114 (55-48)
Write reg115 (47-40)
Write reg116 (39-32)
Write reg117 (31-24)
Write reg118 (23-16)
Write reg119 (15-8)
Write reg120 (7-0)
Write to reg110 with 0x00 (write static table selected)
Write to reg111 with 0x7 (trigger the write operation)

5.3.34 VLAN table

VLAN table is used to do VLAN table look up. If 802.1Q VLAN mode is enabled (Register 5 bit 7 =1), this table will be used to retrieve VLAN information that the ingress packet is associated with. The information includes FID(fiter ID), VID(VLAN ID), VLAN membership described below:

Format of static VLAN table (16 entries)

Bit	Name	R/W	Description	Default
21	Valid	R/W	=1, the entry is valid =0, entry is invalid	1
20-16	Membership	R/W	Specify which ports are members of the VLAN. If a DA look up fails (no match in both static and dynamic tables), the packet associated with this VLAN will be forwarded to ports specified in this field. Eg. 11001 means port 5,4, and 1 are in this VLAN.	11111
15-12	FID	R/W	Filter ID. KS8995M supports 16 active VLANs represented by these four bit fields. FID is the mapped ID. If 802.1Q VLAN is enabled, the look up will be based on FID+DA and FID+SA.	0
11-0	VID	R/W	IEEE 802.1Q 12 bit VLAN ID	1

If 802.1Q VLAN mode is enabled, KS8995M will assign a VID to every ingress packet. If the packet is untagged or tagged with a null VID, the packet is assigned with the default port VID of the ingress port. If the packet is tagged with non null VID, the VID in the tag will be used. The look up process will start from the VLAN table look up. If the VID is not valid, the packet will be dropped and no address learning will take place. If the VID is valid, the FID is retrieved. The FID+DA and FID+SA lookups are performed. The FID+DA look up determines the forwarding ports. If FID+DA fails, the packet will be broadcasted to all the members (excluding the ingress port) of the VLAN. If FID+SA fails, the FID+SA will be learned.

Examples:
(1), VLAN Table Read (read the 3rd entry)
Write to reg110 with 0x14 (read vlan table selected)
Write to reg111 with 0x2 (trigger the read operation)
Then
Read reg118 (Vlan table bits 21-16)
Read reg119 (Vlan table bits 15-8)
Read reg120 (Vlan table bits 7-0)
(2), VLAN Table Write (write the 7th entry)

Write to reg118 (Vlan table bits 21-16)
Write to reg119 (Vlan table bits 15-8)
Write to reg120 (Vlan table bits 7-0)
Write to reg110 with 0x04 (write static table selected)
Write to reg111 with 0x6 (trigger the write operation)

5.3.35 Dynamic MAC address table

This table is read only. The contents are maintained by KS8995M only.

Format of dynamic MAC address table (1K entries)

Bit	Name	R/W	Description	Default
68	MAC empty	RO	=1, there is no valid entry in the table =0, there are valid entries in the table	1
67-58	No of valid entries	RO	Indicates how many valid entries in the table 0x3ff means 1 K entries 0x1 means 2 entries 0x0 and bit 68 = 0: means 1 entry 0x0 and bit 68 = 1: means 0 entry	0
57-56	Time stamp	RO	2-bit counters for internal aging	
55	Data ready	RO	=1, The entry is not ready, retry until this bit is set to 0. =0, The entry is ready	
54-52	Source port	RO	The source port where FID+MAC is learned. 000 port 1 001 port 2 010 port 3 011 port 4 100 port 5	0x0
51-48	FID	RO	Filter ID	0x0
47-0	MAC address	RO	48 bit mac address	0x0

Examples:

(1), Dynamic MAC Address Table Read (read the 1st entry), and retrieve the MAC table size

Write to reg110 with 0x18 (read dynamic table selected)
Write to reg111 with 0x0 (trigger the read operation)
Then
Read reg112 (68-64)
Read reg113 (63-56) ; // the above two registers show # of entries
Read reg114 (55-48) // if bit 55 is 1, restart(reread) from this register
Read reg115 (47-40)
Read reg116 (39-32)
Read reg117 (31-24)
Read reg118 (23-16)
Read reg119 (15-8)
Read reg120 (7-0)

(2), Dynamic MAC Address Table Read (read the 257th entry), without retrieving # of entries info

Write to reg110 with 0x19 (read dynamic table selected)
Write to reg111 with 0x1 (trigger the read operation)
Then
Read reg114 (55-48) // if bit 55 is 1, restart (reread) from this register.

Read reg115 (47-40)
Read reg116 (39-32)
Read reg117 (31-24)
Read reg118 (23-16)
Read reg119 (15-8)
Read reg120 (7-0)

5.3.36 MIB counters

The MIB counters are provided on per port basis. The indirect memory is as below:
For port 1

Table 12-Port 1 MIB Counter Indirect Memory Offsets

Offset	Counter Name	Description
0x0	**RxLoPriorityByte**	Rx lo-priority (default) octet count including bad pkts
0x1	**RxHiPriorityByte**	Rx hi-priority octet count including bad pkts
0x2	**RxUndersizePkt**	Rx undersize pkts w/ good CRC
0x3	**RxFragments**	Rx fragment pkts w/ bad CRC, symbol errors or alignment errors
0x4	**RxOversize**	Rx oversize pkts w/ good CRC (max: 1536 or 1522 bytes)
0x5	**RxJabbers**	Rx pkts longer than 1522B w/ either CRC errors, Alignment errors, or symbol errors. (Depends on max packet size setting).
0x6	**RxSymbolError**	Rx pkts w/ invalid data symbol and legal packet size.
0x7	**RxCRCerror**	Rx pkts within (64,1522) bytes w/ an integral number of bytes and a bad CRC (Upper limit depends on max packet size setting).
0x8	**RxAlignmentError**	Rx pkts within (64,1522) bytes w/ a non-integral number of bytes and a bad CRC (Upper limit depends on max packet size setting).
0x9	**RxControl8808Pkts**	The number of MAC control frames received by a port with 88-08h in EtherType field.
0xA	**RxPausePkts**	The number of PAUSE frames received by a port. PAUSE frame is qualified with EtherType (88-08h), DA, control opcode (00-01), data length (64B min), and a valid CRC
0xB	**RxBroadcast**	Rx good broadcast pkts (not including errored broadcast pkts or valid multicast pkts)
0xC	**RxMulticast**	Rx good multicat pkts (not including MAC control frames, errored multicast pkts or valid broadcast pkts)
0xD	**RxUnicast**	Rx good unicast packets
0xE	**Rx64Octets**	Total Rx pkts (bad pkts included) that were 64 octets in length
0xF	**Rx65to127Octets**	Total Rx pkts (bad pkts included) that are between 65 and 127 octets in length
0x10	**Rx128to255Octets**	Total Rx pkts (bad pkts included) that are between 128 and 255 octets in length
0x11	**Rx256to511Octets**	Total Rx pkts (bad pkts included) that are between 256 and 511 octets in length
0x12	**Rx512to1023Octets**	Total Rx pkts (bad pkts included) that are between 512 and 1023 octets in length
0x13	**Rx1024to1522Octets**	Total Rx pkts (bad pkts included) that are between 1024 and 1522 octets in length (Upper limit depends on max packet size setting).
0x14	**TxLoPriorityByte**	Tx lo-priority good octet count, including PAUSE pkts

0x15	**TxHiPriorityByte**	Tx hi-priority good octet count, including PAUSE pkts
0x16	**TxLateCollision**	The number of times a collision is detected later than 512 bit-times into the Tx of a pkt
0x17	**TxPausePkts**	The number of PAUSE frames transmitted by a port
0x18	**TxBroadcastPkts**	Tx good broadcast pkts (not including errored broadcast or valid multicast pkts)
0x19	**TxMulticastPkts**	Tx good multicast pkts (not including errored multicast pkts or valid broadcast pkts)
0x1A	**TxUnicastPkts**	Tx good unicast pkts
0x1B	**TxDeferred**	Tx pkts by a port for which the 1st Tx attempt is delayed due to the busy medium
0x1C	**TxTotalCollision**	Tx total collision, half duplex only
0x1D	**TxExcessiveCollision**	A count of frames for which Tx fails due to excessive collisions
0x1E	**TxSingleCollision**	Successfully Tx frames on a port for which Tx is inhibited by exactly one collision
0x1F	**TxMultipleCollision**	Successfully Tx frames on a port for which Tx is inhibited by more than one collision

For port 2, the base is 0x20, same offset definition (0x20-0x3f)
For port 3, the base is 0x40, same offset definition (0x40-0x5f)
For port 4, the base is 0x60, same offset definition (0x60-0x7f)
For port 5, the base is 0x80, same offset definition (ox80-0x9f)

Format of Per Port MIB Counters (16 entries)

Bit	Name	R/W	Description	Default
31	Overflow	RO	=1, Counter overflow =0, No Counter overflow	0
30	Count Valid	RO	=1, Counter value is valid =0, Counter value is not valid	0
29-0	Counter values	RO	Counter value	0

Table 13-All Port Dropped Packet MIB Counters

Offset	Counter Name	Description
0x100	**Port1 TX Drop Packets**	Tx packets dropped due to lack of resources
0x101	**Port2 TX Drop Packets**	Tx packets dropped due to lack of resources
0x102	**Port3 TX Drop Packets**	Tx packets dropped due to lack of resources
0x103	**Port4 TX Drop Packets**	Tx packets dropped due to lack of resources
0x104	**Port5 TX Drop Packets**	Tx packets dropped due to lack of resources
0x105	**Port1 RX Drop Packets**	Rx packets dropped due to lack of resources
0x106	**Port2 RX Drop Packets**	Rx packets dropped due to lack of resources
0x107	**Port3 RX Drop Packets**	Rx packets dropped due to lack of resources
0x108	**Port4 RX Drop Packets**	Rx packets dropped due to lack of resources
0x109	**Port5 RX Drop Packets**	Rx packets dropped due to lack of resources

Format of All Port Dropped Packet MIB Counters

Bit	Name	R/W	Description	Default
30-16	Reserved	N/A	Reserved	N/A
15-0	Counter values	RO	Counter value	0

Note: All port dropped packet MIB counters do not indicate overflow or validity; therefore the application must keep track of overflow and valid conditions.

Examples:
(1), MIB counter read (read port 1 rx 64 counter)
Write to reg110 with 0x1c (read MIB counters selected)
Write to reg111 with 0xe (trigger the read operation)
Then
Read reg117 (counter value 31-24) // If bit 31 = 1, there was a counter overflow.
// If bit 30 = 0, restart (reread) from this register.
Read reg118 (counter value 23-16)
Read reg119 (counter value 15-8)
Read reg120 (counter value 7-0)

(2), MIB counter read (read port 2 rx 64 counter)
Write to reg110 with 0x1c (read MIB counter selected)
Write to reg111 with 0x2e (trigger the read operation)
Then
Read reg117 (counter value 31-24) // If bit 31 = 1, there was a counter overflow.
// If bit 30 = 0, restart (reread) from this register.
Read reg118 (counter value 23-16)
Read reg119 (counter value 15-8)
Read reg120 (counter value 7-0)

(3), MIB counter read (read port 1 tx drop packets)
Write to reg 110 with 0x1d
Write to reg 111 with 0x00
Then
Read reg119 (counter value 15-8)
Read reg120 (counter value 7-0)

NOTE:
(1).
To read out all the counters, the best performance over the SPI bus is
(160+3)*8*200 = 260 ms, where
there are 160 register, 3 overhead, 8 clocks per access, **at 5 MHz**. In the heaviest condition, the byte counter will overflow in 2 minutes. It is recommended that the software read all the counters at least every 30 seconds. The per port MIB counters are designed as “read clear”. A per port MIB counter will be cleared after it is accessed. All port dropped packet MIB counters are not cleared after they are accessed. The application needs to keep track of overflow and valid conditions on these counters.

5.4 MIIM registers

(All the registers defined in this section can be also accessed via the SPI interface. Note: different mapping mechanisms used for MIIM and SPI). The “PHYAD” defined in IEEE is assigned as “0x1” for port 1, “0x2” for port 2, “0x3” for port 3, “0x4” for port 4, “0x5” for port 5. The “REGAD” supported are 0,1,2,3,4,5.

5.4.1 Register 0: MII control

Bit	Name	R/W	Description	Default
15	Soft reset	R/W	=1, PHY soft reset =0, normal operation	0
14	Loop back	R/W	=1, loop back mode (loop back at MAC) =0, normal operation	0
13	Force 100	R/W	=1, 100 Mbps =0, 10 Mbps	1
12	AN enable	R/W	=1, Auto-Negotiation enabled =0, Auto-Negotiation disabled	1
11	Power down	R/W	=1, power down =0, normal operation	0
10	PHY Isolate	R/W	=1, electrical PHY isolation of PHY from Tx+/Tx- =0, normal operation	0
9	Restart AN	R/W	=1, restart Auto-Negotiation =0, normal operation	0
8	Force full duplex	R/W	=1, Full duplex =0, half duplex	0
7	Collision test	RO	NOT SUPPORTED	0
6	Reserved	RO		0
5	Reserved	RO		0
4	Force MDI	R/W	=1, Force MDI =0, normal operation	0
3	Disable Auto MDI/MDIX	R/W	=1, Disable auto MDI/MDIX =0, normal operation	0
2	Disable far end fault	R/W	=1, Disable far end fault detection =0, normal operation	0
1	Disable transmit	R/W	=1, Disable transmit =0, normal operation	0
0	Disable LED	R/W	=1, Disable LED =0, normal operation	0

5.4.2 Register 1: MII status

Bit	Name	R/W	Description	Default
15	T4 capable	RO	=0, Not 100 BaseT4 capable	0
14	100 Full capable	RO	=1, 100BaseTX full duplex capable =0, not capable of 100BaseTX full duplex	1
13	100 Half capable	RO	=1, 100BaseTX half duplex capable =0, not 100BaseTX half duplex capable	1
12	10 Full capable	RO	=1, 10BaseT full duplex capable =0, not 10BaseT full duplex capable	1
11	10 Half capable	RO	=1, 10BaseT half duplex capable =0, 10BaseT half duplex capable	1
10-7	Reserved	RO		0
6	Preamble suppressed	RO	NOT SUPPORTED	0
5	AN complete	RO	=1, Auto-Negotiation complete =0, Auto-Negotiation not completed	0
4	Far end fault	RO	=1, Far end fault detected =0, No far end fault detected	0
3	AN capable	RO	=1, Auto-Negotiation capable	1

			=0, Not Auto-Negotiation capable	
2	Link status	RO	=1, Link is up =0, Link is down	0
1	Jabber test	RO	NOT SUPPORTED	0
0	Extended capable	RO	=0, Not extended register capable	0

5.4.3 Register 2: PHYID HIGH

Bit	Name	R/W	Description	Default
15-0	Phyid high	RO	High order PHYID bits	0x0022

5.4.4 Register 3: PHYID LOW

Bit	Name	R/W	Description	Default
15-0	Phyid low	RO	Low order PHYID bits	0x1450

5.4.5 Register 4: Advertisement Ability

Bit	Name	R/W	Description	Default
15	Next page	RO	NOT SUPPORTED	0
14	Reserved	RO		0
13	Remote fault	RO	NOT SUPPORTED	0
12-11	Reserved	RO		0
10	Pause	R/W	=1, advertise pause ability =0, do not advertise pause ability	1
9	Reserved	R/W		0
8	Adv 100 Full	R/W	=1, advertise 100 Full duplex ability =0, do not advertise 100 full duplex ability	1
7	Adv 100 Half	R/W	=1, advertise 100 half duplex ability =0, do not advertise 100 half duplex ability	1
6	Adv 10 Full	R/W	=1, advertise 10 full duplex ability =0, do not advertise 10 full duplex ability	1
5	Adv 10 Half	R/W	=1, advertise 10 half duplex ability =0, do not advertise 10 half duplex ability	1
4-0	Selector field	RO	802.3	00001

5.4.6 Register 5: Link Partner Ability

Bit	Name	R/W	Description	Default
15	Next page	RO	NOT SUPPORTED	0
14	LP ACK	RO	NOT SUPPORTED	0
13	Remote fault	RO	NOT SUPPORTED	0
12-11	Reserved	RO		0
10	Pause	RO	Link partner pause capability	0
9	Reserved	RO		0
8	Adv 100 Full	RO	Link partner 100 full capability	0
7	Adv 100 Half	RO	Link partner 100 half capability	0
6	Adv 10 Full	RO	Link partner 10 full capability	0
5	Adv 10 Half	RO	Link partner 10 half capability	0
4-0	Reserved	RO		00001

6.0 Signal Description

Table 14-I/O Pin Out (by pin #)

Pin #	Pin Name	Type	Port	Brief Description
1	MDIXDIS	I	1-5	Disable auto MDI/MDIX PD (default) = normal operation PU = disable auto MDI/MDIX on all ports
2	GNDA	Gnd		Analog ground
3	VDDAR	Pwr		1.8V analog VDD
4	RXP1	I	1	Physical receive signal + (differential)
5	RXM1	I	1	Physical receive signal - (differential)
6	GNDA	Gnd		Analog ground
7	TXM1	O	1	Physical transmit signal - (differential)
8	TXP1	O	1	Physical transmit signal + (differential)
9	VDDAT	Pwr		2.5V or 3.3V analog VDD
10	RXP2	I	2	Physical receive signal + (differential)
11	RXM2	I	2	Physical receive signal - (differential)
12	GNDA	Gnd		Analog ground
13	TXM2	O	2	Physical transmit signal - (differential)
14	TXP2	O	2	Physical transmit signal + (differential)
15	VDDAR	Pwr		1.8V analog VDD
16	GNDA	Gnd		Analog ground
17	ISET			Set physical transmit output current. Pull down with a 3.01 k Ohm 1% resistor.
18	VDDAT	Pwr		2.5V or 3.3V analog VDD
19	RXP3	I	3	Physical receive signal + (differential)
20	RXM3	I	3	Physical receive signal - (differential)
21	GNDA	Gnd		Analog ground
22	TXM3	O	3	Physical transmit signal - (differential)
23	TXP3	O	3	Physical transmit signal + (differential)
24	VDDAT	Pwr		2.5V or 3.3V analog VDD
25	RXP4	I	4	Physical receive signal + (differential)
26	RXM4	I	4	Physical receive signal - (differential)
27	GNDA	Gnd		Analog ground
28	TXM4	O	4	Physical transmit signal - (differential)
29	TXP4	O	4	Physical transmit signal + (differential)
30	GNDA	Gnd		Analog ground
31	VDDAR	Pwr		1.8V analog VDD
32	RXP5	I	5	Physical receive signal + (differential)
33	RXM5	I	5	Physical receive signal - (differential)
34	GNDA	Gnd		Analog ground
35	TXM5	O	5	Physical transmit signal - (differential)
36	TXP5	O	5	Physical transmit signal + (differential)
37	VDDAT	Pwr		2.5V or 3.3V analog VDD
38	FXSD5	I	5	Fiber signal detect / factory test pin
39	FXSD4	I	4	Fiber signal detect / factory test pin
40	GNDA	Gnd		Analog ground
41	VDDAR	Pwr		1.8V analog VDD

Pin #	Pin Name	Type	Port	Brief Description
42	GNDA	Gnd		Analog ground
43	VDDAR	Pwr		1.8V analog VDD
44	GNDA	Gnd		Analog ground
45	MUX1	NC		MUX1 and MUX2 should be left unconnected for normal operation. They are factory test pins. Mode | Mux1 | Mux2 Normal Operation | NC | NC Remote analog loopback mode for testing only | 0 | 1 Reserved | 1 | 0 power save mode for testing only | 1 | 1
46	MUX2	NC		
47	PWRDN_N	Ipu		Full-chip power down. Active low.
48	RESERVE	NC		Reserved pin. No connect.
49	GNDD	Gnd		Digital ground
50	VDDC	Pwr		1.8V digital core VDD
51	PMTXEN	Ipd	5	PHY[5] MII transmit enable
52	PMTXD3	Ipd	5	PHY[5] MII transmit bit 3
53	PMTXD2	Ipd	5	PHY[5] MII transmit bit 2
54	PMTXD1	Ipd	5	PHY[5] MII transmit bit 1
55	PMTXD0	Ipd	5	PHY[5] MII transmit bit 0
56	PMTXER	Ipd	5	PHY[5] MII transmit error
57	PMTXC	O	5	PHY[5] MII transmit clock. PHY mode MII.
58	GNDD	Gnd		Digital ground
59	VDDIO	Pwr		3.3/2.5V digital VDD for digital I/O circuitry
60	PMRXC	O	5	PHY[5] MII receive clock. PHY mode MII.
61	PMRXDV	Ipd / O	5	PHY[5] MII receive data valid
62	PMRXD3	Ipd / O	5	PHY[5] MII receive bit 3. Strap option: PD (default) = enable flow control; PU = disable flow control
63	PMRXD2	Ipd / O	5	PHY[5] MII receive bit 2. Strap option: PD (default) = disable back pressure; PU = enable back pressure
64	PMRXD1	Ipd / O	5	PHY[5] MII receive bit 1. Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets
65	PMRXD0	Ipd / O	5	PHY[5] MII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement
66	PMRXER	Ipd / O	5	PHY[5] MII receive error. Strap option: PD (default) = 1522/1518 bytes; PU = packet size up to 1536 bytes
67	PCRS	Ipd / O	5	PHY[5] MII carrier sense/Force duplex mode (See section 5.2.13) For port 4 only. PD (default) = Force half duplex if auto-negotiation is disabled or fails. PU = Force full duplex if auto-negotiation is disabled or fails.
68	PCOL	Ipd / O	5	PHY[5] MII collision detect/ Force flow control (See section 5.2.3) For port 4 only. PD (default) = No force flow control. PU = Force flow control.
69	SMTXEN	Ipd		Switch MII transmit enable
70	SMTXD3	Ipd		Switch MII transmit bit 3
71	SMTXD2	Ipd		Switch MII transmit bit 2
72	SMTXD1	Ipd		Switch MII transmit bit 1

Pin #	Pin Name	Type	Port	Brief Description
73	SMTXD0	Ipd		Switch MII transmit bit 0
74	SMTXER	Ipd		Switch MII transmit error
75	SMTXC	I / O		Switch MII transmit clock. Input in MAC mode, output in PHY mode MII.
76	GNDD	Gnd		Digital ground
77	VDDIO	Pwr		3.3/2.5V digital VDD for digital I/O circuitry
78	SMRXC	I / O		Switch MII receive clock. Input in MAC mode, output in PHY mode MII.
79	SMRXDV	Ipd / O		Switch MII receive data valid
80	SMRXD3	Ipd / O		Switch MII receive bit 3. Strap option: PD (default) = Disable Switch MII full-duplex flow control; PU = Enable Switch MII full-duplex flow control
81	SMRXD2	Ipd / O		Switch MII receive bit 2. Strap option: PD (default) = Switch MII in full duplex mode; PU = Switch MII in half-duplex mode.
82	SMRXD1	Ipd / O		Switch MII receive bit 1. Strap option: PD (default) = Switch MII in 100Mbps mode; PU = Switch MII in 10Mbps mode
83	SMRXD0	Ipd / O		Switch MII receive bit 0; Strap option: LED Mode PD (default) = Mode 0; PU = Mode 1. See also register 11.

	Mode 0	Mode 1
LEDX_2	Lnk/Act	100Lnk/act
LEDX_1	Fulld/Col	10Lnk/act
LEDX_0	Speed	Fulld

Pin #	Pin Name	Type	Port	Brief Description
84	SCOL	Ipd / O		Switch MII collision detect
85	SCRS	Ipd / O		Switch MII carrier sense
86	SCONF1	Ipd		Dual MII configuration pin.

Pin# (91,86,87):	Switch MII	PHY[5] MII
000	Disable, Otri	disable, Otri
001	phy mode MII	disable, Otri
010	mac mode MII	disable, Otri
011	phy mode SNI	disable, Otri
100	Disable	Disable
101	phy mode MII	phy mode MII
110	mac mode MII	phy mode MII
111	phy mode SNI	phy mode MII

Pin #	Pin Name	Type	Port	Brief Description
87	SCONF0	Ipd		Dual MII configuration pin
88	GNDD	Gnd		Digital ground
89	VDDC	Pwr		1.8V digital core VDD
90	LED5-2	Ipu / O	5	LED indicator 2. Strap option: Aging setup. See section 3.4 PU (default) = Aging Enable; PD = Aging disable.
91	LED5-1	Ipu / O	5	LED indicator 1. Strap option: PU (default): enable PHY MII I/F. PD: tristate all PHY MII output. See pin#86 SCONF1.
92	LED5-0	Ipu / O	5	LED indicator 0
93	LED4-2	Ipu / O	4	LED indicator 2

Pin #	Pin Name	Type	Port	Brief Description
94	LED4-1	Ipu / O	4	LED indicator 1
95	LED4-0	Ipu / O	4	LED indicator 0
96	LED3-2	Ipu / O	3	LED indicator 2
97	LED3-1	Ipu / O	3	LED indicator 1
98	LED3-0	Ipu / O	3	LED indicator 0
99	GNDD	Gnd		Digital ground
100	VDDIO	Pwr		3.3/2.5V digital VDD for digital I/O
101	LED2-2	Ipu / O	2	LED indicator 2
102	LED2-1	Ipu / O	2	LED indicator 1
103	LED2-0	Ipu / O	2	LED indicator 0
104	LED1-2	Ipu / O	1	LED indicator 2
105	LED1-1	Ipu / O	1	LED indicator 1
106	LED1-0	Ipu / O	1	LED indicator 0
107	MDC	Ipu	All	Switch or PHY[5] MII management data clock
108	MDIO	I / O	All	Switch or PHY[5] MII management data I/O Features internal pull down to define pin state when not driven.
109	SPIQ	Otri	All	1) SPI serial data output in SPI slave mode; 2) Not used in I2C master mode (see pin#113)
110	SPIC/SCL	I / O	All	1) Input clock up to 5MHz in SPI slave mode; 2) Output clock at 81KHz in I2C master mode. (See pin#113)
111	SPID/SDA	I / O	All	1) Serial data input in SPI slave mode; 2) Serial data input/output in I2C master mode (See pin#113)
112	SPIS_N	Ipu	All	Active low. 1) SPI data transfer start in SPI slave mode. When SPIS_N is high, the KS8995M is deselected and SPIQ is held in high impedance state, a high-to-low transition to initiate the SPI data transfer; 2) Not used in I2C master mode.
113	PS1	Ipd		Serial bus configuration pin If EEPROM is not present, the KS8995M will start itself with chip default (00).. Pin Config: Serial bus configuration PS[1:0]=00: I2C master mode for EEPROM PS[1:0]=01: Reserved PS[1:0]=10: SPI slave mode for CPU interface PS[1:0]=11: Factory test mode (BIST)
114	PS0	Ipd		Serial bus configuration pin. See pin#113 description
115	RST_N	Ipu		Reset the KS8995M. Active low.
116	GNDD	Gnd		Digital ground
117	VDDC	Pwr		1.8V digital core VDD
118	TESTEN	Ipd		NC for normal operation. Factory test pin.
119	SCANEN	Ipd		NC for normal operation. Factory test pin
120	NC	NC		No Connection
121	X1	I		25MHz crystal clock connection/or 3.3 V tolerant Oscillator Input. Oscillator should be +/- 100 ppm.
122	X2	O		25MHz crystal clock connection
123	VDDAP	Pwr		1.8V analog VDD for PLL
124	GNDA	Gnd		Analog ground
125	VDDAR	Pwr		1.8V analog VDD

Pin #	Pin Name	Type	Port	Brief Description
126	GNDA	Gnd		Analog ground
127	GNDA	Gnd		Analog ground
128	TEST2	NC		NC for normal operation. Factory test pin.

Note:

Pwr = power supply;
Gnd = ground;
I = input;
O = output;
I / O = bi-directional;
Ipu = input w/ internal pull-up;
Ipd = input w/ internal pull-down;
Ipd / O = input w/ internal pull-down during reset, output pin otherwise;
Ipu / O = input w/ internal pull-up during reset, output pin otherwise;
PU = strap pin pull-up;
PD = strap pull-down;
Otri = output tristated
NC = No Connect

Table 15-I/O Pin Out (by pin name)

Pin #	Pin Name	Type	Port	Brief Description
39	FXSD4	I	4	Fiber signal detect / factory test pin
38	FXSD5	I	5	Fiber signal detect / factory test pin
124	GNDA	Gnd		Analog ground
42	GNDA	Gnd		Analog ground
44	GNDA	Gnd		Analog ground
2	GNDA	Gnd		Analog ground
16	GNDA	Gnd		Analog ground
30	GNDA	Gnd		Analog ground
6	GNDA	Gnd		Analog ground
12	GNDA	Gnd		Analog ground
21	GNDA	Gnd		Analog ground
27	GNDA	Gnd		Analog ground
34	GNDA	Gnd		Analog ground
40	GNDA	Gnd		Analog ground
120	NC	NC		No Connection
127	GNDA	Gnd		Analog ground
126	GNDA	Gnd		Analog ground
49	GNDD	Gnd		Digital ground
88	GNDD	Gnd		Digital ground
116	GNDD	Gnd		Digital ground
58	GNDD	Gnd		Digital ground
76	GNDD	Gnd		Digital ground
99	GNDD	Gnd		Digital ground
17	ISET			Set physical transmit output current. Pull down with a 3.01 kOhm 1% resistor.
106	LED1-0	Ipu / O	1	LED indicator 0
105	LED1-1	Ipu / O	1	LED indicator 1
104	LED1-2	Ipu / O	1	LED indicator 2
103	LED2-0	Ipu / O	2	LED indicator 0
102	LED2-1	Ipu / O	2	LED indicator 1
101	LED2-2	Ipu / O	2	LED indicator 2
98	LED3-0	Ipu / O	3	LED indicator 0
97	LED3-1	Ipu / O	3	LED indicator 1
96	LED3-2	Ipu / O	3	LED indicator 2
95	LED4-0	Ipu / O	4	LED indicator 0
94	LED4-1	Ipu / O	4	LED indicator 1
93	LED4-2	Ipu / O	4	LED indicator 2
92	LED5-0	Ipu / O	5	LED indicator 0
91	LED5-1	Ipu / O	5	LED indicator 1. Strap option: PU (default): enable PHY MII I/F. PD: tristate all PHY MII output. See pin#86 SCONF1.
90	LED5-2	Ipu / O	5	LED indicator 2. Strap option: Aging setup. See section 3.4 PU (default) = Aging Enable; PD = Aging disable.
107	MDC	Ipu	All	Switch or PHY[5] MII management data clock
108	MDIO	I / O	All	Switch or PHY[5] MII management data I/O

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>Type</th><th>Port</th><th>Brief Description</th></tr>
<tr><td>1</td><td>MDIXDIS</td><td>Ipd</td><td>1-5</td><td>Disable auto MDI/MDIX</td></tr>
<tr><td>45</td><td>MUX1</td><td>NC</td><td></td><td rowspan="2">MUX1 and MUX2 should be left unconnected for normal operation. They are factory test pins.
<table>
<tr><td>Mode</td><td>Mux1</td><td>Mux2</td></tr>
<tr><td>Normal Operation</td><td>NC</td><td>NC</td></tr>
<tr><td>Remote analog loopback mode for testing only</td><td>0</td><td>1</td></tr>
<tr><td>Reserved</td><td>1</td><td>0</td></tr>
<tr><td>power save mode for testing only</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>46</td><td>MUX2</td><td>NC</td><td></td></tr>
<tr><td>68</td><td>PCOL</td><td>Ipd / O</td><td>5</td><td>PHY[5] MII collision detect/ Force flow control (See section 5.2.3) For port 4 only. PD (default) = No force flow control. PU = Force flow control.</td></tr>
<tr><td>67</td><td>PCRS</td><td>Ipd / O</td><td>5</td><td>PHY[5] MII carrier sense/Force duplex mode (See section 5.2.13) For port 4 only. PD (default) = Force half duplex if auto-negotiation is disabled or fails. PU = Force full duplex if auto-negotiation is disabled or fails.</td></tr>
<tr><td>60</td><td>PMRXC</td><td>O</td><td>5</td><td>PHY[5] MII receive clock. PHY mode MII.</td></tr>
<tr><td>65</td><td>PMRXD0</td><td>Ipd / O</td><td>5</td><td>PHY[5] MII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement</td></tr>
<tr><td>64</td><td>PMRXD1</td><td>Ipd / O</td><td>5</td><td>PHY[5] MII receive bit 1. Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets</td></tr>
<tr><td>63</td><td>PMRXD2</td><td>Ipd / O</td><td>5</td><td>PHY[5] MII receive bit 2. Strap option: PD (default) = disable back pressure; PU = enable back pressure</td></tr>
<tr><td>62</td><td>PMRXD3</td><td>Ipd / O</td><td>5</td><td>PHY[5] MII receive bit 3. Strap option: PD (default) = enable flow control; PU = disable flow control</td></tr>
<tr><td>61</td><td>PMRXDV</td><td>Ipd / O</td><td>5</td><td>PHY[5] MII receive data valid</td></tr>
<tr><td>66</td><td>PMRXER</td><td>Ipd / O</td><td>5</td><td>PHY[5] MII receive error. Strap option: PD (default) = 1522/1518 bytes; PU = packet size up to 1536 bytes</td></tr>
<tr><td>57</td><td>PMTXC</td><td>O</td><td>5</td><td>PHY[5] MII transmit clock. PHY mode MII.</td></tr>
<tr><td>55</td><td>PMTXD0</td><td>Ipd</td><td>5</td><td>PHY[5] MII transmit bit 0</td></tr>
<tr><td>54</td><td>PMTXD1</td><td>Ipd</td><td>5</td><td>PHY[5] MII transmit bit 1</td></tr>
<tr><td>53</td><td>PMTXD2</td><td>Ipd</td><td>5</td><td>PHY[5] MII transmit bit 2</td></tr>
<tr><td>52</td><td>PMTXD3</td><td>Ipd</td><td>5</td><td>PHY[5] MII transmit bit 3</td></tr>
<tr><td>51</td><td>PMTXEN</td><td>Ipd</td><td>5</td><td>PHY[5] MII transmit enable</td></tr>
<tr><td>56</td><td>PMTXER</td><td>Ipd</td><td>5</td><td>PHY[5] MII transmit error</td></tr>
<tr><td>114</td><td>PS0</td><td>Ipd</td><td></td><td>Serial bus configuration pin. See pin#113 description</td></tr>
<tr><td>113</td><td>PS1</td><td>Ipd</td><td></td><td>Serial bus configuration pin
If EEPROM is not present, the KS8995M will start itself with chip default (00).
<table>
<tr><td>Pin Config</td><td>Serial bus configuration</td></tr>
<tr><td>PS[1:0]=00</td><td>I2C master mode for EEPROM</td></tr>
<tr><td>PS[1:0]=01</td><td>Reserved</td></tr>
<tr><td>PS[1:0]=10</td><td>SPI slave mode for CPU interface</td></tr>
<tr><td>PS[1:0]=11</td><td>Factory test mode (BIST)</td></tr>
</table></td></tr>
<tr><td>47</td><td>PWRDN_N</td><td>Ipu</td><td></td><td>Full-chip power down. Active low.</td></tr>
</table>

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>Type</th><th>Port</th><th>Brief Description</th></tr>
<tr><td>48</td><td>RESERVE</td><td>NC</td><td></td><td>Reserved pin. No connect.</td></tr>
<tr><td>115</td><td>RST_N</td><td>Ipu</td><td></td><td>Reset the KS8995M. Active low.</td></tr>
<tr><td>5</td><td>RXM1</td><td>I</td><td>1</td><td>Physical receive signal - (differential)</td></tr>
<tr><td>11</td><td>RXM2</td><td>I</td><td>2</td><td>Physical receive signal - (differential)</td></tr>
<tr><td>20</td><td>RXM3</td><td>I</td><td>3</td><td>Physical receive signal - (differential)</td></tr>
<tr><td>26</td><td>RXM4</td><td>I</td><td>4</td><td>Physical receive signal - (differential)</td></tr>
<tr><td>33</td><td>RXM5</td><td>I</td><td>5</td><td>Physical receive signal - (differential)</td></tr>
<tr><td>4</td><td>RXP1</td><td>I</td><td>1</td><td>Physical receive signal + (differential)</td></tr>
<tr><td>10</td><td>RXP2</td><td>I</td><td>2</td><td>Physical receive signal + (differential)</td></tr>
<tr><td>19</td><td>RXP3</td><td>I</td><td>3</td><td>Physical receive signal + (differential)</td></tr>
<tr><td>25</td><td>RXP4</td><td>I</td><td>4</td><td>Physical receive signal + (differential)</td></tr>
<tr><td>32</td><td>RXP5</td><td>I</td><td>5</td><td>Physical receive signal + (differential)</td></tr>
<tr><td>119</td><td>SCANEN</td><td>Ipd</td><td></td><td>NC for normal operation. Factory test pin</td></tr>
<tr><td>84</td><td>SCOL</td><td>Ipd / O</td><td></td><td>Switch MII collision detect</td></tr>
<tr><td>87</td><td>SCONF0</td><td>Ipd</td><td></td><td>Dual MII configuration pin</td></tr>
<tr><td>86</td><td>SCONF1</td><td>Ipd</td><td></td><td>Dual MII configuration pin.
<table>
<tr><td>Pin# (91,86,87):</td><td>Switch MII</td><td>PHY[5] MII</td></tr>
<tr><td>000</td><td>disable, Otri</td><td>disable, Otri</td></tr>
<tr><td>001</td><td>phy mode MII</td><td>disable, Otri</td></tr>
<tr><td>010</td><td>mac mode MII</td><td>disable, Otri</td></tr>
<tr><td>011</td><td>phy mode SNI</td><td>disable, Otri</td></tr>
<tr><td>100</td><td>Disable</td><td>Disable</td></tr>
<tr><td>101</td><td>phy mode MII</td><td>phy mode MII</td></tr>
<tr><td>110</td><td>mac mode MII</td><td>phy mode MII</td></tr>
<tr><td>111</td><td>phy mode SNI</td><td>phy mode MII</td></tr>
</table></td></tr>
<tr><td>85</td><td>SCRS</td><td>Ipd / O</td><td></td><td>Switch MII carrier sense</td></tr>
<tr><td>78</td><td>SMRXC</td><td>I / O</td><td></td><td>Switch MII receive clock. Input in MAC mode, output in PHY mode MII.</td></tr>
<tr><td>83</td><td>SMRXD0</td><td>Ipd / O</td><td></td><td>Switch MII receive bit 0; Strap option: LED Mode PD (default) = Mode 0; PU = Mode 1. See also register 11.
<table>
<tr><td></td><td>Mode 0</td><td>Mode 1</td></tr>
<tr><td>LEDX_2</td><td>Lnk/Act</td><td>100Lnk/act</td></tr>
<tr><td>LEDX_1</td><td>Fulld/Col</td><td>10Lnk/act</td></tr>
<tr><td>LEDX_0</td><td>Speed</td><td>Fulld</td></tr>
</table></td></tr>
<tr><td>82</td><td>SMRXD1</td><td>Ipd / O</td><td></td><td>Switch MII receive bit 1. Strap option: PD (default) = Switch MII in 100Mbps mode; PU = Switch MII in 10Mbps mode</td></tr>
<tr><td>81</td><td>SMRXD2</td><td>Ipd / O</td><td></td><td>Switch MII receive bit 2. Strap option: PD (default) = Switch MII in full duplex mode; PU = Switch MII in half-duplex mode.</td></tr>
<tr><td>80</td><td>SMRXD3</td><td>Ipd / O</td><td></td><td>Switch MII receive bit 3. Strap option: PD (default) = Disable Switch MII full-duplex flow control; PU = Enable Switch MII full-duplex flow control</td></tr>
<tr><td>79</td><td>SMRXDV</td><td>Ipd / O</td><td></td><td>Switch MII receive data valid</td></tr>
<tr><td>75</td><td>SMTXC</td><td>I/ O</td><td></td><td>Switch MII transmit clock. Input in MAC mode, output in PHY mode MII.</td></tr>
<tr><td>73</td><td>SMTXD0</td><td>Ipd</td><td></td><td>Switch MII transmit bit 0</td></tr>
<tr><td>72</td><td>SMTXD1</td><td>Ipd</td><td></td><td>Switch MII transmit bit 1</td></tr>
</table>

Pin #	Pin Name	Type	Port	Brief Description
71	SMTXD2	Ipd		Switch MII transmit bit 2
70	SMTXD3	Ipd		Switch MII transmit bit 3
69	SMTXEN	Ipd		Switch MII transmit enable
74	SMTXER	Ipd		Switch MII transmit error
110	SPIC/SCL	I / O	All	1) Input clock up to 5MHz in SPI slave mode; 2) Output clock at 81KHz in I2C master mode. (See pin#113)
111	SPID/SDA	I / O	All	1) Serial data input in SPI slave mode; 2) Serial data input/output in I2C master mode. (See pin#113)
109	SPIQ	Otri	All	1) SPI serial data output in SPI slave mode; 2) Not used in I2C master mode (see pin#113)
112	SPIS_N	Ipu	All	Active low. 1) SPI data transfer start in SPI slave mode. When SPIS_N is high, the KS8995M is deselected and SPIQ is held in high impedance state, a high-to-low transition to initiate the SPI data transfer; 2) Not used in I2C master mode.
128	TEST2	NC		No Connect for normal operation. Factory test pin.
118	TESTEN	Ipd		No Connect for normal operation. Factory test pin
8	TXP1	O	1	Physical transmit signal + (differential)
14	TXP2	O	2	Physical transmit signal + (differential)
23	TXP3	O	3	Physical transmit signal + (differential)
29	TXP4	O	4	Physical transmit signal + (differential)
36	TXP5	O	5	Physical transmit signal + (differential)
7	TXM1	O	1	Physical transmit signal - (differential)
13	TXM2	O	2	Physical transmit signal - (differential)
22	TXM3	O	3	Physical transmit signal - (differential)
28	TXM4	O	4	Physical transmit signal - (differential)
35	TXM5	O	5	Physical transmit signal - (differential)
123	VDDAP	Pwr		1.8V analog VDD for PLL
41	VDDAR	Pwr		1.8V analog VDD
43	VDDAR	Pwr		1.8V analog VDD
3	VDDAR	Pwr		1.8V analog VDD
15	VDDAR	Pwr		1.8V analog VDD
31	VDDAR	Pwr		1.8V analog VDD
125	VDDAR	Pwr		1.8V analog VDD
18	VDDAT	Pwr		2.5V or 3.3V analog VDD
9	VDDAT	Pwr		2.5V or 3.3V analog VDD
24	VDDAT	Pwr		2.5V or 3.3V analog VDD
37	VDDAT	Pwr		2.5V or 3.3V analog VDD
50	VDDC	Pwr		1.8V digital core VDD
89	VDDC	Pwr		1.8V digital core VDD
117	VDDC	Pwr		1.8V digital core VDD
59	VDDIO	Pwr		3.3/2.5V digital VDD for digital I/O circuitry
77	VDDIO	Pwr		3.3/2.5V digital VDD for digital I/O circuitry
100	VDDIO	Pwr		3.3/2.5V digital VDD for digital I/O circuitry
121	X1	I		25MHz crystal clock connection/or 3.3 V tolerant Oscillator Input. Oscillator should be +/- 100 ppm.
122	X2	O		25MHz crystal clock connection

Note:

Pwr = power supply;
Gnd = ground;
I = input;
O = output;
I / O = bi-directional;
Ipu = input w/ internal pull-up;
Ipd = input w/ internal pull-down;
Ipd / O = input w/ internal pull-down during reset, output pin otherwise;
Ipu / O = input w/ internal pull-up during reset, output pin otherwise;
PU = strap pin pull-up;
PD = strap pull-down;
Otri = output tristated
NC = No Connect

7.0 Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level.

Table 16 - Absolute Maximum Ratings

Description	Pins	Value
Storage Temperature	N/A	- 55 °C to 150 °C
Supply Voltages	VDDAR, VDDAP, VDDC	-0.5 V to 2.4 V
	VDDAT, VDDIO	-0.5 V to 4.0 V
Input Voltage	All Inputs	-0.5 V to 4.0 V
Output Voltage	All Outputs	-0.5 V to 4.0 V
Max. Junction Temperature	N/A	

7.1 Recommended Operating Conditions

Table 17 Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply Voltages	VDDAR, VDDAP, VDDC	1.7	1.8	1.9	V
	VDDAT, VDDIO	2.4 or 3.0	2.5 or 3.3	2.6 or 3.6	V
	VDDIO	3.0	3.3	3.6	V
Ambient Operating Temperature Commercial (KS8995M)	T_A	0		70	°C
Ambient Operating Temperature Industrial (KS8995Mi)	T_A	-40		85	°C
Max. Junction Temperature	T_J			125	°C
Thermal Resistance Junction to Ambient	θ_{JA}		32		°C/W

8.0 Electrical Characteristics

Table 18 Electrical Characteristics

Supply Current (including TX output driver current, KS8995M chip only) **Typical values are measured at 1.8/2.5v and max. values at 1.9/3.6v**						
	100BaseTX operation – All ports 100 % Utilization		**Min.**	**Typ.**	**Max.**	**Unit**
100BaseTX (transmitter)	I_{dx}	VDDAT		229	250	mA
100BaseTX (digital core+analog Rx)	I_{ddc}	VDDC, VDDAP		157	230	mA
100BaseTX (digital IO)	I_{ddio}	VDDIO		17	30	mA
	10BaseTX operation – All ports 100 % Utilization		**Min.**	**Typ.**	**Max.**	**Unit**
10BaseT (transmitter)	I_{dx}	VDDAT		350	375	mA
10BaseTX (digital core+analog Rx)	I_{ddc}	VDDC, VDDAP		102	180	mA
10BaseT(digital IO)	I_{ddio}	VDDIO		6	15	mA
	Auto Negotiation Mode		**Min.**	**Typ.**	**Max.**	**Unit**
10BaseT (transmitter)	I_{dx}	VDDAT		25	40	mA
10BaseTX (digital core+analog Rx)	I_{ddc}	VDDC, VDDAP, VDDC		108	180	mA
10BaseT(digital IO)	I_{ddio}	VDDIO		17	20	mA
	TTL Inputs		**Min.**	**Typ.**	**Max.**	**Unit**
Input High Voltage	V_{ih}		½ VDDIO + 0.4 V			V
Input Low Voltage	V_{il}				½ VDDIO –0.4 V	V
Input Current (excluding pull up / pull down)	I_{in}	V_{in} = GND ~ VDDIO	-10		10	µA

	TTL Outputs		Min.	Typ.	Max.	Unit
Output High Voltage	V_{oh}	I_{oh} = - 8 mA	VDDIO-0.4			V
Output Low Voltage	V_{ol}	I_{ol} = 8 mA			0.4 V	V
Output Tri-state Leakage	$\|I_{oz}\|$				10	µA
100BaseTX Transmit (measured differentially after 1:1 transformer)						
Peak Differential Output Voltage	V_o	100 Ω termination on the differential output.	0.95		1.05	V
Output Voltage Imbalance	V_{imb}	100 Ω termination on the differential output			2	%
Rise/Fall time	T_r/T_f		3		5	ns
Rise/Fall time Imbalance			0		0.5	ns
100BaseTX Transmit (measured differentially after 1:1 transformer)						
Duty Cycle Distortion					± 0.5	ns
Overshoot					5	%
Reference Voltage of ISET	V_{set}			0.5		V
Output Jitters		Peak to peak		0.7	1.4	ns
10BaseT Receive						
Squelch Threshold	V_{sq}	5 MHz square wave		400		mV
10BaseT Transmit (measured differentially after 1:1 transformer) VDDAT= 2.5V						
Peak Differential Output Voltage	V_p	100 Ω termination on the differential output.		2.3		V
Jitters Added		100 Ω termination on the differential output.			± 3.5	ns
Rise/Fall time				28	30	ns

9.0 Timing Specifications

9.1 EEPROM Timing

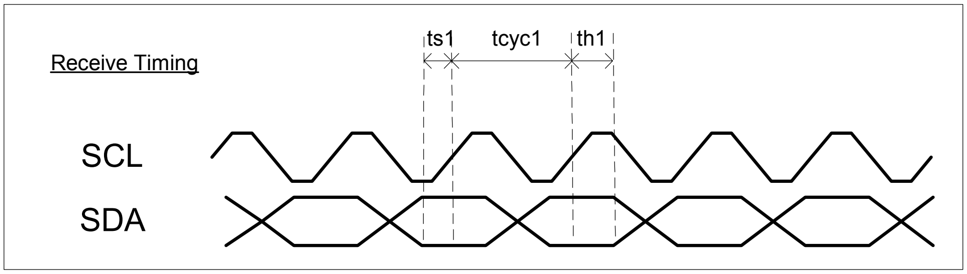


Figure 9 EEPROM Interface Input Timing Diagram

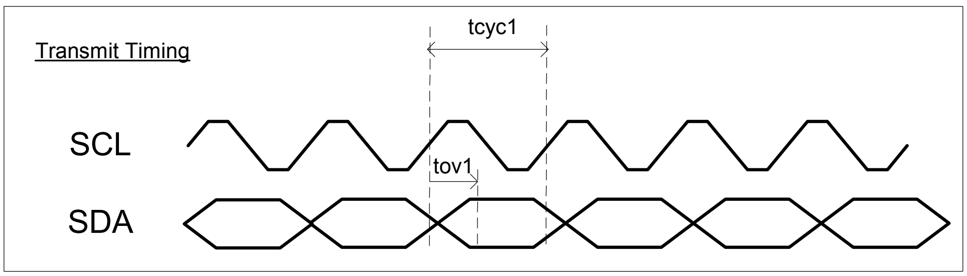


Figure 10 EEPROM Interface Output Timing Diagram

Table 19-EEPROM Timing Parameters

Timing Parameter	Description	Min	Typ	Max	Unit
tcyc1	Clock cycle		16384		ns
ts1	Setup time	20			ns
th1	Hold time	20			ns
tov1	Output Valid	4096	4112	4128	ns

9.2 SNI Timing

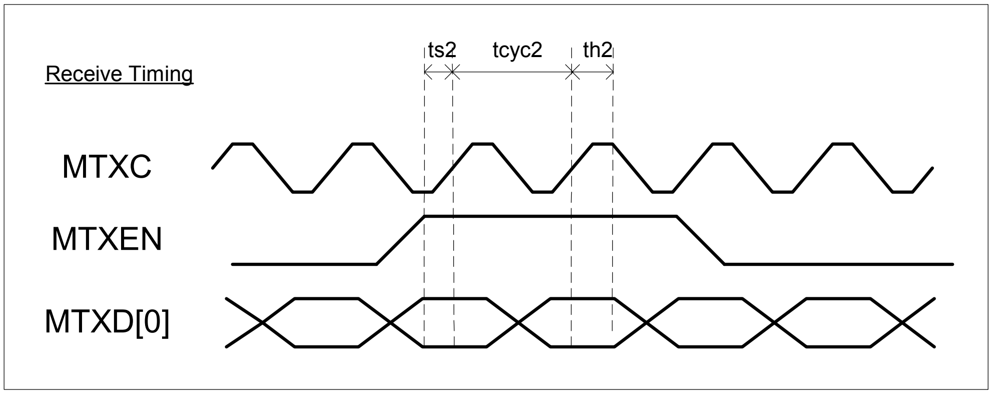


Figure 11 SNI Input Timing Diagram

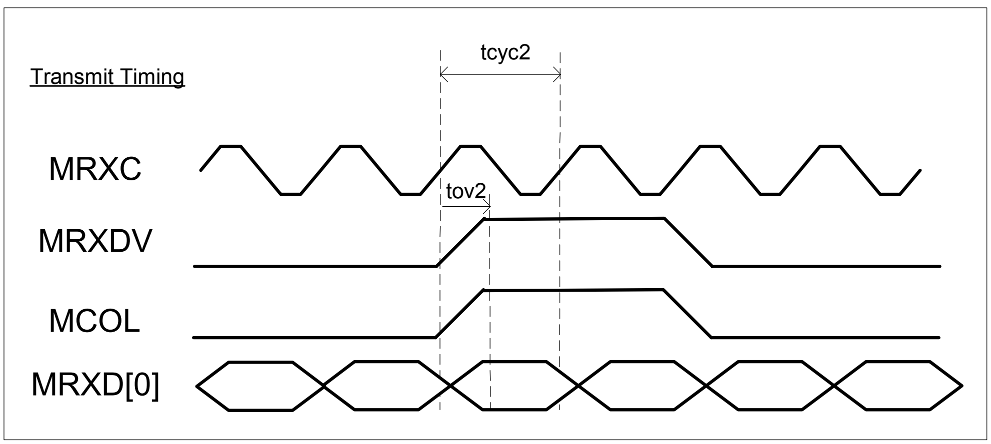


Figure 12 SNI Output Timing Diagram

Table 20 SNI Timing Parameters

Timing Parameter	Description	Min	Typ	Max	Unit
tcyc2	Clock cycle		100		ns
ts2	Setup time	10			ns
th2	Hold time	0			ns
tov2	Output Valid	0	3	6	ns

9.3 MII Timing

9.3.1 MAC Mode MII Timing

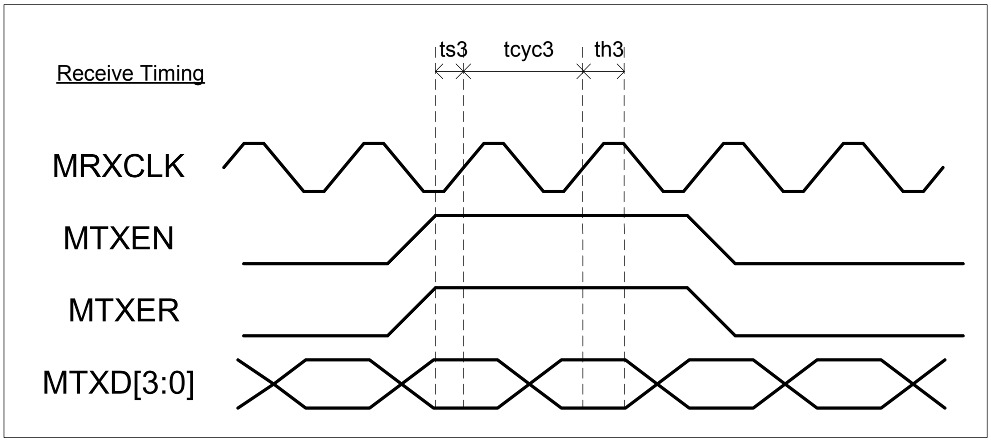


Figure 13 MAC Mode MII Timing-Data received from MII

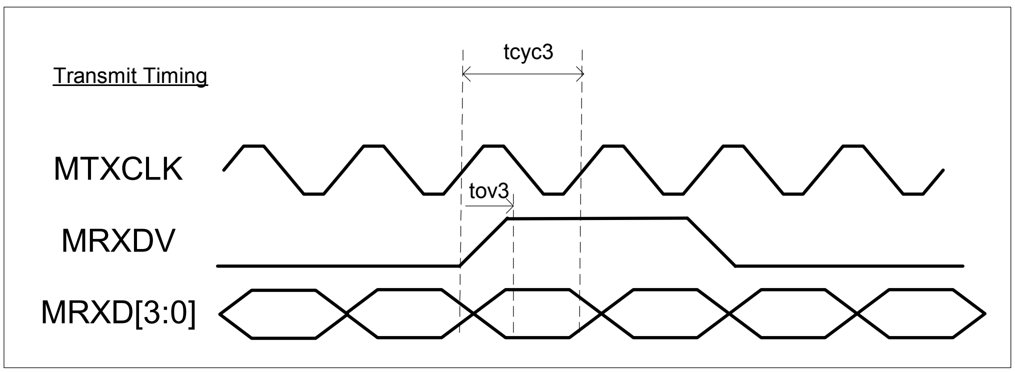


Figure 14 MAC Mode MII Timing-Data transmitted to MII

Table 21 MAC mode MII Timing Parameters

Timing Parameter	Description	Min	Typ	Max	Unit
tcyc3 (100BaseT)	Clock cycle 100BaseT		40		ns
tcyc3 (10BaseT)	Clock cycle 10BaseT		400		ns
ts3	Setup time	10			ns
th3	Hold time	5			ns
tov3	Output Valid	7	11	16	ns

9.3.2 PHY Mode MII Timing

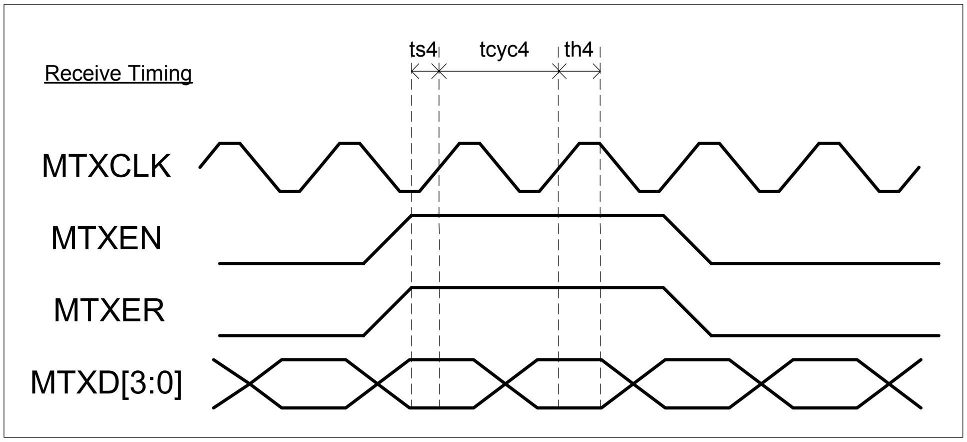


Figure 15 PHY Mode MII Timing – Data received from MII

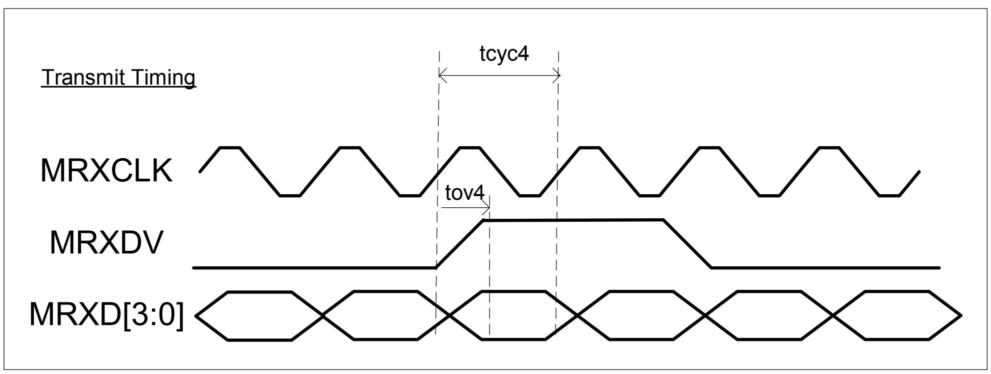


Figure 16 PHY Mode MII Timing-Data transmitted to MII

Table 22 PHY Mode MII Timing Parameters

Timing Parameter	Description	Min	Typ	Max	Unit
tcyc4 (100BaseT)	Clock cycle 100BaseT		40		ns
tcyc4 (10BaseT)	Clock cycle 10BaseT		400		ns
ts4	Setup time	10			ns
th4	Hold time	0			ns
tov4	Output Valid	18	25	28	ns

9.4 SPI Timing

Figure 17 SPI Input Timing

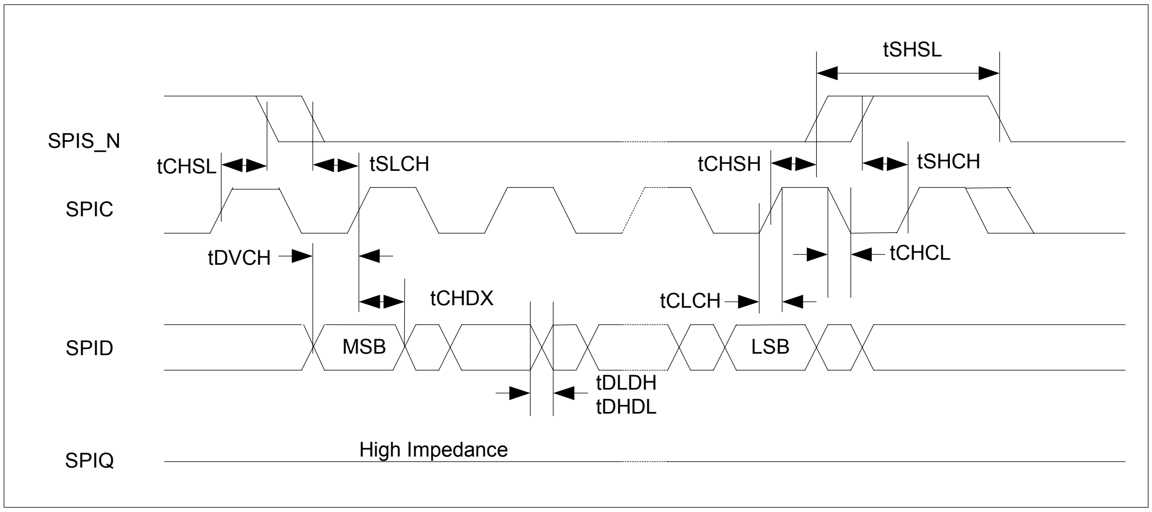


Table 23 SPI Input Timing Parameters

Timing Parameter	Description	Min	Max	Units
fC	Clock Frequency		5	MHz
tCHSL	SPIS_N Inactive Hold Time	90		ns
tSLCH	SPIS_N Active Setup Time	90		ns
tCHSH	SPIS_N Active Hold Time	90		ns
tSHCH	SPIS_N Inactive Setup Time	90		ns
tSHSL	SPIS_N Deselect Time	100		ns
tDVCH	Data Input Setup Time	20		ns
tCHDX	Data Input Hold Time	30		ns
tCLCH	Clock Rise Time		1	us
tCHCL	Clock Fall Time		1	us
tDLDH	Data Input Rise Time		1	us
tDHDL	Data Input Fall Time		1	us

Figure 18 SPI Output Timing

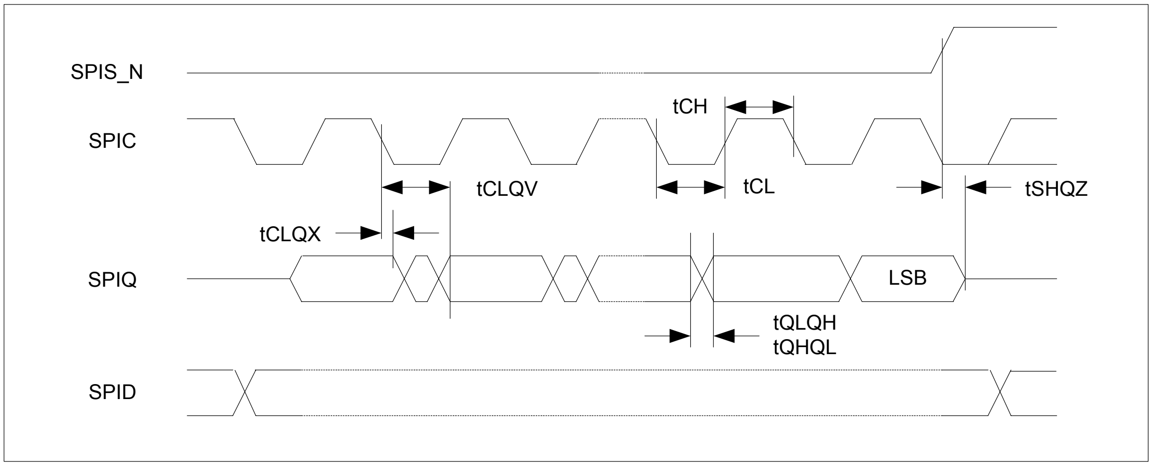


Table 24 SPI Output Timing Paramaters

Timing Parameter	Description	Min	Max	Units
fC	Clock Frequency		5	MHz
tCLQX	SPIQ Hold Time	0	0	ns
tCLQV	Clock Low to SPIQ Valid		60	ns
tCH	Clock High Time	90		ns
tCL	Clock Low Time	90		
tQLQH	SPIQ Rise Time		50	ns
tQHQL	SPIQ Fall Time		50	ns
tSHQZ	SPIQ Disable Time		100	ns

9.5 Reset Timing

Figure 19 Reset Timing

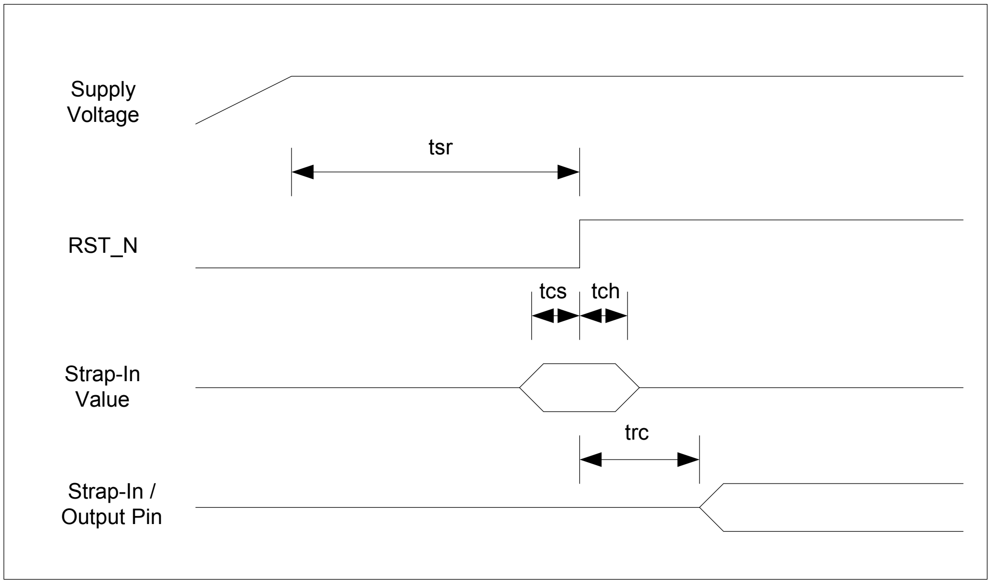


Table 25 Reset Timing Parameters

Parameter	Description	Min	Max	Units
t_{sr}	Stable supply voltages to reset high	10		ms
t_{cs}	Configuration setup time	50		ns
t_{ch}	Configuration hold time	50		ns
t_{rc}	Reset to Strap-In pin output	50		us

10.0 Package Outline and Dimensions

128 Pin PQFP Package Outline Drawing

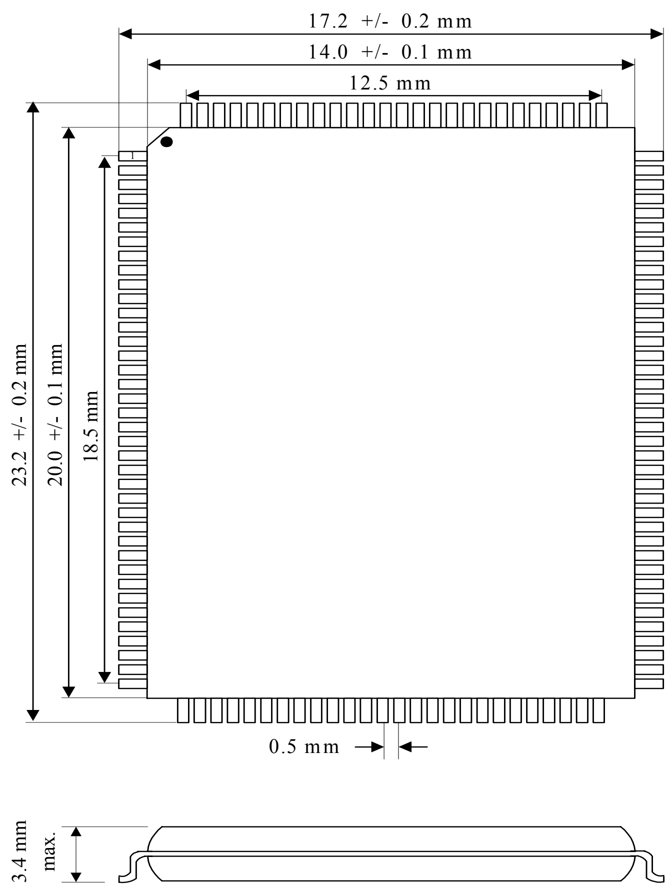


Figure - Package Outline

Thermal resistance θ_{JA} = 32 ˚C/W

11.0 Selection of Isolation Transformers

A 1:1 isiolation transformer is required at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements. The following table gives recommended transformer characteristics.

Table 26 Transformer Selection Criteria

Parameter	Value	Test Condition
Turns Ratio	1 CT : 1 CT	
Open-Circuit Inductance (min.)	350 uH	100 mV, 100 kHz, 8 mA
Leakage Inductance (max.)	0.4 uH	1 MHz (min.)
Inter-Winding Capacitance (max.)	12 pF	
D.C. Resistance (max.)	0.9 Ohms	
Insertion Loss (max.)	1.0 dB	0-65 MHz
HIPOT (min.)	1500 Vrms	

The following transformers have been tested with the KS8995M.

Table 27 Qualified Magnetics

4 port Integrated			
Magnetic manufacturer	Part number	AUTO MDIX	Number of port
Pulse	H1164	Yes	4
Bel Fuse	558-5999-Q9	Yes	4
YCL	PH406466	Yes	4
Transpower	HB826-2	Yes	4
Delta	LF8731	Yes	4
LanKom	SQ-H48W	Yes	4

Single Port			
Magnetic manufacturer	Part number	AUTO MDIX	Number of port
Pulse	H1102	Yes	1
Bel Fuse	S558-5999-U7	Yes	1
YCL	PT163020	Yes	1
Transpower	HB726	Yes	1
Delta	LF8505	Yes	1
LanKom	LF-H41S	Yes	1

12.0 Part Ordering Information

Part Number	Package	Description
KS8995M A	128 pin PQFP	5 port 10/100 Integrated Managed Switch Commercial Temperature
KS8995M-EVAL	N/A	KS8995M Evaluation Kit

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