# GateMate™ FPGA

## Empowering Innovation — Our FPGA Solution: Ideal for Seamless Integration in Projects of Every Scale, from Small to High-Volume Applications

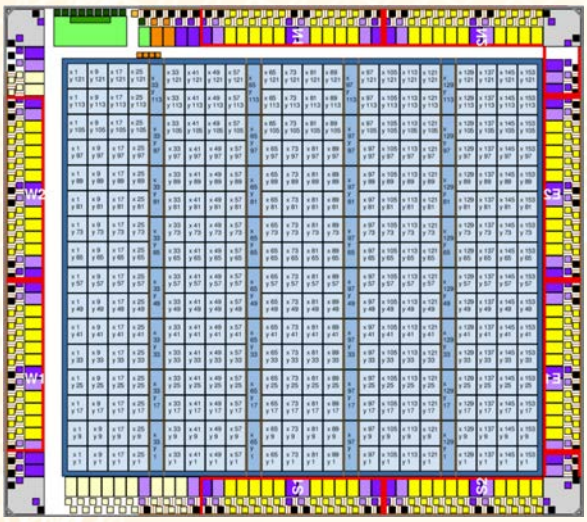
designed and manufactured in Germany

## Overview

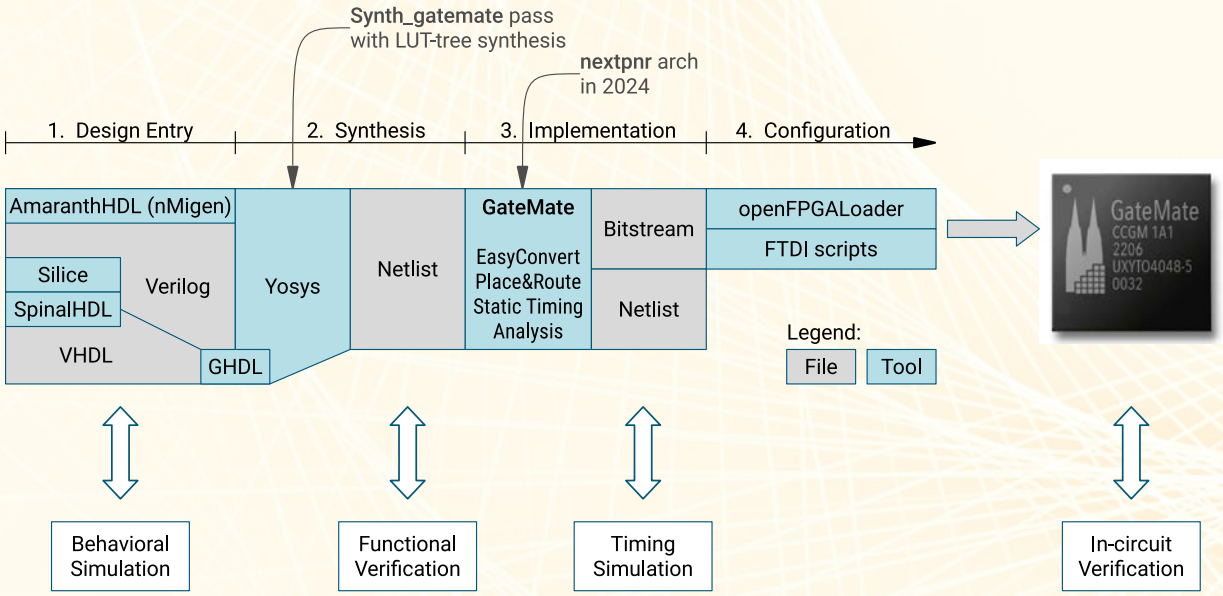
The GateMate FPGA family leverages the complete spectrum of Cologne Chip innovation and benefits from EU based manufacturing. With high logic capacity, multi-die capability, low power footprint and combined with lowest cost in industry make GateMate well suited for small as well as high-volume applications.

The architecture of the GateMate FPGA is based on a novel Cologne Programmable Element (CPE). The CPE architecture enables the efficient construction of arbitrarily sized logic, such as multipliers for digital signal processing applications. Applications can leverage embedded Block RAMs with bit widths in a range from 1 to 80 bits. Fast communication can be archieved with over 162 GPIO pins, which can be configured as single-ended or LVDS differential pairs, each supporting double data rate (DDR) registers. The embedded Serializer-Deserializer (SerDes) blocks allow high-speed serial communication with bandwidths of up to 5 Gb/s.

The strengths of GateMate FPGA devices are reinforced by incorporation of open-source design tools and a proprietary free-of-charge Place & Route tool by Cologne Chip into the design flow. With this integration, Cologne Chip enables an easy start with GateMate FPGAs. The appeal of GateMate is further enhanced by utilizing reliable and advanced process nodes (Globalfoundries™ 28nm SLP) and its availability through EU based manufacturing.




Architecture overview of **GateMate™ CCGM1A1**




Design flow of **GateMate™**

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Cologne Chip
GateMate FPGA

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GateMate FPGA Technology

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## GateMate™ Features

- Logic capacity from 20,480 to 512,000 CPEs
- Block RAM from 1,310,720 to 32,768,000 bits
- 3 Operation Modes: low power (0.9V), economy (1.0V), speed (1.1V)
- Ball grid package for compact size and high pin count, requiring only 4 layers on PCB
- Small configuration file and fast configuration by using Quad SPI interface (up to 100MHz)
- Embedded 5 Gb/s Serializer-Deserializer (SerDes)
- Multiple clock domains (from 4 to 100 embedded PLLs)
- Support for ADC and DAC with additional IPs
- All GPIOs MIPI D-PHY (CSI-2) and HDMI compatible
- No excessive start-up currents
- Globalfoundries™ 28nm Super Low Power (SLP) manufactured in Europe
- Yosys framework coupled with proprietary, free of charge, Place & Route tool
- GateMate is available in different variants and sizes with preserved main pin compatibility
- ITAR free
- An integrated logic analyzer (ILA) for in-system debugging of GateMate FPGA designs during runtime is available free of charge

## GateMate™ Evaluation Board

Interfaces:

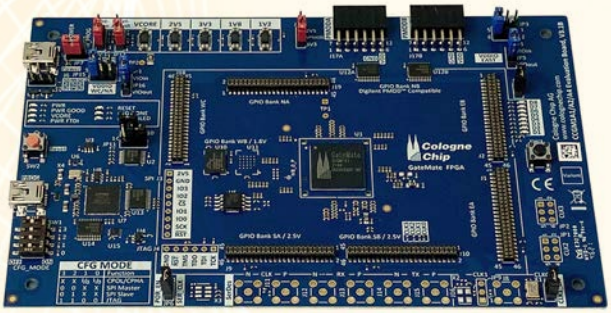
- Six I/O banks + access to SPI/JTAG signals
- Two standard 12-pin Pmod™ connectors
- 5 Gb/s SerDes via SMA connectors
- Access to all dedicated clock inputs
- Configuration via onboard Flash, USB or JTAG

Memory:

- 64 Mbit Quad-I/O SPI Flash
- Up to two HyperBus memories on board (HyperRAM/HyperFlash)

Power:

- User-selectable core and I/O voltages




Evaluation Board of **GateMate™**

| Device | Rel. size | Cologne Programmable Elements 1) 2) | | Block RAMs 3) | | PLLs | SerDes | I/Os | | Package | | Availability |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | CPEs | FF/Latches | 20Kb | 40Kb | | | single-ended | differential | balls | size (mm) | |
| CCGM1A1 | 1 | 20,480 | 40,960 | 64 | 32 | 4 | 1 | 162 | 81 | 324BGA | 15x15 | now |
| CCGM1A2 | 2 | 40,960 | 81,920 | 128 | 64 | 8 | 2 | 162 | 81 | 324BGA | 15x15 | now |
| CCGM1A4 | 4 | 81,920 | 163,840 | 256 | 128 | 16 | 4 | 154 | 77 | 324BGA | 15x15 | 2025 |
| CCGM1A9 | 9 | 184,320 | 368,640 | 576 | 288 | 36 | 9 | tba | tba | tba | tba | tba |
| CCGM1A16 | 16 | 327,680 | 655,360 | 1,024 | 512 | 64 | 16 | tba | tba | tba | tba | tba |
| CCGM1A25 | 25 | 512,000 | 1,024,000 | 1,600 | 800 | 100 | 25 | tba | tba | tba | tba | tba |

1) CPEs have 2x4 or 8 inputs connected to a LUT tree  2) Each CPE can be used as 2x2 Multiplier tile  3) Block RAM can have a data width of 1-80 bits

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