MPQ2026A
40V, 300mA Dual-Channel LDO with Pre-Boost, I²C, and ADC for Digital Diagnosis and Protection, AEC-Q100 Qualified

DESCRIPTION

The MPQ2026A is a dual-channel, low-dropout (LDO) regulator. It contains a boost pre-regulator operating at either 400kHz or 2.2MHz with an I²C interface, as well as one-time programmable (OTP) memory. The device provides phantom power to low-noise amplifiers (LNAs) for active antennas in automotive systems, and can work in cold-crank conditions (3V) up to load-dump conditions (40V).

The device delivers up to 300mA per channel with excellent load and line regulation. When the battery is healthy (meaning the input voltage (V_{IN}) exceeds the pre-boost turn-on threshold) during normal operation, the pre-boost regulator is completely turned off to reduce the quiescent current. This makes the MPQ2026A well-suited for power supplies that are always turned on.

The pre-boost regulator provides an integrated MOSFET to further reduce the external component count and EMI. Both the LDO and boost outputs can be configured via the I²C interface. The pre-boost regulator's output voltage (V_{OUT_BOOST}) can be configured between 6.5V and 15.9V. The LDO output voltages (V_{OUT1} and V_{OUT2}) can be configured between 1V and 13.6V. This protects the LDO output during load dumps.

During bench evaluations, different configurations can be easily obtained via the I²C interface, instead of reworking external components. Once the optimal settings have been reached, the multi-page one-time programmable memory can permanently store the settings.

The MPQ2026A is available in a QFN-16 (4mmx4mm) package.
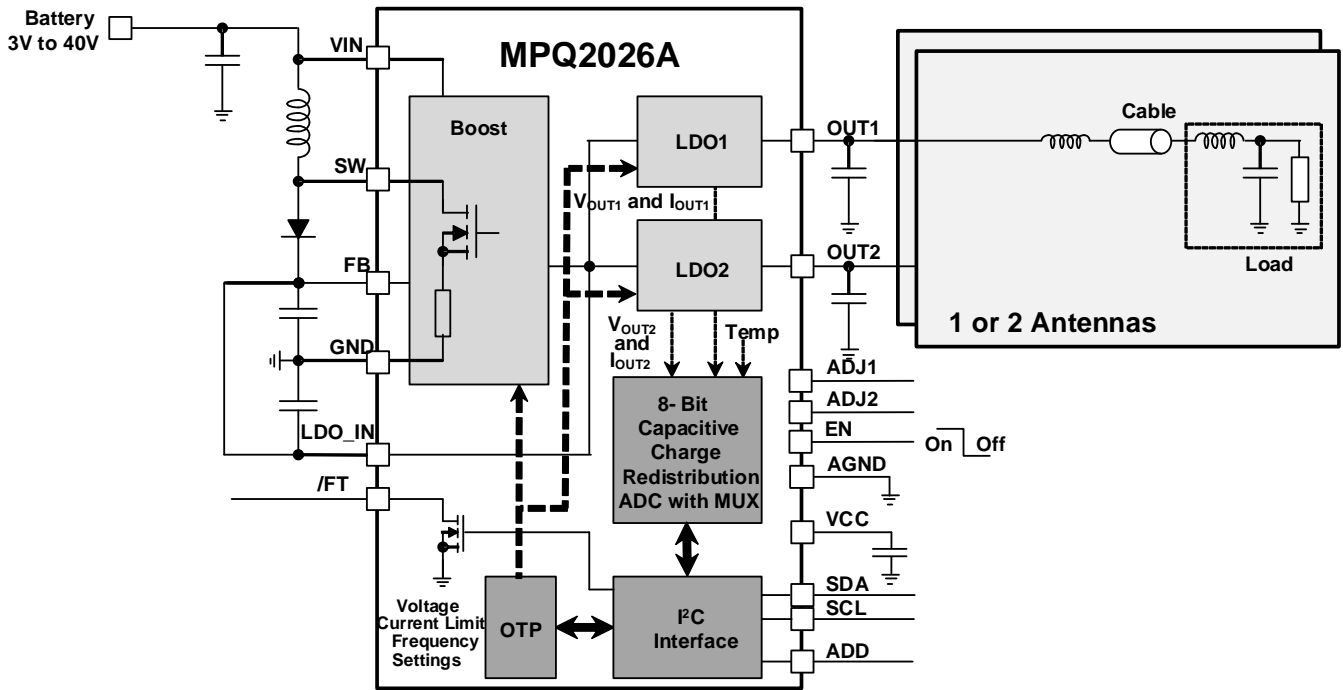
FEATURES

- Powerful Digital Capabilities:
  - No External Resistor Network for Output Voltage Settings
  - Configurable, Dual LDOs:
    - 300mA Continuous Output Current (I_{OUTx}) per Channel
    - 1V to 13.6V Output Voltage (V_{OUTx}) Range
    - Over-Temperature Protection
  - Configurable, Asynchronous Pre-Boost Regulator:
    - 4A/40V Internal MOSFET
    - 6.5V to 15.9V Output Voltage (V_{OUT_BOOST}) Range with 100mV Adjustable Steps
    - 400kHz or 2.2MHz Switching Frequency (f_{SW})
    - Over-Temperature Protection
  - I²C Interface
  - Analog-to-Digital Converter (ADC) for LDO Output Voltages and Load Currents
  - Multi-Page One-Time Programmable (OTP) Memory
- Optimized for EMC/EMI:
  - Frequency Dithering for Low-EMI Operation
- Additional Features:
  - Wide 3V to 40V Input Voltage Range
  - 35µA Low Quiescent Current
  - Soft Start for All Regulator Outputs
  - LDO Short-to-Battery Detection
  - Available in a QFN-16 (4mmx4mm) Package
  - Available with Wettable Flanks
  - Available in AEC-Q100 Grade 1

APPLICATIONS

- Antenna Phantom Power
- Automotive Cameras
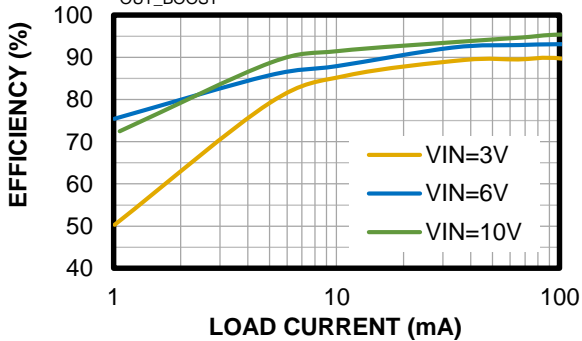- ADAS with Functional Safety and ASIL Requirements

TYPICAL APPLICATION

Battery 3V to 40V

VIN

MPQ2026A

Boost

SW

FB

GND

LDO_IN

/FT

LDO1

LDO2

V_{OUT1} and I_{OUT1}

V_{OUT2} and I_{OUT2}

Temp

8- Bit Capacitive Charge Redistribution ADC with MUX

Voltage Current Limit Frequency Settings

OTP

I²C Interface

OUT1

OUT2

Cable

Load

1 or 2 Antennas

ADJ1

ADJ2

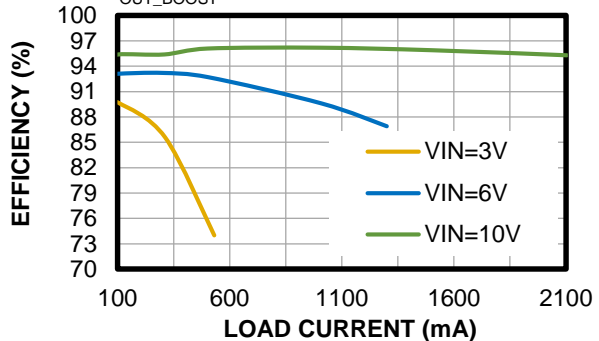**EN**   On ⌐ Off

AGND

VCC

SDA

SCL

ADD

Boost Efficiency vs. Load Current

Dual LDO disabled, V_{OUT_BOOST} = 12V, f_{SW} = 400kHz, L = 10µH (DCR = 45mΩ), rectifier diode B350A-13-F, FSS on, I_{OUT_BOOST} = 1mA to 100mA

EFFICIENCY (%)

LOAD CURRENT (mA)

VIN=3V
VIN=6V
VIN=10V

Boost Efficiency vs. Load Current

Dual LDO disabled, V_{OUT_BOOST} = 12V, f_{SW} = 400kHz, L = 10µH (DCR = 45mΩ), rectifier diode B350A-13-F, FSS on, I_{OUT_BOOST} = 100mA to 2.1A

EFFICIENCY (%)

LOAD CURRENT (mA)

VIN=3V
VIN=6V
VIN=10V

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating***
MPQ2026AGRE-xxxx-AEC1**	QFN-16 (4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ2026AGRE-xxxx-AEC1-Z).

** "-xxxx" is the configuration code identifier for the register settings stored in the OTP register. Each "-x" can be a hexadecimal value between 0 and F. The default code is "-0000." Contact an MPS FAE to create this unique number.
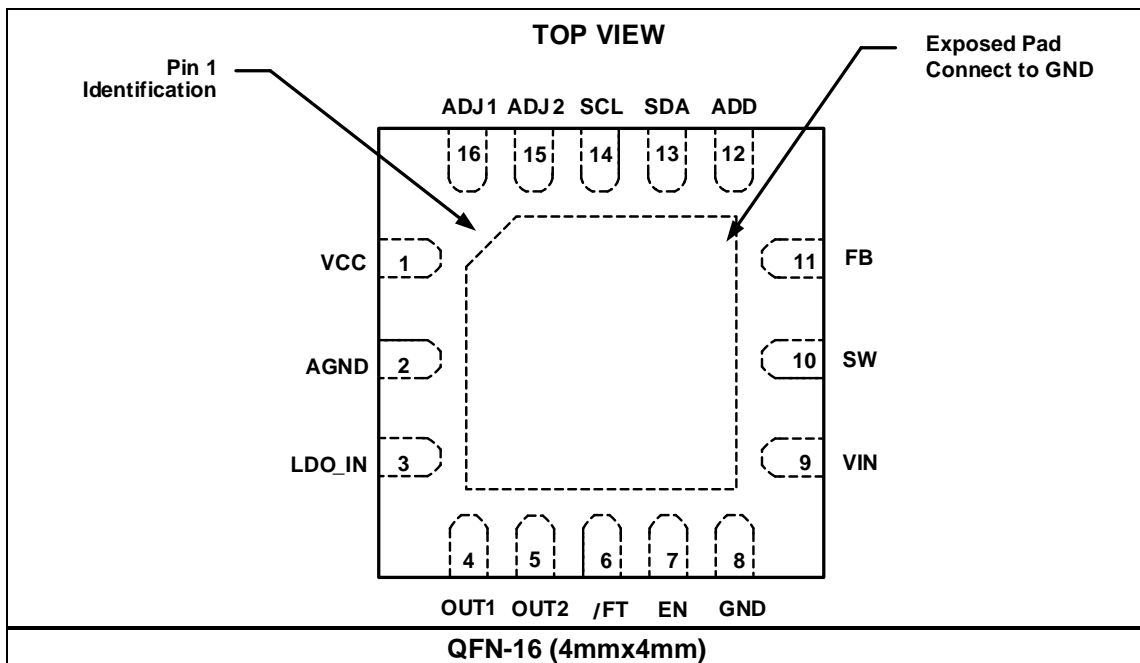
*** Moisture Sensitivity Level Rating

TOP MARKING

MPSYWW
M2026A
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
M2026A: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE

QFN-16 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VCC	**Bias supply.** The VCC pin is a 5V, internal regulator output. VCC supplies power to the I²C interface, internal control circuit, and gate drivers. Place an external, low-ESR decoupling capacitor from VCC to ground, and close to this pin. A 1µF to 10µF ceramic capacitor is recommended.
2	AGND	**Analog ground.** The AGND pin is the ground for the internal logic and signal control blocks.
3	LDO_IN	**Supply input of the dual LDOs.** In addition the capacitors for the boost converter on the FB pin, place a 1µF to 10µF ceramic between the LDO_IN pin and ground.
4	OUT1	**Output of LDO1.** For stability, place a lower-value ceramic capacitor at the OUT1 pin to act as an output capacitor. A 10µF ceramic capacitor is recommended for most applications.
5	OUT2	**Output of LDO2.** For stability, place a lower-value ceramic capacitor at the OUT2 pin to act as an output capacitor. A 10µF ceramic capacitor is recommended for most applications.
6	/FT	**Fault pin output.** The /FT pin is an open-drain status pin. Connect /FT to a voltage source (≤5V) with a resistor (e.g. 100kΩ). Float or ground this pin if it is not used.
7	EN	**Enable.** Pull the EN pin below the falling threshold (2.2V) to shut down the chip. Pull EN above its rising threshold (2.4V) to enable the chip. To enable the chip, EN can be connected to VIN through a pull-up resistor (e.g. 100kΩ). EN has an internal, 3.3MΩ pull-down resistor. Float the EN pin to disable the chip.
8	GND	**Power ground.** The GND pin is the reference ground for the regulated output voltage. Connect GND to larger copper areas to improve the thermal results.
9	VIN	**Input supply.** The VIN pin supplies power to all of the internal control circuitries and the power switch connected to SW. Connect a decoupling capacitor from VIN to ground, and place it as close as possible to VIN.
10	SW	**Switching node.** The SW pin is the switching node of the asynchronous pre-boost converter. Place a Schottky diode and an inductor at SW to form a pre-boost converter. Float the SW pin if it is not used.
11	FB	**Boost converter feedback.** An internal resistor divider is connected between the FB pin and ground. Connect FB to the rectifier diode of the asynchronous pre-boost converter. The output capacitors for the boost should be placed as close to this pin as possible, with a short return path to the ground plane. Float the FB pin if it is not used.
12	ADD	**Address setting for I²C.** Connect a resistor between the ADD pin and ground to set the I²C address. Float the ADD pin if it is not used.
13	SDA	**I²C serial data.** The SDA pin is an open-drain port. An external pull-up resistor is required to connect this pin to the supply rail of the I²C bus. If SDA is not used, it is recommended to connect SDA to the VCC pin through a resistor (e.g. 100kΩ).
14	SCL	**I²C serial clock.** The SCL pin is an open-drain port. An external pull-up resistor is required to connect this pin to the supply rail of the I²C bus. If SCL is not used, it is recommended to connect SCL to the VCC pin through a resistor (e.g. 100kΩ).
15	ADJ2	**The reference voltage input for LDO2.** In tracking mode for the LDO output voltage, connect the ADJ2 pin directly to the voltage reference, or use a voltage divider for lower output voltages. If ADJ2 is not used, float this pin or connect it to GND.
16	ADJ1	**The reference voltage input for LDO1.** In tracking mode for the LDO output voltage, connect the ADJ1 pin directly to the voltage reference, or use a voltage divider for lower output voltages. If ADJ1 is not used, float this pin or connect it to GND.
-	Exposed pad	**Exposed thermal power pad.** Connect the exposed pad (EP) to the ground plane for optimal heat dissipation. Do not use EP as the primary electrical ground connection.

ABSOLUTE MAXIMUM RATINGS [(1)]

VIN, SW, FB, LDO_IN, OUT1, OUT2 ....
....-0.3V to +45V
ADJ1, ADJ2 ....-0.3V to +15V
All other pins ....-0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) [(2)] [(6)]
QFN-16 (4mmx4mm) 4W
Junction temperature ....150°C
Lead temperature ....260°C
Storage temperature................ -65°C to +150°C

ESD Discharge (ESD) Ratings

Human body model (HBM)………………………...
VCC - VIN .... Class 1C [(3)]
Other pins ....Class 2 [(3)]
Charged device model (CDM) .... Class C2b [(4)]

Recommended Operating Conditions

V_{IN} ....3V to 40V
Pre-boost regulator output voltage (V_{OUT_BOOST})..
....6.5V to 15.9V
LDO output voltage (V_{OUT1}, V_{OUT2})………………
…………………………………………1V to 13.6V
LDO load current range (I_{OUT1}, I_{OUT2})....... 300mA
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-16 (4mmx4mm)
JESD51-5/7.........................40.4......6.....°C/W [(5)]
EVQ2026A-R-00A.................31......5.5...°C/W [(6)]

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)- T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on JESD51-5/7, 4-layer PCB, where a thermal via array under the exposed pad. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-5/7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application, the value of θ_{JC} shows the thermal resistance from junction-to-case bottom.
6) Measured on EVQ2026A-R-00A, 4-layer, 2oz, 9cmx9cm PCB, the value of θ_{JC} shows the thermal resistance from junction-to-case top.

ELECTRICAL CHARACTERISTICS

Typical values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Voltage and Current Parameters						
Input voltage	V_{IN}		3		40	V
Supply current (quiescent)	I_Q	LDO enabled, boost disabled, V_{OUT1} = V_{OUT2} = 9V, ADC disabled, no load, T_J = 25°C		35		µA
		LDO enabled, boost disabled, V_{OUT1} = V_{OUT2} = 9V, ADC disabled, no load, T_J = -40°C to +150°C			135	µA
Supply current (shutdown)	I_{SD}	V_{EN} = 0V			5	µA
V_{IN} under-voltage lockout (UVLO) rising threshold	$UVLO_{VTH-R}$	Boost enabled	2.6	2.8	3	V
		Boost disabled		4.2		
V_{IN} UVLO falling threshold	$UVLO_{VTH-F}$	Boost enabled	1.8	2	2.2	V
		Boost disabled		3.8		V
Pre-boost under-voltage filtering time	t_{BST-UV}	Time after V_{IN} falls below boost turn-on threshold to generate the first switching pulse	10		200	µs
Thermal Shutdown and Over-Temperature Protection						
Thermal shutdown [7]	T_{SD}	Junction temperature rising		170		°C
Thermal shutdown hysteresis [7]	T_{SD-HYS}			20		°C
/FT						
/FT sink current capacity	$V_{FT-SINK}$	Sink 4mA			300	mV
/FT delay time	$t_{FT-DELAY}$	Rising edge		40		µs
		Falling edge		40		µs
/FT leakage current	I_{FT-LKG}			10	100	nA
Enable						
Enable rising threshold	EN_{VTH_R}	Level sensitive input	2.1	2.4	2.7	V
Enable falling threshold	EN_{VTH_F}	Level sensitive input	1.9	2.2	2.5	V
Enable threshold hysteresis	V_{EN-HYS}			200		mV
Enable input current	I_{EN}	V_{EN} = 2V		0.6	1.2	µA
Internal VCC						
VCC regulator	V_{CC}	I_{CC} = 0mA	4.8	5	5.2	V
Fault Detection						
Power on short-to-battery detection window	t_{BLK-RC}	Default setting: reg 0x0F, bits[7:6] = 00		15		ms
		Reg 0x0F, bits[7:6] = 01		7		
		Reg 0x0F, bits[7:6] = 10		3		
		Reg 0x0F, bits[7:6] = 11		1		
Short to battery threshold	V_{STB}	V_{OUT} - V_{IN}, check during turn-on sequence		-80	-10	mV

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Dual Linear Regulator (LDO1 and LDO2)						
Regulated output range	$V_{OUT1/2}$	Configurable range	1		13.6	V
		Default setting		9		V
Accuracy of output voltage	$V_{OUT1/2\_ACC}$	Default setting $V_{OUT1/2}$ = 9V, T_J = 25°C	-2		+2	%
		Default setting $V_{OUT1/2}$ = 9V, T_J = -40°C to +150°C	-3		+3	
		$V_{OUT1/2}$ = 1V to 13.6V, T_J = 25°C	-3		+3	
		$V_{OUT1/2}$ = 1V to 13.6V, T_J = -40°C to +150°C	-4		+4	
Line regulation	dV_{ALINE}	V_{IN} = 15V to 40V, 5mA load current, V_{OUT} = 9V,	-10	1	+10	mV
Load regulation	dV_{ALOAD}	I_{LOAD} = 5mA to 300mA, V_{OUT} = 9V, T_J = 25°C		30	50	mV
Power supply rejection ratio [7]	PSRR	I_{LOAD} = 100mA at 100Hz, V_{OUT} = 9V		60		dB
Dropout voltage	$V_{DROPOUT}$	I_{LOAD} = 100mA, measured between LDO_IN and OUTx, T_J = 25°C		250	400	mV
		I_{LOAD} = 100mA, measured between LDO_IN and OUTx, T_J = -40°C to +150°C			700	
Over-current limit	$I_{LDO-LIMIT}$	Configurable range	100		500	mA
		Default value		400		mA
Accuracy of current limit	$I_{LDO-LIMIT\_ACC}$	500mA ≥ $I_{LDO-LIMIT}$ > 200mA, T_J = 25°C	-10		+10	%
		500mA ≥ $I_{LDO-LIMIT}$ > 200mA, T_J = -40°C to +150°C	-15		+15	
		100mA ≤ $I_{LDO-LIMIT}$ ≤ 200mA, T_J = 25°C	-15		+15	
		100mA ≤ $I_{LDO-LIMIT}$ ≤ 200mA, T_J = -40°C to +150°C	-20		+20	
Pre-Boost Regulator						
Pre-boost regulator turn-on threshold	BST_{VTH}	Configurable range, falling edge	6.5		15	V
		Default value		11		V
Pre-boost regulator turn-on threshold hysteresis	$BST_{VTH-HYS}$			200		mV
Pre-boost regulator output voltage range	V_{OUT_BOOST}	Configurable range	6.5		15.9	V
		Default setting		12		V
Accuracy of the pre-boost regulator output voltage	$V_{OUT\_BOOST\_ACC}$	Default setting V_{OUT_BOOST} = 12V, T_J = 25°C	-2		+2	%
		Default setting V_{OUT_BOOST} = 12V, T_J = -40°C to +150°C	-3		+3	
		V_{OUT_BOOST} = 6.5V to 15.9V, T_J = 25°C	-3		+3	
		V_{OUT_BOOST} = 6.5V to 15.9V, T_J = -40°C to +150°C	-4		+4	
Internal N-channel MOSFET current limit	$I_{LS-LIMIT}$	Peak	3	4		A
FB input current	I_{FB}	V_{FB} = 0.85V, T_J = 25°C		1	50	nA

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Low-side switch on-resistance (N-channel MOSFET)	$R_{DSON-BOOST}$			180		mΩ
Low-side switch leakage current (N-channel MOSFET)	I_{N-LKG}	V_{SW} = 13.5V, V_{OUT} = 0V, T_J = 25°C		20	150	nA
		V_{SW} = 13.5V, V_{OUT} = 0V, T_J = -40°C to +150°C			1500	
Switching frequency	f_{SW}	Boost switching frequency, 400kHz/2.2MHz configurable	0.3	0.4	0.5	MHz
			1.8	2.2	2.6	
Minimum on time	t_{ON-MIN}			60		ns
Minimum off time	$t_{OFF-MIN}$			40		ns
Boost soft-start time	t_{SS}	V_{IN} = 5V, V_{OUT_BST} = 12V		1		ms

Note:

7) Not tested in production and guaranteed by design and characterization.

I²C PORT SIGNAL CHARACTERISTICS

Typical values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
I²C Interface Specifications						
Input logic low	V_{IL}		0		0.4	V
Input logic high	V_{IH}		1.3			V
Output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency	f_{SCL}				400	kHz
SCL high time	t_{HIGH}		0.6			µs
SCL low time	t_{LOW}		1.3			µs
Data set-up time	t_{SU_DAT}		100			ns
Data hold time	t_{HD_DAT}		0		0.9	µs
Set-up time for repeated start	t_{SU_STA}		0.6			µs
Hold time for start	t_{HD_STA}		0.6			µs
Bus free time between a start and a stop condition	t_{BUF}		1.3			µs
Set-up time for stop condition	t_{SU_STO}		0.6			µs
SCL and SDA rise time	t_R		20 + 0.1 x C_B		120	ns
SCL and SDA fall time	t_F		20 + 0.1 x C_B		120	ns
Pulse-width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF

S = Start Condition
Sr = Repeated Start Condition
P = Stop Condition
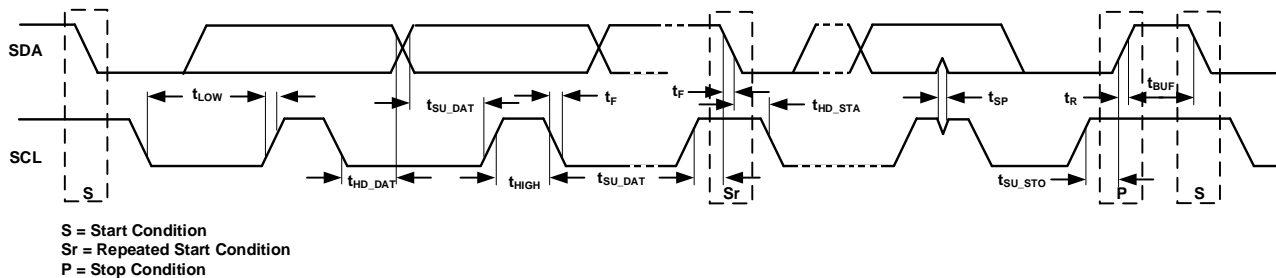
Figure 1: I²C-Compatible Interface Timing Diagram
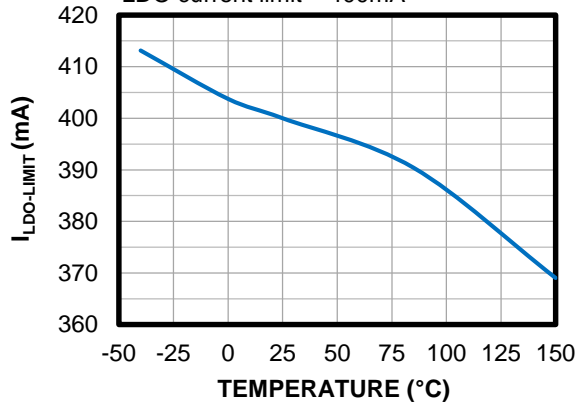
TYPICAL CHARACTERISTICS

V_{IN} = 13.5V, $V_{OUT1/2}$ = 9V, V_{EN} = 3V, T_J = -40°C to +150°C, unless otherwise noted.
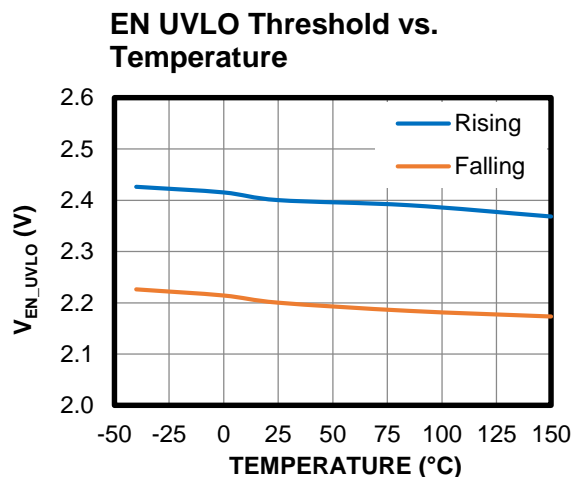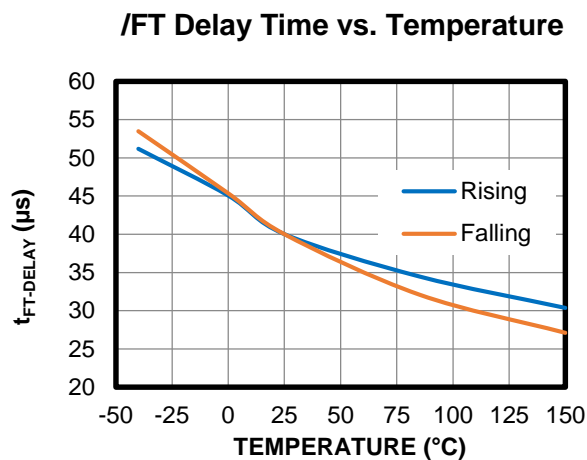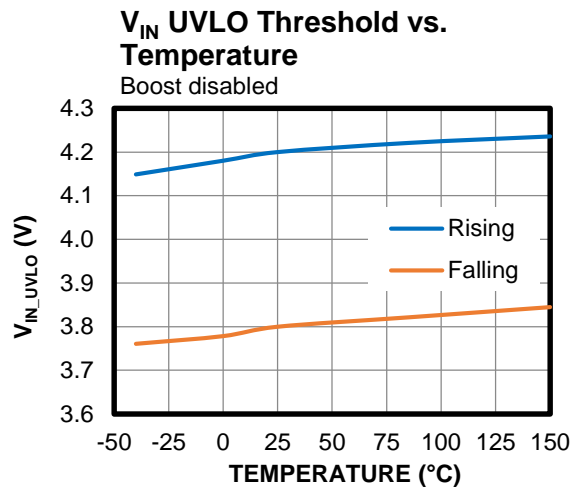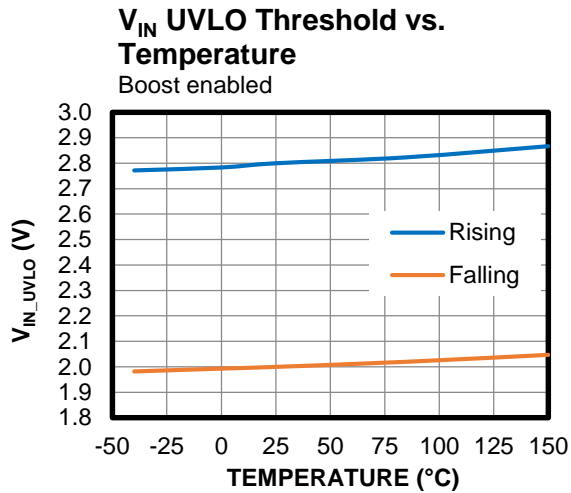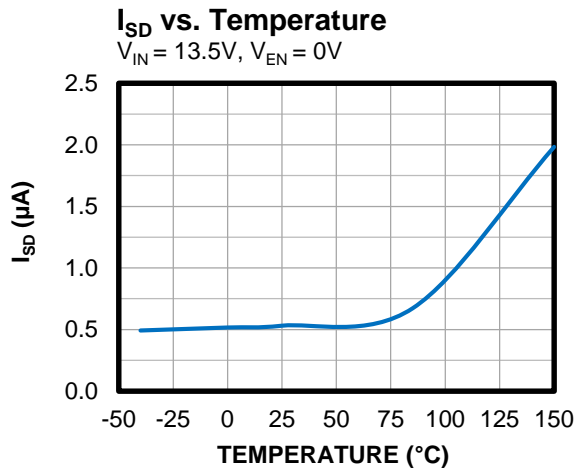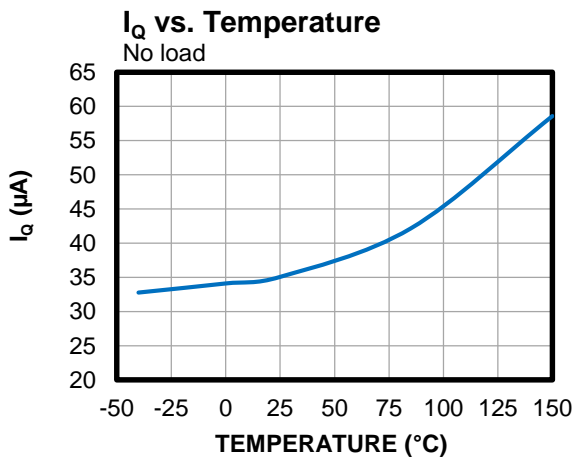
I_Q vs. Temperature
No load

I_{SD} vs. Temperature
V_{IN} = 13.5V, V_{EN} = 0V

V_{IN} UVLO Threshold vs. Temperature
Boost enabled

V_{IN} UVLO Threshold vs. Temperature
Boost disabled

/FT Delay Time vs. Temperature

EN UVLO Threshold vs. Temperature

TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, $V_{OUT1/2}$ = 9V, V_{EN} = 3V, T_J = -40°C to +150°C, unless otherwise noted.

V_{CC} vs. Temperature
V_{IN} = 13.5V
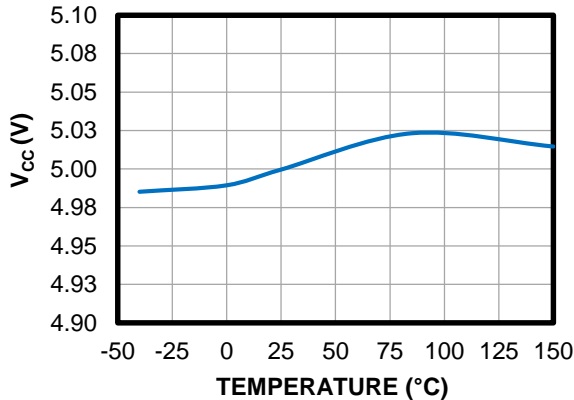
Short to Battery Threshold vs. Temperature
V_{OUT} - V_{IN}, check during turn-on sequence
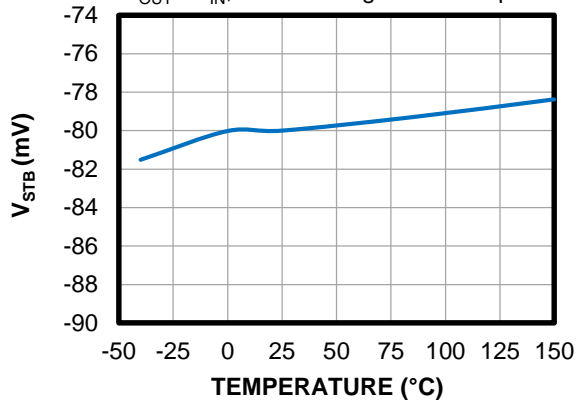
LDO 1 Dropout Voltage vs. Ambient Temperature
V_{LDO_IN} = V_{OUT1} = V_{OUT2}, I_{OUT1} = load, I_{OUT2} = no load
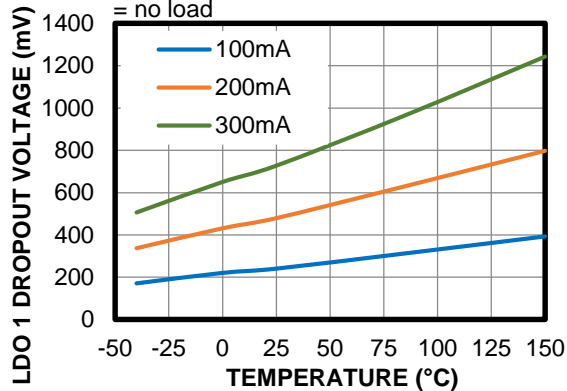
LDO 2 Dropout Voltage vs. Ambient Temperature
V_{LDO_IN} = V_{OUT1} = V_{OUT2}, I_{OUT2} = load, I_{OUT1} = no load
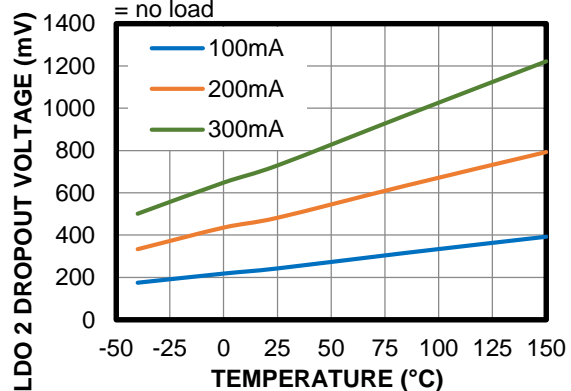
LDO Current Limit vs. Temperature
LDO current limit = 100mA
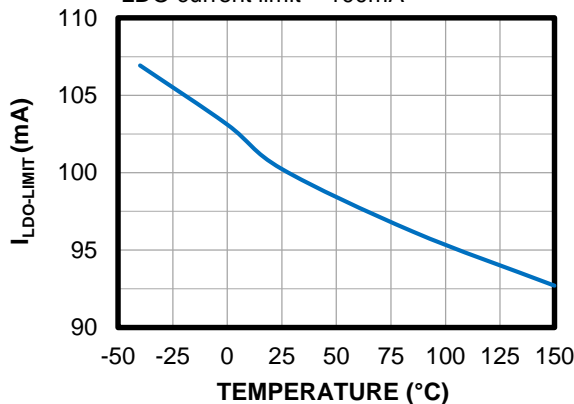
LDO Current Limit vs. Temperature
LDO current limit = 200mA
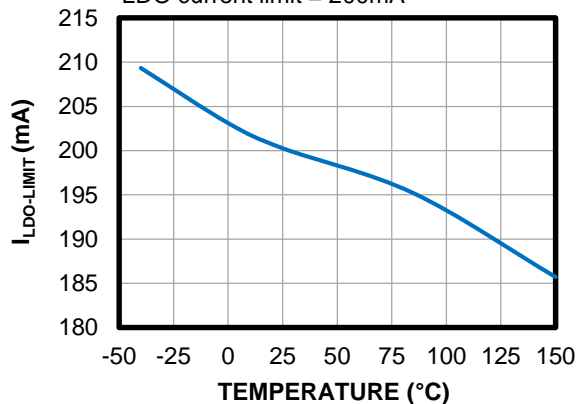
TYPICAL CHARACTERISTICS *(continued)*

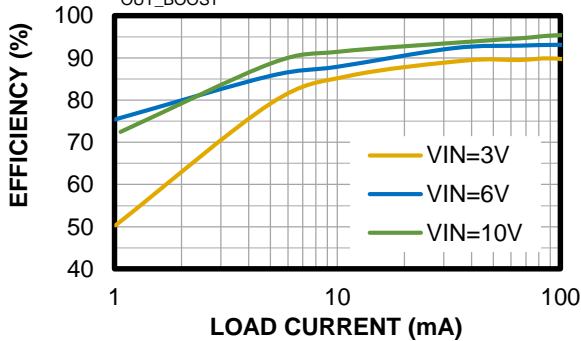V_{IN} = 13.5V, $V_{OUT1/2}$ = 9V, V_{EN} = 3V, T_J = -40°C to +150°C, unless otherwise noted.

LDO Current Limit vs. Temperature
LDO current limit = 300mA
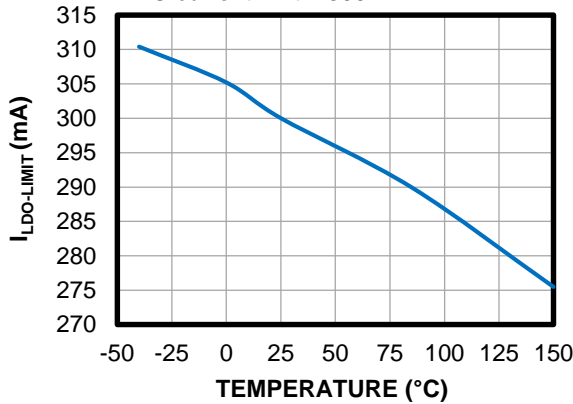
LDO Current Limit vs. Temperature
LDO current limit = 400mA

LDO Current Limit vs. Temperature
LDO current limit = 500mA
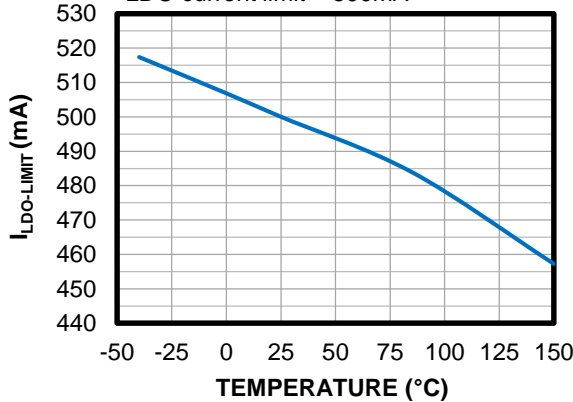
Boost Turn-On Threshold Hystersis vs. Temperature
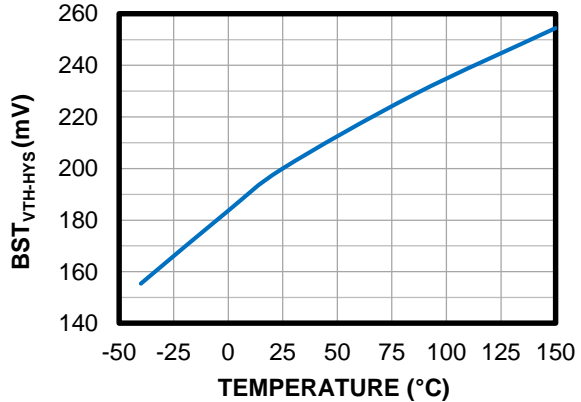
Low-Side Switch Current Limit vs. Temperature
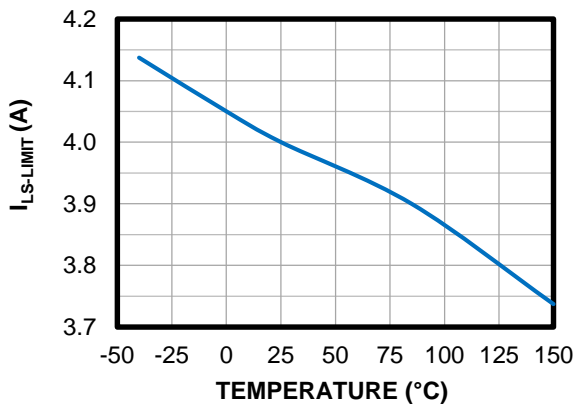
Low-Side Switch On Resistance vs. Temperature
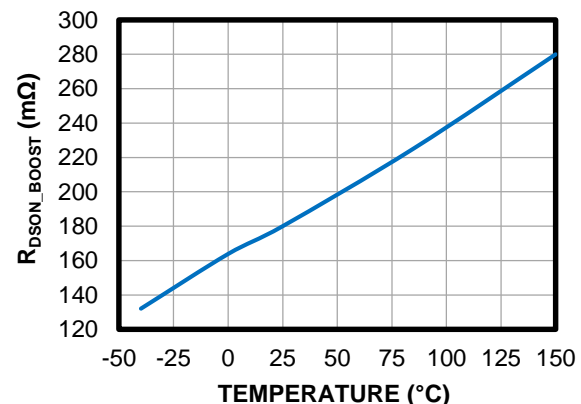
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, $V_{OUT1/2}$ = 9V, V_{EN} = 3V, T_J = -40°C to +150°C, unless otherwise noted.

Switching Frequency vs. Temperature
f_{SW} = 400kHz
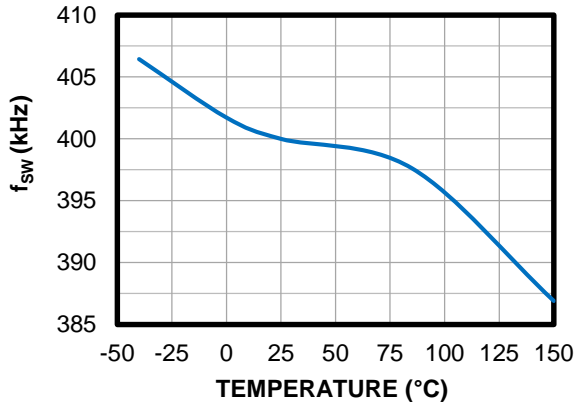
Switching Frequency vs. Temperature
f_{SW} = 2.2MHz
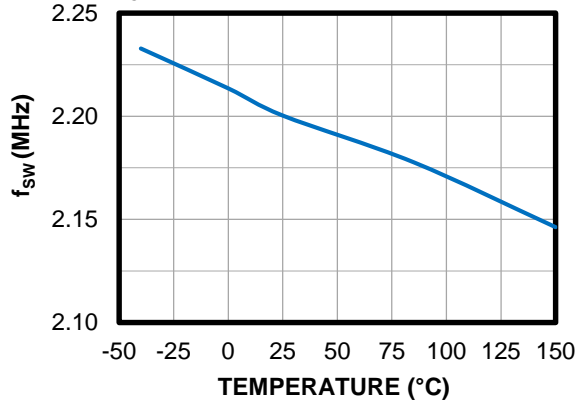
Minimum On Time vs. Temperature
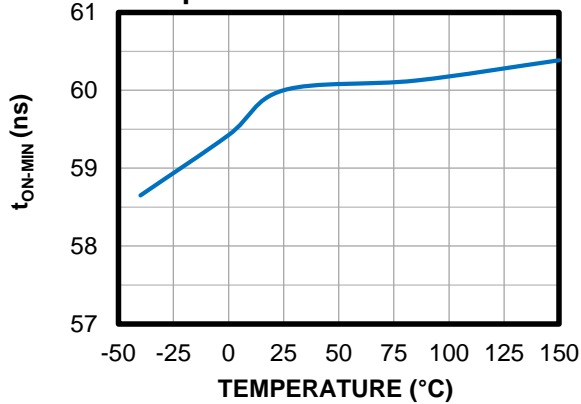
Minimum Off Time vs. Temperature
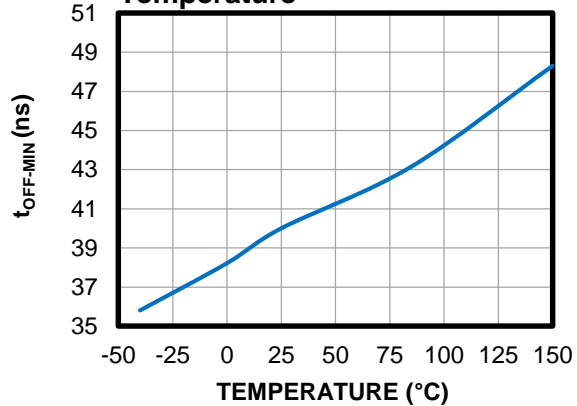
Boost Soft-Start Time vs. Temperature
V_{IN} = 5V, V_{OUT_BOOST} = 12V
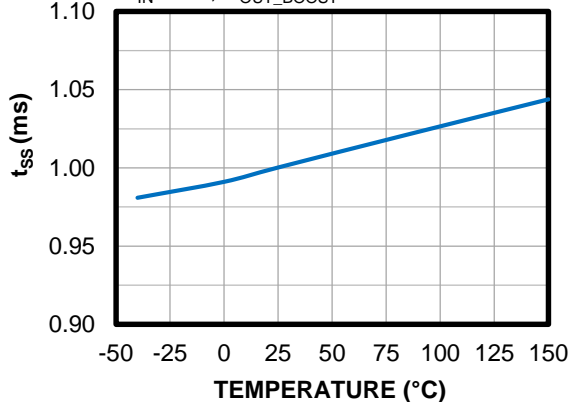
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 6V$, $V_{OUT1/2} = 9V$, $V_{OUT\_BOOST} = 12V$, $L = 10\mu H$, $C_{OUT1} = C_{OUT2} = 10\mu F$, $C_{OUT\_BOOST} = 40\mu F$, $T_A = 25°C$, unless otherwise noted.
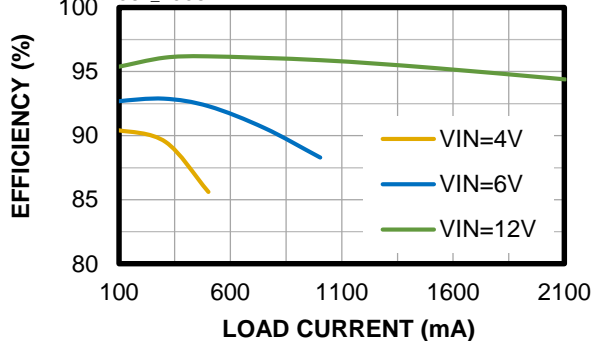
Boost Efficiency vs. Load Current
Dual LDO disabled, $V_{OUT\_BOOST} = 12V$, $f_{SW} = 400kHz$, $L = 10\mu H$ (DCR = 45mΩ), rectifier diode B350A-13-F, FSS on, $I_{OUT\_BOOST} = 1mA$ to 100mA
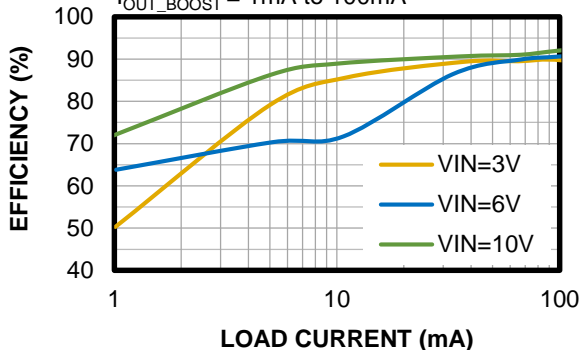

Boost Efficiency vs. Load Current
Dual LDO disabled, $V_{OUT\_BOOST} = 12V$, $f_{SW} = 400kHz$, $L = 10\mu H$ (DCR = 45mΩ), rectifier diode B350A-13-F, FSS on, $I_{OUT\_BOOST} = 100mA$ to 2.1A

Boost Efficiency vs. Load Current
Dual LDO disabled, $V_{OUT\_BOOST} = 14V$, $f_{SW} = 400kHz$, $L = 10\mu H$ (DCR = 45mΩ), rectifier diode B350A-13-F, FSS on, $I_{OUT\_BOOST} = 1mA$ to 100mA

Boost Efficiency vs. Load Current
Dual LDO disabled, $V_{OUT\_BOOST} = 14V$, $f_{SW} = 400kHz$, $L = 10\mu H$ (DCR = 45mΩ), rectifier diode B350A-13-F, FSS on, $I_{OUT\_BOOST} = 100mA$ to 2.1A
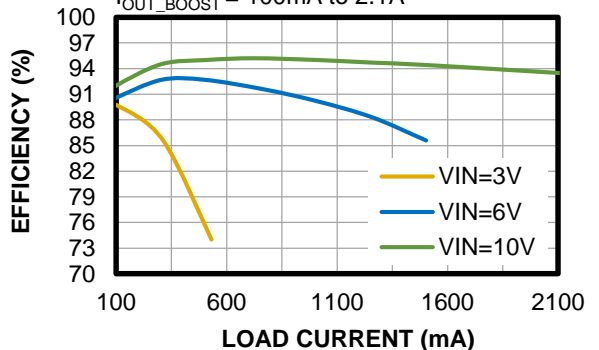

Boost Efficiency vs. Load Current
Dual LDO disabled, $V_{OUT\_BOOST} = 12V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$ (DCR = 35.2mΩ), rectifier diode B350A-13-F, FSS on, $I_{OUT\_BOOST} = 1mA$ to 100mA

Boost Efficiency vs. Load Current
Dual LDO disabled, $V_{OUT\_BOOST} = 12V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$ (DCR = 35.2mΩ), rectifier diode B350A-13-F, FSS on, $I_{OUT\_BOOST} = 100mA$ to 2.1A
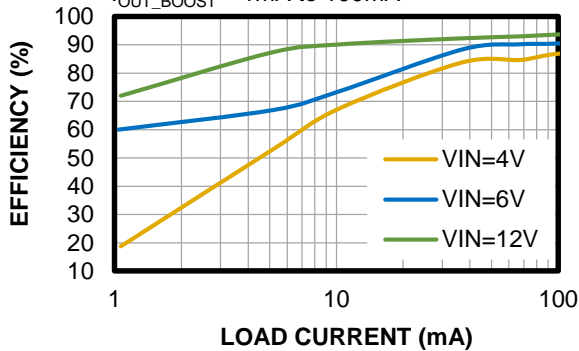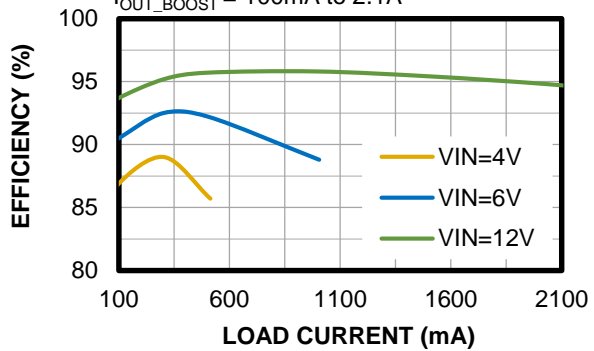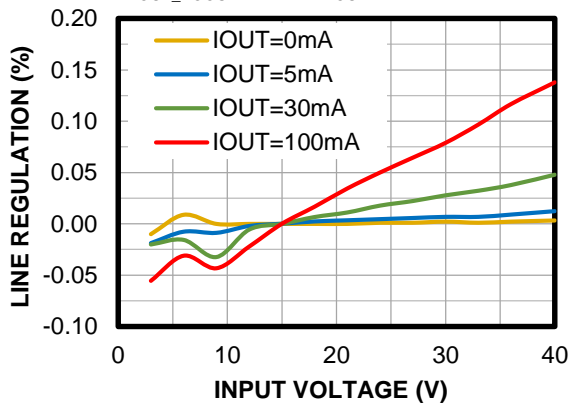
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, $V_{OUT1/2}$ = 9V, V_{OUT_BOOST} = 12V, L = 10µH, C_{OUT1} = C_{OUT2} = 10µF, C_{OUT_BOOST} = 40µF, T_A = 25°C, unless otherwise noted.

Boost Efficiency vs. Load Current

Dual LDO disabled, V_{OUT_BOOST} = 14V, f_{SW} = 2.2MHz, L = 2.2µH (DCR = 35.2mΩ), rectifier diode B350A-13-F, FSS on, I_{OUT_BOOST} = 1mA to 100mA
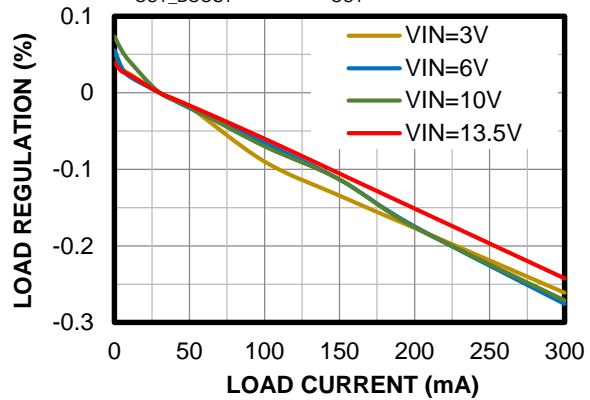

Boost Efficiency vs. Load Current

Dual LDO disabled, V_{OUT_BOOST} = 14V, f_{SW} = 2.2MHz, L = 2.2µH (DCR = 35.2mΩ), rectifier diode B350A-13-F, FSS on, I_{OUT_BOOST} = 100mA to 2.1A
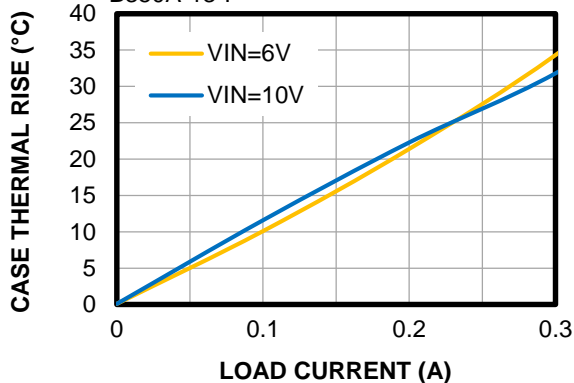

Line Regulation vs. Input Voltage

V_{OUT_BOOST} = 12V, V_{OUT} = 9V
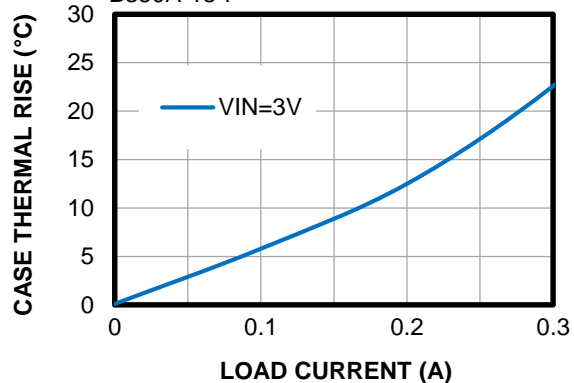

Load Regulation vs. Load Current

V_{OUT_BOOST} = 12V, V_{OUT} = 9V

Case Thermal Rise vs. Load Current

V_{OUT1} = V_{OUT2} = 9V, I_{OUT1} = I_{OUT2} = load, V_{OUT_BOOST} = 12V, f_{SW} = 400kHz, L = 10µH, B350A-13-F

Case Thermal Rise vs. Load Current

V_{OUT1} = V_{OUT2} = 5V, I_{OUT1} = I_{OUT2} = load, V_{OUT_BOOST} = 6.5V, f_{SW} = 400kHz, L = 10µH, B350A-13-F
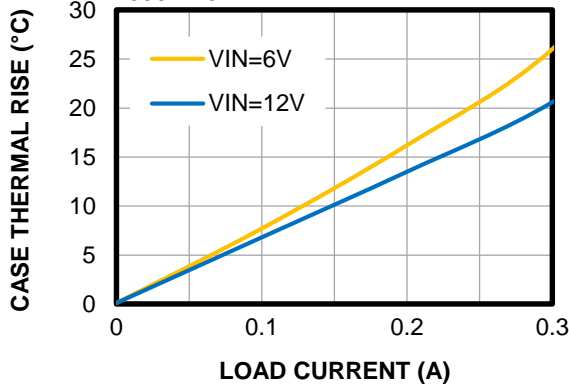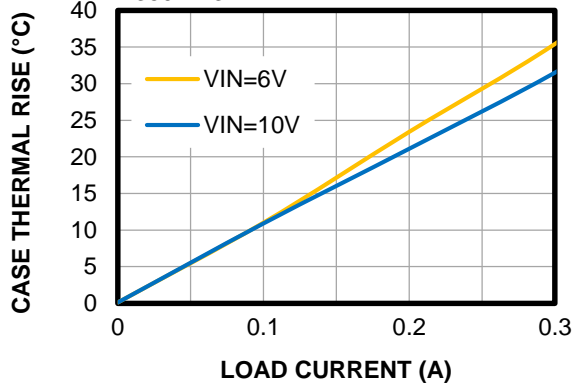
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, $V_{OUT1/2}$ = 9V, V_{OUT_BOOST} = 12V, L = 10µH, C_{OUT1} = C_{OUT2} = 10µF, C_{OUT_BOOST} = 40µF, T_A = 25°C, unless otherwise noted.
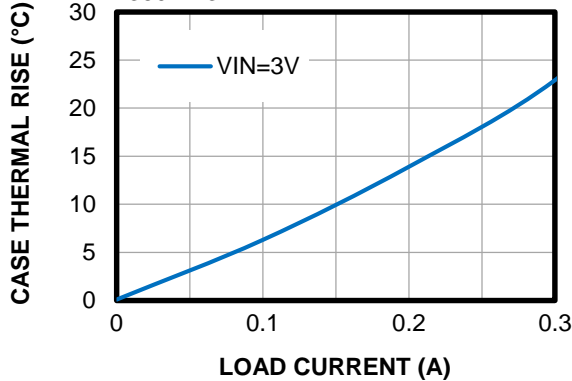
Case Thermal Rise vs. Load Current

V_{OUT1} = V_{OUT2} = 12V, I_{OUT1} = I_{OUT2} = load,
V_{OUT_BOOST} = 14V, f_{SW} = 400kHz, L = 10µH,
B350A-13-F

Case Thermal Rise vs. Load Current

V_{OUT1} = V_{OUT2} = 9V, I_{OUT1} = I_{OUT2} = load,
V_{OUT_BOOST} = 12V, f_{SW} = 2.2MHz, L = 2.2µH,
B350A-13-F

Case Thermal Rise vs. Load Current

V_{OUT1} = V_{OUT2} = 5V, I_{OUT1} = I_{OUT2} = load,
V_{OUT_BOOST} = 6.5V, f_{SW} = 2.2MHz, L =2.2µH,
B350A-13-F

Case Thermal Rise vs. Load Current

V_{OUT1} = V_{OUT2} = 12V, I_{OUT1} = I_{OUT2} = load,
V_{OUT_BOOST} = 14V, f_{SW} = 2.2MHz, L = 2.2µH,
B350A-13-F
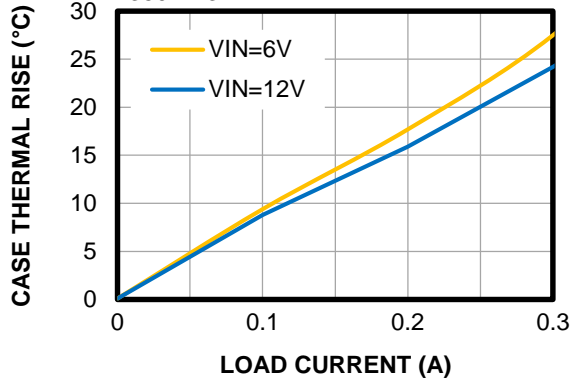
PSRR vs. Frequency

V_{IN} = 13.5V, V_{OUT} = 9V, I_{OUT} = 5mA,
C_{IN} = 100pF, C_{OUT} = 22µF

LDO 1 Dropout Voltage vs. Load Current

V_{LDO_IN} = V_{OUT1} = V_{OUT2}, I_{OUT1} = load, I_{OUT2} = no load

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, $V_{OUT1/2}$ = 9V, V_{OUT_BOOST} = 12V, L = 10µH, C_{OUT1} = C_{OUT2} = 10µF, C_{OUT_BOOST} = 40µF, T_A = 25°C, unless otherwise noted.

LDO 2 Dropout Voltage vs. Load Current

V_{LDO_IN} = V_{OUT1} = V_{OUT2}, I_{OUT2} = load, I_{OUT1} = no load

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, $V_{OUT1/2}$ = 9V, V_{OUT_BOOST} = 12V, L = 10µH, C_{OUT1} = C_{OUT2} = 10µF, C_{OUT_BOOST} = 40µF, T_A = 25°C, rectifier diode: B350A-13-F, unless otherwise noted.

Steady State

V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V, V_{OUT_BOOST} = 12V, I_{OUT1} = I_{OUT2} = 0A

Steady State

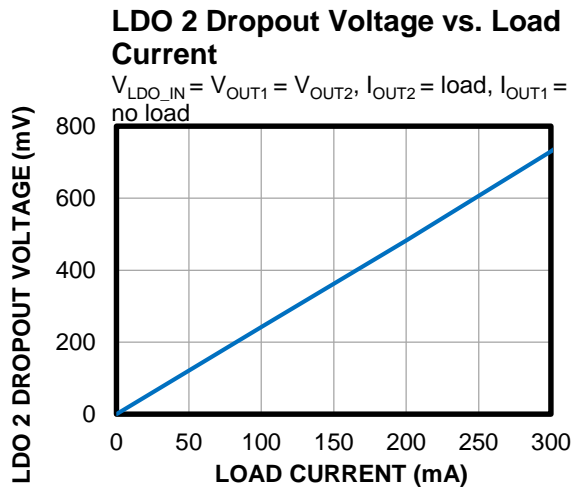V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V, V_{OUT_BOOST} = 12V, I_{OUT1} = I_{OUT2} = 0.3A

Start-Up through VIN

V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V, V_{OUT_BOOST} = 12V, I_{OUT1} = I_{OUT2} = 0A

Start-Up through VIN

V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V, V_{OUT_BOOST} = 12V, I_{OUT1} = I_{OUT2} = 0.3A

Shutdown through VIN

V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V, V_{OUT_BOOST} = 12V, I_{OUT1} = I_{OUT2} = 0A

Shutdown through VIN

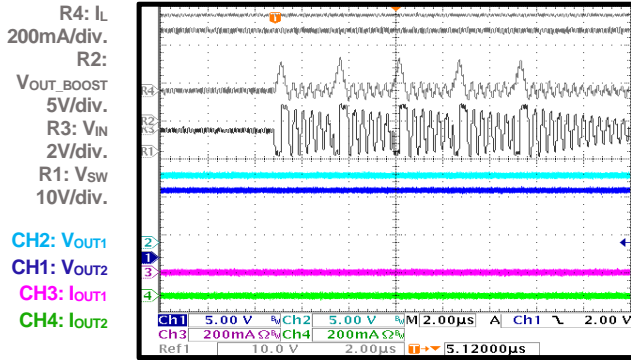V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V, V_{OUT_BOOST} = 12V, I_{OUT1} = I_{OUT2} = 0.3A

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, $V_{OUT1/2}$ = 9V, V_{OUT_BOOST} = 12V, L = 10µH, C_{OUT1} = C_{OUT2} = 10µF, C_{OUT_BOOST} = 40µF, T_A = 25°C, rectifier diode: B350A-13-F, unless otherwise noted.

Start-Up through EN
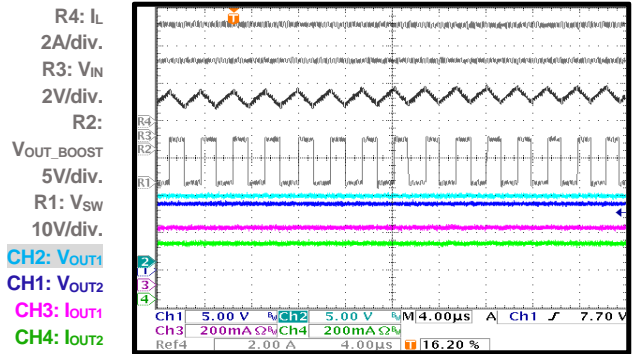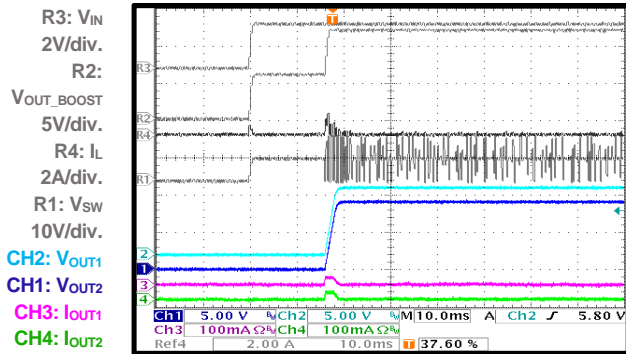V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V,
V_{OUT_BOOST} = 12V, I_{OUT1} = I_{OUT2} = 0A

Start-Up through EN
V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V,
V_{OUT_BOOST} = 12V, I_{OUT1} = I_{OUT2} = 0.3A

Shutdown through EN
V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V,
V_{OUT_BOOST} = 12V, I_{OUT1} = I_{OUT2} = 0A

Shutdown through EN
V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V,
V_{OUT_BOOST} = 12V, I_{OUT1} = I_{OUT2} = 0.3A

SCP Steady State
V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V,
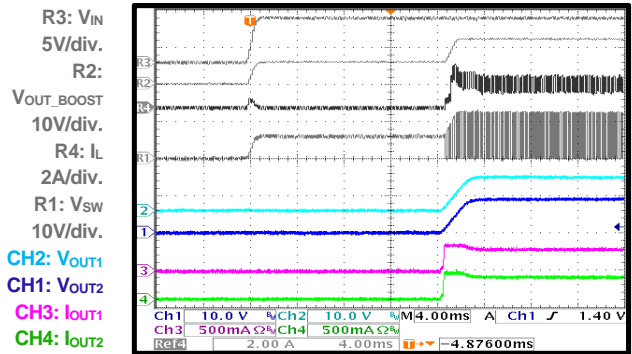V_{OUT_BOOST} = 12V, I_{OUT1} = I_{OUT2} = 0A, V_{OUT2}
short to circuit
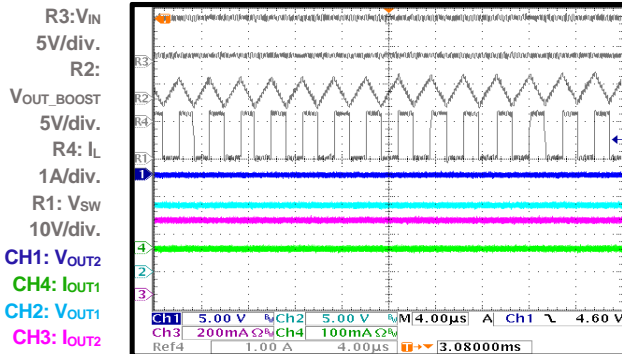
SCP Steady State
V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V,
V_{OUT_BOOST} = 12V, I_{OUT1} = I_{OUT2} = 0A, V_{OUT1} and
V_{OUT2} short to circuit
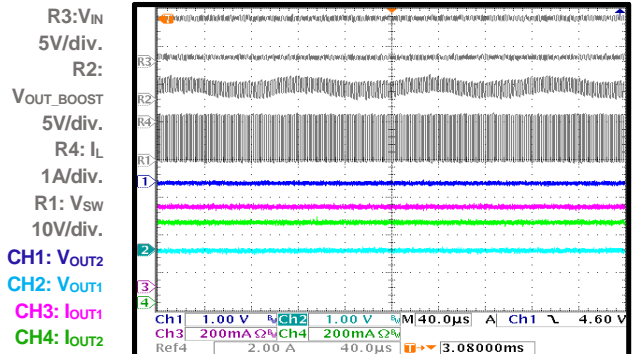
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, $V_{OUT1/2}$ = 9V, V_{OUT_BOOST} = 12V, L = 10µH, C_{OUT1} = C_{OUT2} = 10µF, C_{OUT_BOOST} = 40µF, T_A = 25°C, rectifier diode: B350A-13-F, unless otherwise noted.

SCP Recovery

V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V,
V_{OUT_BOOST} = 12V, I_{OUT1} = I_{OUT2} = 0A,
V_{OUT1} short circuit to I_{OUT1} = 0A

SCP Recovery

V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V,
V_{OUT_BOOST} = 12V, I_{OUT2} = 0.3A, V_{OUT1} short
circuit to I_{OUT1} = 0.3A
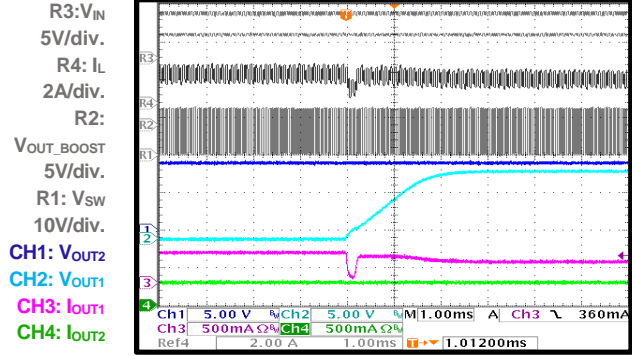
SCP Recovery

V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V,
V_{OUT_BOOST} = 12V, V_{OUT1} and V_{OUT2} short circuit
to I_{OUT1} = I_{OUT2} = 0A
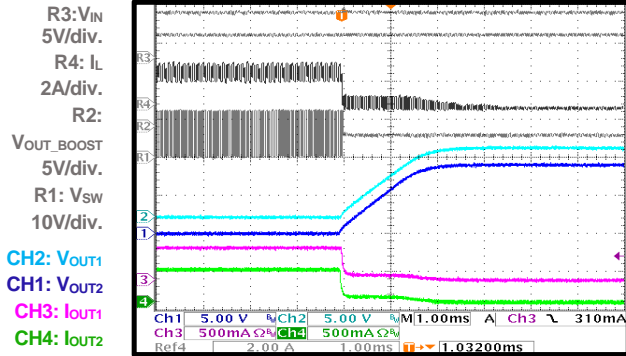
SCP Recovery

V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V,
V_{OUT_BOOST} = 12V, V_{OUT1} and V_{OUT2} short circuit
to I_{OUT1} = I_{OUT2} = 0.3A
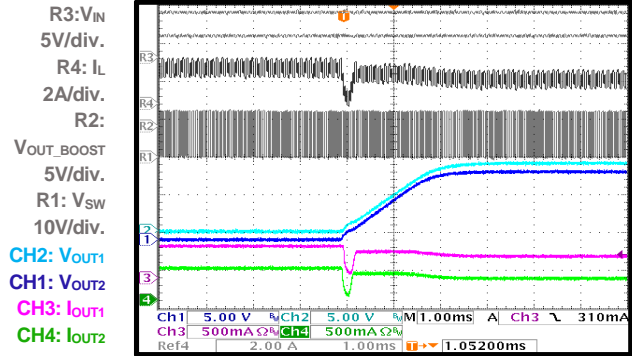
SCP Entry

V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V,
V_{OUT_BOOST} = 12V, I_{OUT2} = 0A, I_{OUT1} = 0A to
short circuit
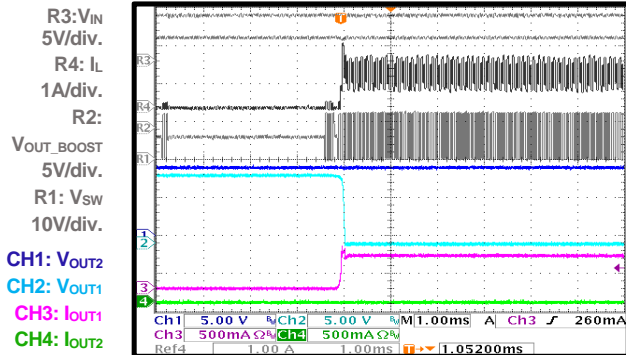
SCP Entry

V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V,
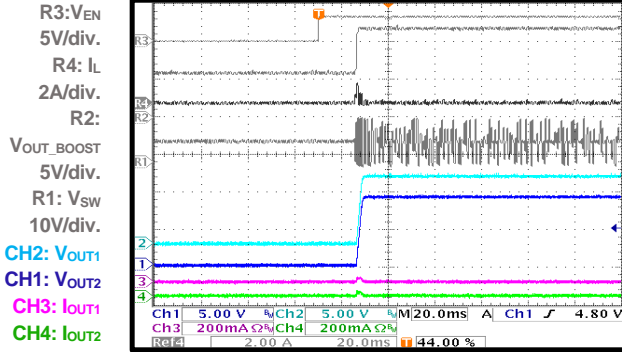V_{OUT_BOOST} = 12V, I_{OUT2} = 0.3A, I_{OUT1}=0.3A to
short circuit
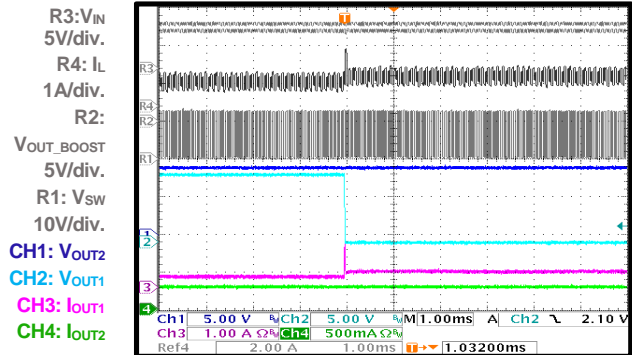
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, $V_{OUT1/2}$ = 9V, V_{OUT_BOOST} = 12V, L = 10µH, C_{OUT1} = C_{OUT2} = 10µF, C_{OUT_BOOST} = 40µF, T_A = 25°C, rectifier diode: B350A-13-F, unless otherwise noted.

SCP Entry
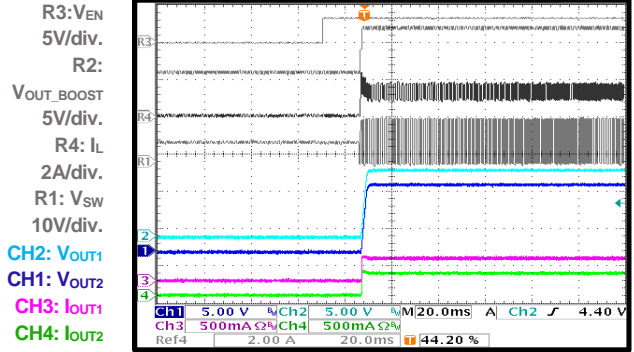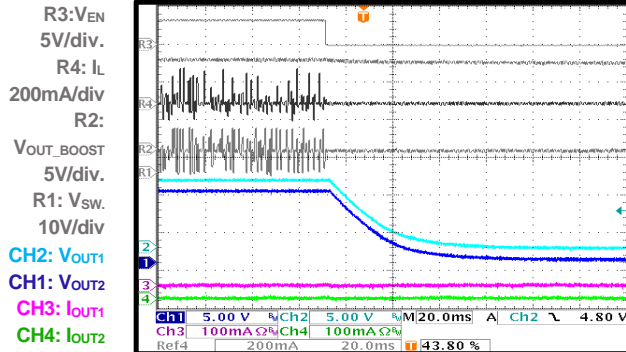V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V, V_{OUT_BOOST} = 12V, I_{OUT1} = I_{OUT2} = 0A to short circuit
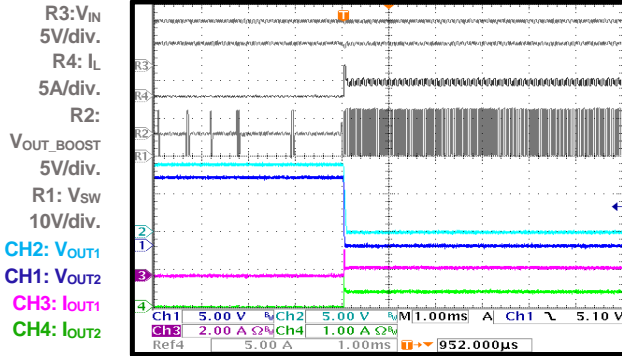
SCP Entry
V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 9V, V_{OUT_BOOST} = 12V, I_{OUT1} = I_{OUT2} = 0.3A to short circuit
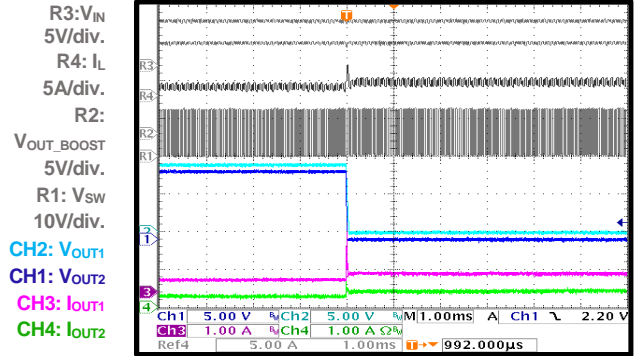
Load Dump
V_{OUT1} = V_{OUT2} = 9V, V_{OUT_BOOST} = 12V, I_{OUT1} = I_{OUT2} = 0A
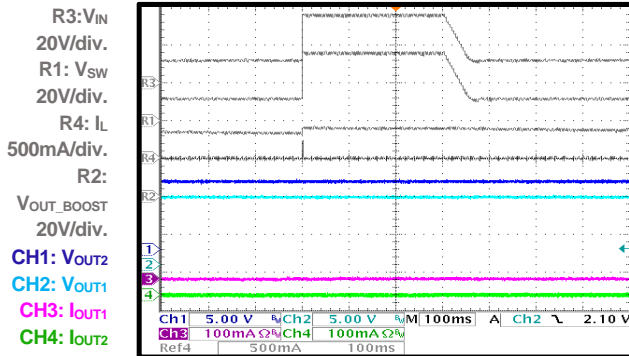
Load Dump
V_{OUT1} = V_{OUT2} = 9V, V_{OUT_BOOST} = 12V, I_{OUT1} = I_{OUT2} = 0.3A
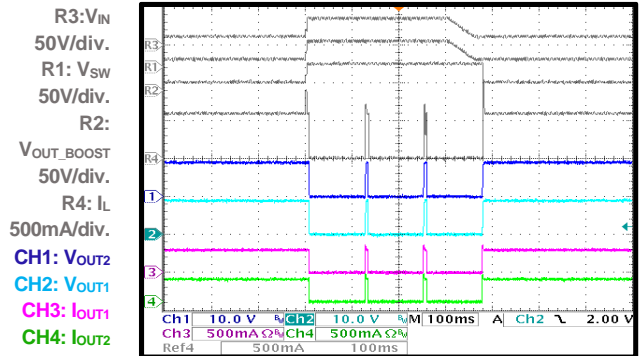
VIN Ramp Down and Up
V_{OUT1} = V_{OUT2} = 9V, V_{OUT_BOOST} = 12V, I_{OUT1} = I_{OUT2} = 0A
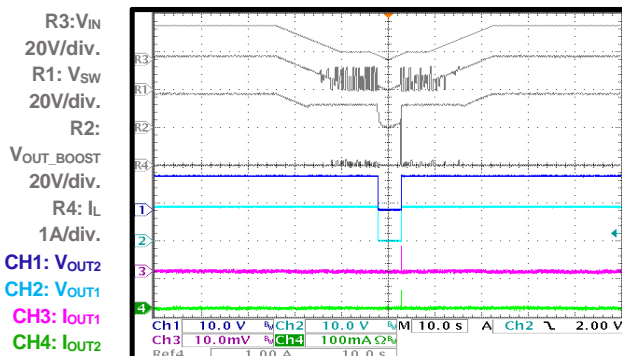
VIN Ramp Down and Up
V_{OUT1} = V_{OUT2} = 9V, V_{OUT_BOOST} = 12V, I_{OUT1} = I_{OUT2} = 0.3A
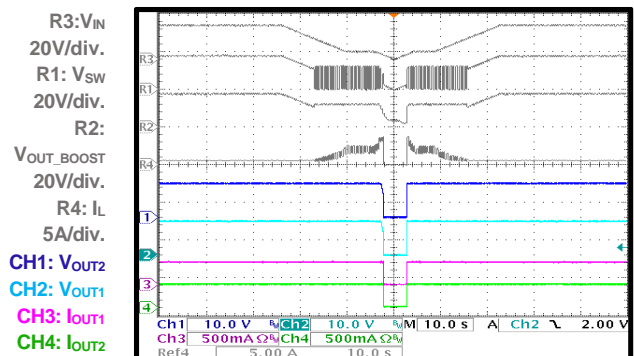
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, $V_{OUT1/2}$ = 9V, V_{OUT_BOOST} = 12V, L = 10µH, C_{OUT1} = C_{OUT2} = 10µF, C_{OUT_BOOST} = 40µF, T_A = 25°C, rectifier diode: B350A-13-F, unless otherwise noted.

Reset Behavior
V_{OUT1} = V_{OUT2} = 9V, V_{OUT_BOOST} = 12V,
I_{OUT1} = I_{OUT2} = 0A
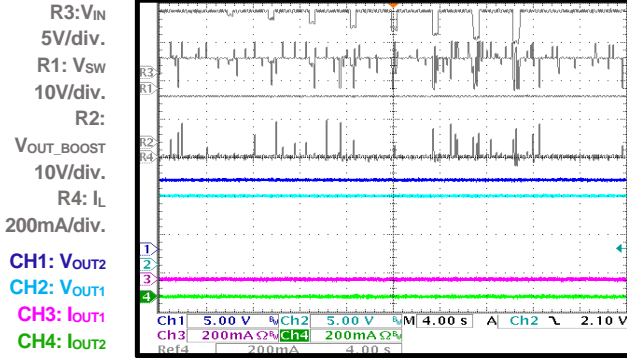
Reset Behavior
V_{OUT1} = V_{OUT2} = 9V, V_{OUT_BOOST} = 12V,
I_{OUT1} = I_{OUT2} = 0.3A
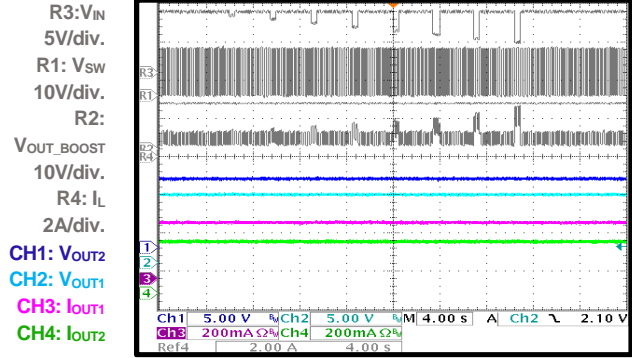
Cold Crank
V_{OUT1} = V_{OUT2} = 9V, V_{OUT_BOOST} = 12V,
I_{OUT1} = I_{OUT2} = 0A

Cold Crank
V_{OUT1} = V_{OUT2} = 9V, V_{OUT_BOOST} = 12V,
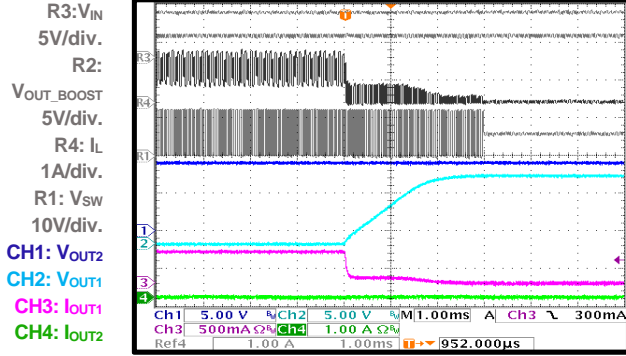I_{OUT1} = I_{OUT2} = 0.3A

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, $V_{OUT1/2}$ = 9V, V_{OUT_BOOST} = 12V, L = 10µH, C_{OUT1} = C_{OUT2} = 10µF, C_{OUT_BOOST} = 40µF, T_A = 25°C, rectifier diode: DFLS240-7, unless otherwise noted. [8]

CISPR25 Class 5 Peak Conducted Emissions
150kHz t o108MHz

CISPR25 Class 5 Average Conducted Emissions
150kHz to 108MHz

CISPR25 Class 5 Peak Radiated Emissions
150kHz to 30MHz

CISPR25 Class 5 Average Radiated Emissions
150kHz to 30MHz

CISPR25 Class 5 Peak Radiated Emissions
Horizontal, 30MHz to 200MHz

CISPR25 Class 5 Average Radiated Emissions
Horizontal, 30MHz to 200MHz

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, $V_{OUT1/2}$ = 9V, V_{OUT_BOOST} = 12V, L = 10µH, C_{OUT1} = C_{OUT2} = 10µF, C_{OUT_BOOST} = 40µF, T_A = 25°C, rectifier diode: DFLS240-7, unless otherwise noted. [8]

CISPR25 Class 5 Peak Radiated Emissions
Vertical, 30MHz to 200MHz

CISPR25 Class 5 Average Radiated Emissions
Vertical, 30MHz to 200MHz

CISPR25 Class 5 Peak Radiated Emissions
Horizontal, 200MHz to 1GHz

CISPR25 Class 5 Average Radiated Emissions
Horizontal, 200MHz to 1GHz

CISPR25 Class 5 Peak Radiated Emissions
Vertical, 200MHz to 1GHz

CISPR25 Class 5 Average Radiated Emissions
Vertical, 200MHz to 1GHz

Note:

8) All EMC test results are based on the application circuit with EMI filters (see Figure 18 on page 51).

FUNCTIONAL BLOCK DIAGRAM
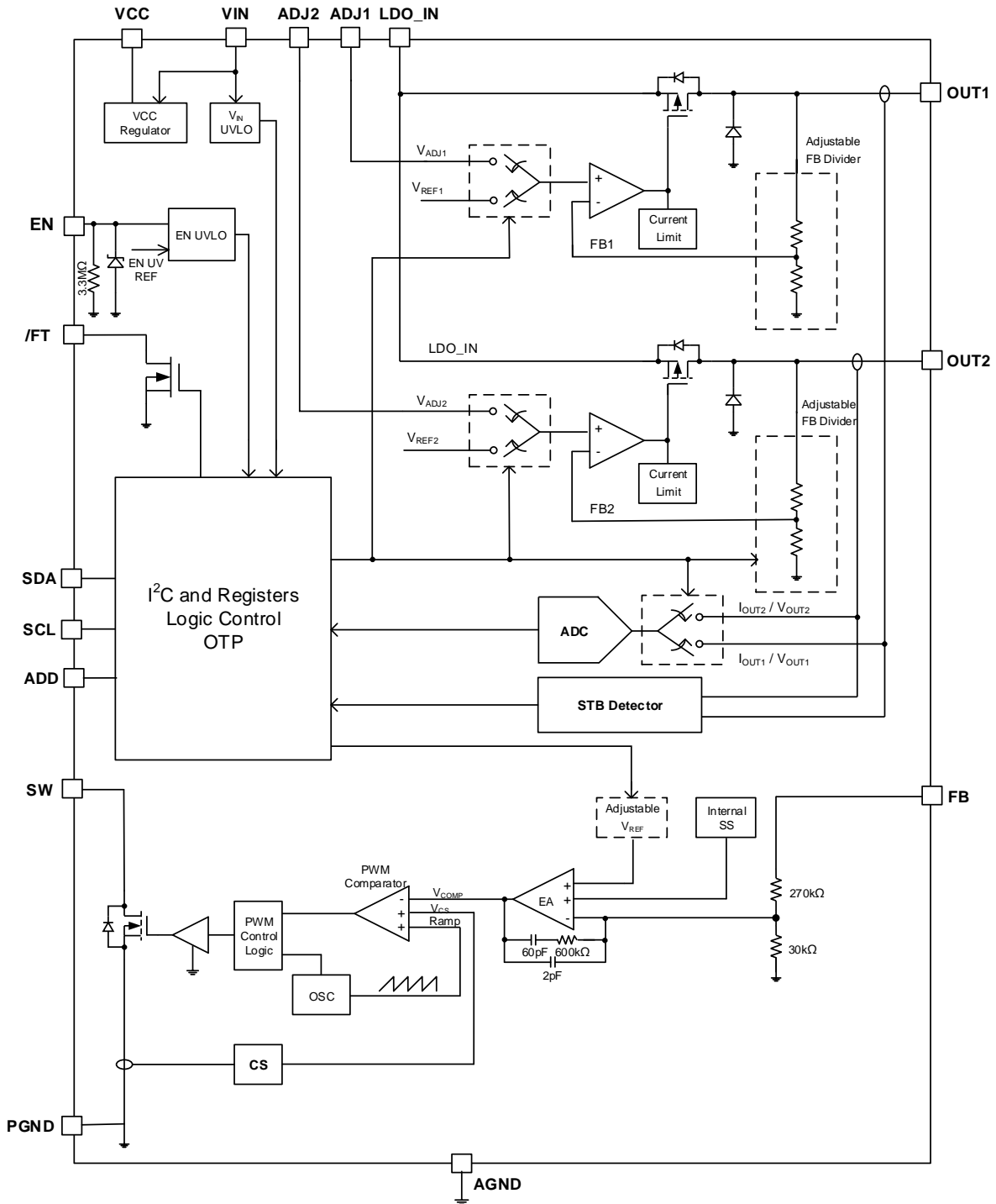
Figure 2: Functional Block Diagram

TIMING SEQUENCES
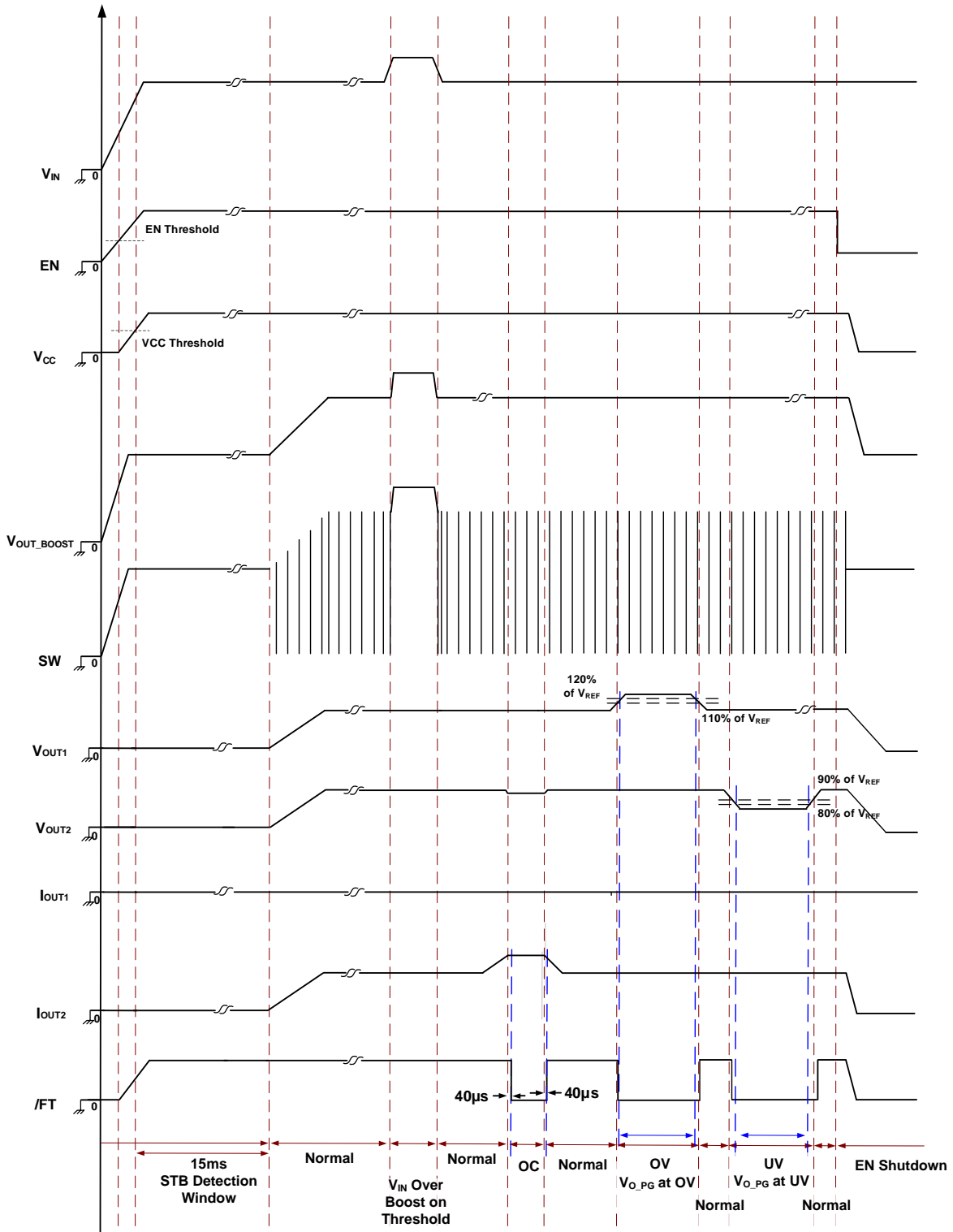
Figure 3: Timing Sequence

TIMING SEQUENCES *(continued)*
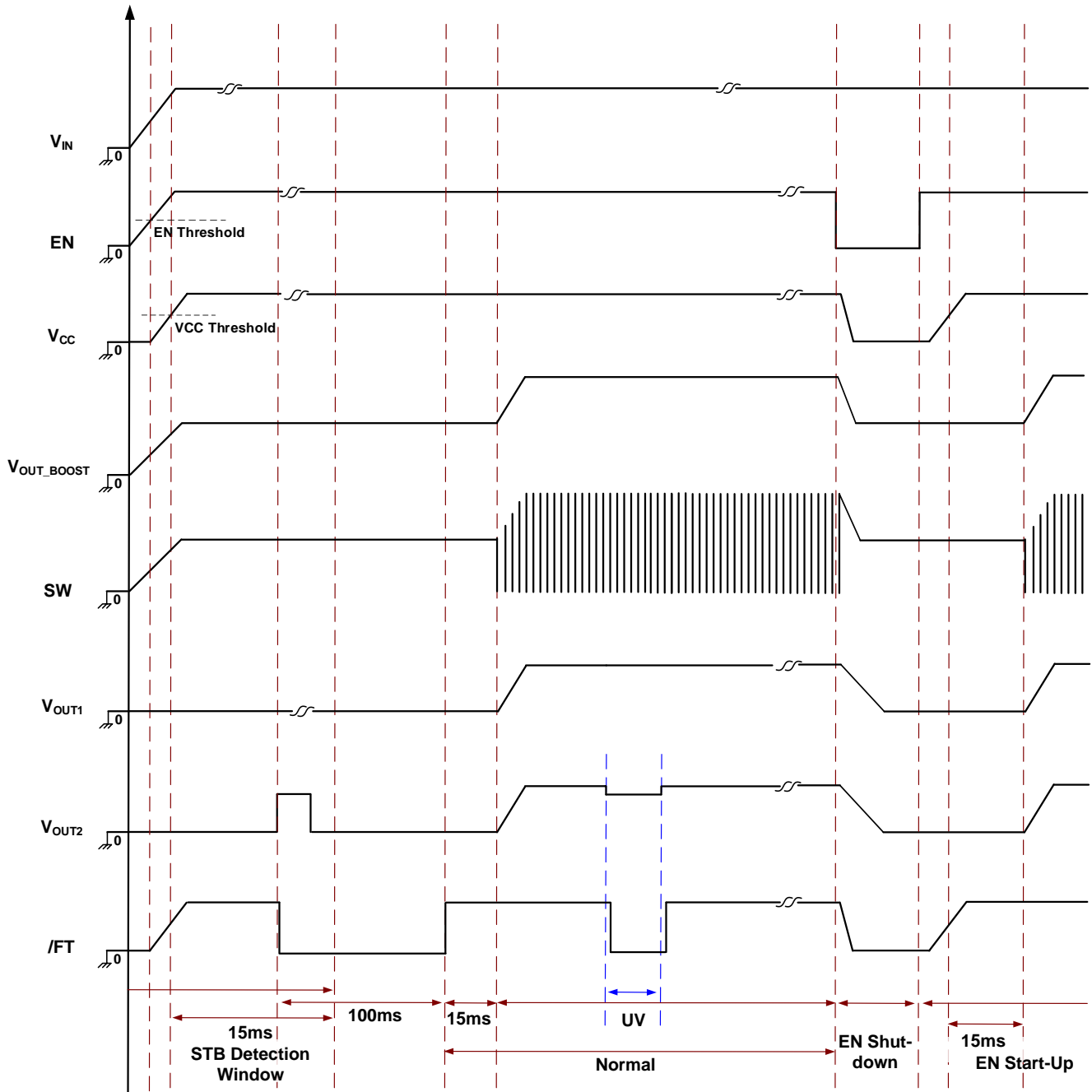
Figure 4: STB Occurs within STB Detection Window and out of STB Detection Window

TIMING SEQUENCES *(continued)*
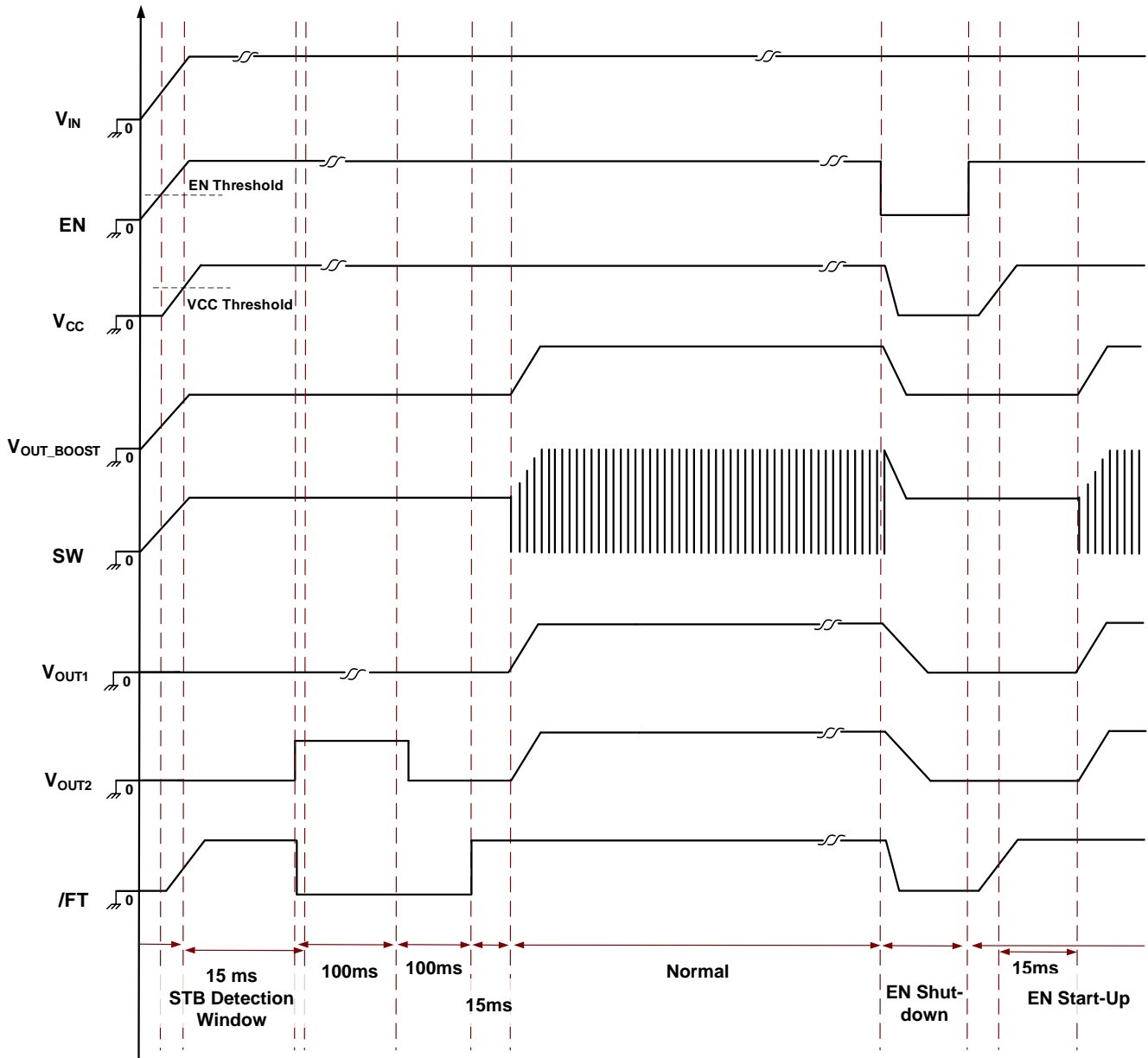
Figure 5: STB Occurs with Retry Protection

TIMING SEQUENCES *(continued)*
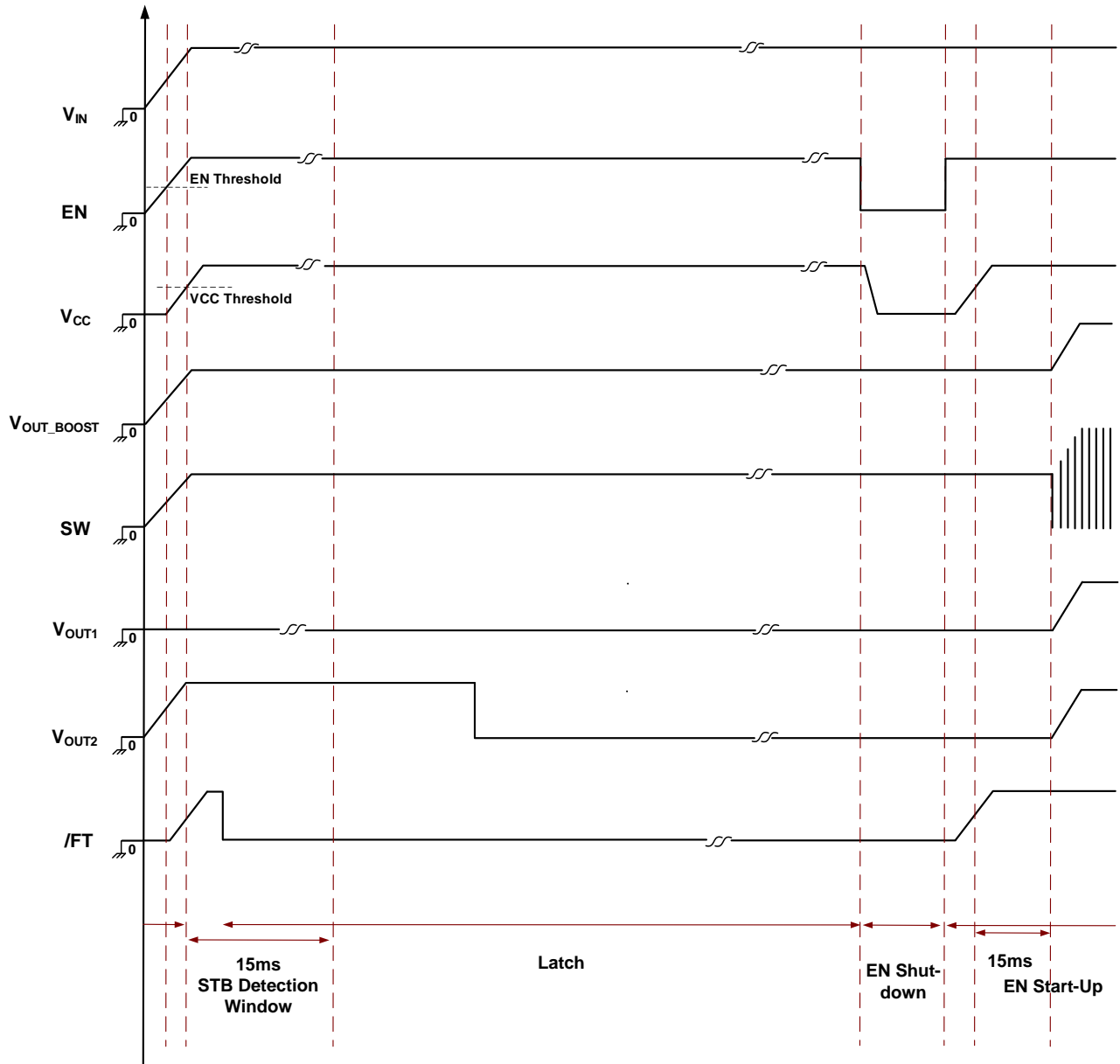
Figure 6: STB Occurs with Latch-Off Protection

OPERATION

The MPQ2026A is a dual phantom antenna linear regulator with a pre-boost regulator and I²C interface. It supplies power to systems with high-voltage batteries. The device features a wide 3V to 40V input voltage (V_{IN}) range, low dropout voltage, and a low quiescent supply current.

The power stage in the MPQ2026A is implemented as a cascade, starting with a step-up pre-boost regulator, and then followed by dual LDOs. The step-up regulator (a DC/DC boost converter) provides the LDO input voltage level, which enables the LDOs to regulate the outputs during cold-crank conditions.

The two adjustable-output LDOs are supplied from LDO_IN. The LDOs have outputs that can be adjusted via the I²C interface, from 1V to 13.6V with 200mV/step, or from 1V to 7.3V with 100mV/step.

The linear regulator output current is limited internally, and the LDO output is protected against short-circuit, overload, short-to-battery, and over-temperature conditions.

The dual LDO peak output current limitation range can be configured to be between 100mA and 500mA via the I²C interface.

If the junction temperature is too high, the thermal sensor sends a signal to the control logic that shuts down the device. The IC restarts when the temperature has sufficiently cooled.

The maximum power output current is a function of the package's maximum power dissipation for a given temperature. The maximum power dissipation is dependent on the thermal resistance of the case and the circuit board, the temperature difference between the die junction and the ambient air, and the rate of airflow. GND and the exposed pad must be connected to the ground plane for proper dissipation.

Pre-Boost Regulator

The boost converter is intended to function as a pre-boost regulator, and it provides a step-up converter function. After the reverse protection circuit, the converter transfers energy from the battery to a higher output voltage (LDO_IN) with high efficiency. The regulator integrates the power switching and the sense resistor for over-current detection.

The pre-boost regulator parameters can be set via the I²C interface. The threshold at which it activates can be selected via the dedicated register. The corresponding pre-boost regulator output voltage (V_{OUT_BOOST}) is also set via a register. If the pre-boost regulator is enabled, its switches automatically start to switch when V_{IN} falls below the selected threshold voltage. Then the switches stop switching when they cross this threshold (including a hysteresis) again. A bit in the I²C register indicates whether the pre-boost regulator has been activated. The boost over-current (OC), under-voltage (UV), and over-voltage (OV) detection stop working when VIN exceeds its boost active threshold.

Note that the normal run time power for the LDOs is provided directly from the battery input connected to VIN, and not from the pre-boost regulator. The regulator is only activated in case of cranking, or other scenarios in which the battery input dips to a voltage below the boost active voltage threshold.

The boost regulator works in pulse-width modulation (PWM) mode and peak current control mode, with a fixed frequency of 400kHz or 2.2MHz. This frequency can be selected via the I²C interface.

The pre-boost regulator's power switching has a minimum turn on time of 60ns, which means that the power switching remains in the on state for at least 60ns once it turns on. To prevent V_{OUT_BOOST} from overshooting at the 2.2MHz frequency, a frequency fold back block is activated to reduce the frequency when V_{IN} is close to V_{OUT_BOOST}. The frequency folds back to 1MHz when $5/6 < V_{IN} / V_{OUT\_BOOST} < 10/11$, and to 500kHz when $V_{IN} / V_{OUT\_BOOST} > 10/11$.

Fault Indicator and Diagnostics

The device provides full diagnostics for different fault conditions. The MPQ2026A monitors the LDO's load current through an internal sense resistor to protect against over-current and short-circuit conditions. In addition, the device also detects output over-voltage (OV) and under-voltage (UV) conditions, and it features LDO

output pin short-to-battery protection and thermal shutdown.

The /FT pin pulls high during normal operation. Any fault or warning pulls this pin down to indicate a fault status (see Table 1). The /FT pin is an open drain of a MOSFET. It should be

connected to a ≤5V voltage source through a resistor (e.g. 100kΩ).

The MPQ2026A has dedicated register bits that serve as fault flags and indicate the device's status for system diagnostics. See the Register Map on page 37 for more details.

Table 1: Fault Indicator

Fault	Registers Fault Flag	/FT Indication	Fault Actions
Thermal	Yes	Yes	If register 0x04, bit[0] = 0b: latch-off mode If register 0x04, bit[0] = 1b: hiccup mode
Short to battery	Yes	Yes	If register 0x04, bit[0] = 0b: latch-off mode If register 0x04, bit[0] = 1b: hiccup mode
LDO over-current (OC)	Yes	Yes	No action. The chip continues operating until thermal shutdown occurs
LDO over-voltage (OV)	Yes	Yes	No action. The chip continues operating with the OV status
LDO under-voltage (UV)	Yes	Yes	No action. The chip continues operating with the UV status until thermal shutdown occurs
LDO open load (OL)	Yes	Yes	No action. The chip continues operating with the OL status until thermal shutdown occurs
Boost OC	Yes	Yes	No action. The chip continues operating with the OC status
Boost OV	Yes	Yes	No action. The chip continues operating in OV status
Boost UV	Yes	Yes	No action. The chip continues operating in the UV status

Fault Handling

After a short-to-battery or thermal shutdown fault occurs, the device operates based on the corresponding fault mode set via register 0x04, bit[0]. There are two operating schemes: hiccup mode and latch-off mode.

In hiccup mode, the chip attempts to restart the converter. After the converter completely shuts down, a fault recovery timer starts. After a 100ms delay time, the converter attempts to soft start automatically. If the fault condition is not removed, the converter reinitiates the fault protection and repeats the auto-recovery process in hiccup mode. If the fault condition is removed once soft start ends, and the converter operates normally for a consecutive 80µs, then the fault status resets.

Latch-off mode stops the converter until the power is cycled on the input supply or EN. The part restarts in normal mode after the blank time set via register 0x0F, bits D[7:6].

Short-Circuit (SC) and Over-Current (OC) Conditions

The current limit of each LDO channel is configured via I²C interface to protect the device during short-circuit to GND or OC conditions.

When the output current of either LDO reaches its internal threshold, the output current of the LDO is limited, and a dedicated bit in the register is set to indicate the fault. The /FT pin also asserts low, but the output is not disabled.

The /FT pin and the status of the internal register diagnostic bits should be monitored by the external microcontroller (MCU), and the channel experiencing the SC or OC condition should be disabled by the MCU by setting the dedicated register bits via the I²C interface. If a severe condition occurs, the MCU can shut down the MPQ2026A by pulling the EN pin low.

If this condition persists, thermal shutdown can occur, and then both outputs are disabled.

Short-to-Battery (STB) Detection

It is possible to short the LDO output pins to the battery due to a system fault. Each LDO channel can detect this failure by comparing the corresponding voltage at the OUT1/2 and VIN pins before the device's internal switches turn on.

An adjustable blank time is asserted each time the device is enabled when both VIN and EN exceed their rising thresholds, or when they recover from thermal shutdown or hiccup mode.

Short-to-battery detection occurs during this adjustable blank time. If the device detects the short-to-battery fault, all the boost regulator's and dual LDO's switches latch off or initiate hiccup mode (based on register 0x04, bit D[0]), the /FT pin asserts low, and the dedicated bits in the register are set to indicate the fault channel. After the short-to-battery fault is removed, the device can recover to normal operation automatically if hiccup mode selected. If latch-off mode is selected, the device can recover to normal operation by cycling the power on VIN or EN to reset VCC. If the short-to-battery condition occurs outside of the blank time, the short-to-battery function does not work.

Note that the blank time can be set between 1ms and 15ms via register 0x0F, bits D[7:6]. The default value is 15ms.

Thermal Shutdown

Thermal shutdown circuitry protects the device from overheating. Typically, the switch turns off immediately when the junction temperature exceeds 170°C. The switch turns on again after the device temperature drops by about 20°C.

Integrated Inductive Clamp

During output shutdown, the cable inductance continues to source the current from the output of the device. The device integrates an inductive clamp to help dissipate the inductive energy stored in the cable. An internal diode is connected between the OUT1/2 and GND pins, with a DC current capability of 300mA for inductive clamp protection. Add an additional diode for higher currents.

VCC Regulator

During normal operation, an internal low-dropout (LDO) regulator outputs a nominal 5V V_{CC} supply from VIN. This supplies power to all control blocks and the I^{2}C block. Add a 1µF to 10µF, low-ESR ceramic capacitor from VCC to GND to act as the bypass capacitor.

The VCC supply cannot maintain a 5V output once V_{IN} drops below 5V. If the boost regulator is enabled, the boost output takes over the VCC supply from FB. VCC has an internal under-voltage lockout (UVLO) block. The chip shuts down when V_{CC} drops below its falling threshold (2.4V), and starts up again when V_{CC} exceeds its rising threshold (2.6V). The part resets to the one-time programmable (OTP) memory value when V_{CC} falls to 2.4V.

Input Under-Voltage Lockout (UVLO)

V_{IN} has a UVLO threshold that is internally fixed. UVLO activates when the voltage on the VIN pin drops below its falling threshold. This threshold is 2V when the pre-boost regulator is enabled, or 3.8V when the boost regulator is disabled. UVLO ensures that the regulator is not latched to an unknown state when the input supply voltage is low. If V_{IN} has a negative transient that drops below the UVLO threshold and then recovers, the regulator shuts down then starts up with a normal start-up sequence when the input voltage exceeds the UVLO rising threshold. This threshold is 2.8V when the boost regulator is enabled, or 4.2V when the boost regulator is disabled.

Enable (EN)

The EN pin can be used to enable and disable the entire device. Pull EN below the falling threshold (2.2V) to shut down the chip. Drive EN above its rising threshold (2.4V) to enable the chip.

There are separate, dedicated register bits to enable the software for the pre-boost regulator, LDO1, and LDO2.

The physical EN pin has a higher priority than the software enable function. This means that pulling EN low turns off the part, regardless of the values set via register 0x04, bit D[4].

Frequency Dithering for Low EMI

The frequency dithering technique reduces EMI, which is especially critical for EMI-sensitive applications. The frequency spread spectrum (FSS) modulation technique spreads the frequency spectrum of the boost converter, which then spreads the energy of the switching harmonics across a wider band while reducing their amplitudes. This enables the device to meet stringent EMI goals.

The MPQ2026A's FSS function provides a ±10% variation range for the selected switching frequency, with a 9kHz dithering cycle.

FSS modulation is enabled by default, though it can be disabled via the I^{2}C interface.

Soft Start

To prevent overshooting during start-up, the MPQ2026A has a built-in, 1ms soft-start (SS) time for the boost regulator's output. When the chip starts, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up slowly. When V_{SS} is below the internal reference voltage (V_{REF}), V_{SS} overrides V_{REF} as the error amplifier reference. When V_{SS} exceeds V_{REF}, V_{REF} acts as the reference. At this point, soft start finishes, and the MPQ2026A's boost output enters steady state.

Adjustable LDO Output Voltage

The dual LDOs' output voltages can be configured to be between 1V and 13.6V via the I²C interface. In addition, the dual LDO output voltages can be adjusted by tracking the external voltage on the ADJ1 and ADJ2 pins.

This external voltage tracking mode can be enabled via the I²C interface. If this function is enabled, the dual LDO output voltages (V_{OUT1}, V_{OUT2}) are equal to the voltages at the separate ADJ1 and ADJ2 pins, respectively. The applied voltage ranges on ADJ1 and ADJ2 are between 3V and 13V. To track higher voltages, a resistor divider can be used to scale down the voltage level.

Note that if external voltage tracking mode enabled, /FT pin indication and LDO output OV, UV, and power good (PG) indication in the I²C registers are invalid, and the /FT pin stays high. The dual LDOs cannot be used in parallel.

LDO Output Voltage and Current Monitor

The dedicated analog-to-digital converter (ADC) block monitors the dual LDOs' output voltages and load currents The ADC can be enabled via the I²C. Read registers 05 through 08 to monitor the LDO 1/2 output voltage and load current. The MPQ2026A provides an open load function. If this function is enabled and the load falls below the open load falling threshold, the MPQ2026A considers the load system to be in an open load state, and then the /FT pin pulls down. The open load function does not work when it is disabled. By default, the open load function is disabled. Contact an MPS FAE for more details.

Multi-Page One-Time Programmable (OTP) Memory

The MPQ2026A features 2 pages of one-time programmable memory to permanently store the desired settings.

For long-term reliability, a differential one-time programmable cell is used instead of a single-ended cell. Data is stored on two floating gate avalanche injection metal oxide semiconductors (FAMOS), and output comparators are used for differential reading.

The first page of the multi-page one-time programmable memory has been configured following custom codes.

Once the device is enabled, the default values on the first page set the control parameters in the registers. If there is data on other pages of the one-time programmable memory, the newest setting is identified by an internal indicator to the write registers. See the Register Map on page 37 for more details.

I²C INTERFACE

I²C Serial Interface Description

The I²C is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address, and arranges the communication sequence. The MPQ2026A interface is an I²C slave that supports fast mode (400kHz), adding flexibility to the power supply solution. The output voltages, transition slew rate, and additional parameters can be instantaneously controlled via the I²C interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 7).
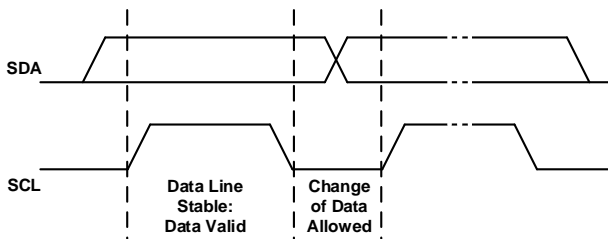
Figure 7: Bit Transfer on the I²C Bus

Start and Stop Commands

The start and stop commands are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start (S) command is defined as the SDA signal transitioning from high to low while the SCL is high. The stop (P) command is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 8).
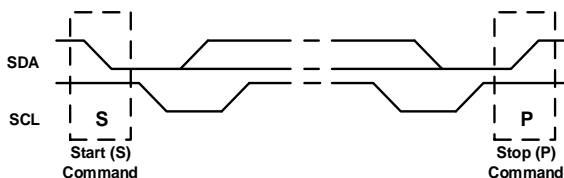
Figure 8: Start and Stop Commands

Start and stop commands are always generated by the master. The bus is considered busy after the start command. The bus is considered free

again after a minimum of 4.7µs after the stop command. The bus stays busy if a repeated start (Sr) command is generated instead of a stop command. The start and repeated start commands are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains stable and low during the high period of the clock pulse.

Figure 9 shows the format for data transfers. After the start command, a slave address is sent. This address is 7-bits long, followed by an eighth data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). A data transfer is terminated by the stop command, which is generated by the master. If the master still wishes to communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.
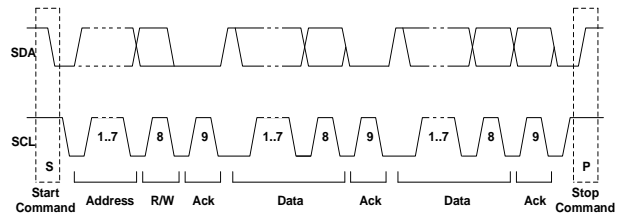
Figure 9: A Complete Data Transfer

Packet Error Checking (PEC)

The packet error checking (PEC) mechanism is employed to improve communication reliability and robustness. When applicable, PEC is implemented by appending a packet error code at the end of each message transfer.

The PEC is a CRC-8 error-checking byte, calculated on all the message bytes (including addresses and read/write bits). The PEC is appended to the message by the device that supplied the last data byte.

Write Sequence

A typical write sequence requires a master's start command, a valid slave address, a register index byte, a corresponding data byte, and ends with a PEC for a single data update.

After receiving each byte, the MPQ2026A acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MPQ2026A. The

MPQ2026A performs an update on the falling edge of the LSB byte.

The PEC byte in a write sequence can be calculated with CRC-8. It requires the slave address, register index, and data to make the calculation. CRC-8 can be estimated with Equation (1):

$$CRC\text{-}8 = X^8 + X^2 + X + 1 \qquad (1)$$

Figure 10 shows a write sequence.
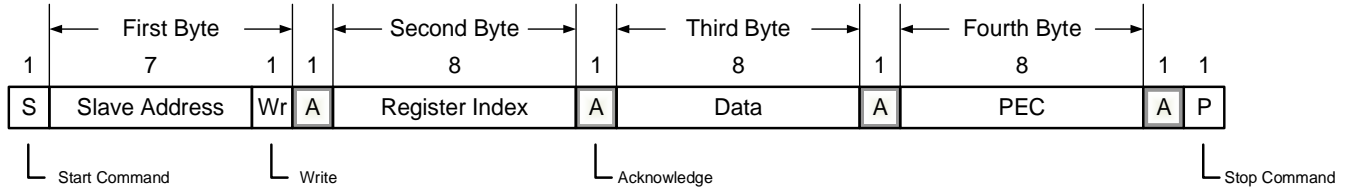
Figure 10: Write Sequence

Read Sequence

A typical read sequence is five bytes long. It starts with the master's start condition, then a write valid slave address, followed by a register index byte. Unlike a write sequence, the master sends a start command again. The bus direction then turns around with the re-broadcast of the slave address, with bit[0] indicating a read cycle. The following fourth byte contains the data being returned by the MPQ2026A. That byte value in the data byte reflects the value of the register

index being queried before. Finally, the MPQ2026A sends a PEC byte to end the read sequence. This means that only one register can be read at a time.

The PEC byte in the read sequence can be calculated with CRC-8. It requires the slave address, register index, slave address and data to make the calculation (see Equation (1) for more details).

Figure 11 shows a read sequence.
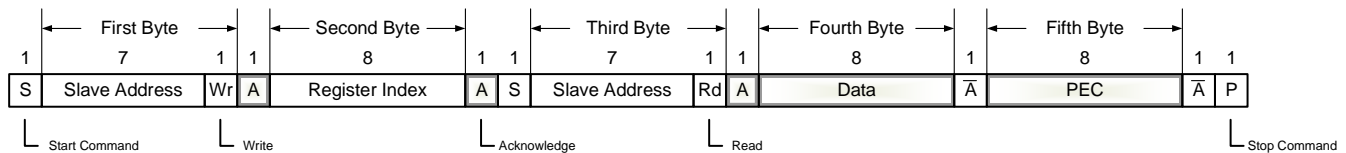
Figure 11: Read Sequence

I²C Update Sequence

The MPQ2026A requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPQ2026A acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MPQ2026A. The MPQ2026A performs an update on the falling edge of the LSB byte.

I²C Chip Address

The ADD pin can be used to configure the I²C address by adjusting the resistor value that is

connected between the ADD pin and ground. A 10µA current flows from the ADD pin and generates a voltage on the ADD resistor at start-up. The MPQ2026A supports 7 addresses, for up to 7 voltage rails, by detecting the different voltages on the ADD pin. Table 2 on page 36 shows the resistor values for different I²C addresses. The resistor's tolerance should not exceed 1% of the recommended resistor value.

When the master sends the address as an 8-bit value, the 7-bit address should be followed by 0 or 1 to indicate a write or read operation, respectively.

Table 2: I²C Address

Address	Resistor (kΩ)	Window Low (mV)	Typical ADDR Voltage (mV)	Window high (mV)	Min (µA)	Typical ADDR Current (µA)	Max (µA)
21h	0 (1%)	0	0	40			
22h	6.98 (1%)	40	70	100			
23h	15 (1%)	100	150	200			
24h	30 (1%)	200	300	400	9.5	10	10.5
25h	54.9 (1%)	400	550	700			
26h	95.3 (1%)	700	950	1200			
27h	>130 (1%) or floating	1200	-	-			

REGISTER MAP

Register Short Name	R/W	Add.	Default (9)	D7	D6	D5	D4	D3	D2	D1	D0
Device Status and Diagnostics											
DEV_REV	R	0x00	00h	SILLICON _INFO							
DEV_STAT	R	0x01	00h	PREBOOST _ACTIVE	LDO_1_ ACTIVE	LDO_2_ ACTIVE	VOUT1_PG	VOUT2_PG	FT_ASSERT	I^2C_ERR	POR
ERR_FLAG_1	R	0x02	00h	VOUT_1_OV	VOUT_1_UV	VOUT_2_OV	VOUT_2_UV	VOUT_BST_OV	VOUT_BST_UV	LDO_1_STB	LDO_2_STB
ERR_FLAG_2	R	0x03	00h	LDO_1_OC	LDO_2_OC	PREBOOST_OC	OT	LDO_1_OL	LDO_2_OL	RSV	RSV
DEV_CTRL	W/R	0x04	E1h	PREBOOST_EN	LDO_1_EN	LDO_2_EN	SHUTDOWN	ADC-EN	SOFT_RST	BOOST_FREQ_SEL	FAULT_HANDLE
Monitoring											
MON_VOUT_1	R	0x05	00h	VOUT1_MON							
MON_VOUT_2	R	0x06	00h	VOUT2_MON							
MON_IOUT_1	R	0x07	00h	IOUT1_MON							
MON_IOUT_2	R	0x08	00h	IOUT2_MON							
Power Management											
SET_VOUT_1	W/R	0x09	68h	FAULT_CLEAR	VOUT1_STEP	VOUT1_SET					
SET_VOUT_2	W/R	0x0A	68h	POWER_SEQ	VOUT2_STEP	VOUT2_SET					
SET_VPREBOOST_1	W/R	0x0B	78h	VPREBOOST_SET							
SET_VPREBOOST_2	W/R	0x0C	9Ch	VPREBOOST_ON_THR				PREBOOST_OV_R		PREBOOST_UV_F	
SET_PG_UVOV	W/R	0x0D	00h	VOUT1_OV_THR	VOUT1_UV_THR	VOUT2_OV_THR	VOUT2_UV_THR	VOUT1_PG_H_THR	VOUT1_PG_L_THR	VOUT2_PG_H_THR	VOUT2_PG_L_THR
SET_IOUT_LIM_1	W/R	0x0E	10h	LDO1_TRC	LDO2_TRC	FSS_DIS	IOUT_1_OC_THR				
SET_IOUT_LIM_2	W/R	0x0F	10h	STB detection window	OC_MIN	IOUT_2_OC_THR					

Note:

9) The default values are for the MPQ2026A-0000 registers. The default value can be redefined if the one-time programmable function is available.

REGISTER DESCRIPTION

DEV_REV (0x00)

Access: Read-only

POR/Soft Reset Value: 00000000

The DEV_REV command returns the device revision and information.

Bits	Name	Description
D[7:0]	SILICON_INFORMATION	Returns the silicon information.

DEV_STAT (0x01)

Access: Read-only

POR/Soft Reset Value: 00000000

The DEV_STAT command returns the device status.

Bits	Name	Description
D[7]	PREBOOST_ACTIVE	0: The pre-boost converter is not active 1: The pre-boost converter is active
D[6]	LDO_1_ACTIVE	0: LDO 1 is not active 1: LDO 1 is active
D[5]	LDO_2_ACTIVE	0: LDO 2 is not active 1: LDO 2 is active
D[4]	VOUT1_PG	0: The LDO 1 output voltage is not within its power good range 1: The LDO 1 output voltage is within its power good range
D[3]	VOUT2_PG	0: The LDO 2 output voltage is not within its power good range 1: The LDO 2 output voltage is within its power good range
D[2]	FT_ASSERT	0: /FT pin is not asserting 1: /FT pin is asserting (active low)
D[1]	I²C_ERR	0: No I²C communication error has occurred 1: An I²C communication error has occurred
D[0]	POR	0: No power-on reset (POR) event has occurred 1: A POR event has occurred and finished

ERR_FLAG_1 (0x02)

Access: Read-only

POR/Soft Reset Value: 00000000

The ERR_FLAG_1 command returns device error flags for over-voltage (OV) and under-voltage (UV) conditions.

Bits	Name	Description
D[7]	VOUT_1_OV	0: Clears to 0 when there is no over-voltage (OV) condition on OUT1 1: An OV condition has been detected on OUT1
D[6]	VOUT_1_UV	0: Clears to 0 when there is no under-voltage (UV) condition on OUT1 1: A UV condition has been detected on OUT1
D[5]	VOUT_2_OV	0: Clears to 0 when there is no OV condition on OUT2 1: An OV condition has been detected on OUT2
D[4]	VOUT_2_UV	0: Clears to 0 when there is no UV condition on OUT2 1: A UV condition has been detected on OUT2

Bits	Name	Description
D[3]	VOUT_BST_OV	0: Clears to 0 when no OV condition has been detected on FB 1: An OV condition has been detected on FB
D[2]	VOUT_BST_UV	0: Clears to 0 when no UV condition has been detected on FB 1: A UV condition has been detected on FB
D[1]	LDO_1_STB	0: Clears to 0 when no short-to-battery condition has been detected on LDO 1 1: A short-to-battery condition has been detected on LDO 1
D[0]	LDO_2_STB	0: Clears to 0 when no short-to-battery condition has been detected on LDO 2 1: A short-to-battery condition has been detected on LDO 2

ERR_FLAG_2 (0x03)

Access: Read-only

POR/Soft Reset Value: 00000000

The ERR_FLAG_2 command returns device error flags for over-current (OC) and over-temperature (OT) conditions.

Bits	Name	Description
D[7]	LDO_1_OC	0: Clears to 0 when no over-current (OC) condition has been detected on OUT1 1: An OC condition has been detected on OUT1
D[6]	LDO_2_OC	0: Clears to 0 when no OC condition has been detected on OUT2 1: An OC condition has been detected on OUT2
D[5]	PREBOOST_OC	0: Clear to 0 when no OC condition has been detected in the pre-boost regulator 1: An OC condition has been detected in the pre-boost regulator
D[4]	OT	0: Clears to 0 when no over-temperature (OT) condition has been detected 1: An OT condition has been detected
D[3]	LDO_1_OL	0: Clears to 0 when no open load (OL) condition has been detected on OUT1 1: An OL condition has been detected on OUT1. Note that this bit is only valid when the open load function is enabled
D[2]	LDO_2_OL	0: Clears to 0 when no OL condition has been detected on OUT2 1: An OL condition has been detected on OUT2. Note that this bit is only valid when the open load function is enabled
D[1:0]	RESERVED	Reserved. Always reads as 0.

DEV_CTRL (0x04)

Access: R/W

POR/Soft Reset Value: 11100001

The DEV_CTRL command controls the device.

Bits	Name	Description
D[7]	PREBOOST_EN	0: The pre-boost converter is disabled 1: The pre-boost converter is enabled
D[6]	LDO_1_EN	0: LDO 1 is disabled 1: LDO 1 is enabled
D[5]	LDO_2_EN	0: LDO 2 is disabled 1: LDO 2 is enabled
D[4]	SHUTDOWN	0: Turn on the device if the EN pin voltage exceeds EN_{VTH_R} 1: The device is forced to shut down
D[3]	ADC-EN	0: The analog-to-digital converter (ADC) is disabled 1: ADC is enabled

D[2]	SOFT_RST	0: No soft reset has been required 1: A soft reset has been requested. The device returns to the state of the OTP code
D[1]	BOOST_FREQ_SEL	0: 400kHz switching frequency 1: 2.2MHz switching frequency
D[0]	FAULT_HANDLE	0: Latch-off mode 1: Hiccup mode with a 100ms blank time

MON_VOUT_1 (0x05)

Access: Read-only

POR/Soft Reset Value: 00000000

The MON_VOUT_1 command returns the monitored LDO 1 output voltage (V_{OUT1}).

Bits	Name	Description
D[7:0]	VOUT1_MON	Records the monitored OUT1 voltage by the ADC. This value refreshes each time it is read. 1 LSB = 55mV. The value can be calculated with the following equation: $$VOUT1\_MON = D[7:0] \times 55mV.$$ For example, if bits D[7:0] = $(10100100)_2$, this is $(164)_{10}$, and V_{OUT1} = 164 x 55mV = 9.02V.

MON_VOUT_2 (0x06)

Access: Read-only

POR/Soft Reset Value: 00000000

The MON_VOUT_2 command returns the monitored LDO 2 output voltage (V_{OUT2}).

Bits	Name	Description
D[7:0]	VOUT2_MON	Records the monitored OUT2 voltage by the ADC. This value refreshes each time it is read. 1 LSB = 55mV. The value can be calculated with the following equation: $$VOUT2\_MON = D[7:0] \times 55mV.$$ For example, if bits D[7:0] = $(10100100)_2$, this is $(164)_{10}$, and V_{OUT2} = 164 x 55mV = 9.02V.

MON_IOUT_1 (0x07)

Access: Read-only

POR/Soft Reset Value: 00000000

The MON_IOUT_1 command returns the monitored LDO 1 output current (I_{OUT1}).

Bits	Name	Description
D[7:0]	IOUT1_MON	Records the monitored OUT1 current by the ADC. This value refreshes each time it is read. 1 LSB = 1.2mA. The value can be calculated with the following equation: $$IOUT1\_MON = D[7:0] \times 1.2mA.$$ For example, if bits D[7:0] = $(11111010)_2$, this is equal to $(250)_{10}$, and I_{OUT1}= 250 x 1.2mA = 300mA.

MON_IOUT_2 (0x08)

Access: Read-only

POR/Soft Reset Value: 00000000

The MON_IOUT_2 command returns the monitored LDO 2 output current (I_{OUT2}).

Bits	Name	Description
D[7:0]	IOUT2_MON	Records the monitored OUT2 current by the ADC. This value refreshes each time it is read. 1 LSB = 1.2mA. The value can be calculated with the following equation: $$IOUT2\_MON = D[7:0] \times 1.2mA.$$ For example, if bits D[7:0] = $(11111010)_2$, this is equal to $(250)_{10}$, and I_{OUT2}= 250 x 1.2mA = 300mA.

SET_VOUT_1 (0x09)

Access: R/W

POR/Soft Reset Value: 01101000

The SET_VOUT_1 command sets the LDO1 output voltage (V_{OUT1}).

Bits	Name	Description
D[7]	FAULT_CLEAR	0: No action (default) 1: Clear all fault flags and de-assert the /FT pin
D[6]	VOUT1_STEP	Sets the OUT1 voltage step. This bit is set to 1 by default. 0: 100mV 1: 200mV
D[5:0]	VOUT1_SET	Sets the OUT1 voltage, calculated with the following equation: $$V_{OUT1} = 1V + VOUT1\_SET \times VOUT1\_STEP$$ If the default is D[5:0] = $(101000)_2$, which is $(40)_{10}$, then the default V_{OUT1} = 1V + 40 x 200mV = 9V

SET_VOUT_2 (0x0A)

Access: R/W

POR/Soft Reset Value: 01101000

The SET_VOUT_2 command sets the LDO 2 output voltage (V_{OUT2}).

Bits	Name	Description
D[7]	POWER_SEQ	0: OUT1 and OUT2 are powered simultaneously 1: OUT2 is delayed by 100ms
D[6]	VOUT2_STEP	Sets the OUT2 voltage step. This bit is set to 1 by default. 0: 100mV 1: 200mV
D[5:0]	VOUT2_SET	Sets the OUT2 voltage, calculated with the following equation: $$V_{OUT2} = 1V + VOUT2\_SET \times VOUT2\_STEP$$ If the default is D[5:0] = $(101000)_2$, which is $(40)_{10}$, then the default V_{OUT2} = 1V + 40 x 200mV = 9V

SET_VPREBOOST (0x0B)

Access: R/W

POR/Soft Reset Value: 01111000

The SET_VPREBOOST command sets the pre-boost regulator output voltage (V_{OUT_BOOST}).

Bits	Name	Description
D[7:0]	VPREBOOST_SET	Sets the pre-boost regulator output voltage. The default value is 12V. 00h~40h: Reserved 41h~9Fh: D[7:0] x 100mV (100mV/step). 6.5V to 15.9V A0h~FFh: Reserved

SET_VPREBOOST_ON (0x0C)

Access: R/W

POR/Soft Reset Value: 10011100

The SET_VPREBOOST_ON command sets the pre-boost regulator's on voltage threshold for over-voltage (OV) and under-voltage (UV) conditions.

Bits	Name	Description
D[7:4]	VPREBOOST_ON_THR	Sets the pre-boost regulator's turn on threshold, The default value is 11V. 00h~0Dh: D[7:4] x 500mV + 6.5V (500mV/step) 0Eh: 14V 0Fh: 15V
D[3:2]	PREBOOST_OV_R	00: 110% of V_{REF} 01: 115 of V_{REF} 10: 120% of V_{REF} 11: 130% of V_{REF}
D[1:0]	PREBOOST_UV_F	00: 70% of V_{REF} 01: 75% of V_{REF} 10: 80% of V_{REF} 11: 85% of V_{REF}

SET_PG_UVOV (0x0D)

Access: R/W

POR/Soft Reset Value: 00000000

The SET_PG_UVOV command sets the power good and LDO under-voltage (UV) and over-voltage (OV) settings.

Bits	Name	Description
D[7]	VOUT1_OV_THR	0: The V_{OUT1} over-voltage (OV) threshold is 115% of the set V_{OUT1} 1: The V_{OUT1} OV threshold is 120% of the set V_{OUT1}
D[6]	VOUT1_UV_THR	0: The V_{OUT1} under-voltage (UV) threshold is 75% of the set V_{OUT1} 1: The V_{OUT1} UV threshold is 80% of the set V_{OUT1}
D[5]	VOUT2_OV_THR	0: The V_{OUT2} OV threshold is 115% of the set V_{OUT2} 1: The V_{OUT2} OV threshold is 120% of the set V_{OUT2}
D[4]	VOUT2_UV_THR	0: The V_{OUT2} UV threshold is 75% of the set V_{OUT2} 1: The V_{OUT2} UV threshold is 80% of the set V_{OUT2}
D[3]	VOUT1_PG_H_THR	0: The upper boundary of the OUT1 power good (PG) threshold is 105% of the set voltage 1: The upper boundary of the OUT1 PG threshold is 110% of the set voltage
D[2]	VOUT1_PG_L_THR	0: The lower boundary of the OUT1 PG threshold is 90% of the set voltage 1: The lower boundary of the OUT1 PG threshold is 95% of the set voltage

D[1]	VOUT2_PG_H_THR	0: The upper boundary of the OUT2 PG threshold is 105% of the set voltage 1: The upper boundary of the OUT2 PG threshold is 110% of the set voltage
D[0]	VOUT2_PG_L_THR	0: The lower boundary of the OUT2 PG threshold is 90% of the set voltage 1: The lower boundary of the OUT2 PG threshold is 95% of the set voltage

SET_IOUT_LIM_1 (0x0E)

Access: R/W

POR/Soft Reset Value: 00010000

The SET_IOUT_LIM_1 command sets the LDO 1 current limit threshold

Bits	Name	Description
D[7]	LDO1-TRC	0: Disable LDO1 tracking mode 1: Enable LDO1 tracking mode
D[6]	LDO2-TRC	0: Disable LDO2 tracking mode 1: Enable LDO2 tracking mode
D[5]	FSS_DIS	0: Enable FSS modulation 1: Disable FSS modulation
D[4:0]	IOUT_1_OC_THR	Sets the OUT1 over-current (OC) threshold. 1 LSB = 6.25mA. This value can be calculated with the following equation: $$I_{LIMIT} = D[4:0] \times 6.25mA + OC\_MIN$$ OC_MIN is set by register 0x0F, bit[5]. The default D[4:0] = $(10000)_2$, which is equal to $(16)_{10}$, and I_{LIMIT} = 16 x 6.25 + 300 = 400mA.

SET_IOUT_LIM_2 (0x0F)

Access: R/W

POR/Soft Reset Value: 00010000

The SET_IOUT_LIM_2 command sets the LDO 2 current limit threshold

Bits	Name	Description
D[7:6]	STB_DETECTION_WINDOW	00: 15ms 01: 7ms 10: 3ms 11: 1ms
D[5]	OC_MIN	Sets the minimum over-current (OC) threshold for LDO1 and LDO2. The default value is 300mA. 0: 300mA 1: 100mA
D[4:0]	IOUT_2_OC_THR	Sets the OUT2 over-current (OC) threshold. 1 LSB = 6.25mA. This value can be calculated with the following equation: $$I_{LIMIT} = D[4:0] \times 6.25mA + OC\_MIN$$ OC_MIN is set by register 0x0F, bit[5]. The default D[4:0] = $(10000)_2$, which is equal to $(16)_{10}$, and I_{LIMIT} = 16 x 6.25 + 300 = 400mA.

APPLICATION INFORMATION

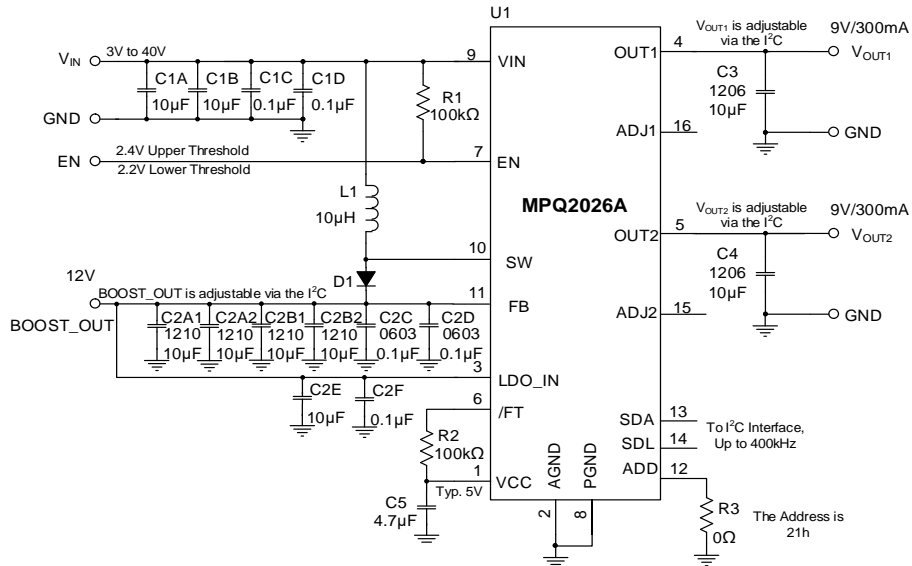Figure 12 shows the typical application circuit for the MPQ2026A.

Figure 12: Typical Application Circuit (Boost + Dual LDOs, V_{OUT1} = 9V, V_{OUT2} = 9V, V_{OUT_BOOST} = 12V, f_{SW} = 400kHz)

Table 3 shows the design guide index. For more details, see Figure 12.

Table 3: Design Guide Index

Pin #	Name	Components	Design Guide Index
1	VCC	C5	Internal VCC (VCC, Pin 1)
2	AGND	-	GND Connection (PGND, Pin 8; AGND, Pin 2)
3	LDO_IN	C2E, C2F	Selecting the Input Capacitors for the Dual LDOs (LDO_IN, Pin 3)
4	OUT1	C3	Selecting the Output Capacitors for LDO1 (OUT1, Pin 4)
5	OUT2	C4	Selecting the Output Capacitors for LDO2 (OUT2, Pin 5)
6	/FT	R2	Fault Indicator (/FT, Pin 6)
7	EN	R1	Enable (EN, Pin 7)
8	GND	-	GND Connection (PGND, Pin 8; AGND, Pin 2)
9	VIN	C1A, C1B, C1C, C1D	Selecting the Input Capacitors for the Pre-Boost Regulator (VIN, Pin 9)
10	SW	L1, D1	Selecting the Inductor for the Pre-Boost Regulator (SW, Pin 10)
			Selecting the Schottky Diode for the Pre-Boost Regulator (SW, Pin 10)
11	FB	C2A1, C2A2, C2B1, C2B2, C2C, C2D	Selecting the Boost Output Capacitor (FB, Pin 11)
12	ADD	R3	Selecting the Resistor for the I²C Address (ADD, Pin 12)
13	SDA	-	I²C Interface (SDA, Pin 13; SCL, Pin 14)
14	SCL	-	I²C Interface (SDA, Pin 13; SCL, Pin 14)
15	ADJ2	-	Setting the Reference Voltage Input for the Dual LDOs (ADJ1, Pin 16; ADJ2, Pin 15)
16	ADJ1	-	Setting the Reference Voltage Input for the Dual LDOs (ADJ1, Pin 16; ADJ2, Pin 15)

Internal VCC (VCC, Pin 1)

The VCC capacitor (C5) should be between 1µF and 10µF. Generally, a 4.7µF ceramic capacitor is recommended.

All of the control blocks and the I2C block are powered by the internal regulator. This regulator uses V_{IN} as its input and operates across the full V_{IN} range. When V_{IN} exceeds 5V, V_{CC} is in full regulation and supplied by V_{IN}. When V_{IN} is below 5V and the pre-boost regulator is enabled, V_{CC} is supplied by the boost output via the FB pin. When V_{IN} drops below 5V and the pre-boost regulator is disabled, the V_{CC} output drops.

In latch-off mode, V_{CC} should drop below its falling threshold before start-up to prevent a failed start-up.

It is not recommended that V_{CC} supplies power to external circuits. Do not use I2C communication when V_{CC} is below its UVLO threshold.

Selecting the Input Capacitor for the Dual LDOs (LDO_IN, Pin 3)

For efficient operation, place a ceramic capacitor with dielectrics (X5R or X7R) between the input pin and ground. It is recommended for the capacitor to be between 1µF and 10µF. Larger-value capacitors improve line transient response.

Selecting the Output Capacitor for the Dual LDOs (OUT1, Pin 4; OUT2, Pin 5)

For stable operation, place a 4.7µF to 22µF, ceramic capacitor with X5R or X7R dielectrics between the OUT pin and ground. Larger- value capacitors improve line transient response and reduce noise. Output capacitors of other dielectric types may be used, but they are not recommended, as their capacitance can deviate greatly from their rated value across different temperatures.

Setting the Boost and LDOs Output Voltage

The MPQ2026A does not require an external resistor to set the output voltage. The one-time programmable register 0x0B sets V_{OUT_BOOST}, while registers 0x09 and 0x0A set the output voltage for the dual LDOs (see the Register Map on page 37 for more details).

V_{OUT_BOOST} is configured via register 0x0B, bits D[7:0], and the voltage can be calculated with

(bits D[7:0] x 100mV). This voltage can be between 6.5V and 15.9V.

For example, if 0x0B is set to 78h, then the output voltage = 0.1V x 120 = 12V.

The dual LDOs' output voltages are configured via registers 0x09 and 0x0A. They can be set between 1V and 13.6V with 200mV per step, or between 1V and 7.3V with 100mV per step. The output voltage can be calculated with (bits D[5:0] x step) + 1V.

For example, if register 0x09, bits D[7:0] are set to 68h, and the step is 200mV, then the LDO output voltage = 1V + (40 x 0.2V) = 9V.

When V_{LDO_IN} is almost equal to V_{OUT}, the LDO enters dropout mode, and LDO's current limit drops by 15%. The difference between V_{LDO_IN} and V_{OUT} must stay above 1.5V when designing the circuit.

Fault Indicator (/FT, Pin 6)

The R_{FT} resistance (R2) value is recommended to be about 100kΩ.

The /FT pin is connected to the open drain of an internal MOSFET. It should be connected to a ⩽ 5V voltage through an external pull-up resistor for fault indication.

Float or ground /FT if it is not used.

At low input voltages, /FT is falsely triggered after start-up. This is because the /FT blanking time may not be long enough during start-up, which can trigger a V_{OUT} UV condition.

EN (EN, Pin 7)

The EN pin can be used to enable and disable the entire device. Pull EN below the falling threshold (2.2V) to shut the chip down. Drive EN above its rising threshold (2.4V) to enable the chip.

There are separate, dedicated register bits to enable the software for the pre-boost regulator, LDO1, and LDO2. The physical EN pin has a higher priority than the software enable function.

Since EN has a 3.3MΩ pull-down resistor, float EN to shut down the chip. EN can be connected to a high-voltage bus (e.g. the VIN pin) through a pull-up resistor. In this scenario, it is recommended to use a 100kΩ pull-up resistor.

The MPQ2026A has an internal, fixed UVLO threshold. In the normal input range, the rising threshold is 2.8V, and the falling threshold is 2V when the pre-boost regulator is enabled. While the pre-boost regulator is disabled, the rising threshold is 4.2V, and the falling threshold is 3.8V. For applications that require a higher UVLO threshold, place an external resistor between the VIN and EN pins to raise the equivalent UVLO threshold.
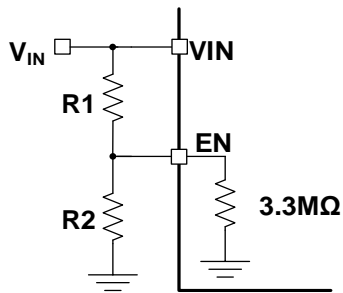

Figure 13: Adjustable UVLO through EN Divider

The UVLO rising and falling thresholds can be calculated with Equation (2) and Equation (3), respectively:

$$UVLO_{VTH\text{-}R} = (1+\frac{R1}{R2||3.3M\Omega}) \times EN_{VTH\_R} \quad (2)$$

$$UVLO_{VTH\text{-}F} = (1+\frac{R1}{R2||3.3M\Omega}) \times EN_{VTH\_F} \quad (3)$$

Where EN_{VTH_R} = 2.4V, and EN_{VTH_F} = 2.2V.

To quickly turn EN on and off, The EN off time should be longer than 500µs.

Selecting the Input Capacitor for the Pre-Boost Regulator (VIN, Pin 9)

The input requires a capacitor to supply the AC ripple current to the inductor, while limiting noise at the input source. Use a low-ESR capacitor with a value >4.7µF to minimize the IC noise. Ceramic capacitors are recommended, but tantalum or low-ESR electrolytic capacitors can also suffice. However, since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. Use a capacitor with an RMS current rating greater than the inductor ripple current.

To ensure stable operation, place the input capacitor as close to the IC as possible. As an alternative, place a small, high-quality ceramic 0.1µF capacitor close to the IC, and place the

larger-value capacitor further away. If using the latter technique, use either tantalum- or electrolytic-type capacitors for the larger-value capacitor. Place all ceramic capacitors close to the MPQ2026A.

Selecting the Inductor for the Pre-Boost Regulator (SW, Pin 10)

The inductor forces V_{OUT} above V_{IN} A larger-value inductor value results in less ripple current and reduces the peak inductor current; this reduces the stress on the internal N-channel switch. However, a larger-value inductor is physically larger, has a higher series resistance, and/or lower saturation current.

A good rule of thumb is to allow the peak-to-peak ripple current to equal 30% to 50% of the maximum input current. To prevent regulator losses due to the current limit, ensure that the peak inductor current is less than 75% of the current limit during duty cycle operation. Also ensure that the inductor does not saturate under the worst-case load transient response and start-up conditions. Calculate the required inductance value with Equation (4):

$$L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I} \quad (4)$$

Where ΔI is the peak-to-peak inductor ripple current, estimated with Equation (5):

$$\Delta I = (30\% \text{ to } 50\%) \times I_{LOAD(MAX)} \quad (5)$$

Where I_{LOAD}(max) is the maximum load current.

Calculate $I_{IN(MAX)}$ with Equation (6):

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{LOAD(MAX)}}{V_{IN} \times \eta} \quad (6)$$

Where η is the efficiency.

Selecting the Schottky Diode for the Pre-Boost Regulator (SW, Pin 10)

The output rectifier diode supplies current to the inductor when the internal MOSFET is off. Use a Schottky diode to reduce losses due to the diode's forward voltage and recovery time. The diode should be rated for a reverse voltage equal to or greater than the expected V_{OUT}. The average current rating must exceed the maximum expected load current, and the peak

current rating must exceed the peak inductor current.

Selecting the Boost Output Capacitor (FB, Pin 11)

The output capacitor maintains the DC output voltage. For the best results, use low-ESR capacitors to minimize the output voltage ripple. The output capacitor's characteristics also affect regulatory control system's stability. For the best results, use ceramic, tantalum, or low-ESR electrolytic capacitors. For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, which means that the output voltage ripple is mostly independent of the ESR. The output voltage ripple (V_{RIPPLE}) can be estimated with Equation (7):

$$V_{RIPPLE} \cong I_{LOAD} \times \frac{1 - \dfrac{V_{IN}}{V_{OUT}}}{C_{OUT} \times f_{SW}} \qquad (7)$$

Where V_{IN} and V_{OUT} are the DC input and output voltages, respectively, I_{LOAD} is the pre-boost regulator's load current, f_{SW} is the switching frequency, and C_{OUT} is the value of the pre-boost regulator's output capacitor.

For tantalum or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency. In this scenario, V_{RIPPLE} can be calculated with Equation (8):

$$V_{RIPPLE} \cong I_{LOAD} \times \frac{1 - \dfrac{V_{IN}}{V_{OUT}}}{C_{OUT} \times f_{SW}} + \frac{I_{LOAD} \times R_{ESR} \times V_{OUT}}{V_{IN}} \quad (8)$$

Where R_{ESR} is the equivalent series resistance of the output capacitor(s).

Choose an output capacitor that satisfies the output ripple and load transient response requirements of the design. A ceramic capacitor exceeding 22µF is recommended for most applications.

Selecting the Resistor for the I²C Address (ADD, Pin 12)

The MPQ2026A supports 7 addresses for up to 7 voltage rails by detecting the voltage on the ADD pin. Table 2 on page 36 shows the resistor values for different I²C addresses. The resistor tolerance should not exceed 1% of recommended resistor value.

I²C Interface (SDA, Pin 13; SCL, Pin 14)

The MPQ2026A interface is an I²C slave that supports fast mode (400kHz), adding flexibility to the power supply solution. See the I²C interface section on page 34 for details.

If the I²C interface is not used, it is recommended to connect the SDA and SCL pins to the VCC pin through a resistor (e.g. 100kΩ).

Setting the Reference Voltage Input for the Dual LDOs (ADJ1, Pin 16; ADJ2, Pin 15)

This external voltage tracking mode can be enabled via the I²C interface. If enabled, the dual LDOs' output voltages (V_{OUT1} and V_{OUT2}) are equal to the voltages at ADJ1 and ADJ2, respectively. For stable operation, use a 10nF to 100nF ceramic capacitor with X5R or X7R dielectrics.

It the ADJ1 and ADJ2 pins are not used, it is recommended to connect them to GND.

GND Connection (PGND, Pin 8; AGND, Pin 2)

See the PCB Layout Guidelines section on page 48 for more details.

PCB Layout Guidelines [10]

Efficient PCB layout (especially the input capacitor, boost output capacitor, inductor, and Schottky diode placement) is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 14 and follow the guidelines below:

1. Place the symmetric input capacitor as close to the VIN and GND pins as possible.

2. Place L1 and D2 as close to the FB pin as possible.

3. Place the symmetric boost output capacitor as close to the Schottky diode as possible.

4. Use a large ground plane to connect directly to PGND.

5. Add vias near PGND if the bottom layer is a ground plane.

6. Ensure that the high-current paths (e.g. PGND and SW/LDO_IN) have short, direct, and wide traces.

7. Place the ceramic input capacitor, especially the small package size (0603) input/output bypass capacitor, as close as possible to the VIN, LDO_IN, FB, VOUT, and PGND pins to minimize high frequency.

8. Keep the connection between the input capacitor and VIN as short and wide as possible.

9. Keep the connection between the inductor and SW pin as short and wide as possible.

10. Keep the connection between the LDO input capacitor and LDO_IN pin as short and wide as possible.

11. Place the VCC capacitor as close to the VCC and AGND pins as possible.

12. Route SW away from sensitive analog areas.

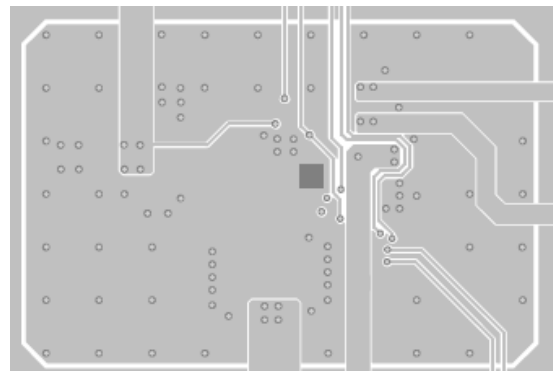13. Use multiple vias to connect the power planes to the internal layers.

Note:

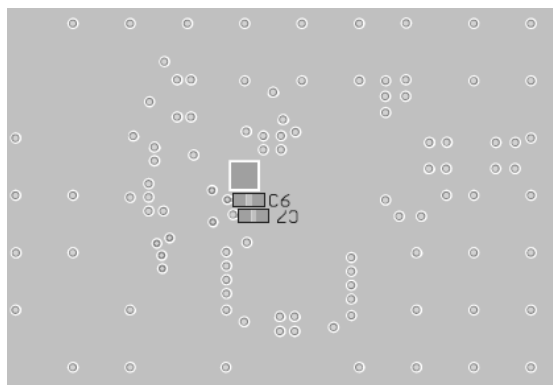10) The recommended PCB layout is based on the typical application circuit (see Figure 18 on page 51).
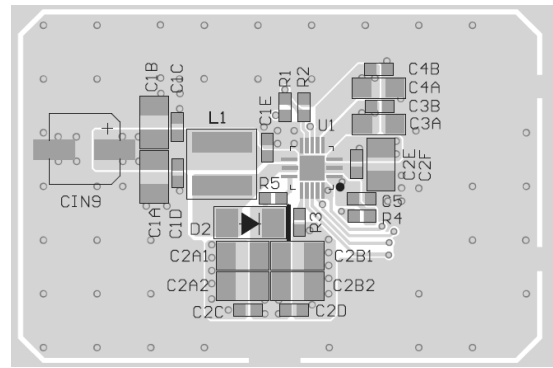
Top Layer
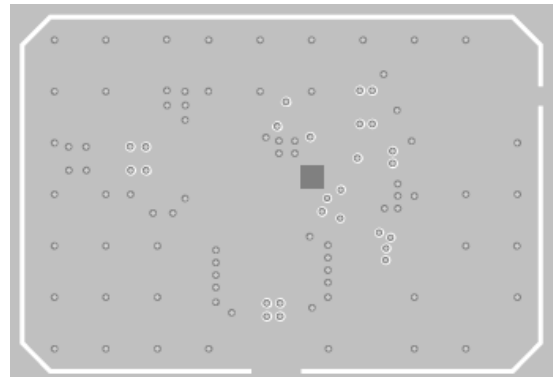
Mid-Layer 1

Mid-Layer 2

Bottom Layer
Figure 14: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

Figure 15: Boost + Dual LDOs, V_{OUT1} = 9V, V_{OUT2} = 9V, V_{OUT_BST} = 12V, f_{SW} = 400kHz

Figure 16: Boost + Dual LDOs, V_{OUT1} = 9V, V_{OUT2} = 9V, V_{OUT_BST} = 12V, f_{SW} = 2.2MHz

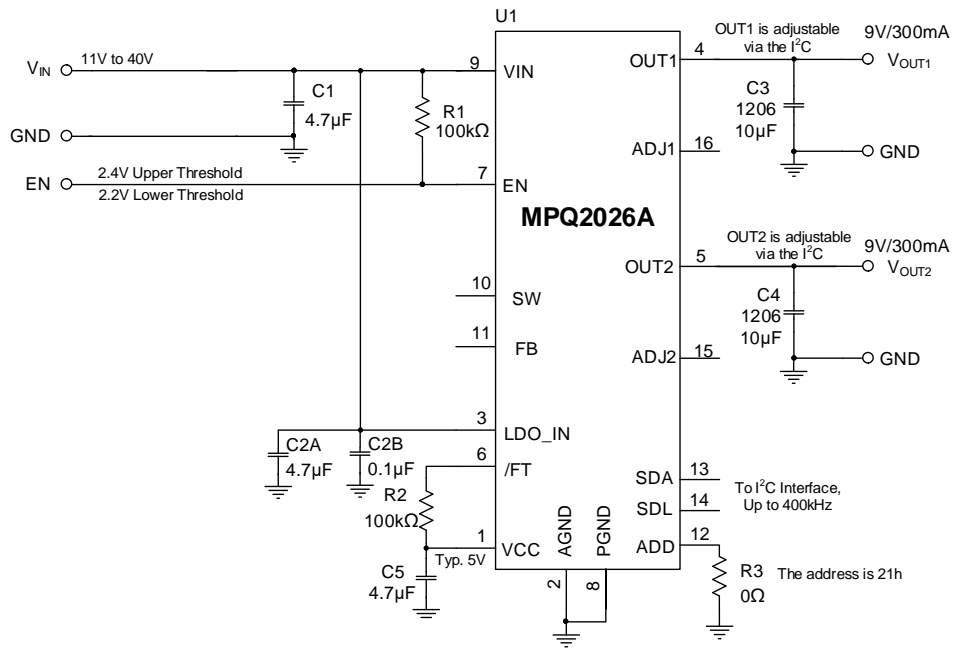# TYPICAL APPLICATION CIRCUITS *(continued)*

Figure 17: Dual LDOs, V_{OUT1} = 9V, V_{OUT2} = 9V
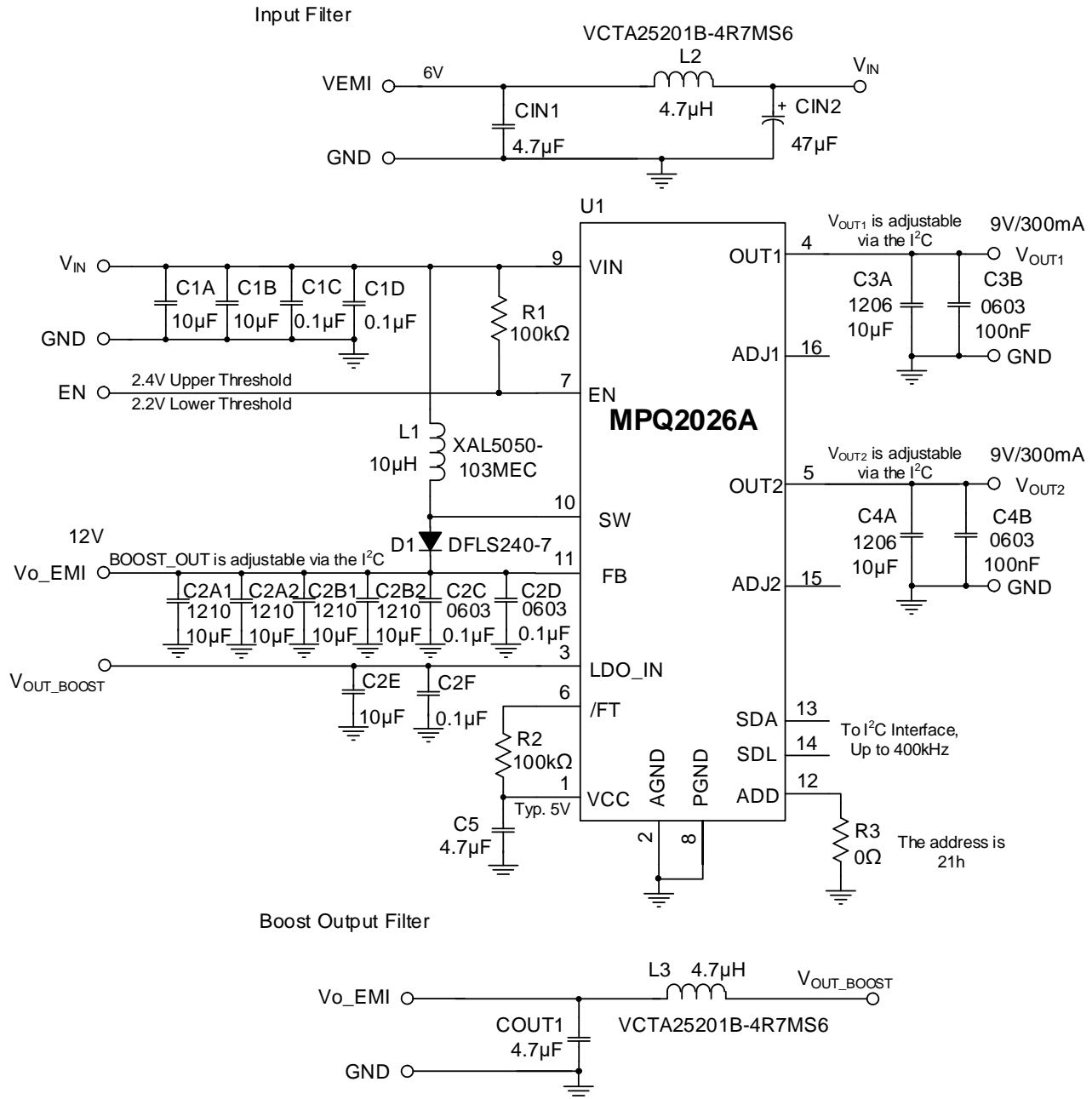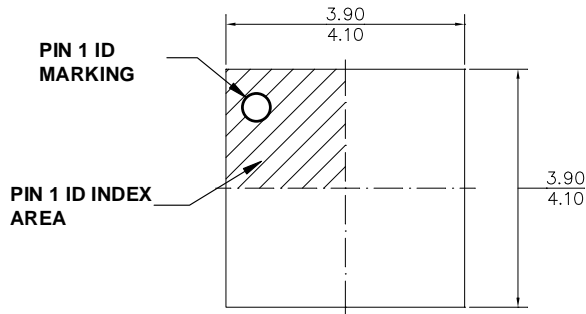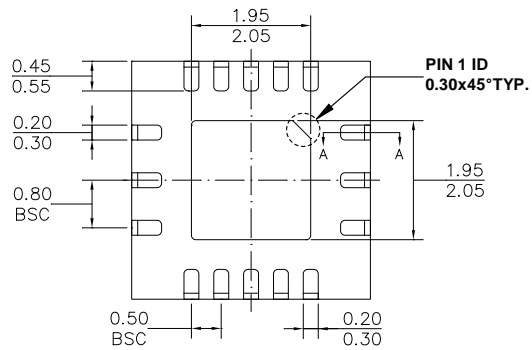
TYPICAL APPLICATION CIRCUITS *(continued)*

Figure 18: Boost + Dual LDOs, V_{OUT1} = 9V, V_{OUT2} = 9V, V_{OUT_BST} = 12V, f_{SW} = 400kHz, with EMI Filters
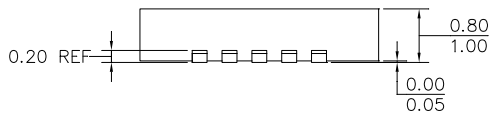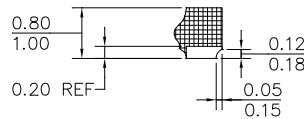
PACKAGE INFORMATION
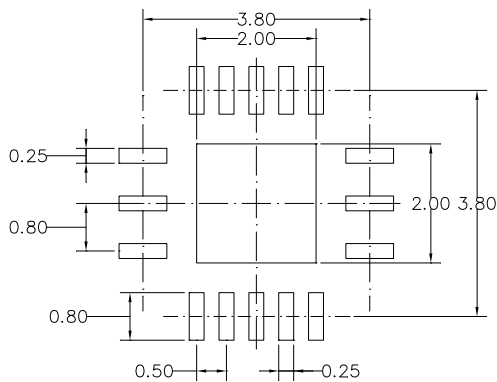
QFN-16 (4mmx4mm)
Wettable Flank

PIN 1 ID
MARKING

PIN 1 ID INDEX
AREA

$\frac{3.90}{4.10}$

$\frac{3.90}{4.10}$

TOP VIEW

$\frac{1.95}{2.05}$

$\frac{0.45}{0.55}$

$\frac{0.20}{0.30}$

0.80
BSC

PIN 1 ID
0.30x45°TYP.

$\frac{1.95}{2.05}$

0.50
BSC

$\frac{0.20}{0.30}$

BOTTOM VIEW

0.20 REF

$\frac{0.80}{1.00}$

$\frac{0.00}{0.05}$

SIDE VIEW

$\frac{0.80}{1.00}$

0.20 REF

$\frac{0.12}{0.18}$

$\frac{0.05}{0.15}$

SECTION A-A

3.80
2.00

0.25

0.80
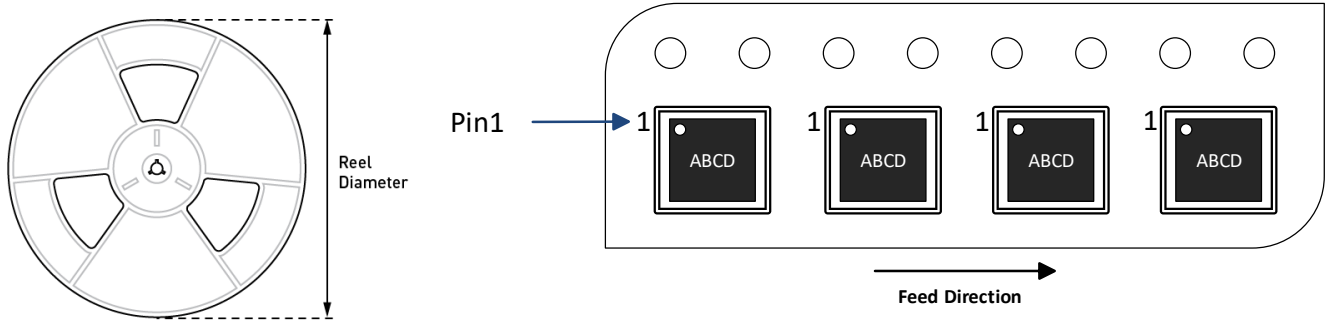
0.80

2.00 3.80

0.50   0.25

RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING REFERENCE TO JEDEC MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION

Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2026AGRE-xxxx-AEC1-Z	QFN-16 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/27/2022	Initial Release	-