MPQ18913

30V, 0.3A High Frequency Transformer Driver for Automotive, AEC-Q100

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MPQ18913 is a high frequency half bridge transformer driver, which is the ideal solution for the primary side switcher used in isolated power supplies. It supports a wide input voltage range of 5V-30V, and integrates two switching FETs which take up to 300 mA average input current.

The device features wide adjustable switching frequency range, which is particularly useful in resonant topologies such as LLC converter. It also comes with input OVP, OCP, and fault indicator. Soft start up is built in to control the inrush current.

The MPQ18913 is available in QFN-10 (2mmx2.5mm) package with wettable flank.

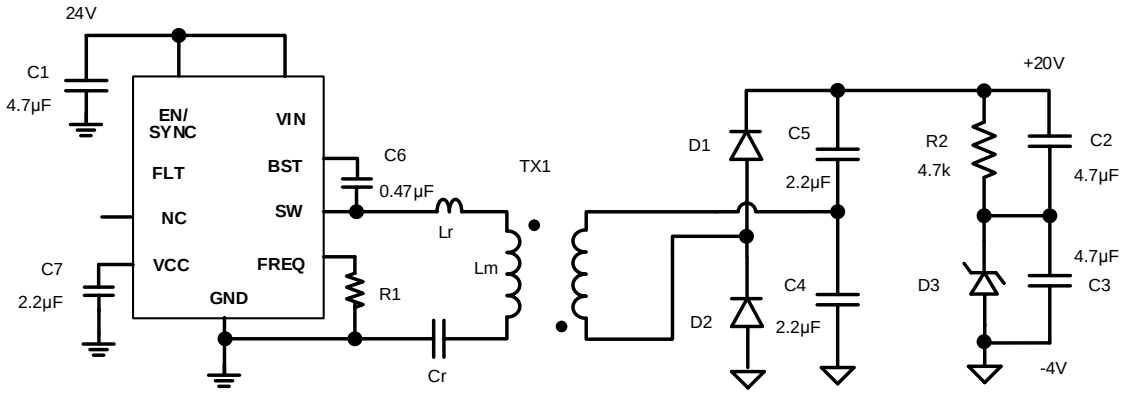
FEATURES

- Half Bridge Transformer Driver for Isolated LLC Resonant Converter
- Adjustable Switching Frequency Range up to 5 MHz
- Supports up to 6W
- QFN-10 (2mmx2.5mm) package with wettable flank
- Available in AEC-Q100 Grade

APPLICATIONS

- Isolated Power Supply
- High Frequency DC-DC Converter
- General Purpose Transformer Driver

TYPICAL APPLICATION



SELECTION GUIDE

Part Number	Soft start time	Hiccup time
MPQ18913GRPE-AEC1-Z	1ms	12ms
MPQ18913GRPE-A-AEC1-Z	20ms	120ms

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ18913GRPE-AEC1	QFN-10 (2mmx2.5mm)	*See Below*	1
MPQ18913GRPE-A-AEC1			
EVQ-18913-D-00A	Evaluation kit		

* For Tape & Reel, add suffix –Z (e.g. MPQ18913GRPE-AEC1-Z).

TOP MARKING

MPQ18913GRPE-AEC1

$\overline{\text{MLY}}$

LLL

ML: Product code of MPQ18913GRPE-AEC1
Y: Year code
LLL: Lot number

TOP MARKING

MPQ18913GRPE-A-AEC1

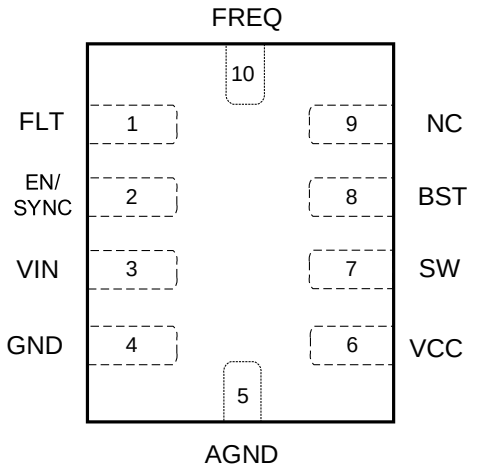
$\overline{\text{MMY}}$

LLL

MM: Product code of MPQ18913GRPE-A-AEC1-Z
Y: Year code
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



Package Diagram

QFN-10 (2mmx2.5mm) package with wettable flank

PIN FUNCTIONS

Package Pin #	Name	Description
1	FLT	**Fault Indicator.** FLT pin is an open-drain output.
2	EN/SYNC	**Enable/External Clock.** Pull high to enable MPQ18913, pull low to disable MPQ18913. Apply external clock to sync switching frequency.
3	VIN	**Input Voltage.** Bypass VIN to GND with a 1µF ceramic capacitor as close as possible to the IC.
4	GND	**Ground.**
5	AGND	**Analog Ground.** Connect to power GND through single point connection.
6	VCC	**Bias Supply.** Decouple with 1µF or larger ceramic capacitor referred to GND. Place the capacitor as close as possible.
7	SW	**Switch Node.**
8	BST	**Drive Voltage for HS FET.** Connect a ceramic capacitor from this pin to SW.
9	NC	Please float NC pin. For internal test use only.
10	FREQ	**Switching Frequency set pin.** Connect a resistor from FREQ to GND. Place the resistor as close as possible.

ABSOLUTE MAXIMUM RATINGS (1)

VIN, EN ..... -0.3V to 35V
V_{SW} ..... -0.3V to (VIN+0.3V)
BST-V_{SW} ..... -0.3V to 6.5V
VCC, V_{DET}, V_{FLT}, V_{FREQ} ..... -0.3V to 6.5V
VIN, EN (surge) ..... -0.3V to 50V
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C
Continuous Power Dissipation (T_A = +25°C) (2)
QFN-10 (2mmx2.5mm) 2.5W

ESD Rating

Human-body model (HBM) ..... ±2000V
Charged-device model (CDM) ..... ±2000V

Recommended Operating Conditions (3)

Input Voltage VIN ..... 5V to 30V
External VCC Bias ..... 4.86V to 5.5V
Junction Temp. (T_J) ..... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

EVQ-18913-D-00A (4)	45.3	7	°C/W
QFN-10 (2mmx2.5mm) (5)	70	2.3	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EVQ18913-D-00A, 6-layer PCB
5) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

VIN = 24V, T_J = -40°C to 150°C, typical values are at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Transformer Driver						
VCC Regulator	VCC	I_{CC}=0-20mA, V_{EN}=1.5V	4.55	4.7	4.85	V
Vcc UVLO Thresholds	VCC_{UV_R}	VCC rising	4.1	4.25	4.4	V
	VCC_{UV_F}	VCC falling	3.95	4.1	4.25	V
	VCC_{UV_HYS}	Hysteresis		150		mV
Vin UVLO Thresholds	VIN_{UV_R}	VIN rising	4.35	4.65	4.9	V
	VIN_{UV_F}	VIN falling	4	4.25	4.5	V
	VIN_{UV_HYS}	Hysteresis		400		mV
Shut Down Current	I_{SD}	V_{EN}=0V		4	12	µA
Supply Current	I_Q	V_{EN}=1.5V, Fsw=1MHz set by Resistor, SW floating		9.5		mA
Input Over Voltage Protection Threshold	V_{OVP_T}	Rising	31	33	35	V
	V_{OVP_F}	Falling	28.5	30.5	32.5	V
Input OVP Hysteresis	V_{OVP_H}			2.5		V
EN Turn on Threshold	V_{EN_ON}	V_{EN} rising	1.0	1.1	1.2	V
EN Turn off Threshold	V_{EN-OFF}	EN falling	0.8	0.9	1.0	V
EN Hysteresis	V_{EN-HYS}			0.2		V
EN Pull Down	R_{EN}			2		MΩ
EN/SYNC Turn Off Blanking[6]	$t_{EN\_SD\_BLK}$	EN OFF to stop switching		6		µs
SYNC Input High Threshold	V_{SYNC_HI}	rising		1.7		V
SYNC Input Low Threshold	V_{SYNC_LO}	falling		0.9		V
SYNC Input Hysteresis	V_{SYNC_HYS}			0.8		V
HS FET Ron	R_{ON_HS}	I_{DS}=0.1A		180		mΩ
LS FET Ron	R_{ON_LS}	I_{DS}=0.1A		180		mΩ
Switch Leakage	SW_{LKG}	V_{EN}=0, V_{SW}=24V, T_J=25°C			1	µA
		V_{EN}=0, V_{SW}=24V, T_J=-40°C to 150°C			6	µA
Average SW capacitance	C_{SW}	V_{EN}=0, Charge SW from 0 to 24V	100	125	150	pF
FLT Output Low Threshold	V_{OL}			0.2	0.3	V

ELECTRICAL CHARACTERISTICS *(continued)*

VIN = 24V, T_J = -40°C to 150°C, typical values are at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switching Frequency Setting	f_{SW}	R_{FREQ}=33kΩ	-3%	3	+3%	MHz
		R_{FREQ}=100kΩ	-3%	1	+3%	MHz
Frequency Setting Resistor Range	R_{FREQ}		20		250	kΩ
SYNC Frequency Range			0.4		5	MHz
First Level OC Limit	I_{LIM}		-15%	1.2	+15%	A
First Level OCP Blanking(6)	t_{OCP}	MPQ18913	-20%	1	+20%	ms
		MPQ18913-A	-20%	20	+20%	ms
Short Circuit Protection Threshold	I_{SC}	Fast off limit		6		A
Hiccup Time(6)	t_{HICCUP}	MPQ18913	-20%	12	+20%	ms
		MPQ18913-A	-20%	120	+20%	
Dead-time(6)	t_D		-20%	25	+20%	ns
Soft-Start Time(6)	t_{SS}	MPQ18913		1		ms
		MPQ18913-A		20		ms
Thermal Shutdown	T_{SD}			170		°C
Thermal Shutdown Hysteresis	ΔT_{SD}			20		°C

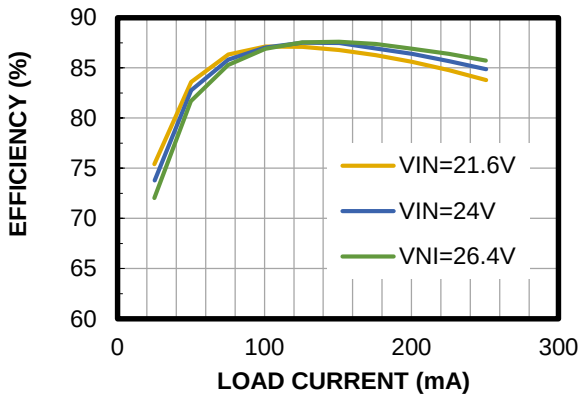
Note:

6) Derived from bench characterization, not production tested.

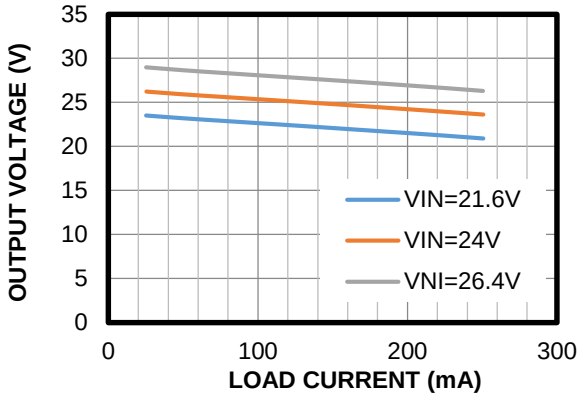
TYPICAL CHARACTERISTICS

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 24V, V_{OUT} = 24V, T_A = 25°C, unless otherwise noted.

Efficiency vs. Load Current



Line&Load Regulation vs. Load Current



TYPICAL PERFORMANCE CHARACTERISTICS

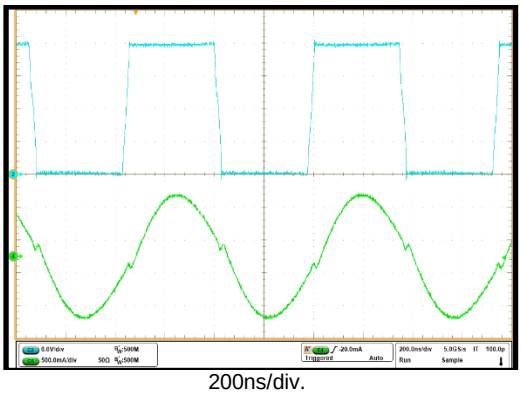
VIN = 24V, IOUT=0.25A, TA = 25°C, unless otherwise noted.

Steady State

I_{OUT} = 0.25A

CH2: SW 6V/div.

CH4: I_{PRI} 0.5A/div.



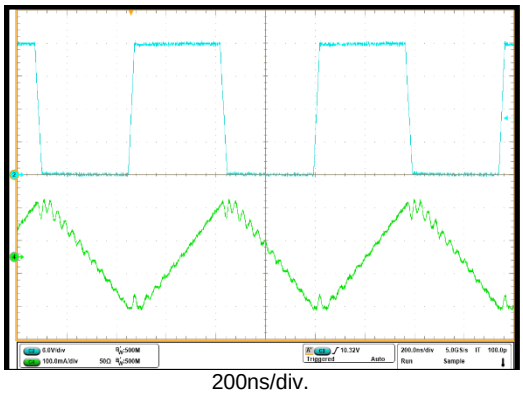
200ns/div.

Steady State

I_{OUT} = 0A

CH2: SW 6V/div.

CH4: I_{PRI} 0.1A/div.



200ns/div.

Vin Turn On

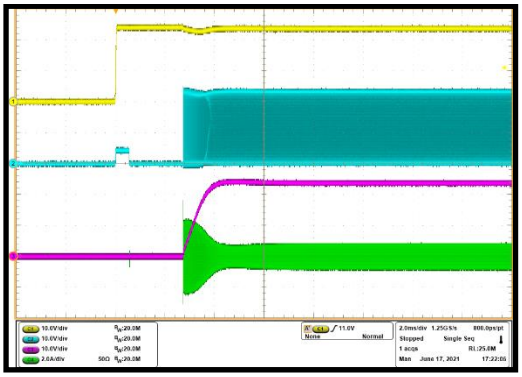
MPQ18913

CH1:V_{IN} 10V/div.

CH2: SW 10V/div.

CH3: V_{OUT} 10V/div.

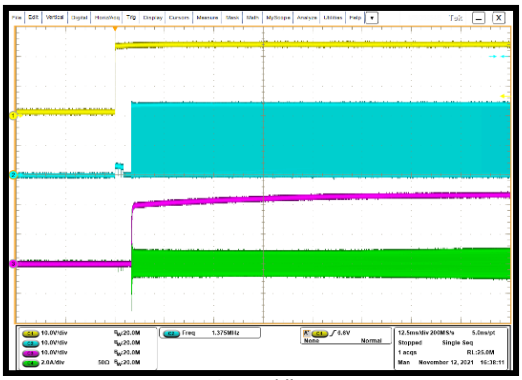
CH4: I_{PRI} 2A/div.



2ms/div.

Vin Turn On

MPQ18913A



12.5ms/div.

EN Turn On

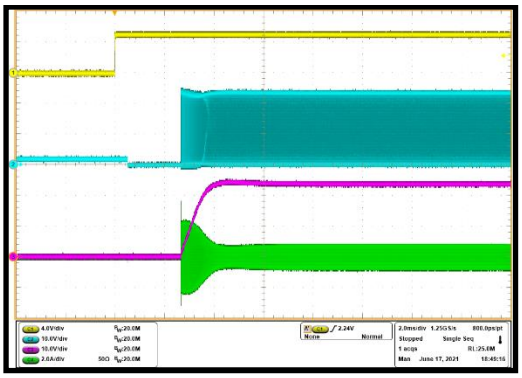
MPQ18913

CH1:EN 5V/div.

CH2: SW 10V/div.

CH3: V_{OUT} 10V/div.

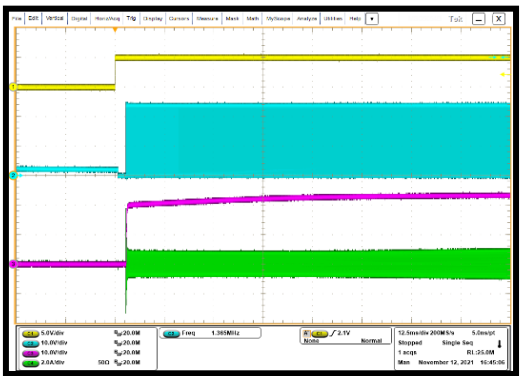
CH4: I_{PRI} 2A/div.



2ms/div.

EN Turn On

MPQ18913A



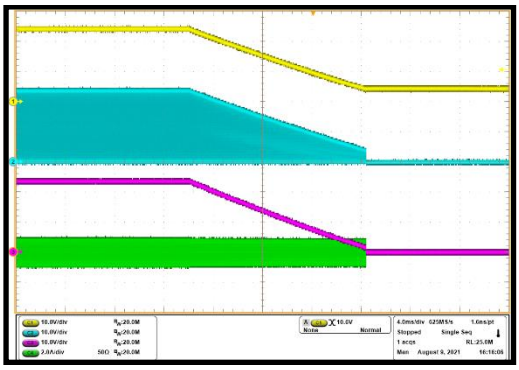
12.5ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 24V, IOUT=0.25A, TA = 25°C, unless otherwise noted.

Vin Turn Off

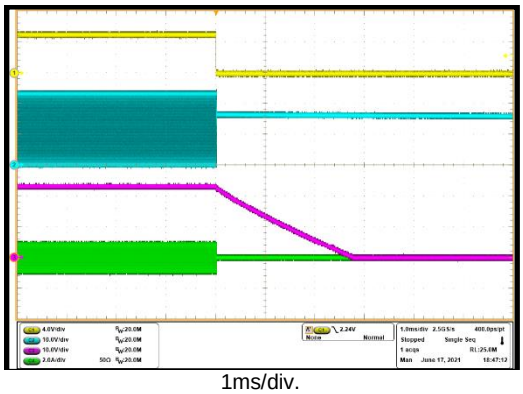
CH1:V_{IN} 10V/div.
CH2: SW 10V/div.
CH3: V_{OUT} 10V/div.
CH4: I_{PRI} 2A/div.



5ms/div.

EN Turn Off

CH1:EN 5V/div.
CH2: SW 10V/div.
CH3: V_{OUT} 10V/div.
CH4: I_{PRI} 2A/div.

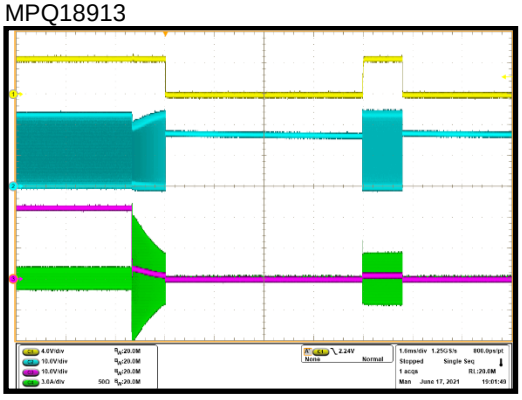


1ms/div.

Output Short

MPQ18913

CH1:FLT 4V/div.
CH2: SW 10V/div.
CH3: V_{OUT} 10V/div.
CH4: I_{PRI} 3A/div.

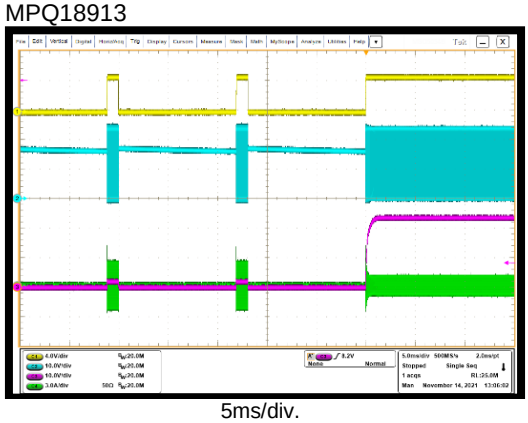


1.5ms/div.

Output Short Recovery

MPQ18913

CH1:FLT 4V/div.
CH2: SW 10V/div.
CH3: V_{OUT} 10V/div.
CH4: I_{PRI} 3A/div.



5ms/div.

FUNCTIONAL BLOCK DIAGRAM

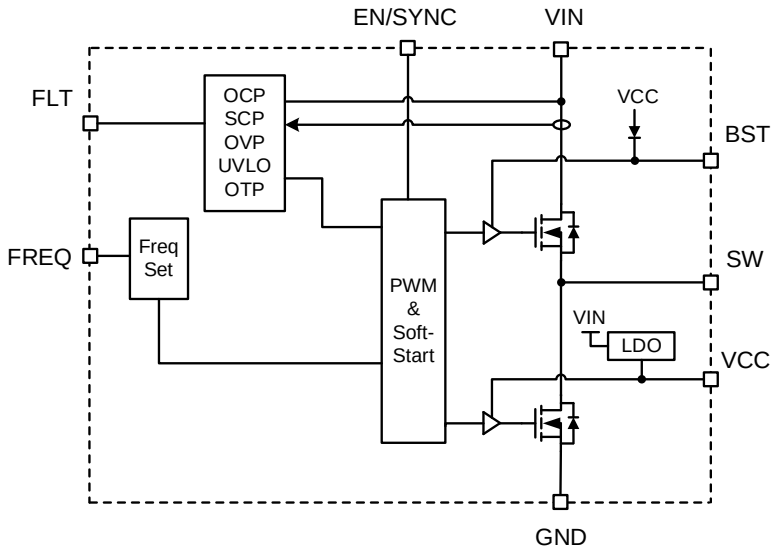


Figure 1: Functional Block Diagram

OPERATION

Enable Control (EN/SYNC)

The EN pin enables and disables the MPQ18913 power converter. When applying a voltage higher than the EN start up threshold the MPQ18913 is enabled and starts switching operation after a delay. The device is disabled when the EN voltage falls below the turn off threshold. EN pin is compatible with voltage up to 30V, for automatic startup, connect EN pin to VIN pin directly.

EN/SYNC pin can also be used for external clock synchronization. Connect a clock with a frequency between 400kHz to 1.67MHz to EN/SYNC pin, the internal clock will scale to be 1x, 3x the external clock while keep operating at 50% duty cycle. The scale factor is set by the resistance placed at the FREQ pin.

SYNC Freq Scale Factor	Output Freq. Range	Resistance at FREQ Pin
1	0.4-1.5MHz	100k
3	1.5-5MHz	33.2k

Under Voltage Lock Out

MPQ18913 implements under voltage lock out (UVLO) on VIN and VCC pins separately. the Vin UVLO rising threshold is as low as 4.9V max so it allows for a direct start-up at wide Vin range.

Note the FLT pin will always be low in VIN or VCC UVLO states.

Soft-Start of Power Converter

Upon start-up, the switching frequency starts at 2 times the set frequency in order to limit the inrush current, and then gradually decreases to the set value.

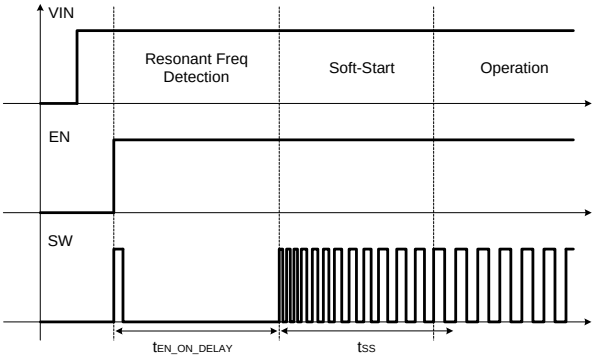


Figure 2: Timing Diagram During Start-up

Over Current & Short Circuit Protection

The MPQ18913 implements a two levels over-current protection scheme on the power converter. First level OC is implemented by measuring the instantaneous current on the low side FET. When the current rises above the OC threshold, switching frequency will increase to limit the input current. If the OC condition persists for longer than 1ms, the part will stop switching, pull low the FLT pin and auto-retries after a waiting time t_{HICCUP}. Upon auto-retry, FLT pin will be released.

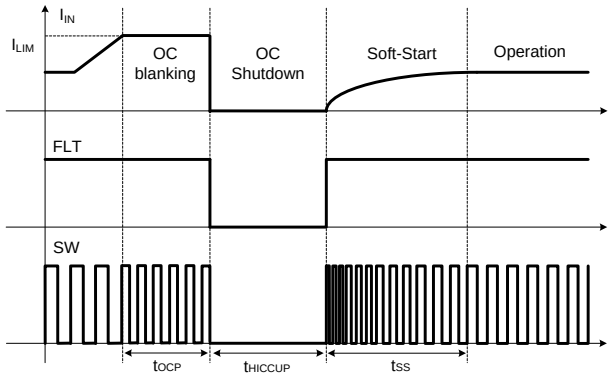


Figure 3: Timing Diagram During Over Current Event

The second level of the protection scheme (SCP) senses the instantaneous input current on high side FET. It is used to protect against the dead short from SW to GND.

Over Voltage Protection

When input voltage goes above the over voltage protection threshold, the converter immediately stops switching and pull low FLT. After the input voltage falls below the OVP threshold (with hysteresis), the part re-starts and releases FLT.

Over Temperature Protection

MPQ18913 consistently monitors the die temperature. When the die temperature goes over the thermal shutdown limit, the part stops switching and pulls low FLT. After the temperature falls back below thermal limit (with hysteresis), the part restarts and releases FLT.

FLT Reporting

FLT pin is an open-drain output. The FLT pin will be pulled low in the following conditions: Vin UVLO, Vcc UVLO, OCP hiccup/latch-off, SCP hiccup/latch-off, OVP, OTP.

Table 1: FLT Reporting Function Table(7)

EN	V_{in}	V_{cc}	FLT
X	P	P	H
X	UP	UP	L
L	P	UP	L
L	UP	P(8)	L
H	P	UP(8)	L
H	UP	P(8)	L

Note:

7) L: Logic Low; H: Logic High; X: Irrelevant; P: Powered; UP: Unpowered, UVLO condition.
8) This operation can happen only when external V_{cc} bias is applied. It is not recommended to power V_{cc} when V_{in} is unpowered, or pull EN high when V_{in} is powered but V_{cc} is unpowered.

APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Rectification Diodes

Schottky diodes are recommended to minimize power losses and help achieve ZVS of MPQ18913, because Schottky diodes feature low forward voltage drop and fast recovery.

The current rating of the diodes can be calculated with Equation (1):

$$I_{pk} \approx \pi \times I_{load} \quad (1)$$

Selecting the Output Capacitor

The output voltage ripple is determined by the value of capacitance and the gate charge of power device, e.g. SiC or IGBT. To maintain an acceptable voltage ripple, V_{ripple} , the output capacitance for the two output voltage rails can be estimated with Equation (2):

$$C_{out,\ positive\ rail} = C_{out,\ negative\ rail} \geq \frac{Q_g}{V_{ripple}} \quad (2)$$

If the capacitance of each rail needs to be larger than 22uF, MPQ18913A should be selected instead of MPQ18913 due to its longer soft start time.

Selecting the Switching Frequency

Higher switching frequency can reduce the size of transformer, but it will lead to larger transformer windings AC resistance, which limits the output power. The recommended switching frequency is as Equation (3):

$$F_{sw} = \begin{cases} \text{0.4MHz-0.75MHz, } P_{out} \leq 6W \\ \text{0.75MHz-2MHz, } P_{out} \leq 3W \\ \text{1.5MHz-5MHz, } P_{out} \leq 2W \end{cases} \quad (3)$$

To setup the switching frequency, the FREQ resistor can be calculated as

$$R_{FREQ} = \frac{100k\Omega}{F_{sw}(MHz)} \quad (4)$$

Selecting the Magnetizing Inductance of the Transformer

The design target of magnetizing inductance based on ZVS achievement can be calculated from equation (5).

$$L_m = \frac{\text{Dead Time}}{8 \times C_{SW} \times F_{SW}} = \frac{25ns}{8 \times 0.17nF \times F_{sw}} \quad (5)$$

If the magnetizing inductance is larger than the target, it does not have enough magnetizing current to achieve full ZVS. With the low input voltage and small parasitic capacitance on the switcher, partial ZVS will not raise concerns in thermal or electrical stress. If the magnetizing inductance is smaller than the design target, it will lead to more magnetizing current than needed, which results in extra conduction loss. Given the small $R_{ds,on}$ and a reasonable ACR of transformer, the conduction loss will not raise thermal concerns as well.

It is recommended that the magnetizing inductance be more than 10 times larger than leakage inductance, in order to decrease the output voltage's sensitivity to the tolerance of inductance and resonant capacitance.

Selecting the Resonant Capacitor

The value of resonant capacitor can be calculated with equation (6):

$$C_r = \frac{1}{4 \times \pi^2 \times L_r \times F_{sw}^2} \quad (6)$$

Where the L_r is the leakage inductance of the transformer, reflected to the primary side.

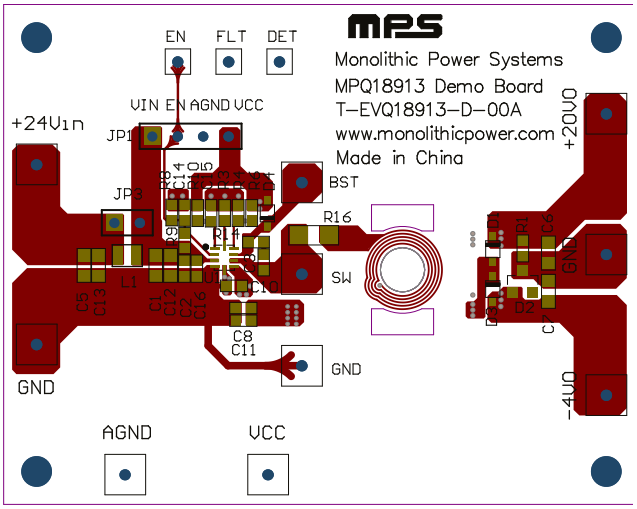
PCB LAYOUT GUIDELINES[9]

Efficient PCB layout is critical for standard operation and EMI performance. For the best results, refer to Figure 4 and follow the guidelines below:

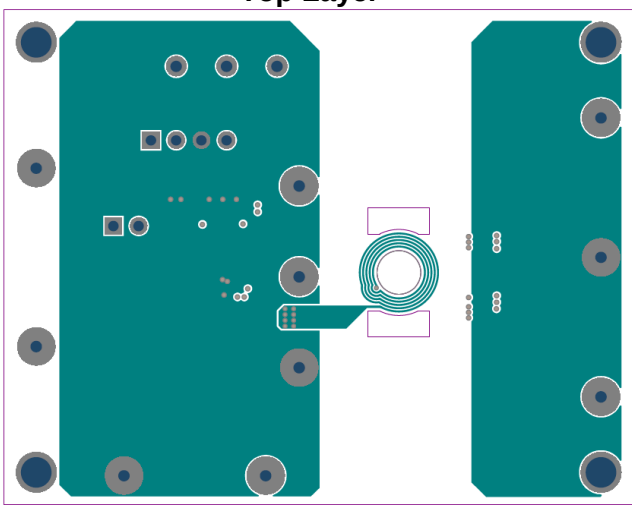
1. Place the input capacitor, Vcc capacitor and BST capacitor as close to the corresponding pins as possible
2. Place the FREQ resistor as close to the FREQ pin as possible. Use short and direct trace to connect the resistor to FREQ pin. The other terminal of FREQ resistor should be connected to AGND.
3. Connect AGND to power GND through single point connection.
4. Minimize the area of switch nodes on both primary side and secondary side to reduce EMI emission.
5. Place the input filter at the bottom layer to improve EMI performance.

Note:

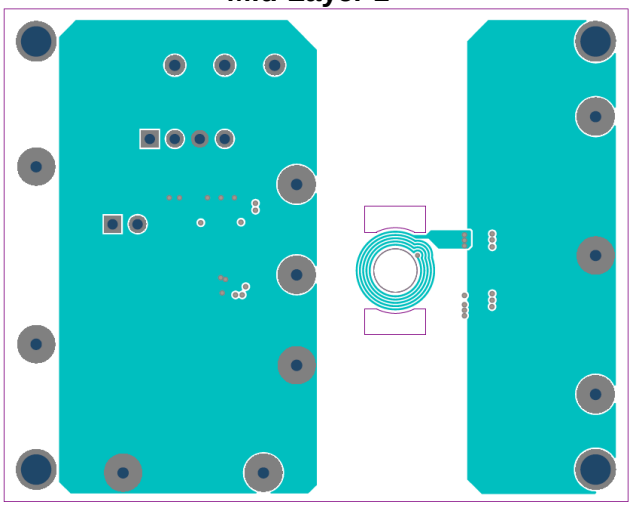
9) The recommended layout is based on the typical application circuit (see Figure 5).



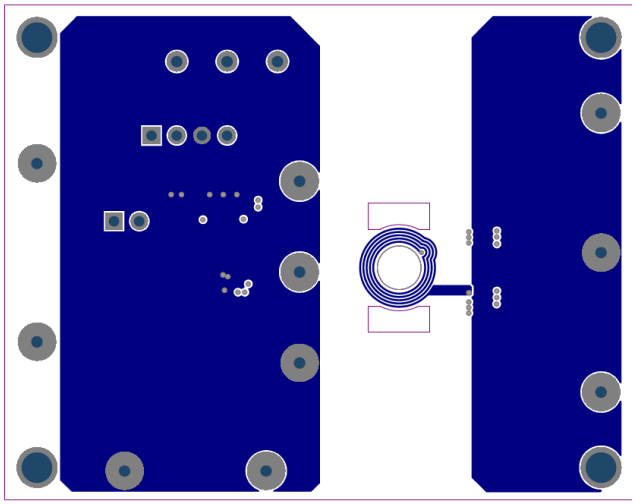
Top Layer



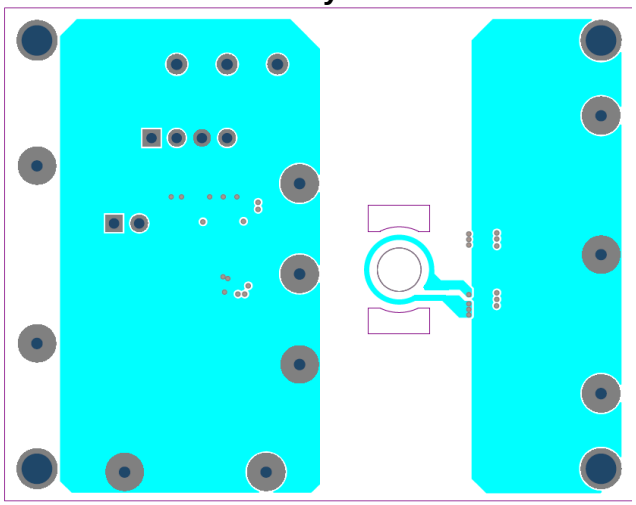
Mid-Layer 1



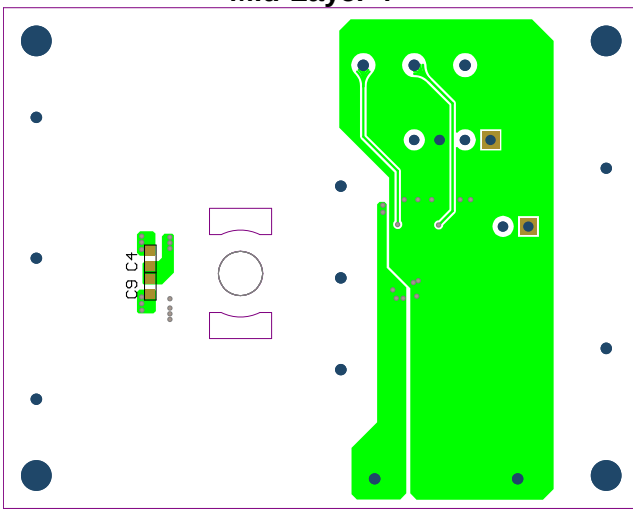
Mid-Layer 2



Mid-Layer 3



Mid-Layer 4



Bottom Layer

Figure 4: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

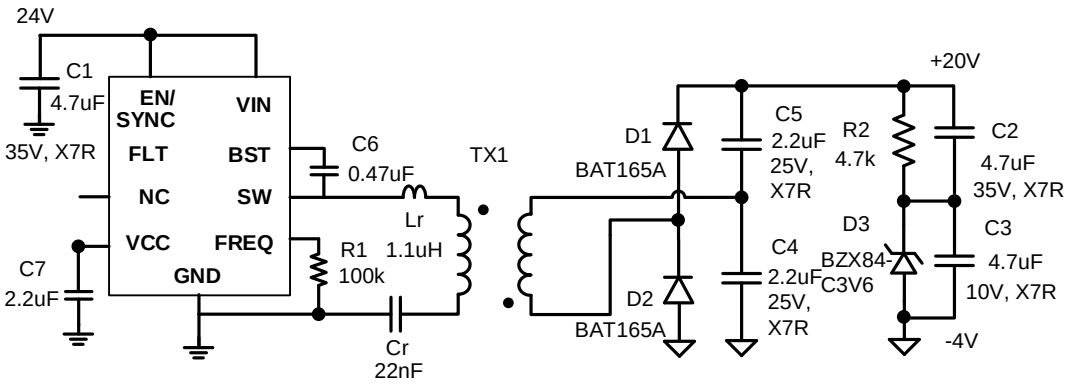
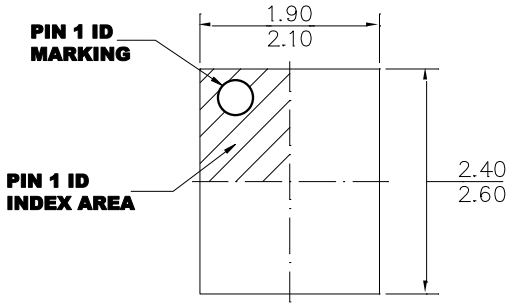


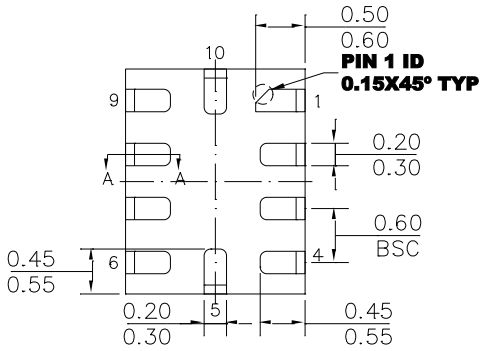
Figure 5: VIN=24V, VOUT=+20V/-4V, 6W LLC with Input Voltage Start Up

PACKAGE INFORMATION

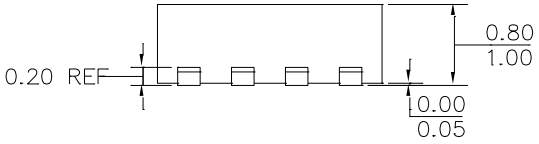
QFN-10 (2mmx2.5mm)



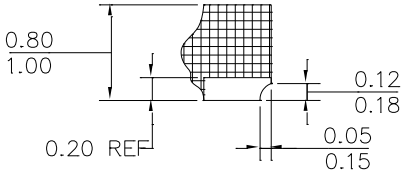
TOP VIEW



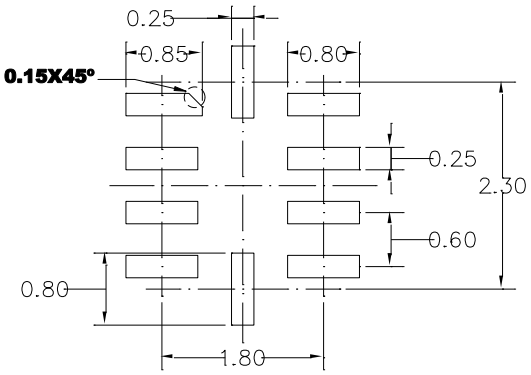
BOTTOM VIEW



SIDE VIEW



SECTION A-A

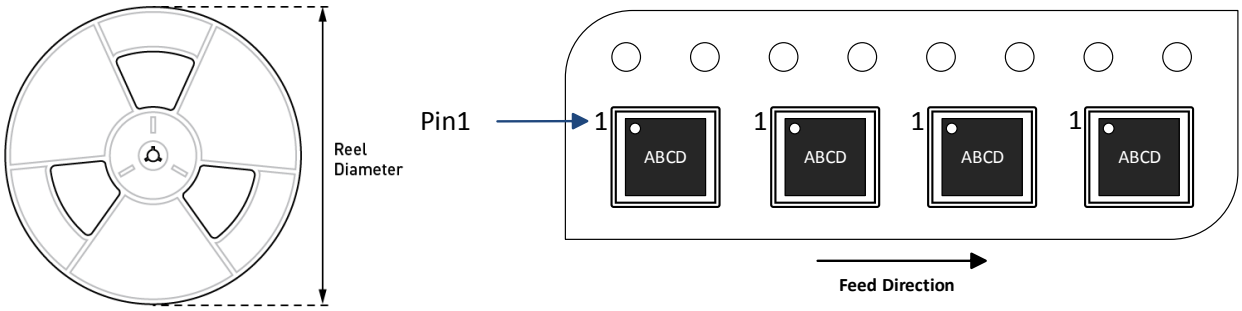


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/Tube	Quantity/Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ18913GRPE-AEC1	QFN-10 (2mmx2.5mm)	5000	N/A	N/A	13 in.	12 mm	8 mm
MPQ18913GRPE-A-AEC1							