MP18871

Isolated PWM-Input Control High-Side/Low-Side Half-Bridge Gate Driver

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MP18871 is an isolated half-bridge gate driver solution with up to 4A source and sink peak current capacity. The gate driver is designed to drive power switching devices with short propagation delay and pulse-width distortion. By utilizing MPS proprietary capacitive-based isolation technology, the driver can provide up to $5kV_{RMS}$ withstand voltage (per UL1577) with SOIC wide-body package and greater than 100kV/μs common-mode transient immunity (CMTI) rating between the input side and output driver. With the advanced features, the drivers operate high efficiency, high power density, and robustness in a wide variety of power applications.

The MP18871 integrates dual-channel gate drivers in one package. Each output can be grounded to the separated grounds or connected to a positive or negative voltage reference. The secondary topology can be configured as a half-bridge high-side/low-side driver controlled by single PWM input signal. To prevent the occurrence of the shoot-through issue in half-bridge driver, the MP18871 provides the programmable dead-time set by an external resister.

A wide primary-side VDDI supply range makes the driver suitable to be interfaced with 3.3V or 5V digital controllers. And the secondary-side driver accepts up to 30V supply. All the supply voltage pins are with various under voltage lock-out (UVLO) level protection.

The MP18871 is available in narrow-/wide-body SOIC-16 and LGA-13 5mmx5mm packages.

FEATURES

- PWM-Input Half-Bridge Driver
- Up to $5kV_{RMS}$ Input to Output Isolation (SOIC-16 WB)
- $1500V_{DC}$ Functional Isolation between Two Secondary-Side Drivers (SOIC-16 NB/WB)
- $700V_{DC}$ Functional Isolation between Two Secondary-Side Drivers (LGA-13 5mmx5mm)
- Common-Mode Transient Immunity (CMTI) >100kV/μs
- 2.8V to 5.5V Input VDDI Range to Interface with TTL and CMOS Compatible Inputs
- Up to 30V Output Drive Supply with Several UVLO Options
- 4A Source, 4A Sink Peak Current Output
- 50ns Typical Propagation Delay
- Overlap Protection and Programmable Dead-time Control
- Operating Temperature Range -40°C to +125°C
- UL 1577 Certified
  - SOIC-16 NB: $3kV_{RMS}$ Isolation for 60 secs.
  - SOIC-16 WB: $5kV_{RMS}$ Isolation for 60 secs.
  - LGA-13: $2.5kV_{RMS}$ Isolation for 60 secs.

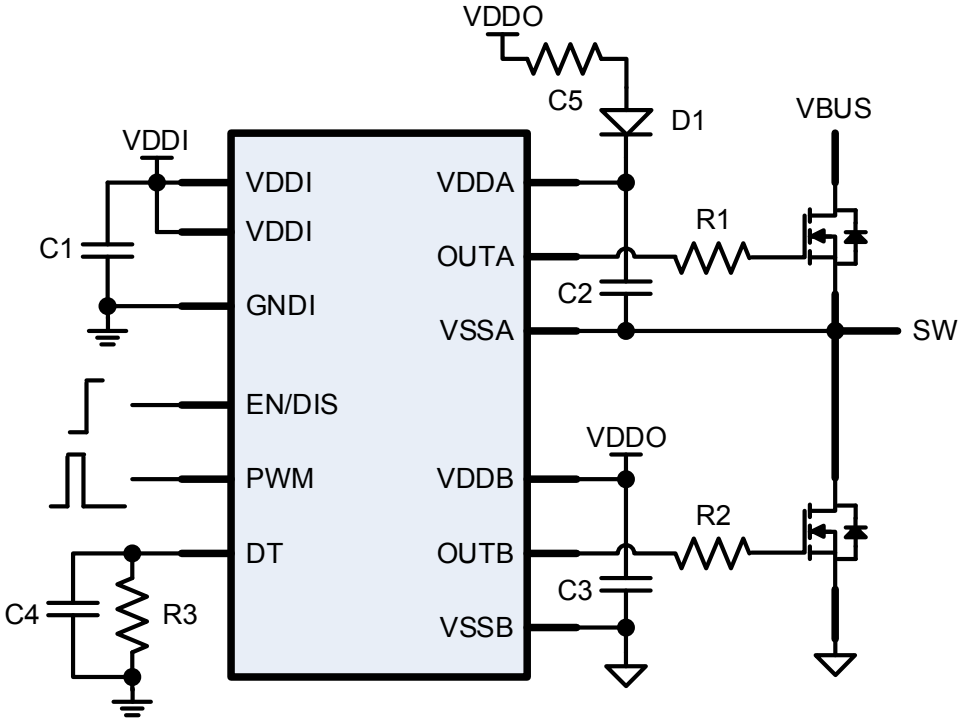
APPLICATIONS

- Half/Full-Bridge Converters
- Isolated DC/DC Converters
- Offline Isolated AC/DC Converters
- DC/AC Inverters

SELECTION GUIDE

Part Number	Peak Output Current (A)	Output UVLO (V)	On/Off Logic	Input Logic	Configura -tion	Overlap Protection	Programm -able Dead-Time	Package Type
MP18871-4A	4	3	EN	PWM	High-Side /Low-Side Half-Bridge	Y	Y	SOIC-16 NB SOIC-16 WB LGA-13 (5mmx5mm)
MP18871-4B		5						
MP18871-4C		8						
MP18871-4D		10						
MP18871-4E		12						
MP18871-A4A	4	3	DIS	PWM	High-Side /Low-Side Half-Bridge	Y	Y	SOIC-16 NB SOIC-16 WB LGA-13 (5mmx5mm)
MP18871-A4B		5						
MP18871-A4C		8						
MP18871-A4D		10						
MP18871-A4E		12						

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP18871-4AGSE	SOIC-16 NB	*See Below*	2
MP18871-4BGSE			
MP18871-4CGSE			
MP18871-4DGSE			
MP18871-4EGSE			
MP18871-4AGY	SOIC-16 WB		3
MP18871-4BGY			
MP18871-4CGY			
MP18871-4DGY			
MP18871-4EGY			
MP18871-4AGLU	LGA-13 (5mmx5mm)		
MP18871-4BGLU			
MP18871-4CGLU			
MP18871-4DGLU			
MP18871-4EGLU			
MP18871-A4AGSE	SOIC-16 NB		2
MP18871-A4BGSE			
MP18871-A4CGSE			
MP18871-A4DGSE			
MP18871-A4EGSE			
MP18871-A4AGY	SOIC-16 WB		3
MP18871-A4BGY			
MP18871-A4CGY			
MP18871-A4DGY			
MP18871-A4EGY			
MP18871-A4AGLU	LGA-13 (5mmx5mm)		
MP18871-A4BGLU			
MP18871-A4CGLU			
MP18871-A4DGLU			
MP18871-A4EGLU			

* For Tape & Reel, add suffix -Z (e.g. MP18871-4AGSE-Z / MP18871-4AGY-Z / MP18871-4AGLU-Z)

Please contact local sales or our distributors to check the latest availability status for the ordering part numbers.

TOP MARKING

MP18871-4X (SOIC-16 NB & SOIC-16 WB)

MPS YYWW

M18871-4X

LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
M18871-4X: Part number
X: UVLO level code, where X=A, B, C, D or E
LLLLLLLLL: Lot number

TOP MARKING

MP18871-A4X (SOIC-16 NB & SOIC-16 WB)

MPS YYWW

18871-A4X

LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
18871-A4X: Part number
X: UVLO level code, where X=A, B, C, D or E
LLLLLLLLL: Lot number

TOP MARKING

MP18871-4X (LGA-13 5mmx5mm)

MPSYYWW
MP18871
LLLLLLL
4X

MPS: MPS prefix
YY: Year code
WW: Week code
MP18871: Part number
LLLLLLL: Lot number
4X: The rest alphanumeric characters of part number
X: UVLO level code, where X=A, B, C, D or E

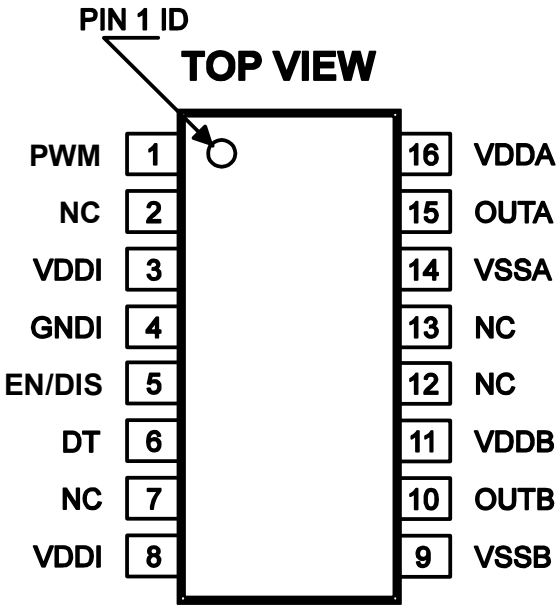
TOP MARKING

MP18871-A4X (LGA-13 5mmx5mm)

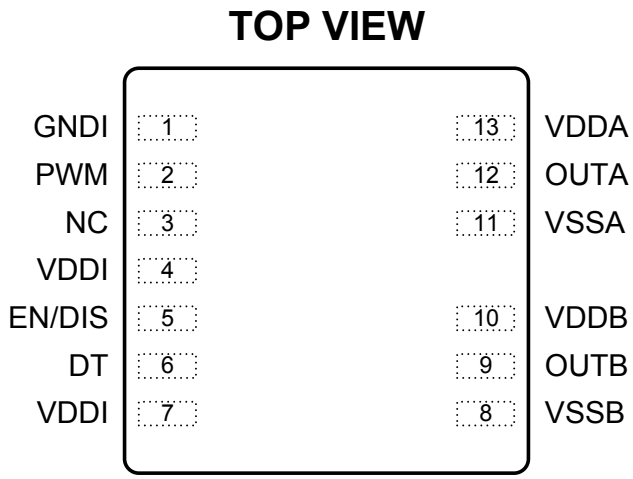
MPSYYWW
MP18871
LLLLLLL
A4X

MPS: MPS prefix
YY: Year code
WW: Week code
MP18871: Part number
LLLLLLL: Lot number
A4X: The rest alphanumeric characters of part number
X: UVLO level code, where X=A, B, C, D or E

PACKAGE REFERENCE



SOIC-16 NB/SOIC-16 WB



LGA-13 (5mmx5mm)

PIN FUNCTIONS

Pin #		Name	Description
SOIC-16	LGA-13		
1	2	PWM	**PWM Logic Control Signal Input.** PWM pin can accept a TTL/CMOS level compatible input logic. This pin is internally pulled down to GNDI. OUTA is in phase with PWM input and OUTB is always complementary with OUTA with a programmed dead-time.
3,8	4,7	VDDI	**Input-Side Power Supply Input.** These two pins are internally shorted. VDDI supplies power to the primary side control circuitry. Locally decoupled to GNDI using a low ESR/ESL bypass capacitor. The capacitor should be placed as close to the chip as possible.
4	1	GNDI	**Input-Side Ground.** Ground reference for all input-side signal and internal control blocks.
5	5	EN	**Enable Control Input.** EN pin can be driven by an external TTL/CMOS level compatible input logic signal to enable/disable the chip. This pin is internally pulled high. Turn on the chip if set high or left open, shutdown the driver output if pulled low.
5	5	DIS	**Disable Control Input.** DIS pin can be driven by an external TTL/CMOS level compatible input logic signal to enable/disable the chip. This pin is internally pulled low. Turn on the chip if set low or left open, shutdown the driver output if pulled high.
6	6	DT	**Dead-Time Programming Input.** Leaving DT open sets the dead time to the minimal value. Tie a 2kΩ to 150kΩ resistor between DT and GNDI to program the dead-time. It is recommended to parallel a 220pF or above ceramic capacitor with this resister for improved noise immunity.
2,7,12,13	3	NC	**No Connection.**
9	8	VSSB	**Output-Side Ground for Driver B.** Ground reference for output driver B.
10	9	OUTB	**Gate Drive Output of Driver B.** Connect to the gate of power device in channel B.
11	10	VDDB	**Output-Side Driver Power Supply Input for Driver B.** This pin supplies power to the secondary side driver B circuitry. Locally decoupled to VSSB using a low ESR/ESL bypass capacitor. The capacitor should be placed as close to the chip as possible.
14	11	VSSA	**Output-Side Ground for Driver A.** Ground reference for output driver A.
15	12	OUTA	**Gate Drive Output of Driver A.** Connect to the gate of power device in channel A.
16	13	VDDA	**Output-Side Driver Power Supply Input for Driver A.** This pin supplies power to the secondary side driver A circuitry. Locally decoupled to VSSA using a low ESR/ESL bypass capacitor. The capacitor should be placed as close to the chip as possible.

ABSOLUTE MAXIMUM RATINGS (1)

VDDI-GNDI ..... -0.3V to 6.5V
V_{PWM}, $V_{EN/DIS}$, V_{DT}
..... (GNDI-0.3V) to (VDDI+0.3V)
V_{PWM}, $V_{EN/DIS}$ Transient for 50ns
..... (GNDI-5.0V) to (VDDI+0.3V)
VDDA-VSSA, VDDB-VSSB ..... -0.3V to 35V
V_{OUTA}..... (VSSA-0.3V) to (VDDA+0.3V)
V_{OUTA} Transient for 200ns
..... (VSSA-2.0V) to (VDDA+0.3V)
V_{OUTB}..... (VSSB-0.3V) to (VDDB+0.3V)
V_{OUTB} Transient for 200ns
..... (VSSB-2.0V) to (VDDB+0.3V)
VSSA-VSSB
SOIC-16 NB/WB .....-1500V to +1500V
LGA-13 (5mmx5mm) .....-700V to +700V
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC-16 WB 2215mW
SOIC-16 NB 2115mW
LGA-13 (5mmx5mm) 1175mW
Junction Temperature..... 150°C
Lead Temperature ..... 260°C
Storage Temperature.....-65°C to +150°C

ESD Ratings

Human body model (HBM) 4kV
Charged device model (CDM)..... 2kV

Recommended Operating Conditions (3)

VDDI-GNDI ..... 2.8V to 5.5V
V_{PWM}, $V_{EN/DIS}$ ..... GNDI to VDDI
VDDA-VSSA, VDDB-VSSB
..... 4.2V to 30V (3V UVLO rev.)
..... 6.5V to 30V (5V UVLO rev.)
..... 9.2V to 30V (8V UVLO rev.)
..... 12V to 30V (10V UVLO rev.)
..... 14.5V to 30V (12V UVLO rev.)
Operating Junction Temp. (T_J) .-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC-16 WB ..... 56 ..... 30 ... °C/W
SOIC-16 NB ..... 59 ..... 35 ... °C/W
LGA-13 (5mmx5mm) ..... 106 ..... 50 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on MP18871 evaluation board, 2 layer PCB.

ELECTRICAL CHARACTERISTICS

2.8V ≤ VDDI-GNDI ≤ 5.5V, VDDA-VSSA = VDDB-VSSB = 5V/12V/15V (5), T_J = -40°C to +125°C, typical value is tested at T_J = +25°C, all voltages with respect to the corresponding grounds, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Side Supply Voltage						
VDDI Under-Voltage Lockout Threshold	$VDDI_{UVLO}$	(VDDI-GNDI) falling	2.42	2.6	2.78	V
VDDI Under-Voltage Lockout Hysteresis	$VDDI_{UVLO\_HYS}$		110	135	160	mV
Input Side Supply Current						
VDDI Shutdown Current	I_{VDDI_SD}	V_{EN}=GNDI or V_{DIS}=VDDI		1.0	1.3	mA
VDDI Operation Current	I_{VDDI}	f=500kHz, 50% duty, C_{LOAD}=100pF		2.0	2.8	mA
Logic Input (PWM, EN/DISABLE)						
Logic Input High Threshold	V_{LI_H}	(V_{LI}-GNDI) rising		1.6	1.8	V
Logic Input Low Threshold	V_{LI_L}	(V_{LI}-GNDI) falling	1.0	1.2		V
Logic Input Hysteresis Voltage	V_{LI_HYS}		360	400	440	mV
Internal Pull-Up Resistance	R_{LI_PU}	EN		200		kΩ
Internal Pull-Down Resistance	R_{LI_PD}	PWM, DIS		200		kΩ
Output Side Supply Voltage						
VDDA/VDDB Under-Voltage Lockout Threshold (VDDA-VSSA)/(VDDB-VSSB) falling	$VDDA_{UVLO}$ $VDDB_{UVLO}$	-A, 3V threshold	2.7	3.2	3.7	V
		-B, 5V threshold	5	5.5	6	V
		-C, 8V threshold	7.5	8	8.5	V
		-D, 10V threshold	9.3	10	10.7	V
		-E, 12V threshold	11	12	13	V
VDDA/VDDB Under-Voltage Lockout Hysteresis	$VDDA_{UVLO\_HYS}$ $VDDB_{UVLO\_HYS}$	-A/-B, 3V/5V threshold	200	300	400	mV
		-C, 8V threshold	420	520	620	mV
		-D/-E, 10V/12V threshold	0.8	1	1.2	V
Output Side Supply Current						
VDDA/VDDB Shutdown Current	I_{VDDA_SD} I_{VDDB_SD}	V_{EN}=GNDI or V_{DIS}=VDDI		1.0	1.3	mA
VDDA/VDDB Quiescent Current (current per channel)	I_{VDDA_Q} I_{VDDB_Q}	V_{EN}=VDDI or V_{DIS}=GNDI, Set PWM to turn off the corresponding channel		1.0	1.3	mA
VDDA/VDDB Operation Current (current per channel)	I_{VDDA} I_{VDDB}	f=500kHz, C_{LOAD}=100pF, VDDA/VDDB=12V		2.5	3.0	mA
		f=500kHz, C_{LOAD}=100pF, VDDA/VDDB=15V		3.0	4.6	mA

ELECTRICAL CHARACTERISTICS *(continued)*

2.8V ≤ VDDI-GNDI ≤ 5.5V, VDDA-VSSA = VDDB-VSSB = 5V/12V/15V (5), T_J = -40°C to +125°C, typical value is tested at T_J = +25°C, all voltages with respect to the corresponding grounds, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Gate Driver						
Logic High Output Voltage	V_{OUTA_H} V_{OUTB_H}	$I_{OUTA/OUTB}$=-10mA	VDDA/ VDDB -0.03	VDDA/ VDDB -0.01		V
Logic Low Output Voltage	V_{OUTA_L} V_{OUTB_L}	$I_{OUTA/OUTB}$=10mA		VSSA/ VSSB +0.01	VSSA/ VSSB +0.03	V
Output Peak Source Current (6)	I_{OUTA_SRC} I_{OUTB_SRC}	VDDA-VSSA=VDDB-VSSB=15V, $V_{OUTA/OUTB}$-VSSA/VSSB =5V (5V miller plateau) f=1kHz		-4		A
Output Peak Sink Current (6)	I_{OUTA_SNK} I_{OUTB_SNK}	VDDA-VSSA=VDDB-VSSB=15V, $V_{OUTA/OUTB}$-VSSA/VSSB =5V (5V miller plateau) f=1kHz		4		A
Output Source Resistance	R_{OUTA_H} R_{OUTB_H}	$I_{OUTA/OUTB}$=-10mA		1.3	2.5	Ω
Output Sink Resistance	R_{OUTA_L} R_{OUTB_L}	$I_{OUTA/OUTB}$=10mA		1.0	2.0	Ω
Dead-time and Overlap Protection						
Dead-Time	t_{DT}	Leave DT open, (minimum dead-time)		10	30	ns
		R_{DT}=20kΩ	130	190	250	ns
		R_{DT}=100kΩ	700	900	1100	ns
Dead-Time Matching $\lvert t_{DTAB}-t_{DTBA}\rvert$	t_{DTM}			0	10	ns
Bias Voltage for Dead-Time Set	V_{DT}	R_{DT}=20kΩ	0.6	0.65	0.7	V
DT Resistance Range	R_{DT}		2		150	kΩ
Switching (Refer to the time sequence diagram for details)						
Output Rise Time	t_R	($V_{OUTA/OUTB}$-VSSA/VSSB) rising, C_{LOAD}=1.8nF		10	20	ns
Output Fall Time	t_F	($V_{OUTA/OUTB}$-VSSA/VSSB) falling C_{LOAD}=1.8nF		10	20	ns
Minimum Pulse Width	t_{PW_MIN}	Output pulse off if shorter than t_{PW_MIN}, C_{LOAD}=0pF		23	35	ns
Propagation Delay from PWM to OUTA/OUTB Rising Edge	t_{PDLH}	V_{EN}=VDDI or V_{DIS}=GNDI, C_{LOAD}=0pF	35	50	65	ns
Propagation Delay from PWM to OUTA/OUTB Falling Edge	t_{PDHL}	V_{EN}=VDDI or V_{DIS}=GNDI, C_{LOAD}=0pF	35	50	65	ns

ELECTRICAL CHARACTERISTICS *(continued)*

2.8V ≤ VDDI-GNDI ≤ 5.5V, VDDA-VSSA = VDDB-VSSB = 5V/12V/15V (5), T_J = -40°C to +125°C, typical value is tested at T_J = +25°C, all voltages with respect to the corresponding grounds, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Switching (Refer to the time sequence diagram for details)						
Propagation Delay from Enable True to OUTA/OUTB Rising Edge	t_{PDEN}	Set OUTA/OUTB outputs high, C_{LOAD}=0pF	35	50	65	ns
Propagation Delay from Disable True to OUTA/OUTB Falling Edge	t_{PDDIS}	Set OUTA/OUTB outputs high, C_{LOAD}=0pF	35	50	65	ns
Pulse Width Distortion $\|t_{PDLH}-t_{PDHL}\|$	t_{PWD}	C_{LOAD}=0pF		1	6	ns
Propagation Delay Matching (Channel-to-Channel)	t_{PDM}	C_{LOAD}=0pF		1	6	ns
Startup Delay from Input Supply UVLO Exit to Output Rising Edge	t_{STU_VDDI}	V_{EN}=VDDI or V_{DIS}=GNDI, Set OUTA/OUTB outputs high, C_{LOAD}=0pF	15	25	35	µs
Shutdown Delay from Input Supply UVLO Entry to Output Falling Edge(7)	t_{SHD_VDDI}	V_{EN}=VDDI or V_{DIS}=GNDI, Set OUTA/OUTB outputs high, C_{LOAD}=0pF		500		ns
Startup Delay from Output Supply UVLO Exit to Output Rising Edge	t_{STU_VDDA} t_{STU_VDDB}	V_{EN}=VDDI or V_{DIS}=GNDI, Set OUTA/OUTB outputs high, C_{LOAD}=0pF	10	20	30	µs
Shutdown Delay from Output Supply UVLO Entry to Output Falling Edge(7)	t_{SHD_VDDA} t_{SHD_VDDB}	V_{EN}=VDDI or V_{DIS}=GNDI, Set OUTA/OUTB outputs high, C_{LOAD}=0pF		500		ns
Static Common-Mode Transient Immunity (6)	$CMTI_{STC}$	V_{EN}=VDDI or V_{DIS}=GNDI, V_{PWM}=GNDI or VDDI, slew rate of GNDI versus VSSA/VSSB, V_{CM}=1500V	100			kV/µs
Dynamic Common-Mode Transient Immunity (6)	$CMTI_{DYN}$	V_{EN}=VDDI or V_{DIS}=GNDI, f=100kHz pulse at PWM, slew rate of GNDI versus VSSA/VSSB, V_{CM}=1500V	100			kV/µs

NOTES:

5) For the test condition, VDDA-VSSA=VDDB-VSSB=5V is used for 3V UVLO devices; VDDA-VSSA=VDDB-VSSB =12V is used for 5V and 8V UVLO devices; VDDA-VSSA=VDDB-VSSB =15V is used for 10V and 12V UVLO devices.
6) Guaranteed by characterization, not production tested.
7) Guaranteed by design.

INSULATION & SAFETY-RELATED SPECIFICATIONS

Parameters	Symbol	Condition	SOIC-16 WB	SOIC-16 NB	LGA-13 5x5	Units
External Air Gap (Clearance) (8)	CLR	Shortest pin-to-pin distance through air between primary and secondary side	>8	>4	3.5	mm
External Tracking (Creepage) (8)	CPG	Shortest pin-to-pin distance across the package surface between primary and secondary side	>8	>4	3.5	mm
Distance Through Insulation	DTI	Internal Clearance	>20	>20	>20	μm
Comparative Tracking Index	CTI	According to IEC60112	>600	>600	>600	V
Material Group		According to IEC 60664-1	I	I	I	
Overvoltage Category per IEC 60664-1		Rated mains voltages ≤ 150V_{RMS}	I-IV	I-IV	I-IV	
		Rated mains voltages ≤ 300V_{RMS}	I-IV	I-III	I-III	
		Rated mains voltages ≤ 600V_{RMS}	I-III	I-II	--	
UL 1577, 5th Ed						
Recognized under UL 1577 Component Recognition Program, Single Protection. File number: E322138						
Dielectric Withstand Insulation Voltage	V_{ISO}	V_{TEST}=V_{ISO} for t=60 sec. (qualification), V_{TEST}=1.2 x V_{ISO} for t=1 sec. (100% production)	5000	3000	2500	V_{RMS}
DIN V VDE V 0884-11: 2017-01						
Certified according to DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01. Certification number: pending						
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	AC voltage (bipolar)	891	560	560	V_{PK}
Maximum Working Isolation Voltage	V_{IOWM}	AC voltage (sine wave)	630	400	400	V_{RMS}
		DC voltage	891	560	560	V_{DC}
Maximum Transient Isolation Voltage	V_{IOTM}	V_{TEST}=V_{IOTM} for t=60 sec (qualification); V_{TEST}=1.2 x V_{IOTM} for t=1 sec (100% production)	7071	4242	3535	V_{PK}
Apparent Charge (9) Measuring Voltage	$V_{pd(m)}$	Method b1, at routine test (100% production). $V_{pd(ini)}$=1.2 x V_{IOTM}, t_{ini}=1 sec; $V_{pd(m)}$=1.875 x V_{IORM}, t_m=1 sec; partial discharge<5 pC	1697	1061	1061	V_{PK}
Maximum Surge Isolation Voltage (10)	V_{IOSM}	Tested per IEC 62368-1 with 1.2/50μs pulse, V_{TEST}=1.3 x V_{IOSM} (qualification)	4000	4000	3500	V_{PK}
Barrier Capacitance (11)	C_{IO}	f=1MHz	~1	~1	~1	pF
Insulation Resistance (11)	R_{IO}	V_{IO}=500V, T_A=25°C	>10^{12}			Ω
		V_{IO}=500V, 100°C≤T_A≤125°C	>10^{11}			Ω
		V_{IO}=500V, T_A=T_S=150°C	>10^9			Ω
Pollution Degree		per DIN VDE 0110, Table 1	2			
Climatic Category			40/125/21			

NOTES:
8) Refer to package information for detailed dimensions. As isolated solution, the recommended land pattern is helpful to keep enough safety creepage and clearance distances on a printed-circuit board.
9) Electrical discharge caused by a partial discharge in the coupler.
10) Surge test is carried out in oil.
11) The primary side terminals as well as the secondary side terminals of the barrier are connected together forming a two-terminal device. Then C_{IO} and R_{IO} are measured between the two terminals of the coupler.

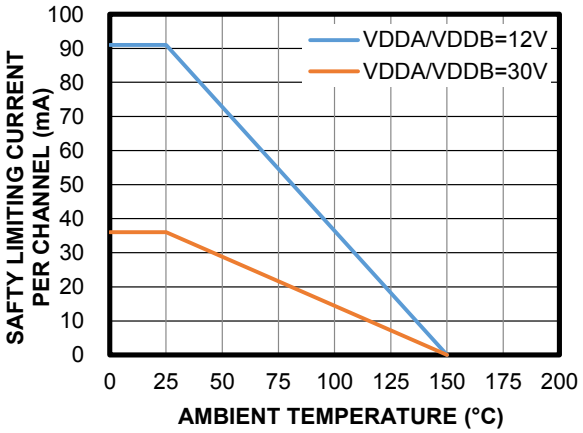
SAFETY LIMITING VALUES (12)

Parameters	Symbol	Condition	SOIC-16 WB	SOIC-16 NB	LGA-13 5x5	Units
Maximum Safety Temperature (13)	T_S		150	150	150	°C
Maximum Output Safety Current (current per channel)	I_{S_O}	VDDA-VSSA=VDDB-VSSB =12V (14), T_J=150°C, T_A=25°C	91	87	48	mA
		VDDA-VSSA=VDDB-VSSB=30V, T_J=150°C, T_A=25°C	36	35	19	mA
Safety Power Dissipation (15)	P_S	Input side	15	15	15	mW
		Output side, channel A	1100	1050	580	mW
		Output side, channel B	1100	1050	580	mW
		Total	2215	2115	1175	mW

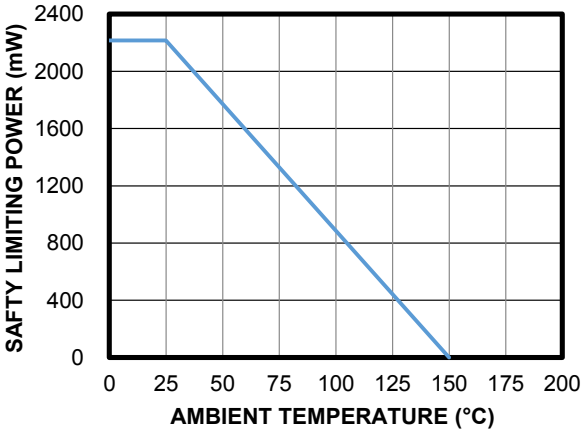
NOTES:
12) Maximum value allowed in the event of a failure.
13) The maximum safety temperature T_S has the same value as the maximum junction temperature T_J (MAX) specified in ABSOLUTE MAXIMUM RATINGS.
14) Tested for 5V and 8V UVLO devices
15) Test condition: VDDI-GNDI=5.5V, VDDA-VSSA=VDDB-VSSB=30V, T_J=150°C, T_A=25°C.
The safety power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A :
$T_S=T_J(MAX)=T_A+(\theta_{JA} \times P_S)$,
$P_S=I_S \times V_I$, where V_I is the input voltage

THERMAL DERATING CURVE FOR SAFETY LIMITING VALUES

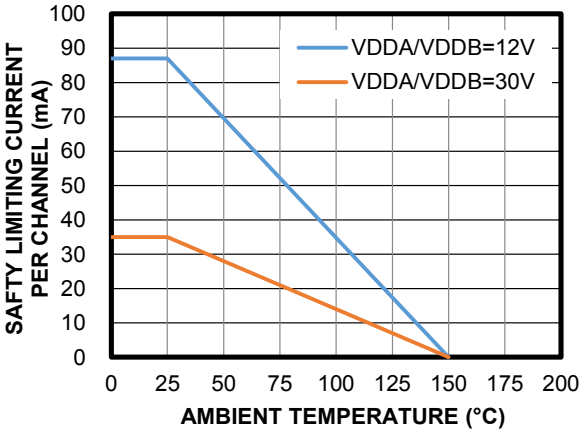
Thermal Derating Curve for Safety Limiting Current
SOIC-16 WB



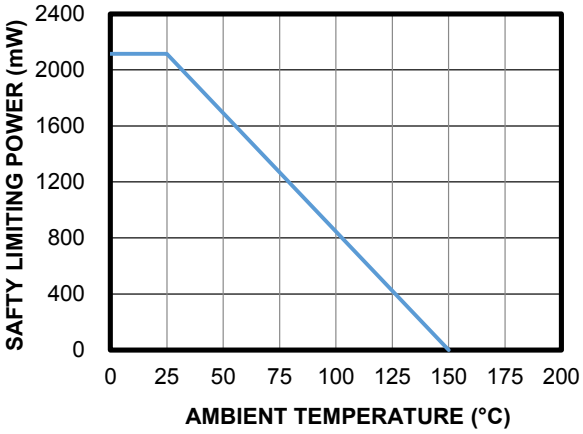
Thermal Derating Curve for Safety Limiting Power
SOIC-16 WB



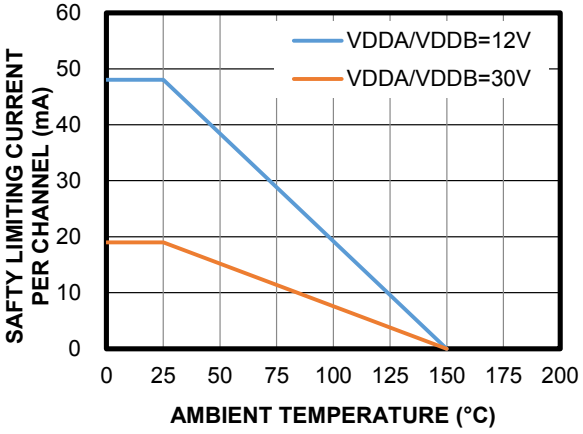
Thermal Derating Curve for Safety Limiting Current
SOIC-16 NB



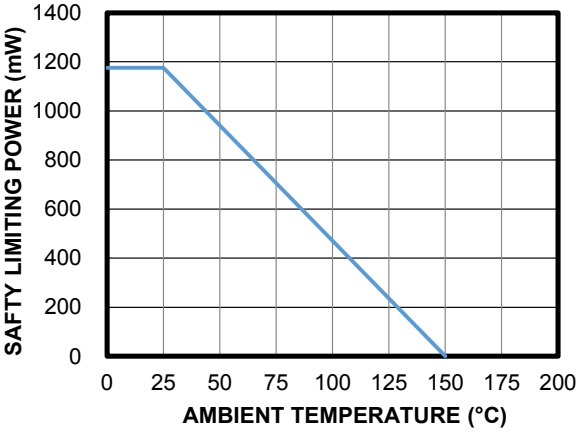
Thermal Derating Curve for Safety Limiting Power
SOIC-16 NB



Thermal Derating Curve for Safety Limiting Current
LGA-13 5x5



Thermal Derating Curve for Safety Limiting Power
LGA-13 5x5

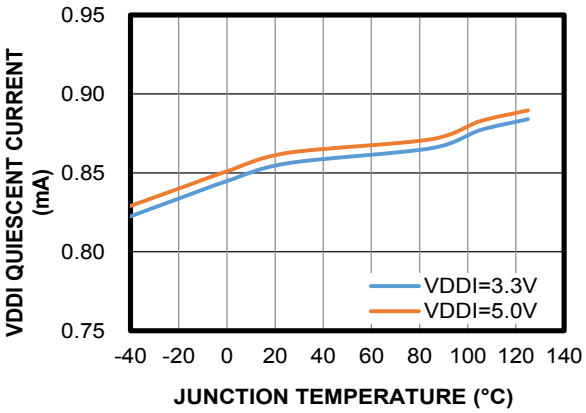


TYPICAL CHARACTERISTICS

VDDI-GNDI = 5V, VDDA-VSSA = VDDB-VSSB = 12V, C_{LOAD}=0pF, T_J = 25°C, all voltages with respect to the corresponding grounds, unless otherwise noted.

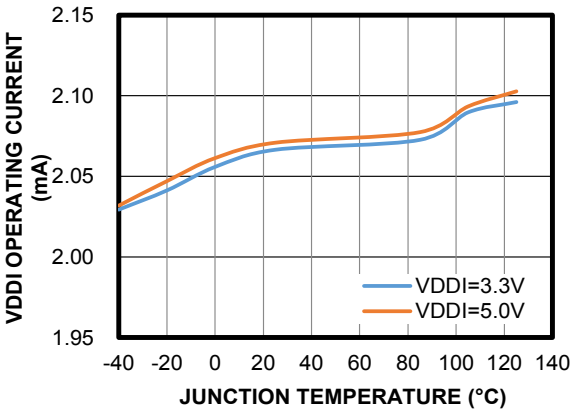
VDDI Quiescent Current vs. Junction Temperature

no switching



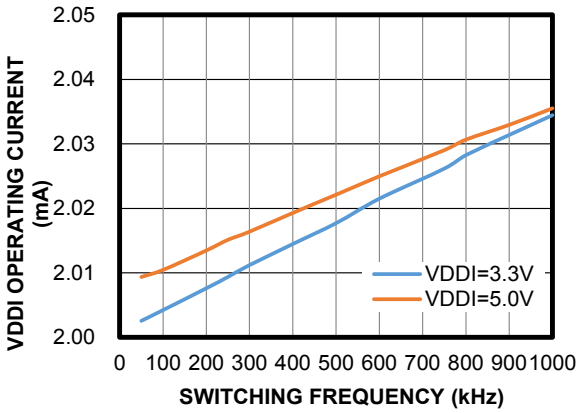
VDDI Operating Current vs. Junction Temperature

f=500kHz, Duty Cycle=50%



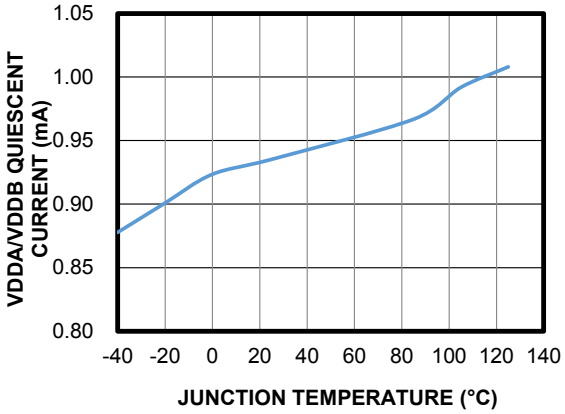
VDDI Operating Current vs. Switching Frequency

Duty Cycle=50%



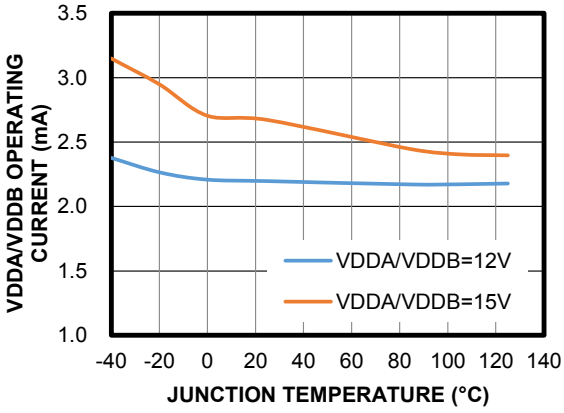
VDDA/VDDB Quiescent Current vs. Junction Temperature

per channel, no switching



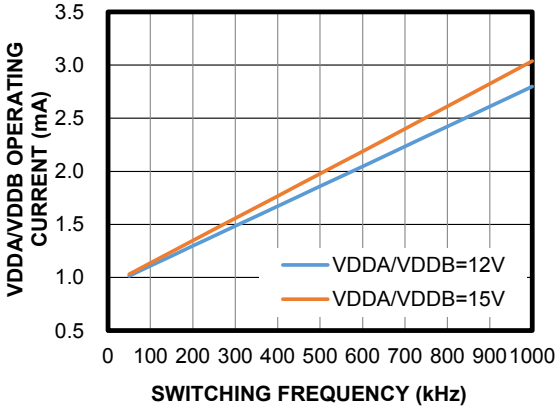
VDDA/VDDB Operating Current vs. Junction Temperature

per channel, f=500kHz, Duty Cycle=50%, C_{LOAD}=100pF



VDDA/VDDB Operating Current vs. Switching Frequency

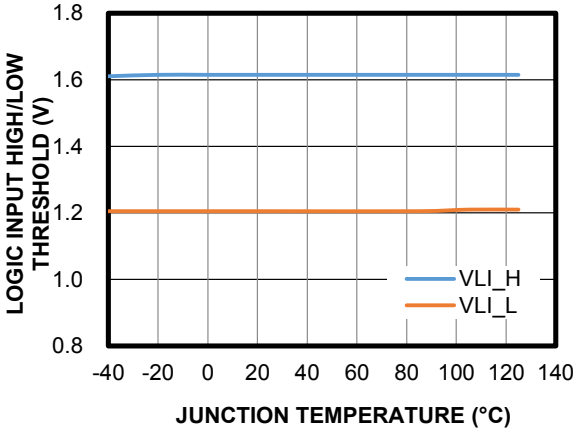
per channel, Duty Cycle=50%



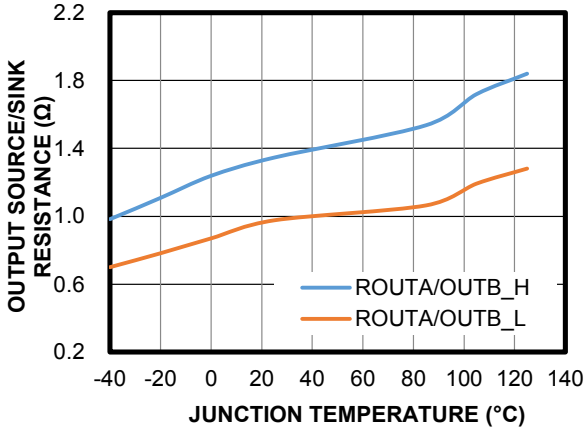
TYPICAL CHARACTERISTICS *(continued)*

VDDI-GNDI = 5V, VDDA-VSSA = VDDB-VSSB = 12V, C_{LOAD} = 0pF, T_J = 25°C, all voltages with respect to the corresponding grounds, unless otherwise noted.

Logic Input High/Low Threshold vs. Junction Temperature

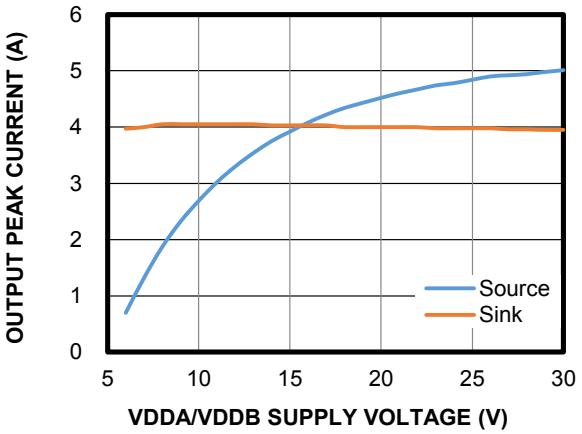


Output Source/Sink Resistance vs. Junction Temperature



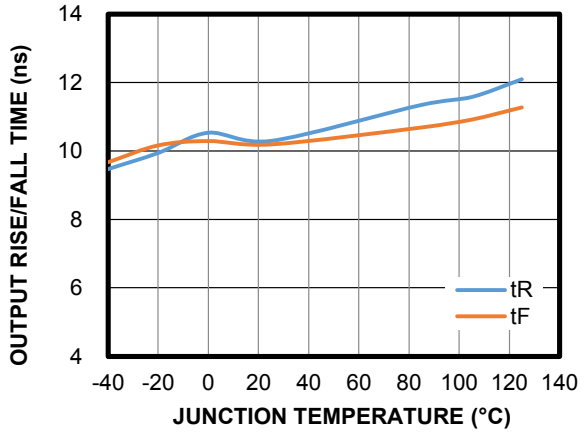
Output Peak Source/Sink Current vs. VDDA/VDDB Supply Voltage

5V UVLO version at 5V miller plateau

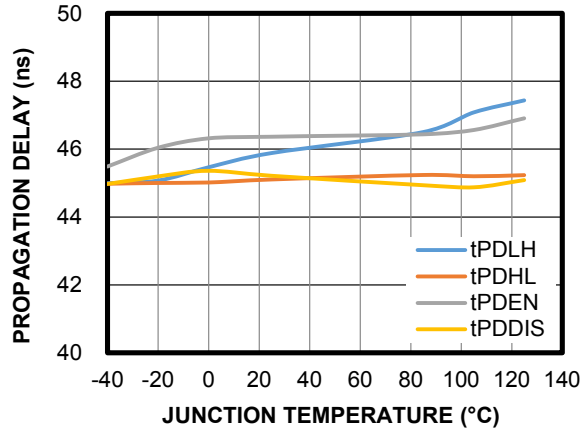


Output Rise/Fall Time vs. Junction Temperature

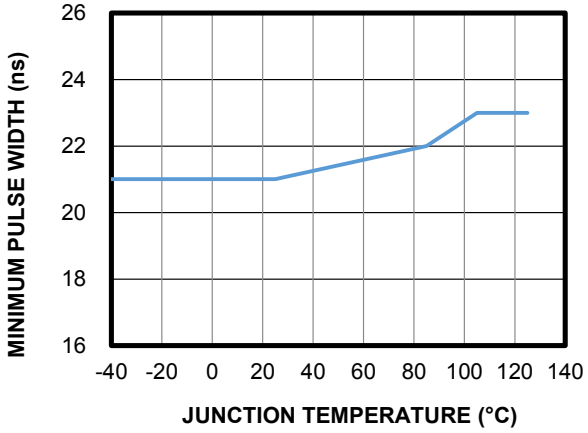
C_{LOAD} = 1.8nF



Propagation Delay vs. Junction Temperature



Minimum Pulse Width vs. Junction Temperature

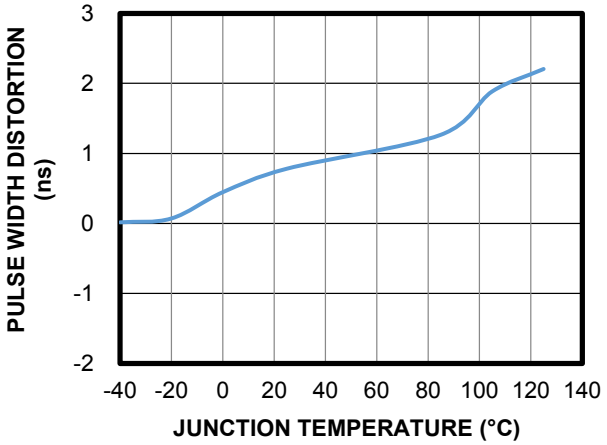


TYPICAL CHARACTERISTICS *(continued)*

VDDI-GNDI = 5V, VDDA-VSSA = VDDB-VSSB = 12V, C_{LOAD} = 0pF, T_J = 25°C, all voltages with respect to the corresponding grounds, unless otherwise noted.

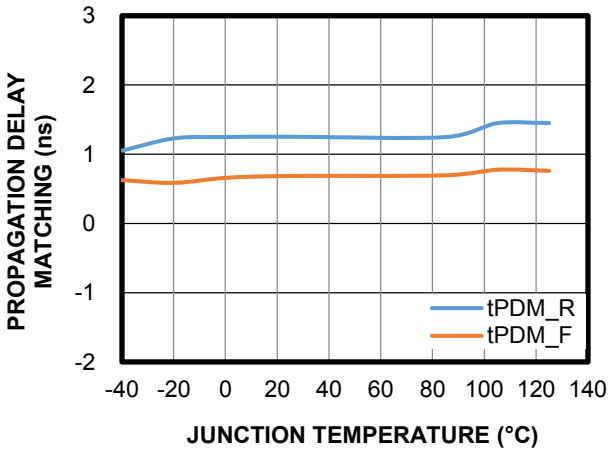
Pulse Width Distortion vs. Junction Temperature

t_{PDLH}-t_{PDHL}

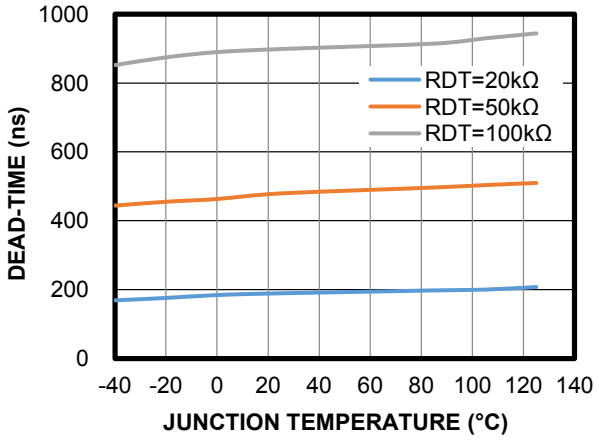


Propagation Delay Matching vs. Junction Temperature

t_{PDA}-t_{PDB}

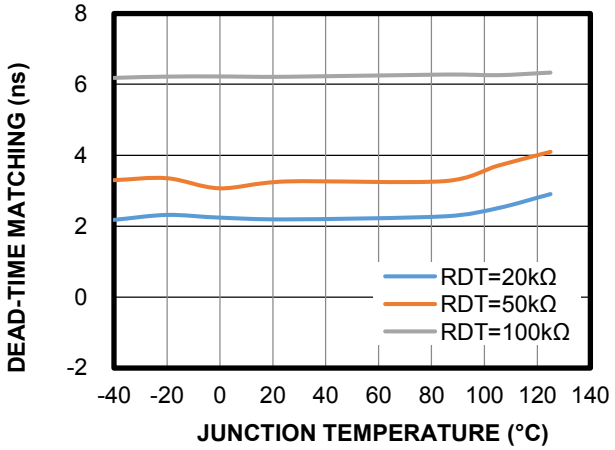


Dead-Time vs. Junction Temperature



Dead-Time Matching vs. Junction Temperature

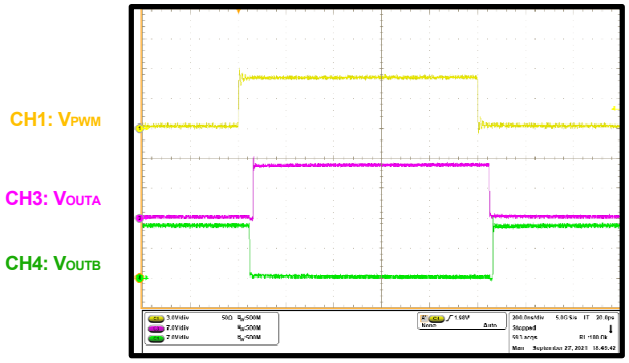
t_{DTAB}-t_{DTBA}



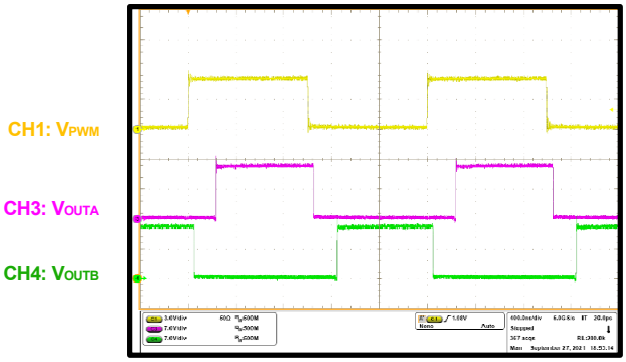
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board.
VDDI-GNDI = 5V, VDDA-VSSA = VDDB-VSSB = 12V, C_{LOAD}=0pF, T_A = 25°C, all voltages with respect to the corresponding grounds, unless otherwise noted.

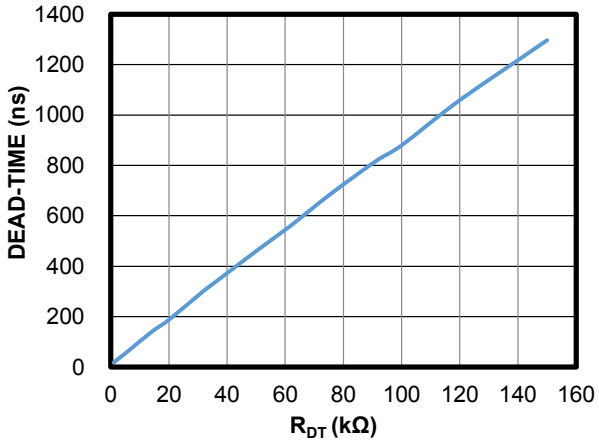
Typical Switching Waveforms
DT open



Dead-Time Control
R_{DT} = 20kΩ



Dead-Time vs. R_{DT}



DEFINITIONS OF DYNAMIC PARAMETERS

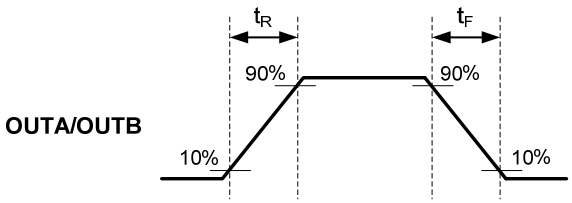


Figure 1: Output Rising and Falling Time

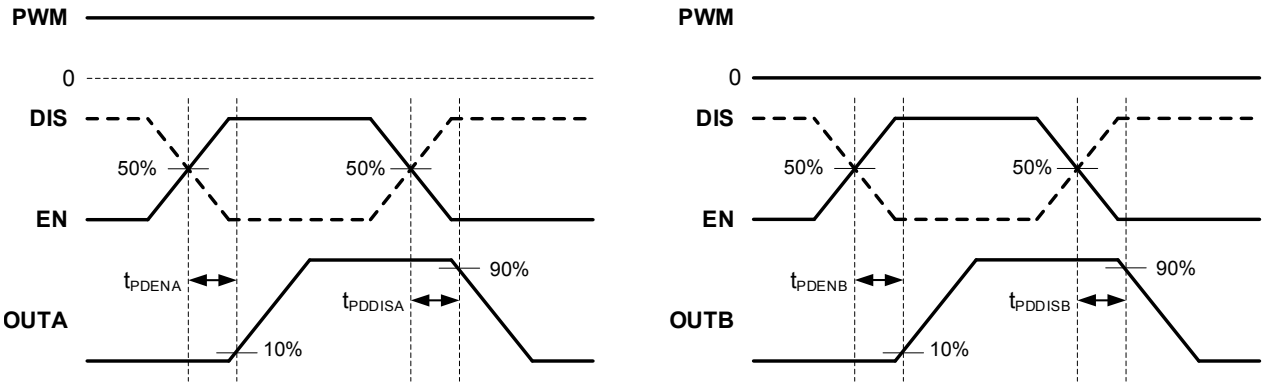


Figure 2: Enable/Disable Response Time (Disable Dead-Time Function)

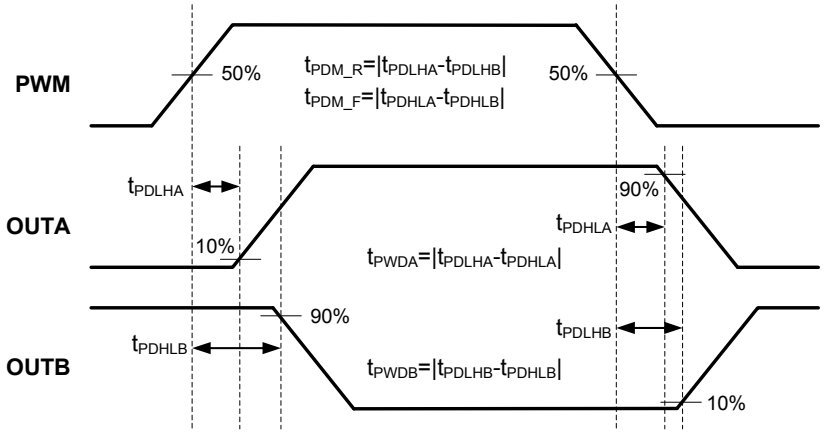


Figure 3: Propagation Delay Matching and Pulse Width Distortion (Disable Dead-Time Function)

DEFINITIONS OF DYNAMIC PARAMETERS *(continued)*

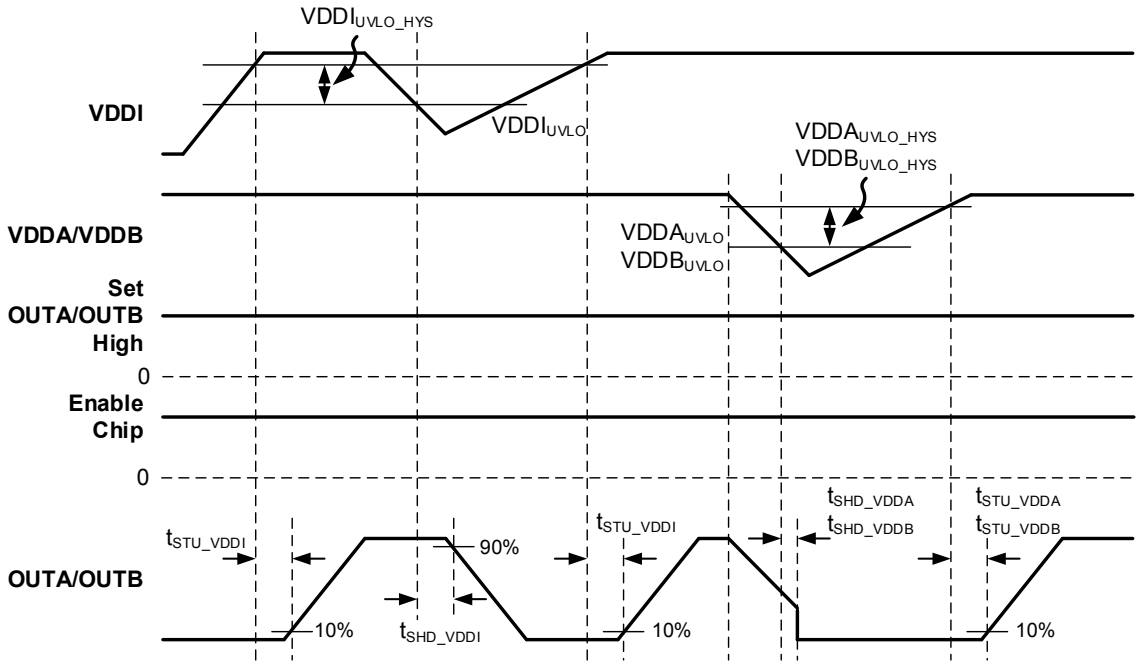


Figure 4: VDDI and VDDA/VDDB Under-Voltage Lockout (UVLO) (Disable Dead-Time Function)

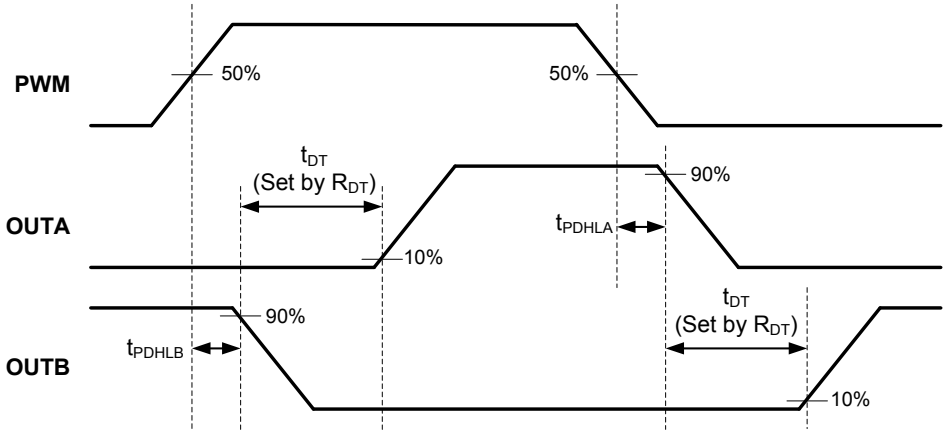


Figure 5: Dead-Time Set

DEVICE FUNCTIONAL MODES

Table 1: Logic True Table (16)(17)

Inputs			Power Supply			Outputs		Notes
PWM	EN	DIS	VDDI	VDDA	VDDB	OUTA	OUTB	
L or O	H or O	L or O	P	P	P	L	H	Output transition occurs after the dead-time expires.
H	H or O	L or O	P	P	P	H	L	
X	L	H	P	X	X	L	L	Disable chip
X	X	X	UP	X	X	L	L	VDDI is unpowered
L or O	H or O	L or O	P	UP	P	L	H	VDDA is unpowered
H	H or O	L or O	P	UP	P	L	L	
L or O	H or O	L or O	P	P	UP	L	L	VDDB is unpowered
H	H or O	L or O	P	P	UP	H	L	

NOTES:
16) L: Logic Low; H: Logic High; O: Left Open; X: Irrelevant; P: Powered; UP: Unpowered, UVLO condition.
17) If VDDI is powered, the output can operate functionally as long as this channel is powered normally.

BLOCK DIAGRAM

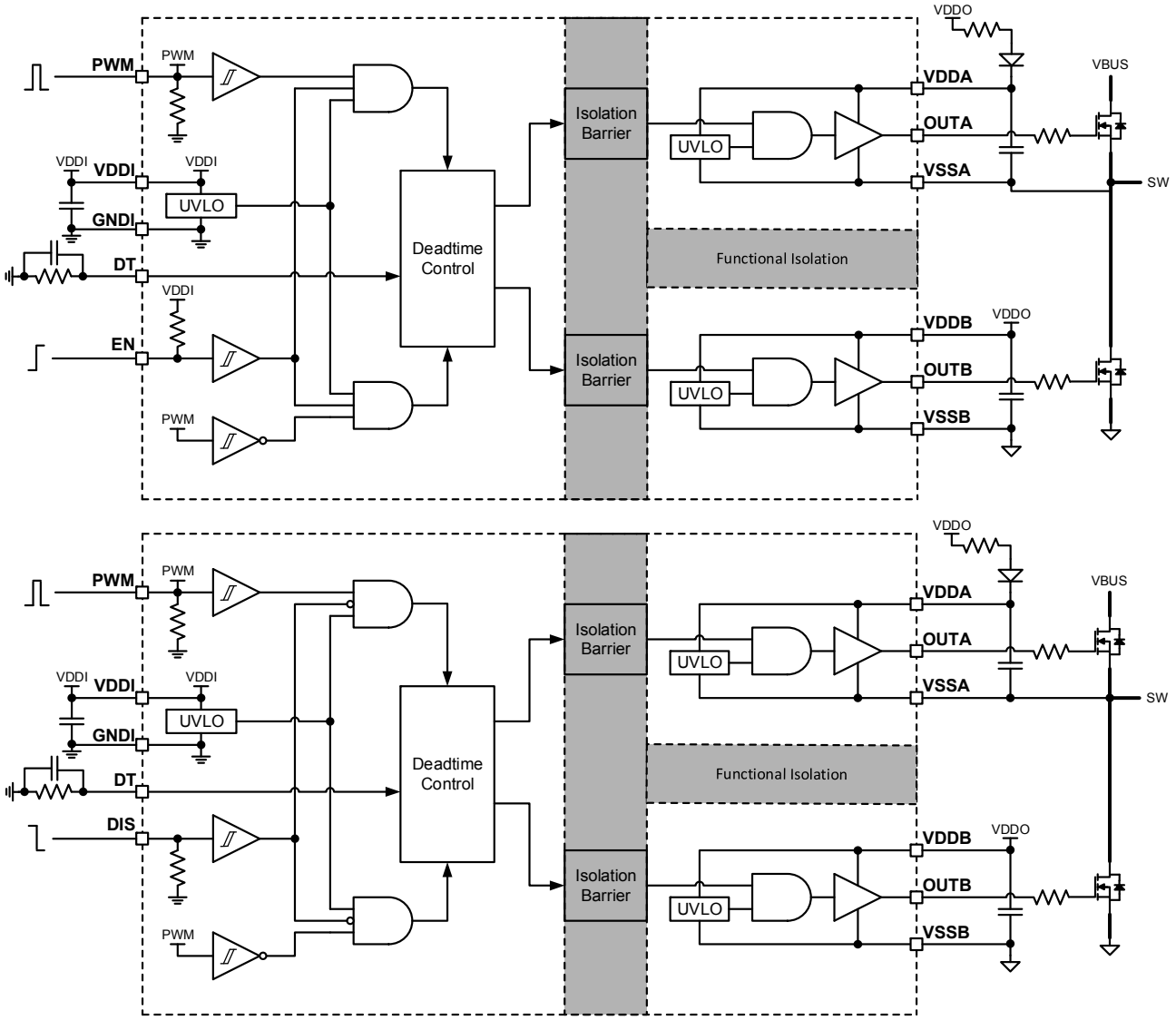


Figure 6: Functional Block Diagram

OPERATION

The MP18871 is an isolated PWM-input control, half-bridge gate driver solution with 4A peak output current capacity. This IC is designed to drive power switching devices with short propagation delay and pulse-width distortion. With the advanced features, the MP18871 operates high efficiency, high power density, and robustness in a wide variety of power applications.

Please see Table 1 for whole device functional modes.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to avoid the chip or some blocks from operating at insufficient supply voltage. The MP18871 incorporates the internal UVLO comparators for all input and output supply circuit blocks to monitor VDDI, VDDA and VDDB, respectively. Figure 4 shows the input and output supply UVLO time sequence diagram.

If the input bias voltage VDDI is unpowered or under supply UVLO level, the chip is not activated and the output stages does not receive the control signal from the input stage. Then the UVLO mechanism holds the output forced low, regardless of the present logic levels of the input signals (including EN/DIS and PWM).

When either output stage of the driver is unpowered or below UVLO level, the corresponding channel's output is also pulled low. As long as either channel is powered normally, the corresponding channel can accept the related control signal functionally.

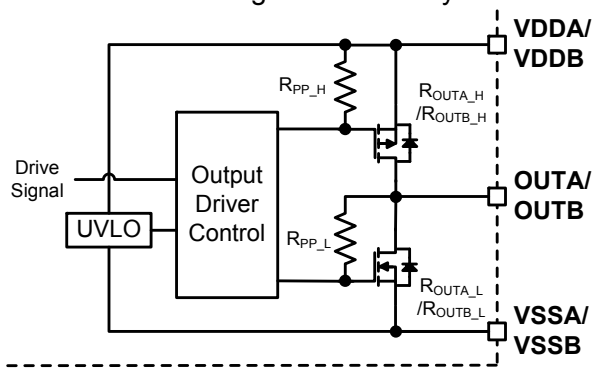


Figure 7: Output Stage

Input Stage and On/Off Control

All of the control input pins (EN/DIS and PWM) accept a TTL/CMOS compatible logic inputs that is reliably isolated from each output. These control pins are easy to be driven with common logic-level signals from a digital controller. But, any input signal applied to these control pins must never be at a higher level than the input stage supply VDDI. So, it is recommended to tie VDDI to the same power supply of the control signal sources. The control logic of EN are active-high while the control logic of DIS are active-low. OUTA is in phase with PWM input and OUTB is always complementary with OUTA.

If the PWM input is left open, it is forced logic low thru the internal pull-down resistor. Provide a determined control signal to PWM pin for stable operation and do not let it floating.

Similarly, for on/off control, the EN pin is tied to VDDI thru the internal pull-up resistor while the DIS pin is connected to GNDI thru the internal pull-down resistor. Although leaving EN/DIS pin floating enables the chip to operate normally after start-up, it is still recommended to provide stable external signal input for on/off control in actual applications.

Output Stage

The output stage comprises an upper P-channel MOSFET and a lower N-channel MOSFET (refer to Figure 7). The effective output pull-up source resistance R_{OUTA_H}/R_{OUTB_H} is the on-resistance of the upper P-channel MOSFET, which delivers the large peak source current during the external power-switch turn-on transition. The pull-down structure is simply an N-channel MOSFET, whose on-resistance R_{OUTA_L}/R_{OUTB_L} is the output effective pull-down impedance during the drive-low state of the device.

The output stage is optimized to provide strong driving capacity to a power device during the miller plateau interval of the switching on/off procedure. So the MP18871 is capable of delivering 4A peak source/sink current pulses. And the rail-to-rail output ensures the voltage swings between VDDA/VDDB and VSSA/VSSB, respectively.

Programmable Dead-Time and Overlap Protection

To prevent the occurrence of the shoot-through issue in half-bridge driver, the MP18871 allows the user to adjust dead-time (DT), which inserts a user-programmable delay between transitions of OUTA and OUTB. The MP18871 always selects the driver's programmed dead-time as the operating dead-time.

When the dead-time control is enabled, in the meanwhile, the overlap protection scheme is activated. It prevents both channels from outputting logic-high synchronously. This overlap protection doesn't affect the dead-time setting of normal operation.

The dead-time delay operation is present on all output transitions from low to high. Refer to Figure 5 for more information about the operation of dead-time mechanism.

The chip's dead-time is set thru the DT pin. An around 0.65V steady-state bias voltage is generated at DT pin, and the DT pin's source current is monitored to adjust the dead-time delay. When leave DT pin open, a minimum dead-time duration (t_{DT}) is set. Normally, the dead-time is programmed by placing a single resistor R_{DT} connected from the DT pin to input stage's ground GNDI. This R_{DT} resistance should be between the values of 2kΩ and 150kΩ and a filter capacitor of 220pF or above in parallel is recommended. The curve of the dead-time vs. R_{DT} is illustrated in TYPICAL PERFORMANCE CHARACTERISTICS.

Common-Mode Transient Immunity

Common-Mode Transient Immunity (CMTI) is one of the key characteristics that correlate to an isolator's robustness, especially important in high-voltage applications with fast transient devices (like SiC/GaN FET). When a power device is switching, the high slew rate dv/dt or di/dt transient noise can corrupt the signal transmission across the isolation barrier. CMTI is defined as maximum tolerable rate-of-rise (or fall) of a common-mode voltage applied between two isolated circuits, given in volts per second (V/ns or kV/μs). Below the maximum slew rate of a common mode voltage, the output of the isolator remains at the specific logic level and at the specified timing.

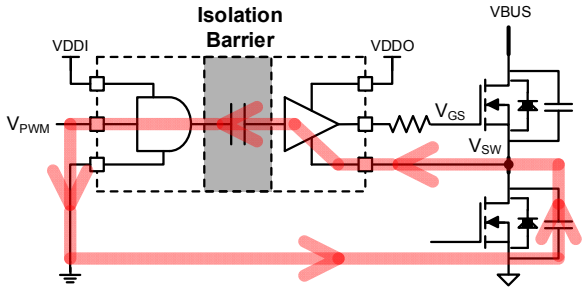


Figure 8: High Slew Rate Transient Noise Coupling Path

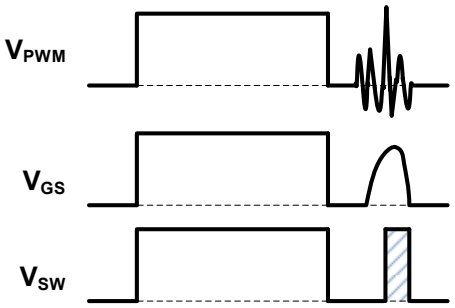


Figure 9: Abnormal Pulse Caused by Coupled Noise if dv/dt > CMTI

Figure 10 shows the CMTI test setup to measure the CMTI of a coupler in both static and dynamic operation, under specified common-mode pulse magnitude (V_{CM}) and specified slew rate of the common-mode pulse (dV_{CM}/dt) and other specified test or ambient conditions. The isolator's output should stay in the correct state as long as the pulse magnitude and the slew rate meet the CMTI specification.

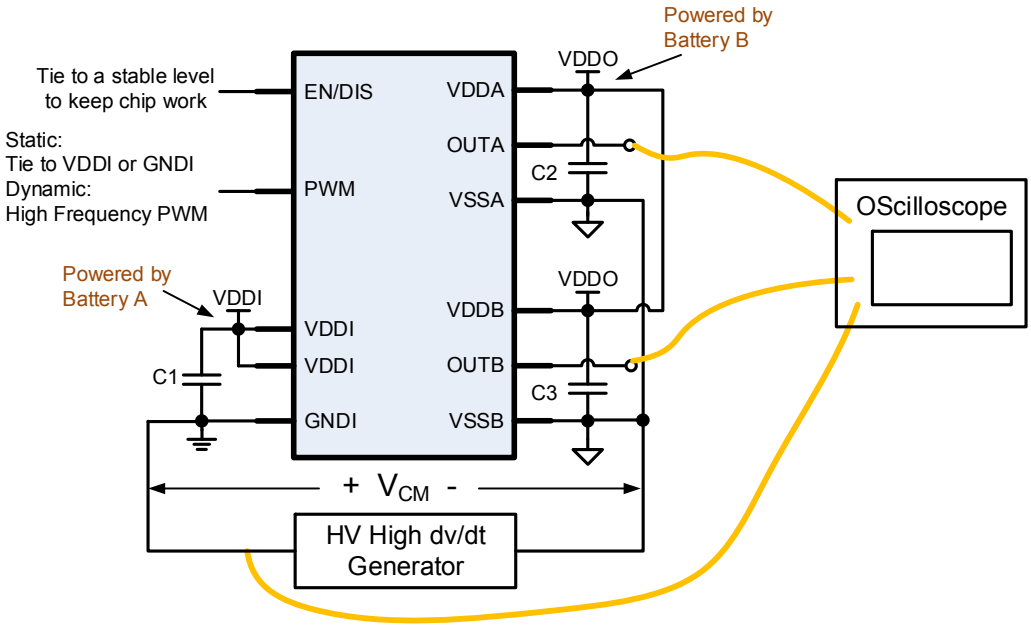


Figure 10: CMTI Test Setup

APPLICATION INFORMATION

Figure 13 is a reference design for typical application circuit.

Selecting the VDDI Capacitor

The input supply VDDI capacitor reduces the surge current drawn from the input supply and supports the current consumption for the primary logic interface and transmitter block. Since the input side's operating current is only a few mA, a 100nF ceramic capacitor with X5R or X7R dielectrics is highly recommended because of its low ESR and small temperature coefficients. For most applications, add a >1μF capacitor in parallel with this 100nF as the bypass capacitor if the real supply power is far away from the VDDI pin.

Selecting the VDDA/VDDB Capacitor

As the bypass capacitor of the output gate driver, besides the consumption of driving control block, the VDDA/VDDB capacitor maintains the stable driving voltage and supports up to 4A the transient source current.

Assume the allowable VDDA/VDDB voltage ripple is ΔVDDA/VDDB which guarantees that the driver supply voltage cannot drop close to UVLO level, the minimum VDDA/VDDB capacitor is

$$C_{VDDA/VDDB} = \frac{I_{VDDA/VDDB} \times \frac{1}{f_{SW}} + Q_G}{\Delta VDDA/VDDB} \quad (1)$$

where,
$I_{VDDA/VDDB}$ is VDDA/VDDB operation current;
f_{SW} is the switching frequency;
Q_G is the gate charge of the power device.

Care should be taken when the loop resistance, voltage drop and DC bias voltage ripple have impact on supply voltage. Especially for channel A which usually operates as the high-side driver in a half-bridge converter and is powered by a bootstrap circuity, too large VDDA capacitor is not a good option. It may not be charged fast at system power-up or bootstrap cycle. VDDA could stay below UVLO level and fails to power the high-side driver. Generally, a 1μF capacitor is chosen for channel A. If channel A is powered by a special supply, a larger VDDA capacitor can be selected.

Channel B is powered by a special supply and the VDDB capacitor needs to support the VDDA capacitor's charging current thru bootstrap, so a large bypass capacitor can be chosen, like a 10μF ceramic capacitor. Similarly, a secondary high frequency bypass capacitor of 100nF in parallel is recommended.

Selecting the Bootstrap Diode and Series Resistor

A bootstrap configuration is often applied to power the high-side driver in a half-bridge converter. The bootstrap capacitor is charged thru the bootstrap diode and series resistor during the low-side turn-on interval. And the diode needs to load the high reverse voltage (higher than bus voltage) during the low-side turn-on interval. To reduce the conduction losses and reverse recovery losses, a high-voltage, fast recovery diode or schottky diode should be chosen.

Meanwhile, a bootstrap series resistor is also used to limit the inrush charging current, which could generate a spike on VDDA pin. The recommended value is not larger than 10Ω. Then the estimated peak charging current is

$$I_{BST} = \frac{VDDA/VDDB - V_{D\_BST}}{R_{BST}} \quad (2)$$

where,
V_{D_BST} is the forward voltage drop of the bootstrap diode;
R_{BST} is the bootstrap series resistor.

Selecting the Input Filter for PWM

Theoretically, the PWM input filter is not necessary. The low pass filter slows the PWM signal's rising/falling edge and affects the propagation delay. However, it is still recommended to add a simply RC filter at input close to PWM pin if the high frequency ringing introduced by PCB traces is terrible.

Generally, to avoid increasing the input resistance, a smaller than 100Ω resistor can be selected. When selecting the filter capacitor, make sure the filter's cut-off frequency is at least ten times higher than the switching frequency, a dozens of PF capacitor should be enough.

Selecting the External Driving Resistor

The external driving resistor can be applied to limit the ringing noise on driving signal and adjust the switching speed to improve EMI performance. But large driving resistor increases the switching losses, reduces system efficiency and brings thermal issue. In actual applications, the turn-on and turn-off speeds can be adjusted by different driving resistors, respectively. The sink resistor is in series with an anti-parallel diode to be separated from the source resistor. And the total driving resistor when pulling down the power device is the sink resistor in parallel with the source resistor.

The peak driving current is the key feature to evaluate the effect of the driving resistors. Without driving resistor, the MP18871 can drive both 4A peak source/sink current.

Considering the driving resistor, the peak source driving current is

$$I_{OUTA\_SRC} = \frac{VDDA}{R_{OUTA\_H} + R_{G\_SRC} + R_{G(int)}} \quad (3)$$

$$I_{OUTB\_SRC} = \frac{VDDB}{R_{OUTB\_H} + R_{G\_SRC} + R_{G(int)}} \quad (4)$$

The peak sink driving current is

$$I_{OUTA\_SNK} = \frac{V_{GSA\_ON}}{R_{OUTA\_L} + R_{G\_SRC} \parallel R_{G\_SNK} + R_{G(int)}} \quad (5)$$

$$I_{OUTB\_SNK} = \frac{V_{GSB\_ON}}{R_{OUTB\_L} + R_{G\_SRC} \parallel R_{G\_SNK} + R_{G(int)}} \quad (6)$$

where,
R_{G_SRC} is the external source resistor;
R_{G_SNK} is the external sink resistor;
$R_{G(int)}$ is internal gate resistance of the power device;
V_{GSA_ON}/V_{GSB_ON} is the stable gate-source voltage of the power device in ON interval. Generally, it should be close to VDDA/VDDB.

Since the driving current cannot higher than 4A, select the smaller value of the estimated $I_{OUTA\_SRC/OUTB\_SRC}$ or $I_{OUTA\_SNK/OUTB\_SNK}$ and 4A as the actual peak driving current.

Setting the Dead-Time on DT pin

In half-bridge power converter, a dead-time is inserted during dynamic switching transition between high-side and low-side power devices to prevent shoot-through. The MP18871's dead-time can be controlled by DT setting. The chip always selects the driver's programmed dead-time as the operating dead-time.

The dead-time setting needs to be determined by actual system requirements. By observing the real V_{GS}, V_{DS} and switch node's waveforms of both high-/low-side devices and considering ZVS control logic. Make sure the dead-time interval is with enough margin at any load condition.

The MP18871's dead-time setting is programmed by DT pin. Select the suitable resistor according to the curve of the dead-time vs. R_{DT}.

Estimate Gate Driver's Power Loss

The total power loss on the gate driver is used to estimate the thermal performance. The MP18871 needs to operate under Safety Limiting Values.

The first element is the chip's operation power consumption P_{OP}:

$$P_{OP} = VDDI \times I_{VDDI} + VDDA \times I_{VDDA} + VDDB \times I_{VDDB} \quad (7)$$

The driver self-power consumption is related to the switching frequency and supply voltage. Typical Characteristics provide the relationship reference of input and output channels' current consumption vs. operating frequency.

The key element is the driving power loss at switching operation. As a conventional totem-pole gate driver, the MP18871's each channel charges and discharges the gate capacitance of the power device one time during every switching cycle.

During the charging and the discharging period, the total energy is supplied by VDDA/VDDB. If there is no external gate driving resistor, the equation of power dissipation is given as

$$P_{SW} = \left(VDDA \times \int_0^{t_{ON}} i_{GA}(t)dt + VDDB \times \int_0^{t_{ON}} i_{GB}(t)dt \right) \times f_{SW}$$

$$= (VDDA + VDDB) \times Q_G \times f_{SW} \quad (8)$$

where,
t_{ON} is the turn-on time;
$i_{GA/GB}(t)$ is the driving current.

Considering the action of the external source/sink resistors, the dynamic power dissipation estimation becomes complicated.

If the driving current is not saturated to 4A in whole switching cycle with external gate resistors, this power dissipation is shared between the internal source/sink resistances of the gate driver and the external gate driving resistors based on the ratio of these series resistances (see Equation 9).

$$P_{SW} = \frac{VDDA \times Q_G \times f_{SW}}{2} \times \left(\frac{R_{OUTA\_H}}{R_{OUTA\_H} + R_{G\_SRC} + R_{G(int)}} + \frac{R_{OUTA\_L}}{R_{OUTA\_L} + R_{G\_SRC} \parallel R_{G\_SNK} + R_{G(int)}} \right)$$
$$+ \frac{VDDB \times Q_G \times f_{SW}}{2} \times \left(\frac{R_{OUTB\_H}}{R_{OUTB\_H} + R_{G\_SRC} + R_{G(int)}} + \frac{R_{OUTB\_L}}{R_{OUTB\_L} + R_{G\_SRC} \parallel R_{G\_SNK} + R_{G(int)}} \right) \quad (9)$$

$$P_{SW\_SAT} = 4A \times \int_0^{t_{ON\_SAT}} (VDDA - V_{GSA}(t))dt + 4A \times \int_0^{t_{OFF\_SAT}} (V_{GSA}(t))dt$$
$$+ 4A \times \int_0^{t_{ON\_SAT}} (VDDB - V_{GSB}(t))dt + 4A \times \int_0^{t_{OFF\_SAT}} (V_{GSB}(t))dt \quad (10)$$

where,
t_{ON_SAT/OFF_SAT} is the turn-on/off time with saturated 4A current output;
$V_{GSA/GSB}(t)$ is the gate voltage of the power device in these saturation time.

In some conditions, the MP18871 outputs the saturated 4A current at the beginning of the turn-on/off interval. It results in the power loss calculation in these saturation time becomes Equation 10.

The actual power loss should be the combination of Equation 9 and Equation 10. Then the total power loss dissipated in the MP18871 is

$$P_{LOSS} = P_{OP} + P_{SW} \quad (11)$$

Taking the total power loss multiplied by Junction-to-Ambient Thermal Resistance θ_{JA} to know the junction temperature rise above the ambient temperature. Make sure the junction temperature T_J is below the maximum safety temperature T_S.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to the guidelines below.

1. Place the bypass/decoupling capacitors as close as possible to the VDDI/VDDA/VDDB supply pins and the corresponding grounds. For each supply pin, it is recommended to add a low ESR/ESL, high frequency bypass capacitor of 100nF.
2. Place the dead-time setting resistor and its bypassing capacitor close to DT pin.
3. If input RC filter is used, it is recommended to place this filter close to the corresponding control pin.
4. Place the high current paths, like supply path, drive path and the connection between the source of the external power device and VSSA/VSSB pin very close to the driver chip with short, direct, and wide traces to minimize the parasitic inductances and avoid large transient and ringing noise.
5. It is highly recommended to place large power and ground planes or multiple layers to help dissipate heat from the gate driver chip to PCB to improve the thermal performance. However, must take care of splitting the traces or coppers to allow sufficient insulation distance between different low-/high-voltage planes.
6. Keep the driving loop, form OUTA/OUTB, the gate-to-source of the power device to VSSA/VSSB, short in a minimal area. Try to avoid the driving trace across different PCB layers thru vias, since it can bring parasitic inductances. Meanwhile, the driver IC should be placed as close as possible to the power device.
7. Refer to the recommended land pattern design of each package type for adequate insulation space between the primary and secondary side. Avoid placing any components, tracks or copper below the chip's body in any PCB layer.
8. A board cutout under the chip is not necessary, but it is still recommended to create it to extend the creepage distance on PCB surface, except for small size LGA package. The LGA package's bottom side is pressed on the PCB surface, so the PCB cutout is not effective but can make the board easy to be twisted.
9. If the driver chip is used in half-bridge configuration, keep enough space and try to increase creepage distance between dual channels.

Take a 2-layer PCB layout with SOIC-16 WB package as an example. Figure 11 and 12 shows the layout around the chip. The components labels are consistent with those in Figure 13.

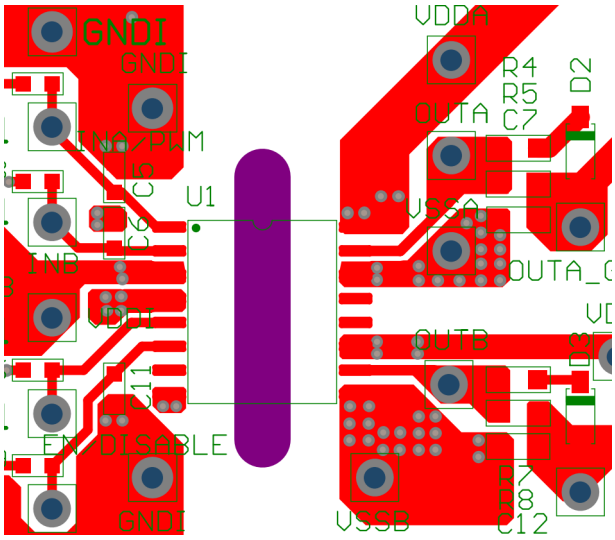


Figure 11: Top Layer Layout Reference

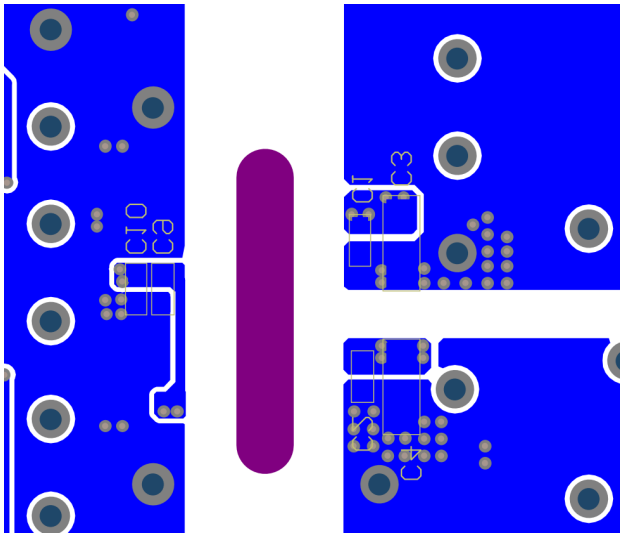


Figure 12: Bottom Layer Layout Reference

TYPICAL APPLICATION CIRCUITS

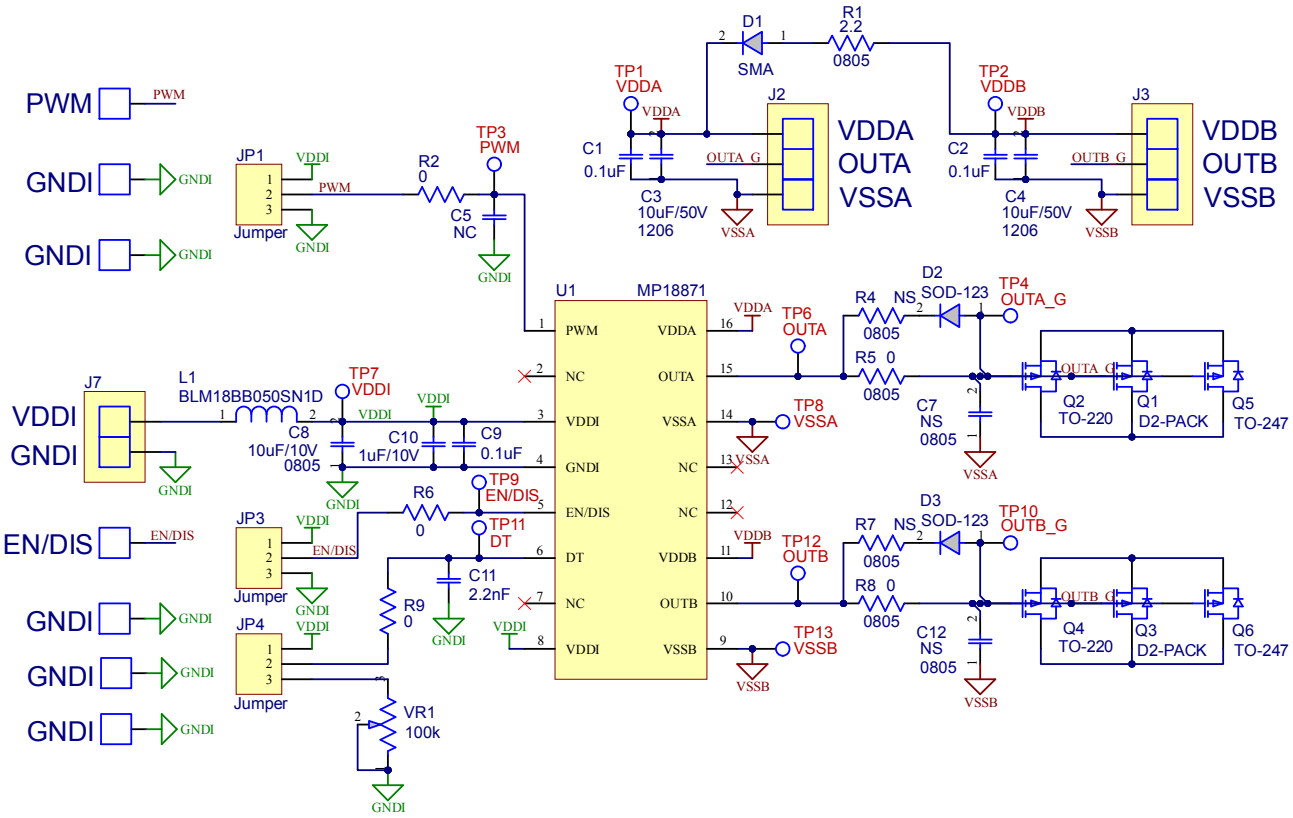
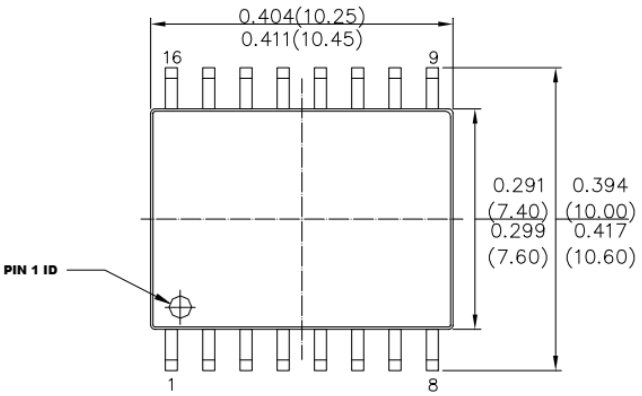


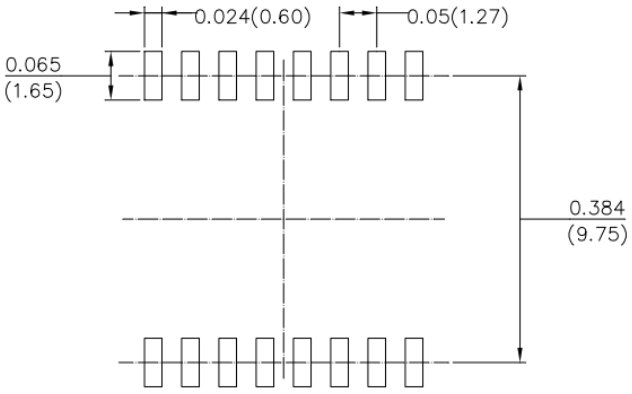
Figure 13: Typical Application Circuit Reference Design

PACKAGE INFORMATION

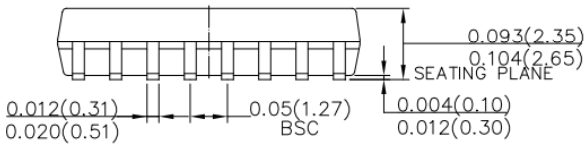
SOIC-16 WB (HV ISOLATION)



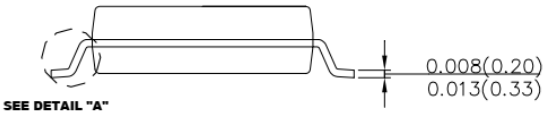
TOP VIEW



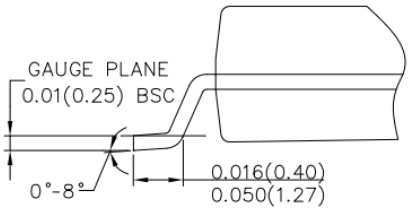
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



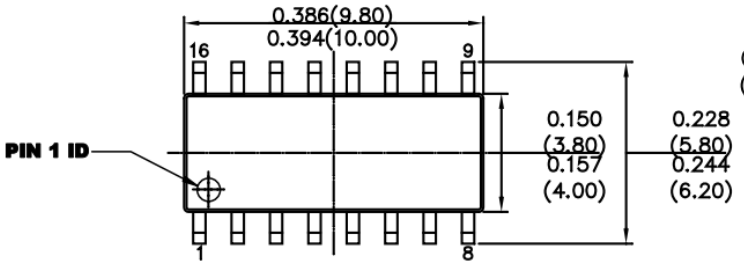
DETAIL "A"

NOTE:

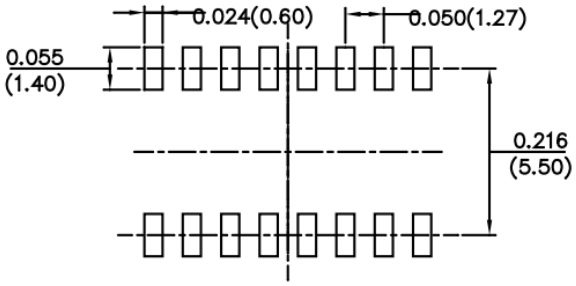
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-013, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

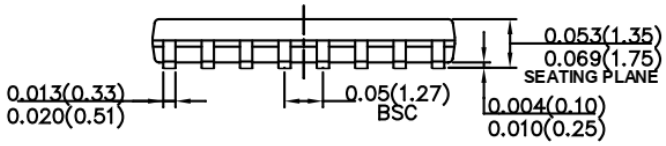
SOIC-16 NB (HV ISOLATION)



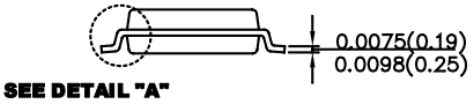
TOP VIEW



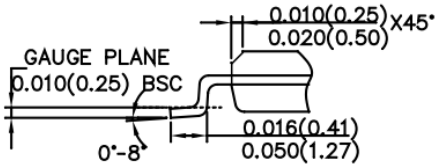
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



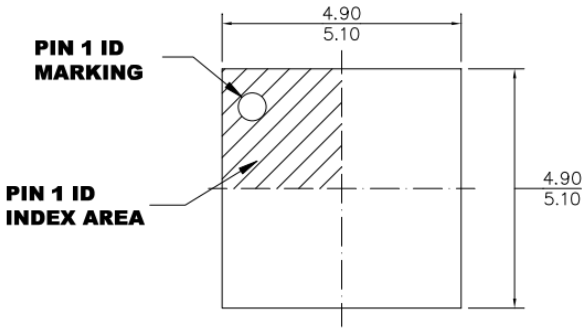
DETAIL "A"

NOTE:

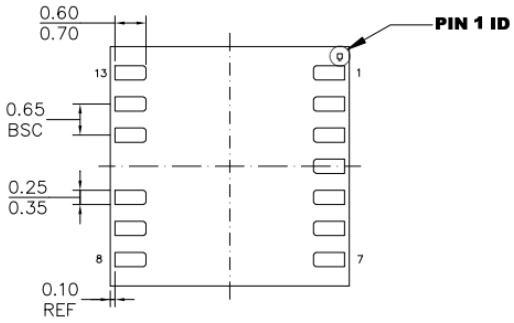
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BC.
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

LGA-13 (5mm X 5mm)

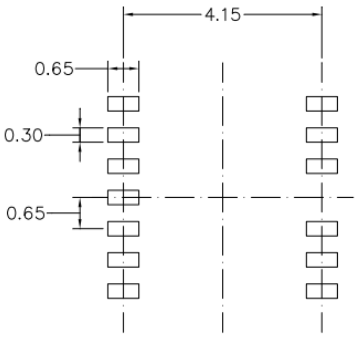


TOP VIEW



BOTTOM VIEW

SIDE VIEW



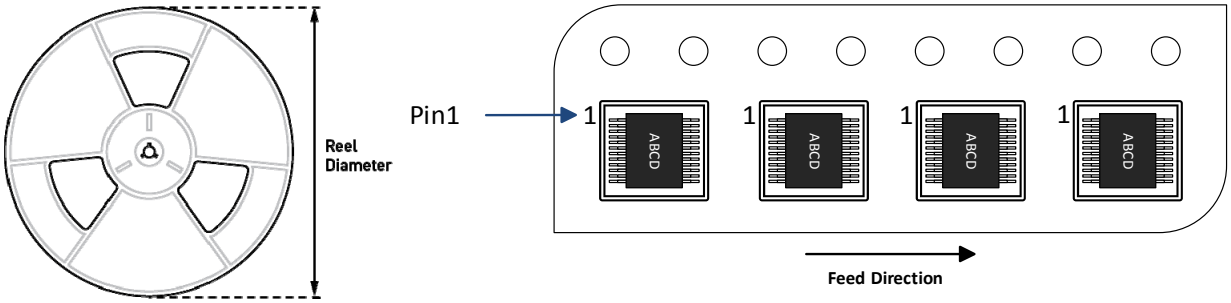
RECOMMENDED LAND PATTERN

NOTE:

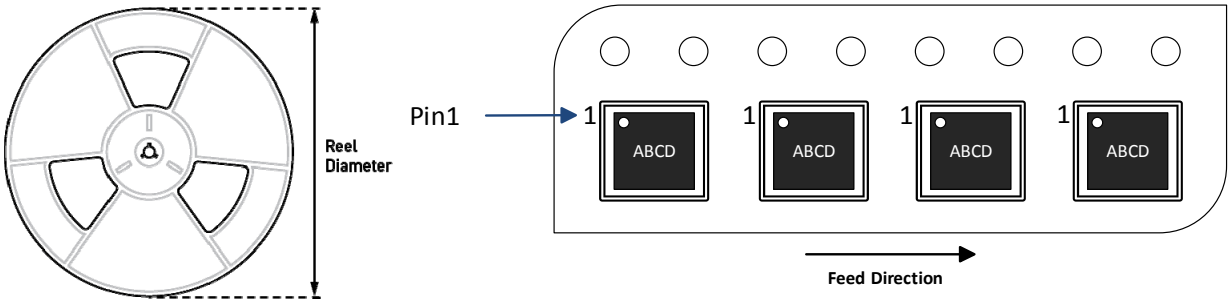
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION

SOIC-16 NB & SOIC-16 WB



LGA-13 (5mmx5mm)



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP18871-4AGSE-Z	SOIC-16 NB	2500	50	13 in.	16 mm	8 mm
MP18871-4BGSE-Z						
MP18871-4CGSE-Z						
MP18871-4DGSE-Z						
MP18871-4EGSE-Z						
MP18871-4AGY-Z	SOIC-16 WB	1000	47	13 in.	24 mm	12 mm
MP18871-4BGY-Z						
MP18871-4CGY-Z						
MP18871-4DGY-Z						
MP18871-4EGY-Z						
MP18871-4AGLU-Z	LGA-13 (5mmx5mm)	5000	N/A	13 in.	12 mm	8 mm
MP18871-4BGLU-Z						
MP18871-4CGLU-Z						
MP18871-4DGLU-Z						
MP18871-4EGLU-Z						

CARRIER INFORMATION *(continued)*

Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP18871-A4AGSE-Z	SOIC-16 NB	2500	50	13 in.	16 mm	8 mm
MP18871-A4BGSE-Z						
MP18871-A4CGSE-Z						
MP18871-A4DGSE-Z						
MP18871-A4EGSE-Z						
MP18871-A4AGY-Z	SOIC-16 WB	1000	47	13 in.	24 mm	12 mm
MP18871-A4BGY-Z						
MP18871-A4CGY-Z						
MP18871-A4DGY-Z						
MP18871-A4EGY-Z						
MP18871-A4AGLU-Z	LGA-13 (5mmx5mm)	5000	N/A	13 in.	12 mm	8 mm
MP18871-A4BGLU-Z						
MP18871-A4CGLU-Z						
MP18871-A4DGLU-Z						
MP18871-A4EGLU-Z						