PAW-A350: Optical Finger Navigation (OFN) Module

General Description

The module PAW-A350 is a highly integrated and small form factor (SFF) optical finger navigation system. It has a low-power architecture and automatic power management modes, making it ideal for battery and power sensitive applications such as mobile phones. The PAW-A350 is capable of high-speed motion detection – up to 20 ips. In addition, it has an on-chip oscillator and integrated LED for optical navigation to minimize external components. There are no moving parts, thus provide high reliability and less maintenance for the end user. In addition, precision optical alignment is not required, facilitating high volume assembly. The chip is programmed via registers through either the SPI interface or the I2C interface port. It is packaged into a 17-pin FPC module for ease of assembly via ZIF connector.

Key Features

- Single 1.8V supply voltage for analog and digital
- Selectable I/O voltage at 1.8V or 2.8V nominal
- 4-wire SPI or I2C interface
- Low power architecture
- Self-adjusting power-saving modes for longer battery life
- High speed motion detection up to 20 ips
- Motion detection interrupt output
- Finger detection interrupt output
- Soft click and Tap detect interrupt output
- Selectable resolution (CPI) : 125, 250, 500, 750, 1000 and 1250
- Integrated chip-on-board LED with wavelength of 870nm

Applications

- Finger input devices
- Skin touch devices
- Mobile devices (Phone, Tablet)
- Integrated input devices

Key Parameters

Parameter	Value
Supply Voltage	VDD : 1.7 ~ 2.1V VDDIO : 1.65 ~ 3.6V
Control Interface	I2C or 4-wire SPI
Max. tracking speed (max)	20 ips (inches/sec)
Resolution (CPI)	125, 250, 500, 750, 1000, 1250
Operating current (Average @ VDD = VDDIO = 1.8V)	Run : 2.9mA Rest1/2/3 : 350µA/70uA/30uA Power down : 1.5µA
Light Source	Infrared LED 870 nm
Module type	17-pin FPC module

Ordering Information

Part Number	Package Type
PAW-A350	17-pin FPC module

RoHS compliant

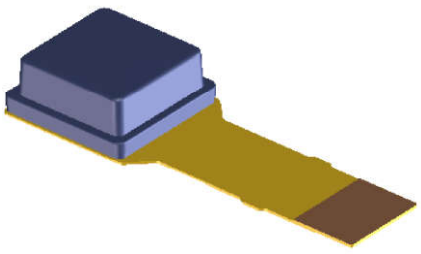

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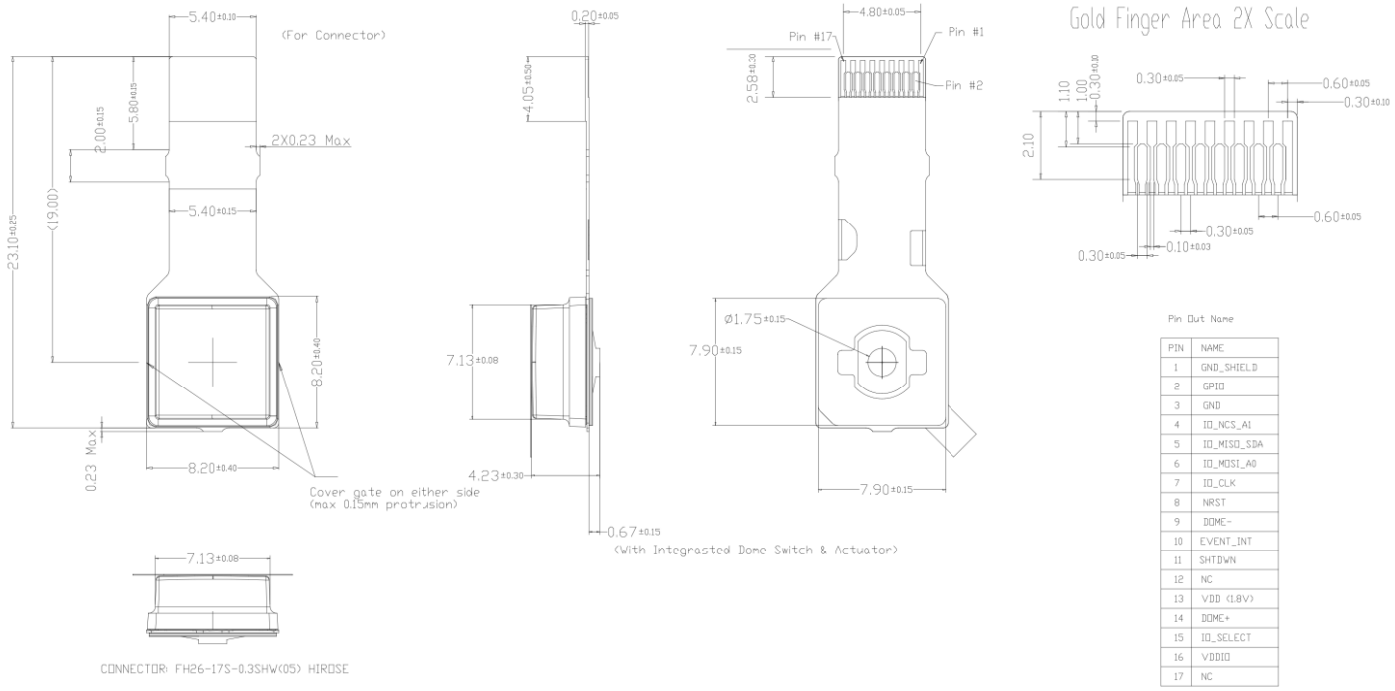
Table of Contents

1.0 Introduction

The PAW-A350 is based on Optical Finger Navigation (OFN) Technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement. The PAW-A350 contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a communication system. The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the Δx and Δy relative displacement values. The host reads the Δx and Δy information from the chip serial port if a motion interrupt is published. The microcontroller then translates the data into cursor navigation, rocker switch, scrolling or other system dependent navigation data.

2.0 Mechanical Specifications



Pin Out Name

PIN	NAME
1	GND_SHIELD
2	GPIO
3	GND
4	IO_NCS_A1
5	IO_MISO_SDA
6	IO_MOSI_A0
7	IO_CLK
8	NRST
9	DOME-
10	EVENT_INT
11	SHTDWN
12	NC
13	VDD (1.8V)
14	DOME+
15	IO_SELECT
16	VDDIO
17	NC

3.0 Module Pinout Signal Descriptions

Pin	Name	Type	Descriptions
1	GND_SHIELD	GND	Ground for ESD protection
2	GPIO	IN (Schmitt trigger input) Out (CMOS output)	General purpose I/O. Pin can be used for FPD output, PWM output or Dome/ Button click input. If configure as input do not leave pin unconnected
3	GND	GND	System Ground
4	IO_NCS_A1	IN (Schmitt trigger input)	SPI : NCS (chip select) active low signal I2C Address Select, A1 Do no leave pin unconnected
5	IO_MISO_SDA	IN SPI – CMOS output IN I2C – Open drain I/O	SPI : MISO (Master Input Slave Out) signal I2C : Serial data signal
6	IO_MOSI_A0	IN (Schmitt trigger input)	SPI : MOSI (Master Out Slave In) signal I2C Address Select, A0 Do no leave pin unconnected
7	IO_CLK	IN (Schmitt trigger input)	Serial clock signal
8	NRST	IN (Schmitt trigger input)	Hardware Chip Reset. Set to high when not used Active low signal
9	DOME-	Metal Dome -	When the metal dome switch is pressed down, this pin will be conducted to DOME+
10	EVENT_INT	Out (CMOS output)	Event Interrupt. Open when not used Default active low signal, can be changed in EVENT_CTRL register 0x1D
11	SHTDWN	IN (Schmitt trigger input)	Shutdown the module. Set to low when not used Active high signal
12	NC	NC	No connection
13	VDD	Power	Power supply 1.8V
14	DOME+	Metal Dome +	When the metal dome switch is pressed down, this pin will be conducted to DOME-
15	IO_SELECT	IN (Schmitt trigger input)	SPI/I2C mode selection. I2C : GND or SPI : High
16	VDDIO	Power	Power supply 1.8V or 2.8V
17	NC	NC	No connection

Note. NC pins can be tied to VDD, GND or left open / unconnected.

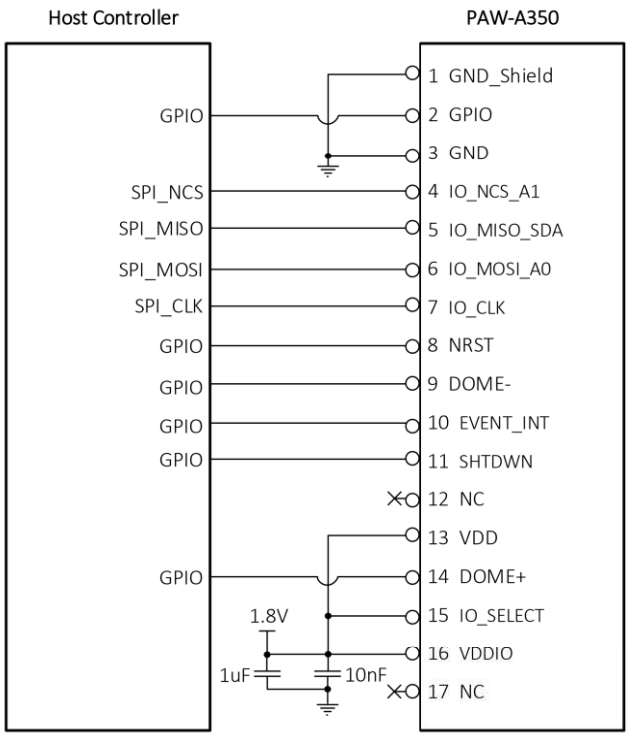
4.0 Reference Schematics

Reference schematic diagram for interface between PAW-A350 and 1.8V microcontroller via SPI or I2C bus.

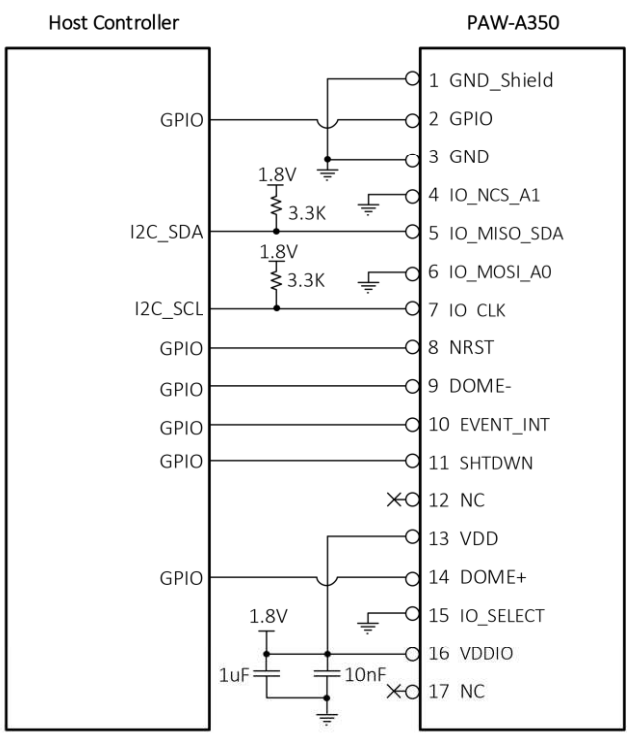
Note :

1. Dome+ must be connected to MCU to detect button change state and Dome– can be connected to GND.
2. The 3.3K ohm pull-up resistors are just for reference. The value might have to be adjusted according to the wire load of the bus.

SPI mode



I2C mode



IO_MOSI_A0	IO_NCS_A1	Slave Address (Hex)
0	0	33
0	1	3b
1	0	53
1	1	57

5.0 Operating Specifications

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-40	85	^{O}C	
Analog and Digital Supply Voltage	VDD	-0.5	2.1	V	
I/O Supply Voltage	VDDIO	-0.5	3.7	V	
ESD (sensor only)	-	-	2	kV	All pins, human body model JESD22-A114-E
Input Voltage	V_{IN}	-0.5	VDD+0.5 VDDIO+0.5	V	
Latch-up Current	Iout	-	20	mA	All Pins

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are the stress ratings only and functional operation of the device at these or any other condition beyond those indicated may affect device reliability

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Temperature	T_A	-20	-	70	°C	
Analog and Digital supply voltage [1]	VDD	1.7	1.8	2.1	Volts	Including V_{NA} noise.
I/O supply voltage	VDDIO	1.65	1.8 or 2.8	3.6	Volts	Including V_{NA} noise. Sets I/O voltages.
Power supply rise time	t_{VRT}	0.001	-	10	ms	0 to VDD
Power supply off time for valid POR (power on reset)	t_{OFF}	10	-	-	ms	Refer to section "Power on Reset (POR) During Power Cycling"
Power off voltage level for valid POR (power on reset)	V_{OFF}	0	-	300	mV	Refer to section "Power on Reset (POR) During Power Cycling"
Supply noise (Sinusoidal)	V_{NA}	-	-	100	mVp-p	10 kHz – 50 MHz
Speed	SP	-	-	20	in/sec	Using prosthetic finger as surface
Transient Supply Current	I_{DDT}	-	-	80	mA	Max supply current for 500 usec for each supply voltages ramp from 0 to 1.8V

Notes:
1. Operating temperature of less than -20°C down to -30°C, minimum VDD of 1.8V must be met.
2. To ensure minimum leakage current, VDDIO should be greater than or equal to VDD

DC Characteristics

Electrical Characteristics over recommended operating conditions. Typical values at 25° C, VDD=VDDIO=1.8V at default LED setting 13 mA.

Parameter	Symbol	Typical	Max	Units	Notes
Average current in Run mode	I_{VDD}	2.90	4.03	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=pull high.
Average current in Rest1 mode	I_{VDD}	0.35	0.50	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=pull high.
Average current in Rest2 mode	I_{VDD}	0.07	0.12	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=pull high.
Average current in Rest3 mode	I_{VDD}	0.03	0.06	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=pull high.
Analog shutdown supply current	$I_{DDSHTDWN}$ VDD	1.54	26	uA	GPIO=pull low, SHTDWN=IO_MISO=NRST=pull high.

Electrical Characteristics over recommended operating conditions. Typical values at 25° C, VDD=VDDIO=1.8V at default LED setting 13 mA.

Parameter	Symbol	Min	Typ	Max	Units	Notes
VDDIO DC Supply Current	I VDDIO	-	-	20	uA	Average current VDDIO.
Digital peak supply current	I_{PEAK} VDD	-	-	10	mA	-
LED+ peak supply current	I_{PEAK} LED+	-	-	35	mA	At LED register setting of 27mA.
Input Low Voltage	V_{IL}	-0.05	0	V_{DDIO}*0.35	V	IO_MOSI_A0, IO_CLK, IO_MISO_SDA, IO_NCS_A1, NRST, SHTDWN, IO_SELECT
Input High Voltage	V_{IH}	VDDIO*0.7	VDDIO	VDDIO+0.05	V	IO_MOSI_A0, IO_CLK, IO_MISO_SDA, IO_NCS_A1, NRST, SHTDWN, IO_SELECT
Input hysteresis	V_{HYS}	100	-	-	mV	
Input leakage current	I_{leak}	-	±1	±10	uA	IO_MOSI_A0, IO_CLK, IO_MISO_SDA, IO_NCS_A1, NRST, SHTDWN, IO_SELECT
Output Low Voltage	V_{OL}	-	-	0.2	V	I_{out}=1.2mA
Output High Voltage	V_{OH}	VDDIO-0.2	VDDIO-0.1	-	V	I_{out}=600uA
Input Capacitance	C_{in}	-	-	10	pF	MOSI, NCS, SCLK, SHTDWN

Timing Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, VDD=1.8V.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Motion delay after reset	$t_{MOT-RST}$	3.5	-	23	ms	From Hard reset or SOFT_RESET register write to valid register write/read and motion, assuming motion is present
Shutdown	t_{SHTDWN}	-	-	50	ms	From SHTDWN pin active to low current
Wake from shutdown	t_{WAKEUP}	100	-	-	ms	From SHTDWN pin inactive to valid motion. Refer to section "Notes on Shutdown and Reset", also note $t_{MOT-RST}$
EVENT_INT rise time	$t_{r-EVENT\_INT}$	-	150	300	ns	C_L = 100pF
EVENT_INT fall time	$t_{f-EVENT\_INT}$	-	150	300	ns	C_L = 100pF
SHTDWN pulse width	$t_{P-SHTDWN}$	150	-	-	ms	
NRST pulse width	t_{NRST}	20	-	-	us	From edge of valid NRST pulse
Reset wait time after stable supply voltage	$t_{VRT-NRST}$	100	-	-	ms	

6.0 Operation Descriptions

Note on Power-up Sequence

Below is the power up sequence for PAW-A350:

1. Apply power.
2. Set NCS pin high, Shutdown pin low. Set IO_Select pin to low (for I2C) or high (for SPI).
3. If in I2C mode, set A0 and A1 according to the Table I2C slave address in datasheet. This step is skipped if SPI mode is used.
4. Read Product ID to ensure chip is powered up and communicating properly with host.
5. Write 0xC9 to address 0x61.

Note on Register Settings

Please refer to the PAW-A350_AN01_FW Guide for tuning of Speed Switching, Assert/De-assert, Finger Presence Detect and XY Quantization register settings.

Notes on Shutdown and Reset

The PAW-A350 can be set in Shutdown mode by asserting or setting SHTDWN pin high. During the shutdown state, supply voltages VDD must be maintained above the minimum level. If these conditions are not met, then the chip must be restarted by powering down then powering up again for proper operation. Any register settings must then be reloaded. During the shutdown state, supply voltage VDD must be maintained above the minimum level. For proper operation, SHTDWN pulse width must be at least tP-SHTDWN.

Shorter pulse widths may cause the chip to enter an undefined state. In addition, the SPI or I2C port of the chip should not be accessed when SHTDWN is asserted. Other devices on the same SPI bus can be accessed, as long as the chip's NCS pin is not asserted. The table below shows the state of various pins during shutdown. After deasserting SHTDWN, wait tWAKEUP before accessing the SPI port. Reinitializing the chip from shutdown state will retain all register data that were written to the chip prior to shutdown.

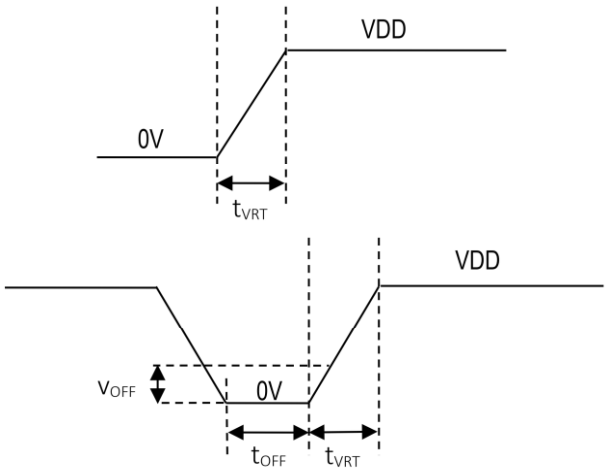
The reset of the chip via SOFT_RESET register or through the NRST pin would reset all registers to the default value. Any register settings must then be reloaded.

Pin	SHTDWN active
IO_NCS_A1	Functional*
IO_MISO_SDA	Undefined
IO_CLK	Undefined
IO_MOSI_A0	Undefined
EVENT_INT	Undefined
NRST	High
IO_Select	SPI:High, I2C
GPIO	Undefined

Note: There are long wakeup times from shutdown. These features should not be used for power management during normal chip motion.

Power on Reset (POR) During Power Cycling

tVRT is the power supply (VDD) rise time specification for a valid power on reset to happen when the chip is powered up from 0V to VDD. At condition whereby the VDD of the chip is cycled from VDD to 0 V and then to VDD again, the two parameters that govern a valid power on reset are vOFF and tOFF. Refer to timing diagram below.



Power Management Modes

The PAW-A350 has three power-saving modes. Each mode has a different motion detection period, affecting response time to chip motion (Response Time). The chip automatically changes to the appropriate mode, depending on the time since the last reported motion (Downshift Time). The parameters of each mode are shown in the following table.

Mode	Response Time (nominal)	Downshift Time (nominal)
Rest 1	19.5 ms	250 ms
Rest 2	96 ms	9.5 s
Rest 3	482 ms	582 s

EVENT_INT Pin

The Event_Int pin is a level-sensitive interrupt output that is used to trigger the host micro-controller when one of these events occurs:

- FPD – A change in finger state (finger on to finger off and vice versa) is detected
- Soft Click – Soft Click is detected
- Button – Mechanical button is asserted or de-asserted
- Motion – Motion delta is present.

A read to event register is required to determine the specific event that toggles the interrupt for user to act upon. The EVENT_INT will be reset after the user responds to it by reading the respective event status register:

- FPD – reading FPD_STATUS register (0x7a)
- Soft Click – reading SC_STATUS register (0x7f)
- Button – reading BUTTON_STATUS register (0x12)
- Motion – reading DELTA_X and DELTA_Y registers until motion are cleared.

GPIO Pin

The GPIO pin is a level-sensitive input/ output that can be used as

- FPD output – to display FPD status
- Pulse Width Modulated (PWM) output – to control LED driver to enable illumination feature in a product e.g. mobile phone
- Dome/ Button click input – can be connected to a dome switch that provides an input to the chip and when a click is detected, chip can respond by triggering button interrupt and channel the interrupt status through EVENT pin.

Refer to PAW-A350_AN01_FW Guide for more details and settings of registers for these features.

LED Mode

For power savings, the LED will not be continuously on. PAW-A350 will flash the LED only when needed.

I/O Pin Status Test

This feature allows the user to verify the connectivity and the state of the I/O pin. To run the test for input pins such as GPIO, SHUTDOWN, NRST and IO_SELECT, first enable the PAD_Chk_On bit (or bit-1) of OFN_Engine2 (0x61) register. Then write any value to PAD_STATUS (0x31) register to start the test. Wait for approximately 12us before reading the actual pin status and PAD_STATUS register. The test will be considered a PASS to indicate the chip is responding accordingly if the actual pin status matches PAD_STATUS register content. Refer to the table below for I/O pin status definition.

For output pins (EVENT_INT, GPIO, MOSI and MISO) testing, first enable bit-4 of PAD_FUNCTION (0x34) register. Then program or set the output state via PAD_TEST_OUT register (0x33) and do a READ on the actual pin status. Actual pin status results should match the output set in PAD_TEST_OUT. (Note: SPI/I2C communication will be disabled after this test is enabled. Once this test is completed, an external hardware reset on chip is required)

Bit(s)	Name	Reset	Description	Remarks
7:6	NRST_STATE	0x0	0x0: unknown	
			0x1: Low	Invalid as the chip will be in reset state.
			0x2: High	
			0x3: Hi-Z	Indicate a floating high
5:4	SHUTDOWN_STATE	0x0	0x0: unknown	
			0x1: Low	
			0x2: High	Invalid as the chip will be in shutdown state.
			0x3: Hi-Z	Indicate a floating low
3:2	GPIO_STATE	0x0	0x0: unknown	
			0x1: Low	
			0x2: High	
			0x3: Hi-Z	
1:0	IO_SELECT_STATE	0x0	0x0: unknown	
			0x1: Low	
			0x2: High	
			0x3: Hi-Z	

7.0 4-wire Serial Peripheral Interface (SPI)

SPI Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, VDD=1.8V.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Serial Port Clock Frequency	f_{sclk}	-	-	1	MHz	Active drive, 50% duty cycle
MISO rise time	$t_{r\text{-}MISO}$	-	150	300	ns	CL = 100pF
MISO fall time	$t_{f\text{-}MISO}$	-	150	300	ns	CL = 100pF
MISO delay after SCLK	t_{DLY_MISO}	-	-	120	ns	From SCLK falling edge to MISO data valid, no load conditions
MISO hold time	t_{hold_MISO}	0.5	-	$1/f_{SCLK}$	µs	Data held until next falling SCLK edge
MOSI hold time	t_{hold_MOSI}	200	-	-	ns	Amount of time data is valid after SCLK rising edge
MOSI setup time	t_{setup_MOSI}	120	-	-	ns	From data valid to SCLK rising edge
SPI time between write commands	t_{SWW}	30	-	-	µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI time between write and read commands	t_{SWR}	20	-	-	µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte.
SPI time between read and subsequent commands	t_{SRW} t_{SRR}	500	-	-	ns	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command.
SPI read address-data delay	t_{SRAD}	4	-	-	µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read.
NCS inactive after motion burst	t_{BEXIT}	500	-	-	ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS to SCLK active	$t_{NCS\text{-}SCLK}$	120	-	-	ns	From NCS falling edge to first SCLK falling edge
SCLK to NCS inactive (for read operation)	$t_{SCLK\text{-}NCS}$	120	-	-	ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer
SCLK to NCS inactive (for write operation)	$t_{SCLK\text{-}NCS}$	20	-	-	us	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer
NCS to MISO high-Z	$t_{NCS\text{-}MISO}$	-	-	500	ns	From NCS rising edge to MISO high-Z state

Synchronous Serial Port

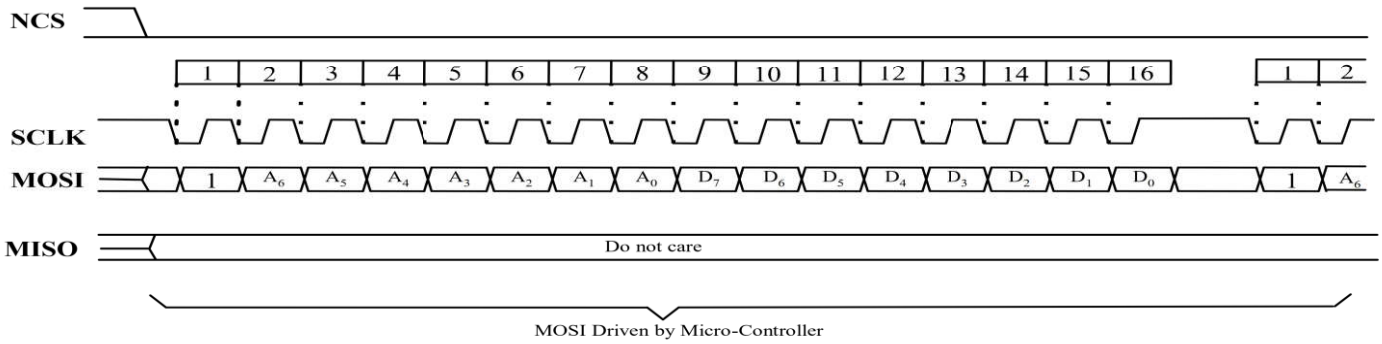
The synchronous serial port is used to set and read parameters in the PAW-A350, and to read out the motion information. The port is a four wire serial port. The host micro-controller always initiates communication; the PAW-A350 never initiates data transfers. SCLK, MOSI, and NCS may be driven directly by a micro-controller. The port pins may be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored and the output is tri-stated.

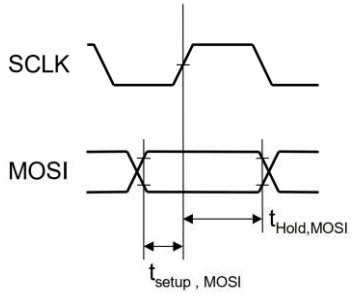
The lines that comprise the 4-wire SPI port :

SCLK - Clock input. It is always generated by the master (the micro-controller).
MOSI - Input data. (Master Out/Slave In)
MISO - Output data. (Master In/Slave Out)
NCS - Chip select input (active low). NCS needs to be low to activate the serial port; otherwise, MISO will be high Z, and MOSI & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. This is true for all transactions. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction. To improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because ESD events could be interpreted as serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.



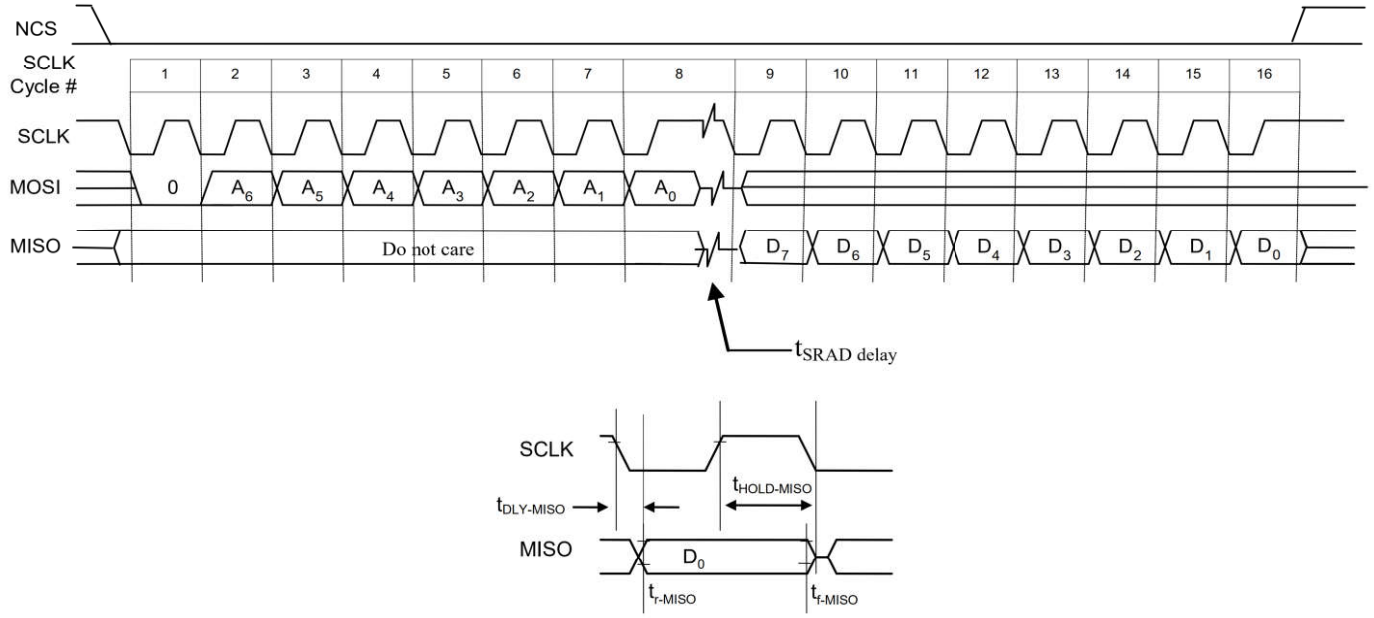


Write Operation

Write operation, defined as data going from the microcontroller to the PAW-A350, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The PAW-A350 reads MOSI on rising edges of SCLK.

Read Operation

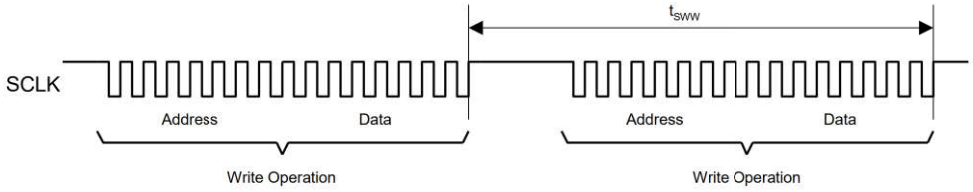
A read operation, defined as data going from the PAW-A350 to the micro-controller, is always initiated by the microcontroller and consists of two bytes. The first byte contains the address, is sent by the micro-controller over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the PAW-A350 over MISO. The chip outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.



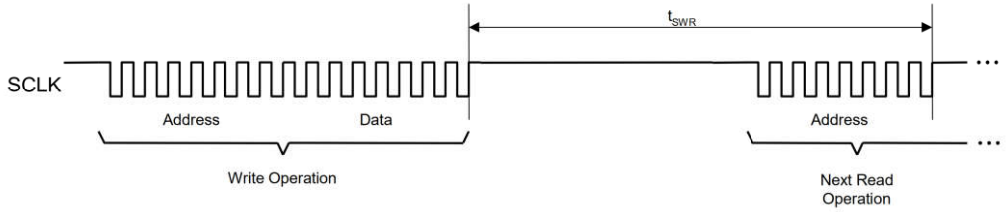
NOTE: The 0.5/fSCLK minimum high state of SCLK is also the minimum MISO data hold time of the PAW-A350. Since the falling edge of SCLK is actually the start of the next read or write command, the PAW-A350 will hold the state of data on MISO until the falling edge of SCLK.

Required Timing between Read and Write Commands

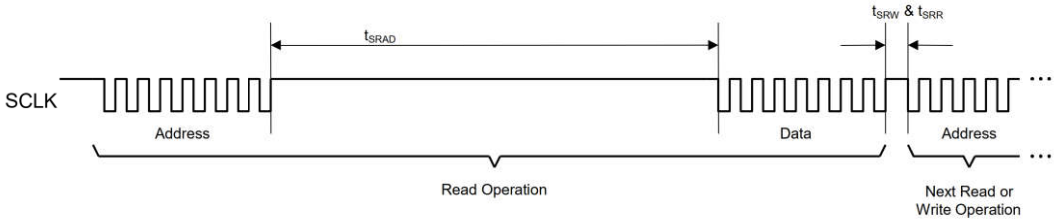
There are minimum timing requirements between read and write commands on the serial port.



If the rising edge of the SCLK for the last data bit of the second write command occurs before the required delay (t_{SWW}), then the first write command may not complete correctly.



If the rising edge of SCLK for the last address bit of the read command occurs before the required delay (tSWR), the write command may not complete correctly.

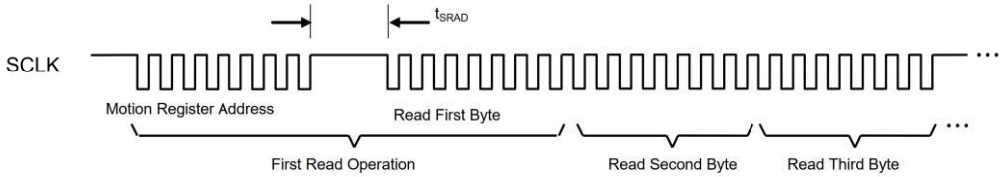


During a read operation SCLK should be delayed at least tSRAD after the last address data bit to ensure that the PAW-A350 has time to prepare the requested data. The falling edge of SCLK for the first address bit of either the read or write command must be at least tSRR or tSRW after the last SCLK rising edge of the last data bit of the previous read operation.

Burst Mode Operation

Burst mode is a special serial port operation mode that may be used to reduce the serial transaction time for a motion read. The speed improvement is achieved by continuous data clocking from multiple registers without the need to specify the register address, and by not requiring the normal delay period between data bytes.

Burst mode is activated by writing 0x10 to register 0x1c IO_MODE. Then the burst mode data can be read by reading the Motion register 0x02. The PAW-A350 will respond with the contents of the Motion, Delta_Y, Delta_X, SQUAL, Shutter_Upper, Shutter_Lower and Maximum_RawData registers in that order. The burst transaction can be terminated after the first 3 bytes of the sequence are read by bringing the NCS pin high. After sending the register address, the micro-controller must wait tSRAD and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data is latched into the output buffer after the last address bit is received. After the burst transmission is complete, the micro-controller must raise the NCS line for at least tBEXIT to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.



8.0 I2C Interface

I2C Interface Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25° C, VDD = 1.8 V.

Parameter	Symbol	Min	Max	Units	Notes
SCL clock frequency	fscl	-	400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	t_{HD_STA}	0.6	-	µs	
LOW period of the SCL clock	t_{LOW}	1.0	-	µs	
HIGH period of the SCL clock	t_{HIGH}	0.6	-	µs	
Set up time for a repeated START condition	t_{SU_STA}	0.6	-	µs	
Data hold time	t_{HD_DAT}	0[(2)]	0.9[(3)]	µs	
Data set-up time	t_{SU_DAT}	100	-	ns	
Rise time of both SDA and SCL signals	t_r	20+0.1C_b [(4)]	300	ns	
Fall time of both SDA and SCL signals	t_f	20+0.1C_b [(4)]	300	ns	
Set up time for STOP condition	t_{SU_STO}	0.6	-	µs	
Bus free time between a STOP and START condition	t_{BUF}	1.3	-	µs	
Capacitive load for each bus line	C_B	-	400	pF	
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 VDD	-	V	
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 VDD	-	V	

Notes:

1. All values referred to V_{IHMIN} and V_{ILMAX} levels.
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum has t_{HD_DAT} only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. C_B = total capacitance of one bus line in pF.

Device Salve Address

The PAW-A350 responds to one of the following selectable slave device addresses depending on the IO_MOSI_A0 and IO_NCS_A1 input pin state. These pins should be set to avoid conflict with any other devices that might be sharing the bus.

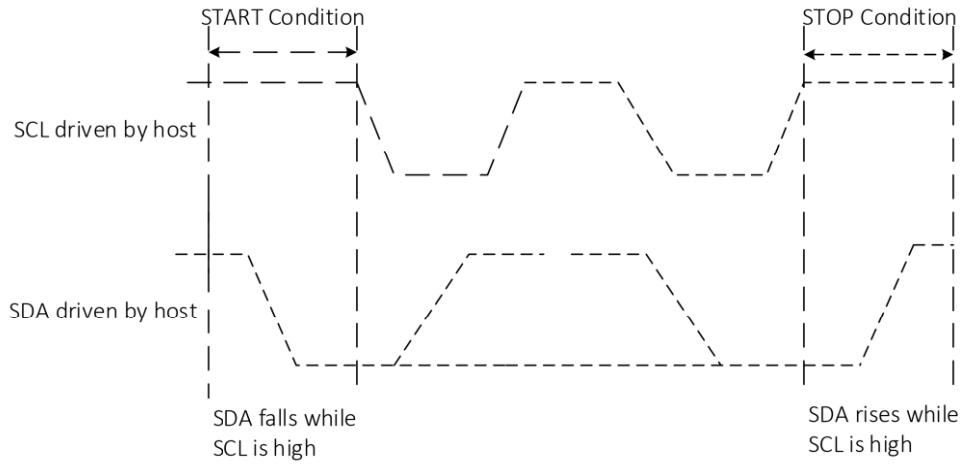
IO_MOSI_A0	IO_NCS_A1	Slave Address (Hex)
0	0	33
0	1	3b
1	0	53
1	1	57

Serial Transfer Clock and Serial Data Signals

The serial control interface uses two signals: a serial transfer clock (SCL) signal and a serial data (SDA) signal. Always driven by the master, SCL synchronizes the serial transmission of data bits on SDA. The frequency of SCL may vary throughout a transfer, as long as the timing is greater than the minimum timing. SDA is bi-directional. The host (master) can read from or write to the PAW-A350. The host (typically a microcontroller) drives SCL and SDA in a write operation or requesting information from the PAW-A350. The PAW-A350 drives the SDA only under two conditions. First, when responding with an acknowledge (ACK) bit after receiving data from the host, or second, when sending data to the host at the host's request. Data is sent in Eight-bit packets.

Start and Stop of Synchronous Operation

The host initiates and terminates all data transfers. Data transfers are initiated by driving SDA from high to low while holding SCL high. Data transfers are terminated by driving SDA from low to high while SCL is held high.



Acknowledge/Not Acknowledge Bit

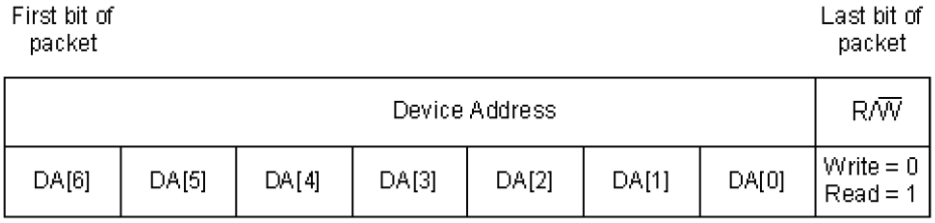
After a start condition, a single acknowledge/not acknowledge bit follows each Eight-bit data packet. The device receiving the data drives the acknowledge/not acknowledge signal on SDA. Acknowledge (ACK) is defined as 0 and not acknowledge (NAK) is defined as 1.

Packet Formats

Read and write operations between the host and the PAW-A350 use three types of host driven packets and one type of PAW-A350 driven packet. All packets are eight bits long with the most significant bit first, followed by an acknowledge bit.

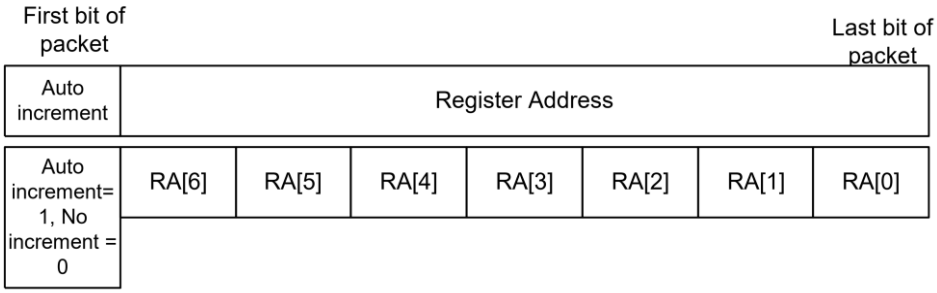
Slave Device Address (DA)

Command packets contain a 7-bit PAW-A350 device address and an active low read/write bit (R/W).



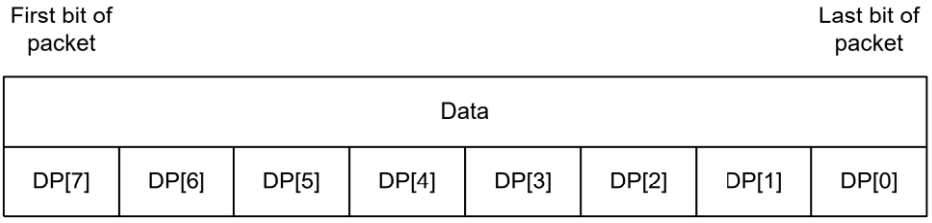
Register Address Packets (RA)

The address packets contain an auto-increment (ai) bit and a 7-bit address. If the 'ai' bit is set, the slave will process data from successive addresses in successive bytes. For example, registers 0x01, 0x02, and 0x03 can be written by setting the 'ai' bit to one with address 0x01. The host would send three bytes of data, and the host would terminate with a P condition.



Data Packet (DP)

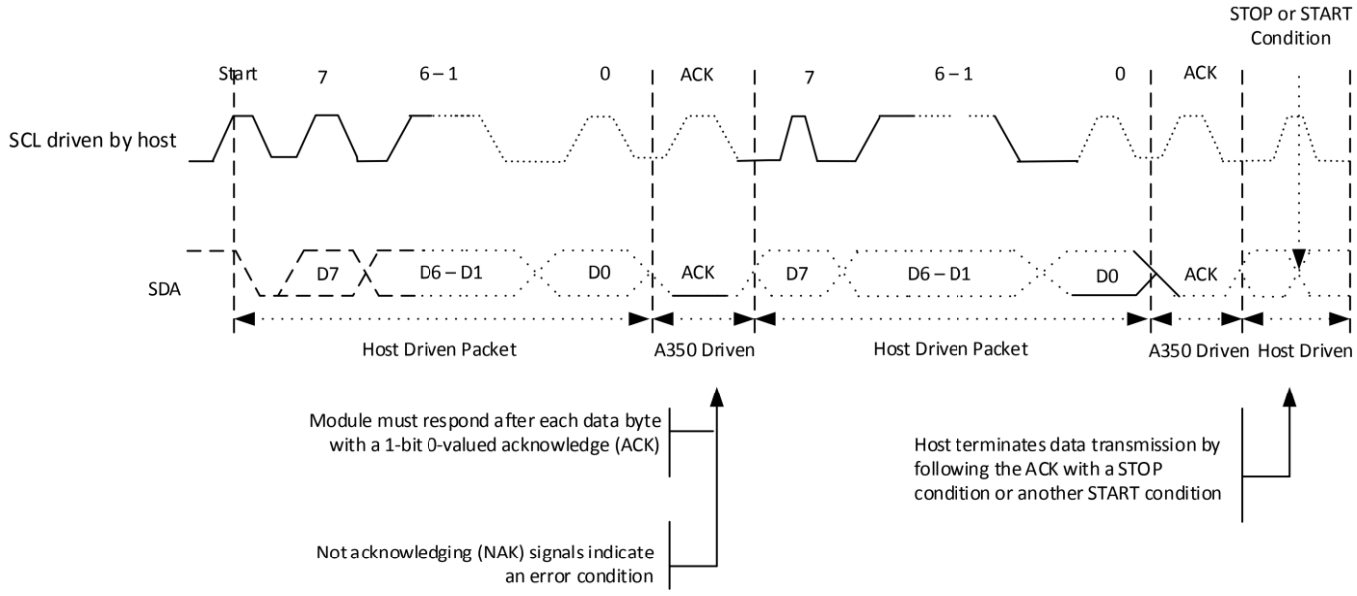
Contains 8 data bits and may be sent by the host or the PAW-A350.



Host Driven Packets

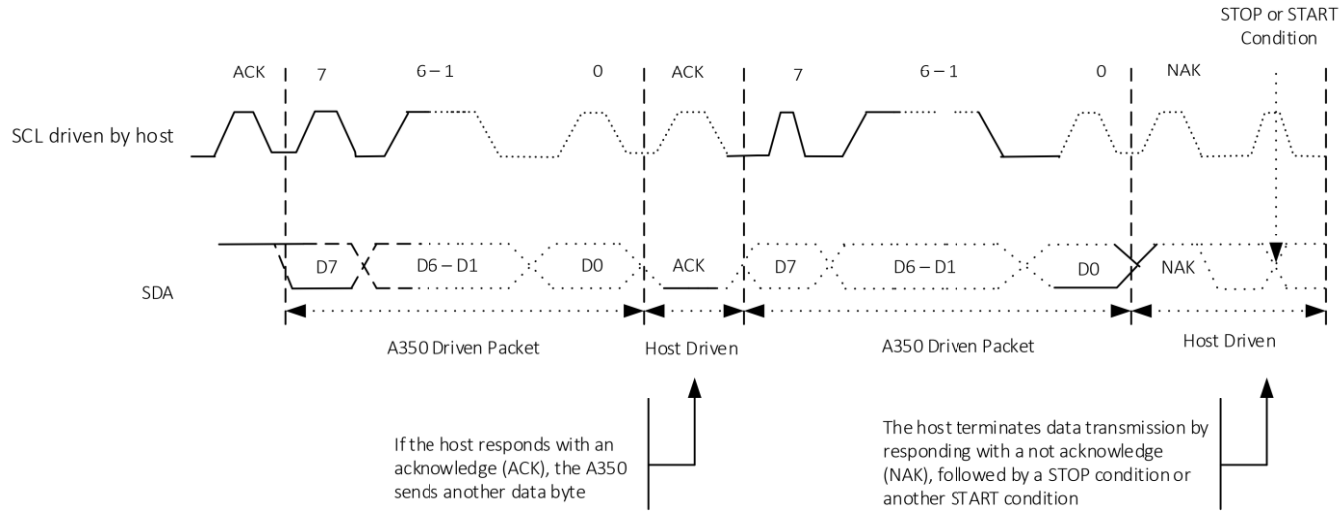
The host initiates all data transmission with a START condition. Next, slave address and register address packets are sent. If there is a device address match, the PAW-A350 then responds to each Eight-bit data transmission with an acknowledge signal (SDA = 0). Data is transmitted with the most significant bit first.

To terminate the transfer of host driven packets, the host follows the PAW-A350's ACK with a STOP condition. The host can also issue a START condition after the PAW-A350's ACK if it wants to start a new data transfer.



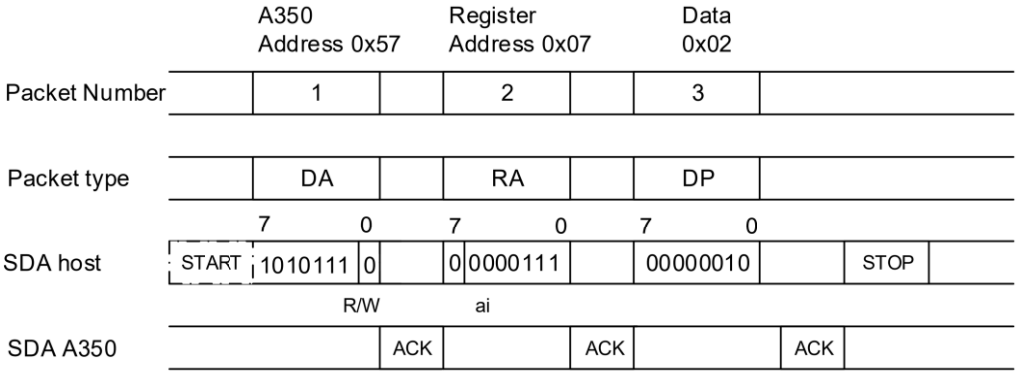
PAW-A350 Driven Packets

By request of the host, the PAW-A350 acknowledges a read request and then outputs a data byte transmitting the most significant bit (7) first. If the host intends to continue the data transfer, the host acknowledges the PAW-A350. If the host intends to terminate the transfer, it responds with not acknowledge (SDA = 1), and then drives SDA to generate a STOP condition. The host can also drive a START condition if it wants to begin a new data transfer with the same PAW-A350.



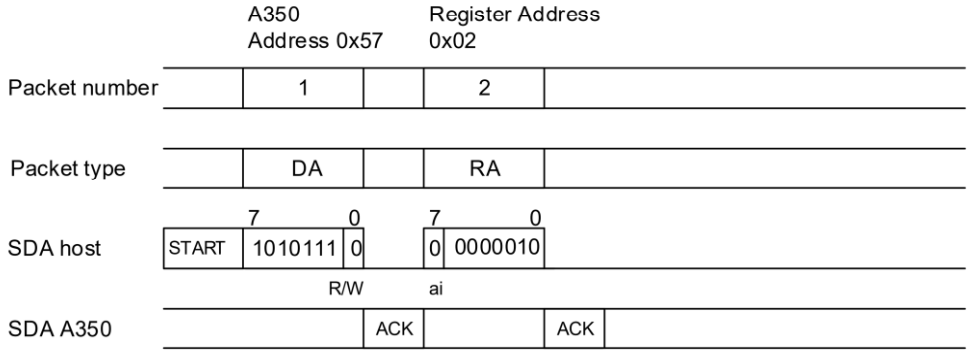
Example: Writing Data to Sensor Registers

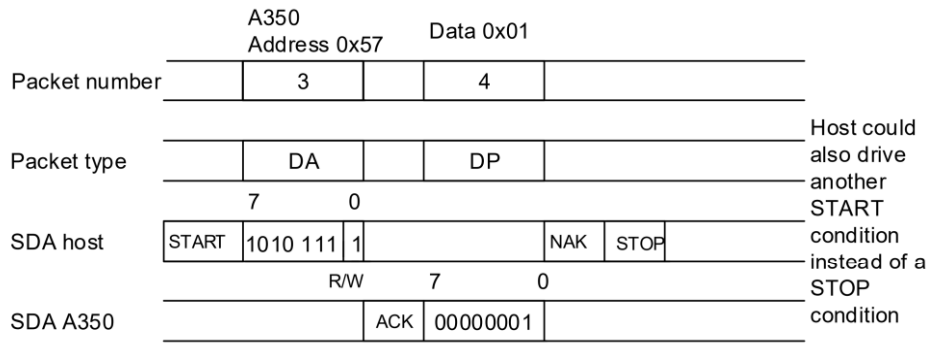
The host writes a value of 0x02 to address 0x07 in the following illustration. The example PAW-A350 address is 0x57.



Example: Single Byte Read from Sensor Register

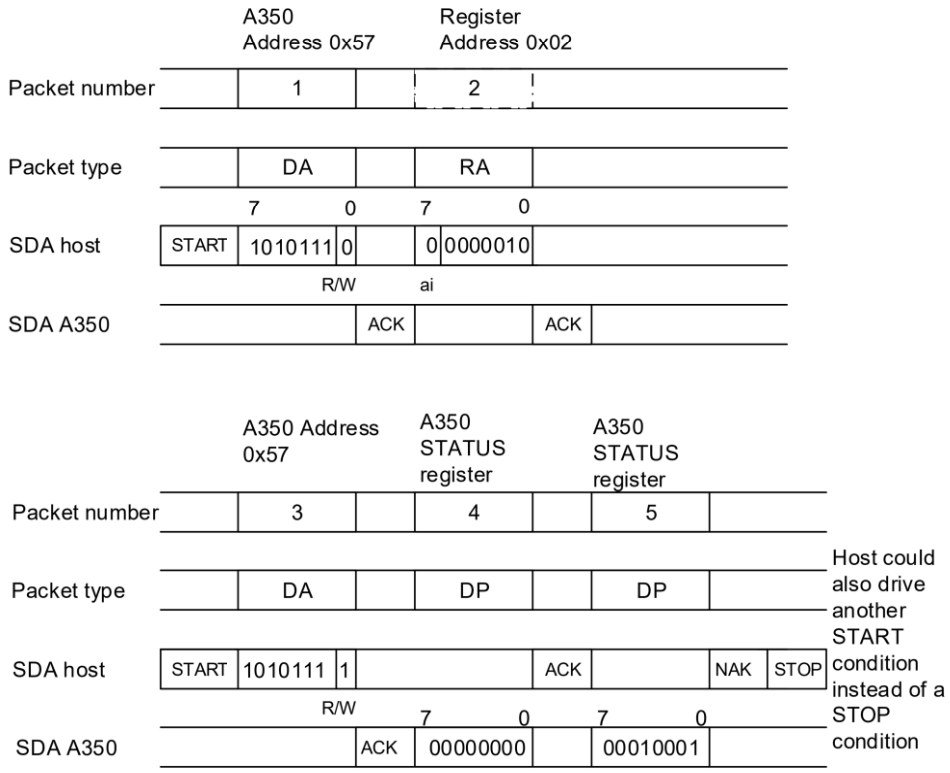
The sensor reads a value 0x01from the register address 0x02 in the following illustration. Again, the example PAW-A350 address is 0x57.





Example: Polling of Status Register (X-Y Motion Bit and Button bits)

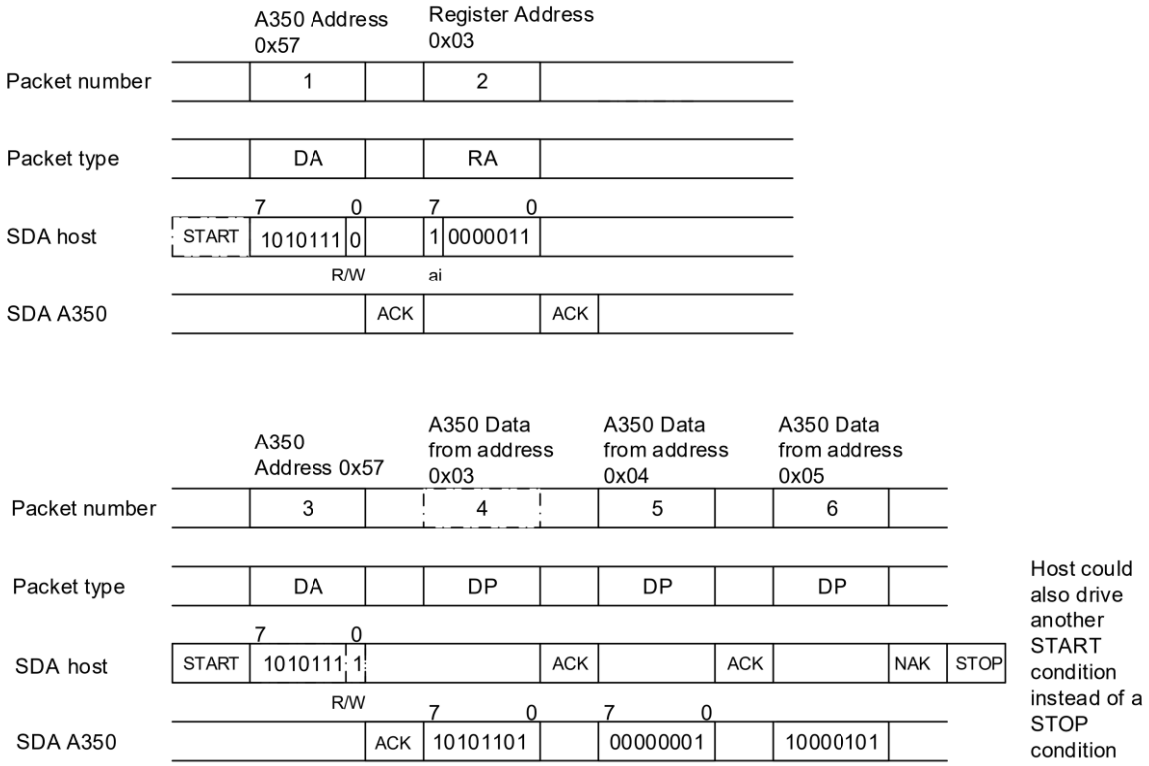
To poll the STATUS register, the following structure can be used:



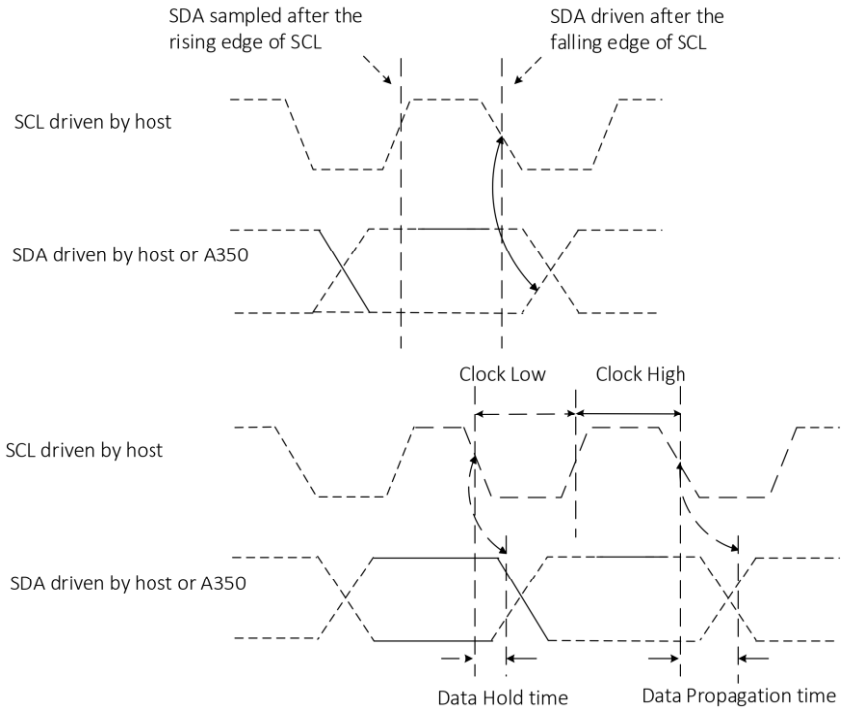
In this case, the host read PAW-A350 data packets until the update bit (bit 4). Then the host could read successive registers using the ai bit example below.
Note: polling the Status register rather than using the DATA_RDY pin increases power consumption

Example: Multiple-Byte Read from Sensor Register using 'ai' bit

The ai is a useful feature, especially in the case of reading Delta_X, Delta_Y, and Delta_HI in succession once either the DATA_RDY interrupt pin and/or update bit in the STATUS register bit are set.
Once the ai bit is set, the slave will deliver data packets from successive addresses until the 'STOP' condition from the host. In the example below, 3 bytes are read successively from registers 0x03, 0x04 and 0x05.



SCL and SDA Timing



PAW-A350 driven SDA