PAF9701C1: Low Power IR Thermal Array Sensor

General Description

The PAF9701C1 is an 8 x 8 pixels low-power infrared (IR) thermal array sensor with integrated temperature computation function. It measures a target object's temperature (To) without direct contact the object. The object temperature is converted from the voltage of the thermal array sensor and ambient temperature Sensor (Ta). Both temperatures will be calibrated with built-in calibration coefficients which stored in the internal memory.

The chip supports one-shot operation and four continuous operation modes with different report rate. And It also offers three alert mode based on low power and application requirements.

The low power consumption advantage makes this thermal array sensor is ideal for battery-operated cordless applications.

Key Features

- Integrated MEMS thermal array for non-contact temperature measurement
- 16-bit object temperature data length
  - *Accuracy ±1°C @ To 32 to 40°C and Ta 15 to 40°C
  - Resolution : 0.0625°C
  - FOV : 60°
- 16-bit ambient temperature data length
  - Accuracy ±0.5°C @15°C to 45°C
  - Resolution : 0.03125°C
- Integrated temperature computation function
  - Direct output object temperature
  - Programmable alert temperature
  - Built-in memory for calibration coefficients.
- I/O interface
  - Support two-wire I²C, 400kbps
  - Support two programmable I²C addresses
- Integrated operation mode for difference report rate request
  - Programmable report rate
  - Normal operation mode for full run application.
  - Three detection mode for slow report rate and low power requirement.
- Embedded Emissivity and Decay compensation
- Low power design

Applications

- Non-Contact Object temperature sensing
- Smart Appliance-Non-contact temperature monitor
- Temperature feedback control application.
- Human detection

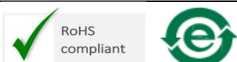
Key Parameters

Parameter	Value
Operating Temp.	-20 to 85 °C
Object Temperature, To	Measurement Range: -20 to 380°C
	*Accuracy :±1°C @ To:32 to 40°C , Ta:15 to 40°C
Ambient Temperature, Ta	Measurement Range : -20 to 85 °C
	Accuracy : ±0.5°C @ 15°C to 45°C
Supply Voltage	VDDMA: 3.0 to 3.6 V VDDIO: 1.62 to 3.6 V
Typical Current Consumption @ 3.3V, Report Rate = 10Hz	Operation: 2 mA Suspend: TBD µA **Note:** pure chip current without I/O toggling. Normal mode @ $t_{CONVERSION}$ < t_{REPORT}
Package Size	8 x 8 x 3.85 mm³

Note: * The higher accuracy could be tuned to optimize for application requiring narrow object temperature range (such as body temperature). For more information, please approach your PixArt local contact.

Ordering Information

Part Number	Description	Package Type	Packing Type	MOQ
PAF9701C1	Thermal Array Sensor	Ceramic	Tray	TBD



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1.0 Introduction

1.1 Overview

The PAF9701C1 is an 8 x 8 pixels low-power infrared (IR) thermal array sensor with integrated temperature computation function. It measures a target object's temperature (To) without direct contact the object. The object temperature is converted from the thermal array sensor and ambient temperature sensor (Ta). Both temperatures will be calibrated with built-in calibration coefficients which stored in the internal memory.

It offers a one-shot operation and four continuous operation mode (normal operation and detection 1/2/3 operation mode) with difference report rate and low power requirements. It also offers three alert modes where there are normal interrupt, absolute value interrupt and difference interrupt output mode base on application requirements.

PAF9701C1 supports wide temperature range measurement from -20 to 380°C with 60° FOV. It offers normal and compare output mode base on application requirements. The low power consumption advantage makes this thermal array sensor is ideal for battery-operated cordless applications. The communication I/O interface is two-wire I^2C with speed up to 400kbps.

Note: Throughout this document, the PAF9701C1 is referred to as the "chip".

1.2 Block Diagram

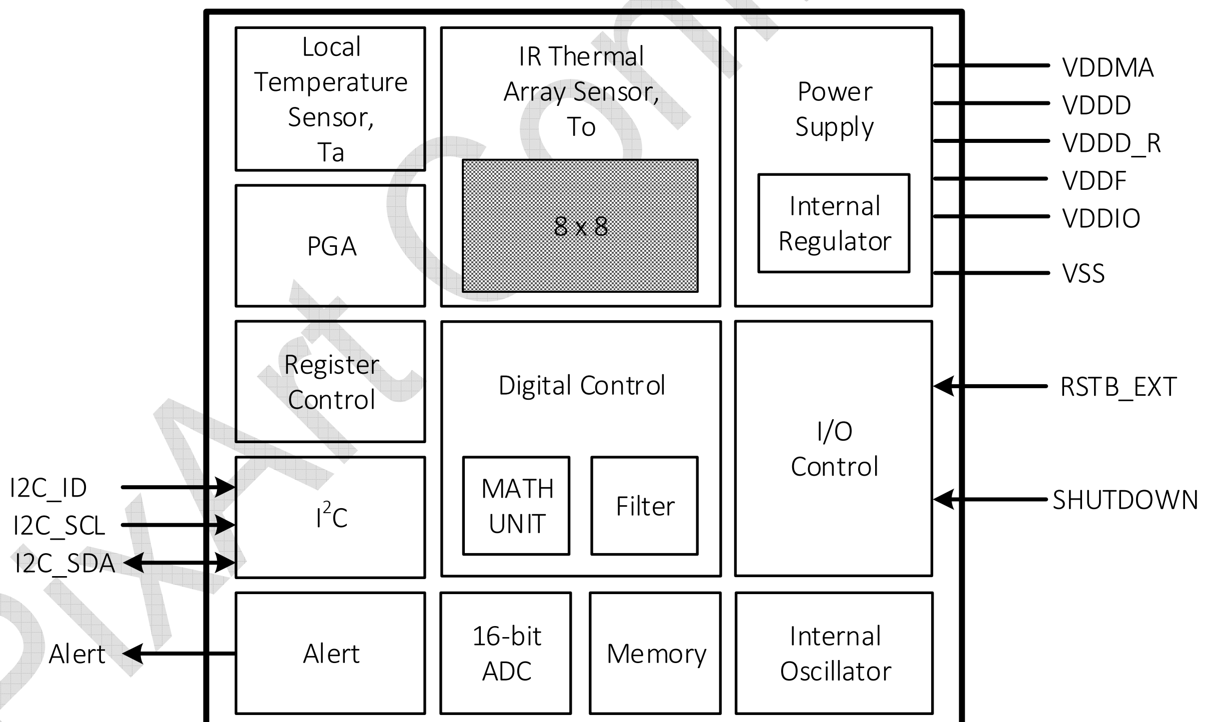

Figure 1. Functional Block Diagram

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1.3 Terminology

Term	Description
Ta	Ambient temperature
To	Object temperature
FOV	Field of View

1.4 Signal Description

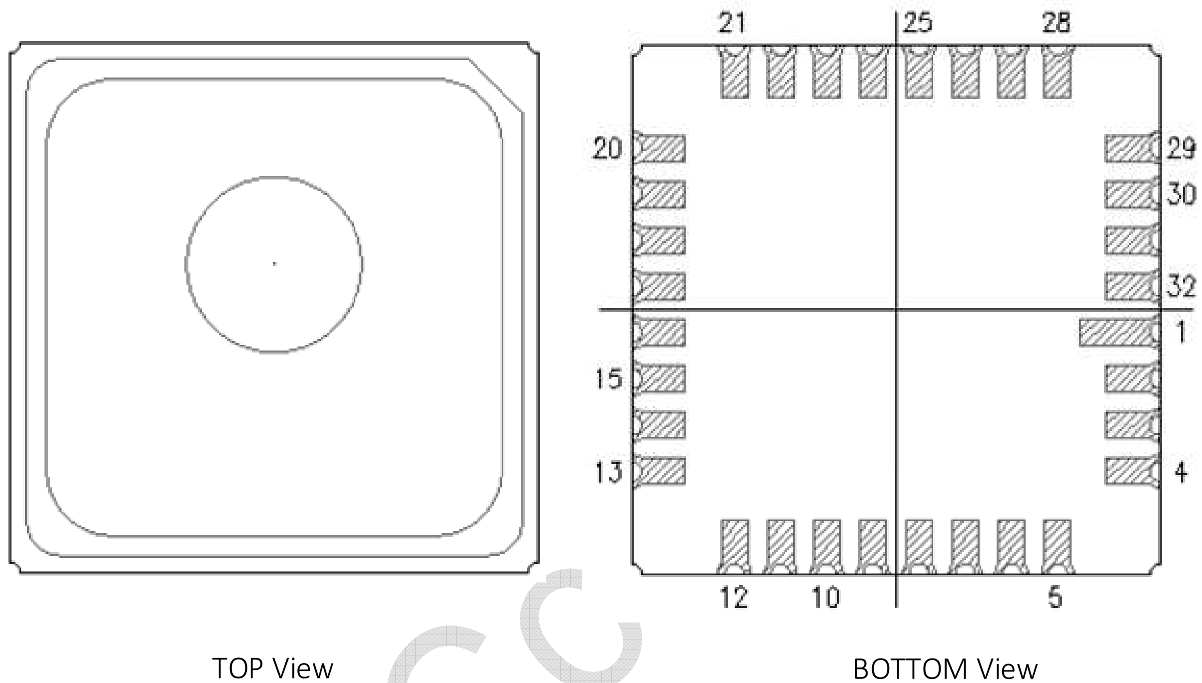

Figure 2. Pin Configuration

Table 1. Signal Pins Description

Function	Pin No.	Signal Name	Type	Description
Power Supplies	1	VSS	Ground	Ground
	2	VSS	Ground	Ground
	3	VDDD_R	Output	Digital power supply. Connect 1µF capacitor to Ground than connect to VDDD.
	4	VDDD	Input	Digital power supply
	5	VDDF	Input	Flash power supply for integrate flash. Connect to VDDMA with 1µF and 0.1µF capacitor to Ground.
	12	VDDIO	Input	I/O Power Supply (1.62 to 3.6V) Connect 1µF and 0.1µF capacitor to Ground.
	13	VSS	Ground	Ground
	19	VSS	Ground	Ground
	32	VDDMA	Input	Main power supply (3.0 to 3.6V) for internal power regulator. Connect 1µF and 0.1µF capacitor to Ground.
Interface	15	I2C_SCL	Input	I^2C clock pin
	16	I2C_SDA	I/O	I^2C bidirectional data pin.

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Function	Pin No.	Signal Name	Type	Description
Functional I/O	9	Alert	Output	Alert output pin; active low It can be programmed register 0x2F bit[0] as a push-pull or open drain. Push-pull is default.
	11	I2C_ID	Input	I²C 7-bit address selection pin High: I²C ID = 0x57 Low/ Floating: I²C ID = 0x34.
	14	RSTB_EXT	Input	Hardware reset pin; active low Floating when not in use.
	17	SHUTDOWN	Input	Shutdown pin; active high High: the chip enters shutdown state and I²C interface is disabled. Low/ Floating: chip normal operation
TEST	10	TEST1	NC	Test Pin. Floating.
	18	TEST2	NC	Test Pin. Floating.
Reserved pin	6 to 8 20 to 31	NC1	NC	Reserved. Floating or connect to Ground

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2.0 Operating Specification

2.1 Absolute Maximum Rating

Table 2. Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	-25	105	°C	
Lead-free Solder Temperature	T_P	-	245	°C	Refer to Section 4.3 Assembly Guide
Main Power Voltage	$VDDMA_{MAX}$	-0.4	3.6	V	
Flash Power Voltage	$VDDF_{MAX}$	-0.4	3.6	V	
I/O Voltage	$VDDIO_{MAX}$	-0.4	3.6	V	
I/O Pin Input High Voltage	$VDDIO_{IN}$	-0.4	VDDIO + 0.3	V	All I/O pins
Relative Humidity	RH	TBD	TBD	%	Non-condensing, Non-biased
ESD	ESD_{HBM}	-	TBD	kV	Class 2 on all pins. Human body model, JESD22-A114E.

Notes:

1. At room temperature.
2. If the chip operated beyond the maximum rating values, it may cause device damage.
3. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability.

2.2 Recommended Operating Condition

Table 3. Recommended Operating Condition

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Temperature	T_{OP}	-20	-	85	°C	
Main Power Supply Voltage	VDDMA	3.0	3.3	3.6	V	Power regulator input supply. Includes ripples
Memory Power Supply Voltage	VDDF	3.0	3.3	3.6	V	Power regulator input supply. Includes ripples
Digital Supply Voltage	VDDD	1.62	1.8	1.98	V	Digital power input. Includes ripples
I/O Supply Voltage	VDDIO	1.62	3.3	3.6	V	Includes ripples
I^2C Speed	SCL_I^2C	-	-	400	kHz	Max value for Fast mode

Note: PixArt does not guarantee the performance if the operating temperature is beyond the specified limit.

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2.3 DC Characteristic

Table 4. DC Electrical Specification

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Regulator Output	VDDD_R	1.62	1.8	1.92	V	For internal used.
Peak Power Supply Current	I_{DDMA_MAX}	-	2.2	-	mA	For VDDMA @ $t_{CONVERSION} < t_{REPORT}$
Peak I/O Supply Current	I_{DDIO_MAX}	-	0.3	-	µA	For VDDIO @I²C 400kHz
Power Consumption						
Main Supply Current @ Suspend	$I_{DDMA_SUSPEND}$	-	TBD	TBD	µA	For chip only Suspend without I²C signal toggling
Main Supply Current @ Operation	$I_{DDMA_OPERATION}$	-	2	TBD	mA	$t_{CONVERSION} < t_{REPORT}$ T_O Number=2^9 T_A Number = 2^7 Report Rate = 10Hz
Flash Supply Current @ Boot-load	I_{DDF_READ}			6	mA	
Flash Supply Current @ Boot-load done	$I_{DDF_STANDBY}$			2	uA	
I/O						
Input High Voltage	V_{IH}	0.7 x VDDIO	-	-	V	
Input Low Voltage	V_{IL}	-	-	0.3 x VDDIO	V	
Output High Voltage	V_{OH}	VDDIO - 0.4	-	VDDIO + 0.4	V	
Output Low Voltage	V_{OL}	-0.4	-	0.4	V	

Notes: All the parameters are tested under operating conditions: VDDMA = 3.3V, VDDIO = 1.8 and 3.3V, T_A = 25°C

2.4 AC Characteristic

Table 5. AC Electrical Specification

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Power up from V_{DDMA} Rising	t_{PU}	200	-	-	ms	From V_{DDMA} rising to valid interface communication
Chip Pulse Interrupt Width	t_{INT}	-	5	-	µs	One-shot mode only.
Sensor settling time	t_{SETTLE}		3		sec	Thermal equilibrium and ready for the conversion.

Notes: All the parameters are tested under operating conditions: T_A = 25°C, VDDMA = 3.3V, VDDIO = 3.3V for 3.3V IO application and VDDIO = 1.8 V for 1.8V IO application.

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2.5 Optical FOV Specification

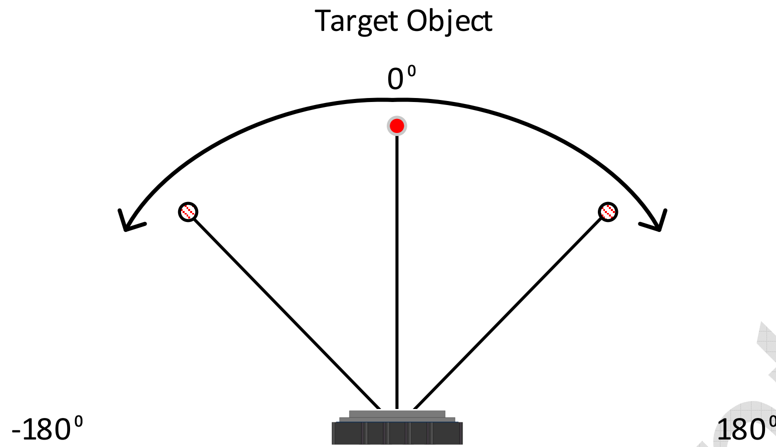


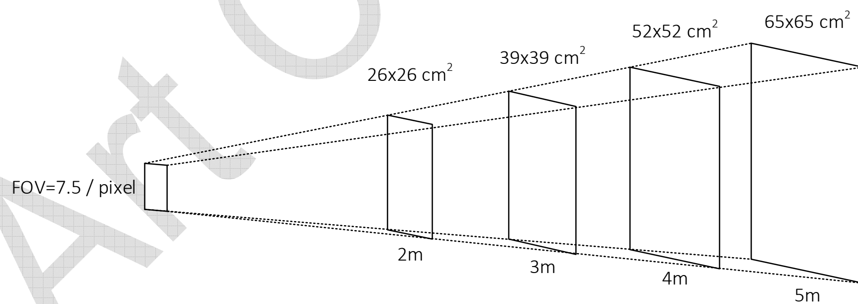
Figure 3. FOV Measurement Setup

TBD

Figure 4. FOV Angle

Table 6. Field Of View

Parameter	50% of Maximum
FOV H angle	60 ± 10 °
FOV V angle	60 ± 10 °



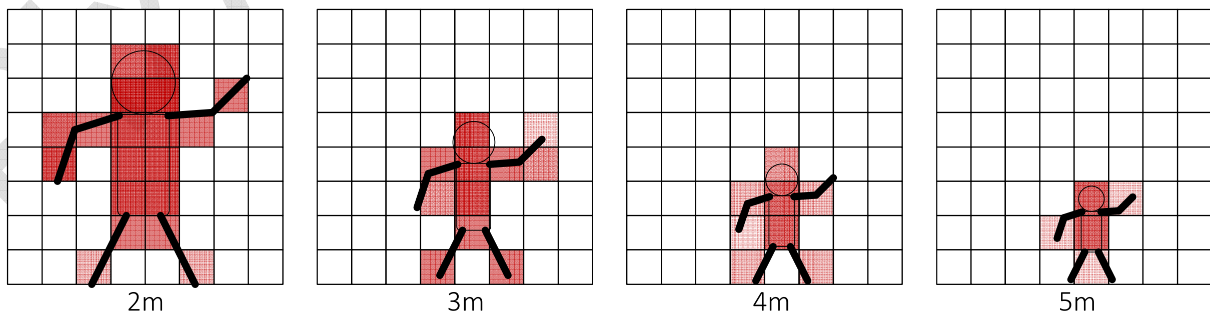


Figure 5. Pixel Sensing Area

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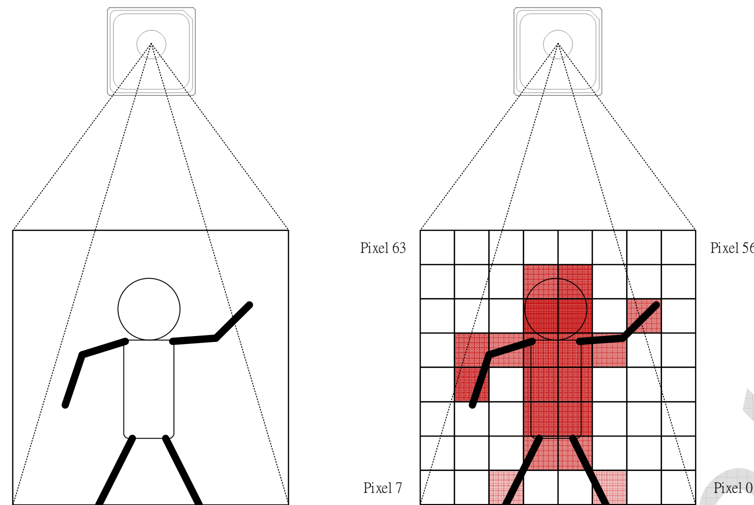

Figure 6. Thermal Array

2.6 Performance

2.6.1 Accuracy

All the sensor unit will be calibrated before delivery. All the calibration and thermal transient coefficients' data is stored in integrated memory. The accuracy specifications listed in Table 7. Accuracy Specification are based on below conditions.

- Under the isothermal conditions
- At VDDMA = 3.3V
- The target object needs to be larger than FOV
- The emissivity of the object is 0.98.
- Ta and To sampling numbers are set to 128 and 512, refer to Section 8.1.6 for details.

Table 7. Accuracy Specification

Parameters	Temperature Sensing Range	Accuracy
T_object, To	To =32 to 40 °C and Ta=15 to 40 °C	*±1°C
T_ambient, Ta	Ta =15 to 45 °C	±0.5°C
	Ta =0 to 85 °C	±1°C

Note:

*The higher accuracy could be tuned to optimize for application requiring narrow object temperature range (such as body temperature). For more information, do approach your PixArt local contact.

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3.0 Mechanical Specification

3.1 Mechanical Dimension

Offset of optical center position and chip center position is 0.65mm.

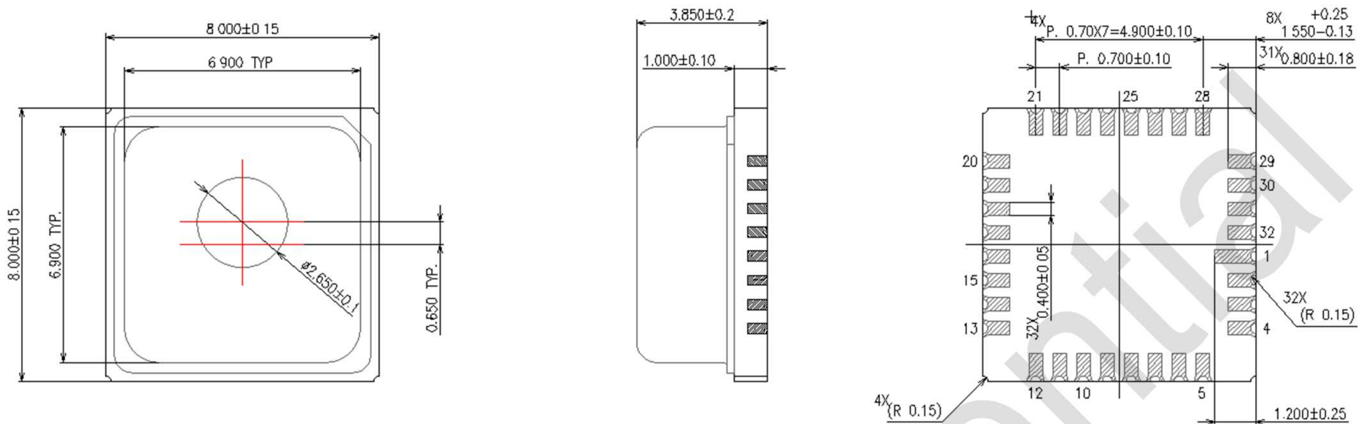

Figure 7. Package Outline Drawing

3.2 Package Marking

Refer to Figure 8. Package marking for the code marking location on the chip package.

TBD

Figure 8. Package Marking

3.3 Packing Information

3.3.1 Carrier Drawing

Table 8. Packing Information

Parameter	Quantity	Unit	Note
Chips per tray	TBD	piece	
Trays per stack	TBD	tray	Plus a top cover on top of each stack. Refer to Figure 9.
Stacks per packing bag	TBD	stack	Refer to Figure 10.
Packing bags per packing box	TBD	bag	Refer to Figure 11.
Max. chips per packing box	TBD	piece	

Figure 9. Stack 5 +1 JEDEC Tray

Figure 10. Al Packing Bag

Figure 11. Packing Box

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3.3.2 Unit Orientation

Packing method of using JEDEC Tray. CLCC Pin 1 orientation towards the edge of the JEDEC tray chamfer location.

TBD

Figure 12. Orientation

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4.0 Design Reference

4.1 Reference Schematic

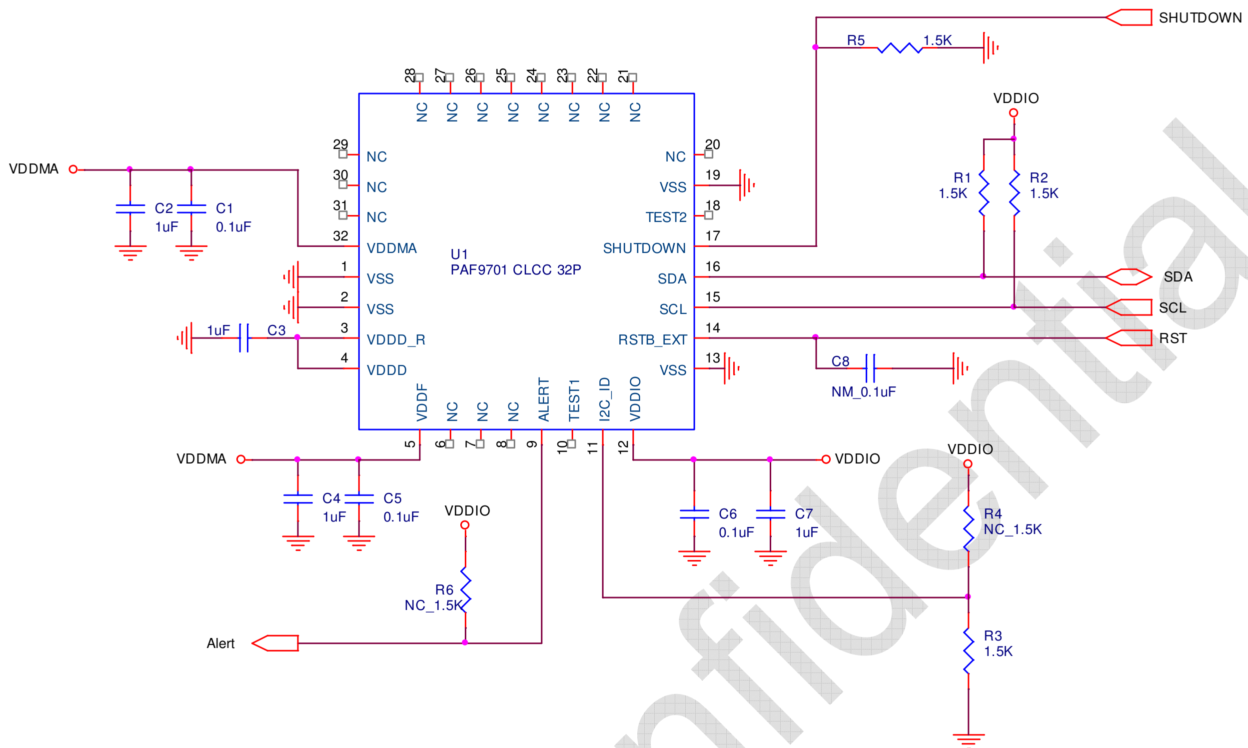

Figure 13. Reference Schematic

Notes:

1. VDDMA=3.0 to 3.6V, VDDF=3.0 to 3.6V, VDDIO=3.3V for 3.3V system.
2. VDDMA=3.0 to 3.6V, VDDF=3.0 to 3.6V, VDDIO=1.8V for 1.8V system.
3. I2C_SDA and I2C_SCL are open drain output and must pull high to VDDIO
4. Alert pin can be programmed as a push-pull or open drain (push-pull is the default setting) and recommend connect to the MCU GPIO as data ready for power saving.
5. VDDMA, VDDF and VDDIO, connect 1µF and 0.1µF capacitor to the ground and place close to the chip.
6. VDDD_R connect 1µF capacitor to the ground and place close to the chip then connect to VDDD.
7. For this reference, I2C_ID address is setting 0x34 and chip in normal operation (shutdown pin is setting to low).

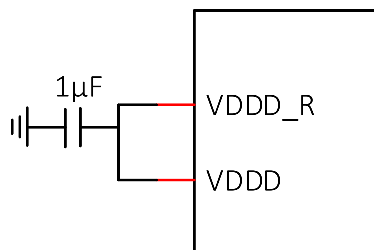

Figure 14. VDDD_R and VDDD Layout Path

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4.2 PCB Layout Design Guide

4.2.1 Recommended IC Footprint Layout

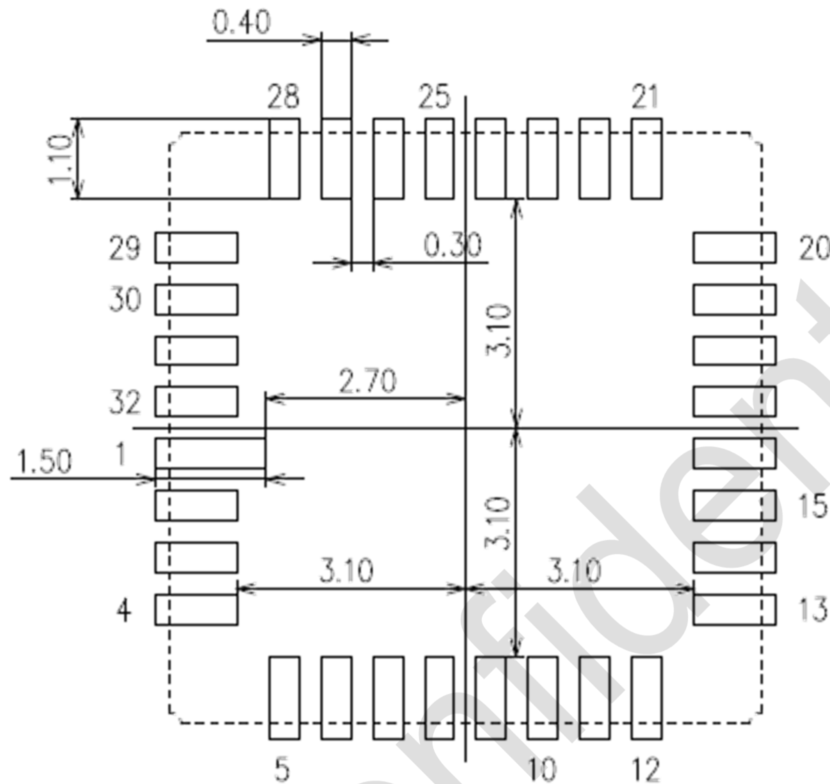

Figure 15. Recommend Package Footprint Layout (unit in mm)

4.2.2 Layout Guideline

1. Minimum 10 mils traces width for VDDMA, VDDF, VDDIO, VDDD and VSS.
2. Place capacitors close to the chip.
3. Keep chip away from any heat sources (e.g., MCU, power source, etc.).
4. VDDD_R connect 1µF capacitor to the ground and place close to the chip then connect to VDDD.

4.2.3 FPC Stiffener Design

For FPC board design, a stiffener at the FPC bottom side is required to strengthen the board.

Recommended stiffener:

1. FR4 with minimum thickness of 0.4mm.
2. Stainless steel with minimum thickness 0.15mm.

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4.3 Assembly Guide

4.3.1 Recommended Pb-free Solder Paste

1. Almit LFM-48W TM-HP
2. Senju M705-GRN360-K

4.3.2 IR Reflow Solder Profile

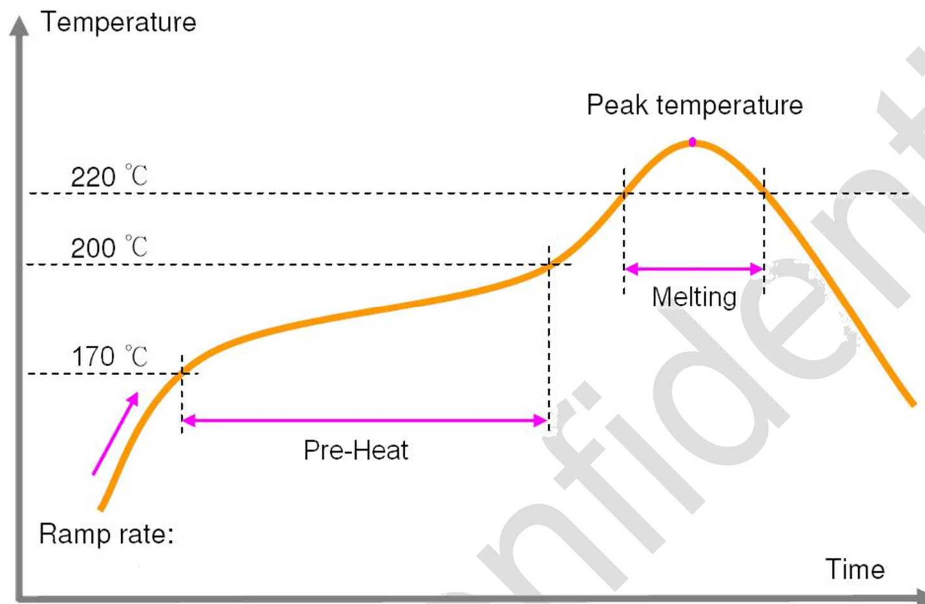

Figure 16. IR Reflow Soldering Profile

Parameter	Symbol	Min	Max	Unit	Note
Ramp-up slope to preheat area	T_{RAMP}	1.5	2.5	°C/sec	From 30 °C to preheat Area
Preheat area temperature	T_{PRE}	170	200	°C	
Preheat area duration	t_S	60	120	sec	
Melting duration	t	30	90	sec	Melting area temp ≥220 °C
Melting Temperature	T_{MELT}	220	245	°C	

4.3.3 Stencil for SMT process.

Recommended SMT process, stencil thickness from 0.1 to 0.12 mm.

1. The stencil thickness selection will need to consider passive component around the chip.
2. For surface mounted chip on FPC, the cover layer and adhesive layer total thickness recommended to be less than 40 µm.
3. The recommended ratio of the stencil opening to the pad size is 1:1.

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