Design Example Report

Title	***15 W Isolated Flyback Power Supply with StackFET Using InnoSwitch™3-AQ INN3996CQ***
Specification	30 VDC – 1200 VDC Input; 12 V / 1.25 A Output (>60 VDC Input)
Application	High Input Voltage for Automotive
Author	Applications Engineering Department
Document Number	DER-889Q
Date	April 20, 2021
Revision	1.2

Summary and Features

- High input voltage: up to 1200 VDC
- InnoSwitch3-AQ – industry first AC/DC ICs with isolated, safety rated integrated feedback
- Built-in synchronous rectification for >82% efficiency
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
  - Extremely fast transient response independent of load timing

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using a DC supply to provide the DC input to the prototype board.

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1 Introduction

This document is an engineering report describing a 30 VDC to 1200 VDC input, 12 V output, 15 W (maximum) power supply utilizing INN3996CQ from Power Integrations. The document contains the power supply specification, schematic, bill-of-materials and basic performance data.

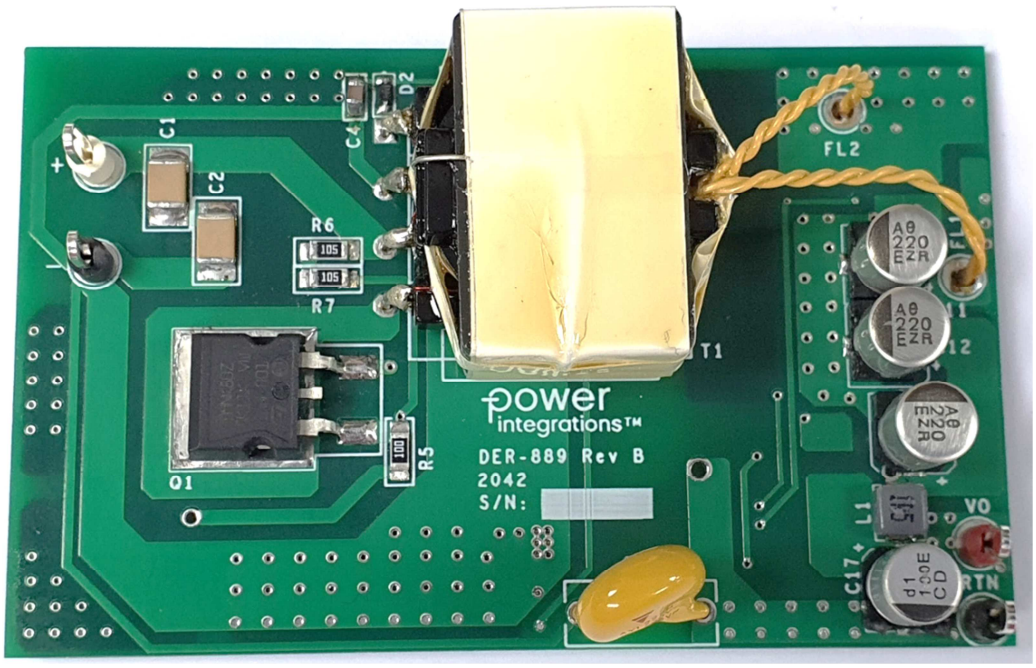

Figure 1 – Populated Circuit Board Photograph, Top.

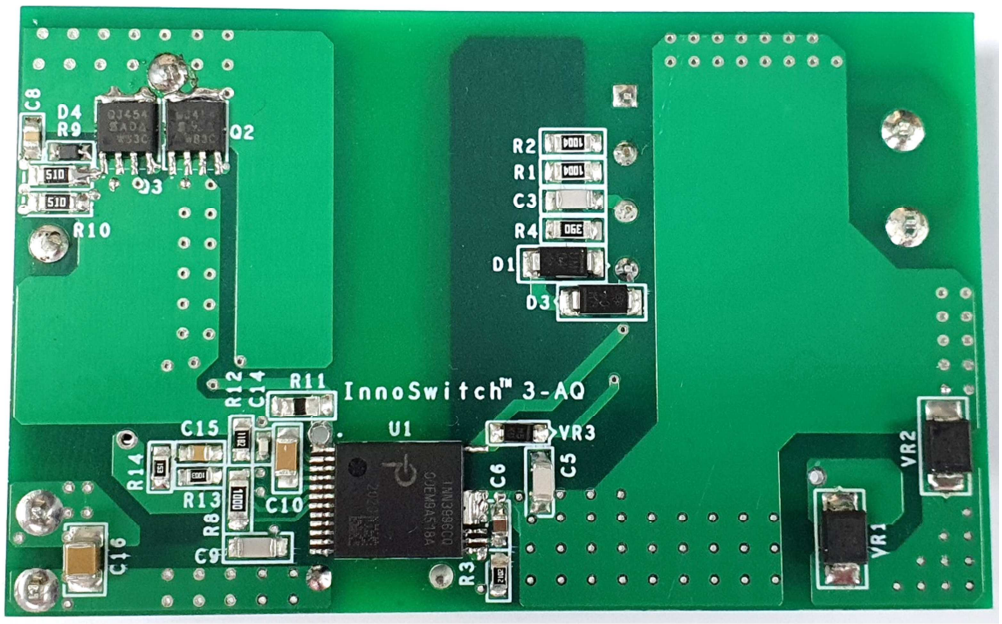

Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	$\mathbf{V_{IN}}$	30	800	1200	VDC	For Electric Vehicle Emergency PSU.
Maximum Output Power						
	$\mathbf{P_{OUT}}$			2.2	W	V_{IN} of 30 VDC, P_{MAX} < 0.75 W for Start-up, P_{MAX} < 2.2 W for Reducing Input Voltage
	$\mathbf{P_{OUT}}$			15	W	V_{IN} of 60 VDC to 1200 VDC.
Output						
Output Voltage	$\mathbf{V_{OUT}}$		12		V	±5% (V_{IN} > 400 VDC).
Output Current	$\mathbf{I_{OUT}}$			1.25	A	
Output Ripple Voltage	$\mathbf{V_{RIPPLE}}$			300	mV	On Board.
Isolation						Meets IEC 60664-1 as a Minimum. Reinforce Better.
Ambient Temperature	$\mathbf{T_{AMB}}$	-40			W	

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3 Schematic

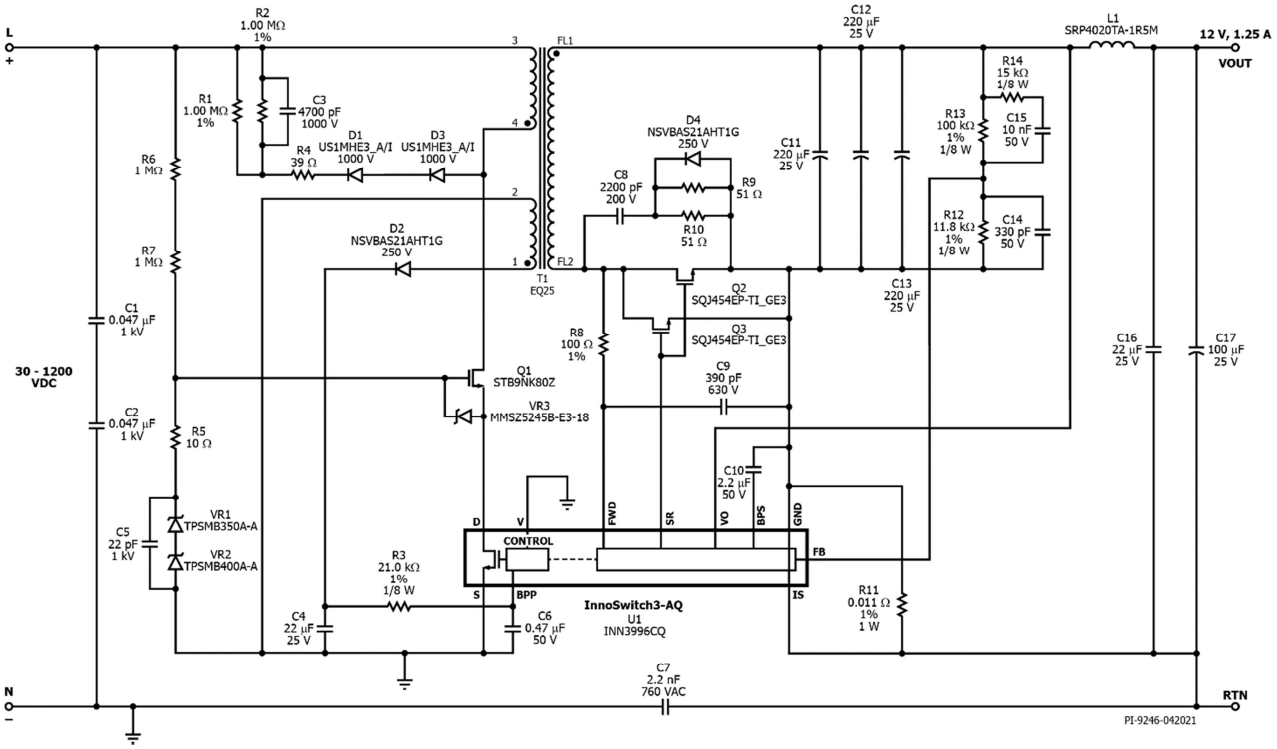

Figure 3 – Schematic.

4 Circuit Description

4.1 *INN3996CQ IC Primary*

One end of the transformer primary is connected to the DC bus. The other is connected to a high-voltage (800 V) MOSFET (Q1) that is a cascode connected to the Drain of the integrated power MOSFET inside the INN3996CQ IC (U1). In this configuration the effective Drain-Source voltage rating of the primary is 1700 V_{PK}.

High-voltage ceramic capacitors C1 and C2 are used for the decoupling capacitor for the DC input voltage, and a low cost RCD clamp formed by D1, D3, R4, R1, R2 and C3 limits the peak total drain voltage, which is the sum of STACKFET and INN3996CQ drain voltages, to about 1460 V at 1200 VDC input due to the effects of transformer leakage inductance. Capacitor C7, Y capacitor, is used to attenuate the high frequency common mode noise on the output.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C6, when DC input voltage is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D2 and capacitor C4, and fed in the BPP pin via a current limiting resistor R3.

Zener diode VR1 and VR2 clamp the maximum drain-source voltage across the INN3997CQ IC (U1) to below 800 V. Zener diode VR3 ensures that the maximum gate-source voltage of Q1 does not exceed 15 V. Resistor R6, R7, and C5 provide bias to enhance the gate of Q1 when its source is switched low by the drain of U1.

4.2 *INN3996CQ IC Secondary*

The secondary-side of the INN3996CQ IC provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

Output rectification for the 12 V output is provided by SR FETs Q2 and Q3. Low ESR capacitors, C11, C12, C13, C16, C17 and output inductor L1 provide filtering. RC snubber network comprising R9, R10, and C8 for Q2 and Q3 damps high frequency ringing across SR FETs, which results from leakage inductance of the transformer windings and the secondary trace inductances. The gates of Q2 and Q3 are turned on based on the winding voltage sensed via R8 and the FWD pin of the IC. In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary-side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below ground. Secondary-side control of the primary-side MOSFET ensures that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR pin. The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the

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device, fed into the VO pin. It will charge the decoupling capacitor C10 via an internal regulator.

Resistors R12 and R13 form a voltage divider network that senses the output voltage. INN3996CQ IC has an internal reference of 1.265 V. Capacitor C14 provides decoupling from high frequency noise affecting power supply operation, and C15 and R14 is the feedforward network to speed up the response time to lower the output ripple. The output current is sensed by R11 with a threshold of approximately 35 mV to reduce losses. Once the current sense threshold across these resistors is exceeded, the device adjusts the number of switch pulses to maintain a fixed output current.

5 PCB Layout

Layers: 4
Board Thickness: 0.062”
Board Material: FR4
Copper Weight: 2 oz
Surface finish: LF HASL

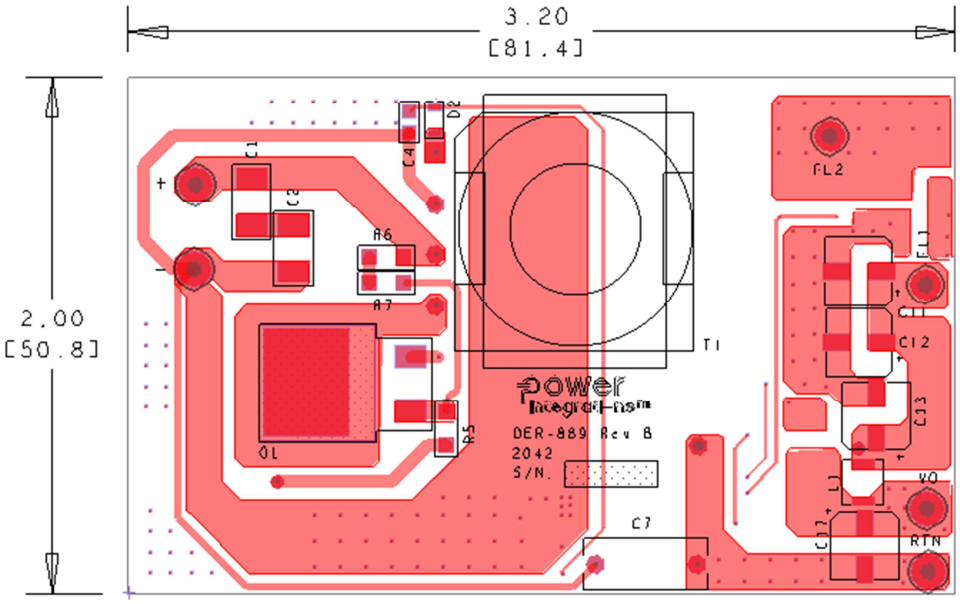

Figure 4 – Printed Circuit Board Layout (Top).

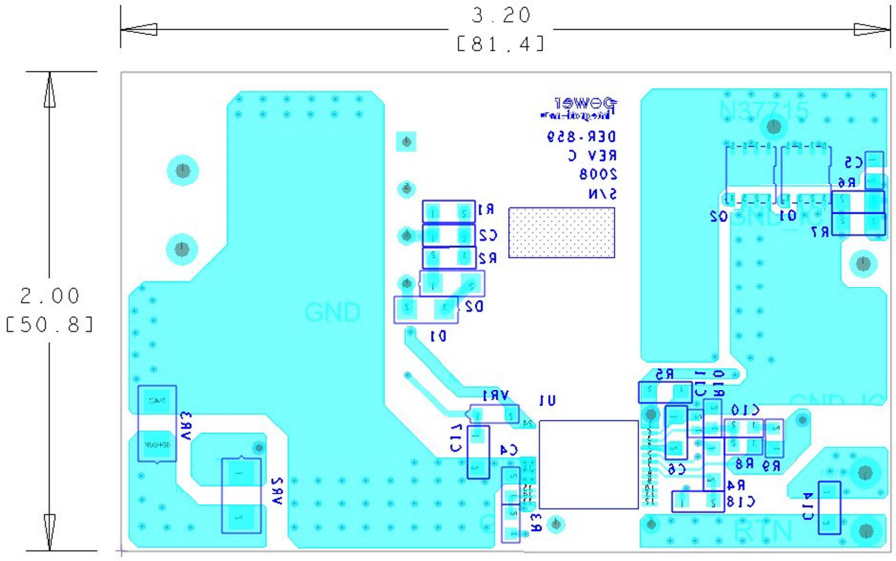

Figure 5 – Printed Circuit Board Layout (Bottom).

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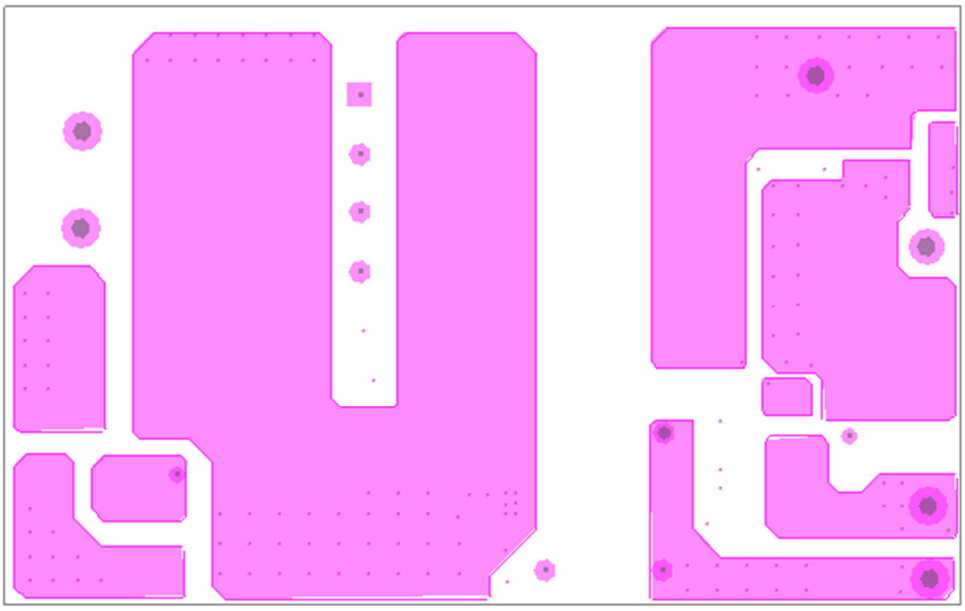

Figure 6 – Printed Circuit Board Layout (Internal layer 1).

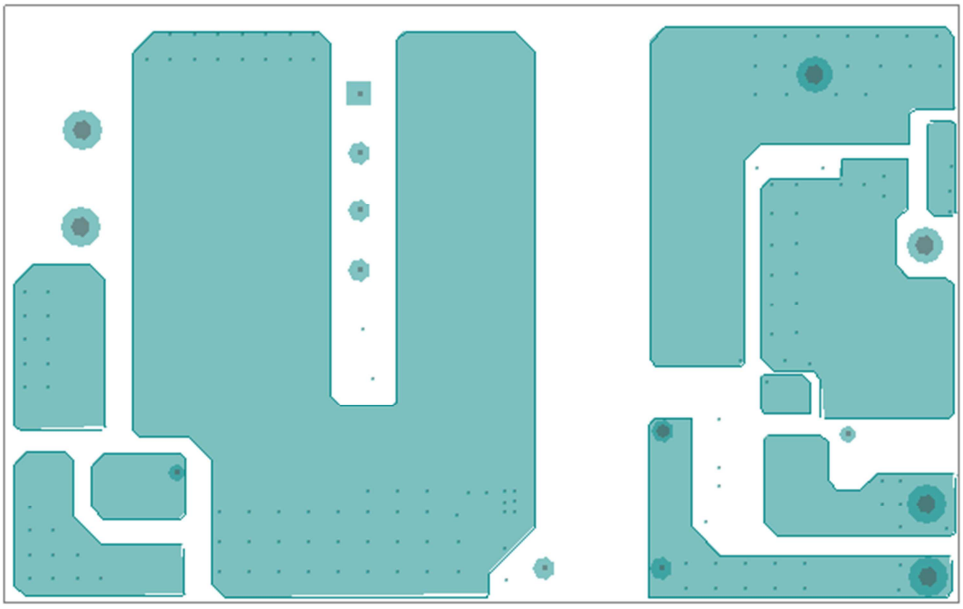

Figure 7 – Printed Circuit Board Layout (Internal layer 2).

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	C1 C2	0.047 µF, ±10%, 1000V (1kV), Ceramic, X7R, 1812	1812Y1K00473KST	Knowles Syfer
2	1	C3	4700pF, ±10%, 1000V (1kV), Ceramic Capacitor, X7R, 1206	C1206C472KDRACAUTO	Kemet
3	1	C4	22 µF ±20% 25V Ceramic X5R 0805	GRT21BR61E226ME13L	Murata
4	1	C5	22 pF, ±5%, 1000V (1kV), Ceramic, C0G, NP0, 1206	C1206C220JDGACAUTO	Kemet
5	1	C6	0.47 µF,±10% ,50 V, Ceramic, X7R, 0805,-55°C ~ 125°C	CGA4J3X7R1H474K125AB	TDK
6	1	C7	2200 pF, ±20% ,760VAC, Ceramic Y5U (E) Radial, Disc	AY1222M47Y5UC63L0	Vishay
7	1	C8	2200 pF, ±10%, 200V, Ceramic, X7R, 0805	08052C222K4T2A	AVX
8	1	C9	390 pF ±5% 630VDC, Ceramic C0G, NP0 1206	GCM31A5C2J391JX01D	Murata
9	1	C10	2.2 µF, ±10%, 50 V, Ceramic, X7R, Bypass, Decoupling, 1206	C1206C225K5RACAUTO7210	KEMET Murata
10	3	C11 C12 C13	220 µF, 25 V, Electrolytic, 0.260" L x 0.260" W (6.60mm x 6.60mm) x 0.315" H (8.00mm), SMD	EMZR250ARA221MF80G	United Chemi-Con
11	1	C14	330 pF, ±5%, 50 V, Ceramic, C0G, NP0, 0603	C0603C331J5GACAUTO	KEMET
12	1	C15	10 nF, ±10%, 50 V, Ceramic, X7R, 0805	08055C103K4Z2A	AVX
13	1	C16	22 µF ±20%, 25 V, Ceramic, X7R, 1210	CGA6P3X7R1E226M250AB	TDK
14	1	C17	100 µF, ±20%, 25 V, Z=320 mΩ, Electrolytic, 0.260" L x 0.260" W (6.60 mm x 6.60 mm) x 0.315" H (8.00mm), SMD	UCD1E101MCL1GS	Nichicon
15	2	D1 D3	Diode Standard 1000 V 1 A SMT DO-214AC (SMA)	US1MHE3_A/I	Vishay
16	2	D2 D4	Diode, General Purpose, 250 V, 200 mA, SC-76, SOD-323	NSVBAS21AHT1G	ON Semi
17	1	L1	1.5 µH, ±20%, Shielded, Wirewound, Inductor, 4.5 A, 42 mΩ Max, Automotive, AEC-Q200, 2-SMD	SRP4020TA-1R5M	Bourns
18	1	Q1	N-Channel 800V 5.2A (Tc) 125 W (Tc) SMT D2PAK	STB9NK80Z	ST Micro
19	2	Q2 Q3	MOSFET, N-Channel, 200 V, 13 A (Tc), 68W (Tc), Automotive, AEC-Q101, PowerPAK® SO-8, PowerPAK SO-8	SQJ454EP-T1_GE3	Vishay
20	2	R1 R2	RES, 1.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1004V	Panasonic
21	1	R3	RES, 21.0 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2102V	Panasonic
22	1	R4	RES, 39 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ390V	Panasonic
23	1	R5	RES, 10 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ100V	Panasonic
24	2	R6 R7	RES, 1.0 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ105V	Panasonic
25	1	R8	RES, 100 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1000V	Panasonic
26	2	R9 R10	RES, 51 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ510V	Panasonic
27	1	R11	0.011 Ω, ±1%, ±75ppm/°C, 1 W, 1206, Automotive AEC-Q200, Current Sense,-55°C ~ 155°C	ERJ-8CWFR011V	Panasonic
28	1	R12	RES, 11.8 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1182V	Panasonic
29	1	R13	RES, 100 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1003V	Panasonic
30	1	R14	RES, 15 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ153V	Panasonic
31	1	T1	Bobbin, EQ25, 4 pins, 4pri, 0sec	EQ-2506	Shen Zhen Xin Yu Jia Tech
32	1	U1	InnoSwitch3-AQ, InSOP-24D	INN3996CQ	Power Integrations
33	1	VR1	TVS DIODE, 482 V Clamp, 1.3A Ipp, SMT, DO-214AA (SMBJ)	TPSMB350A-A	Littlefuse
34	1	VR2	TVS DIODE, 548 V Clamp, 1.1A Ipp, SMT, DO-214AA (SMBJ)	TPSMB400A-A	Littlefuse
35	1	VR3	Zener Diode, 15 V, 500 mW, ±5%, SMT, SOD-123	MMSZ5245B-E3-18	Vishay

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7 Transformer Design

7.1 *Electrical Diagram*

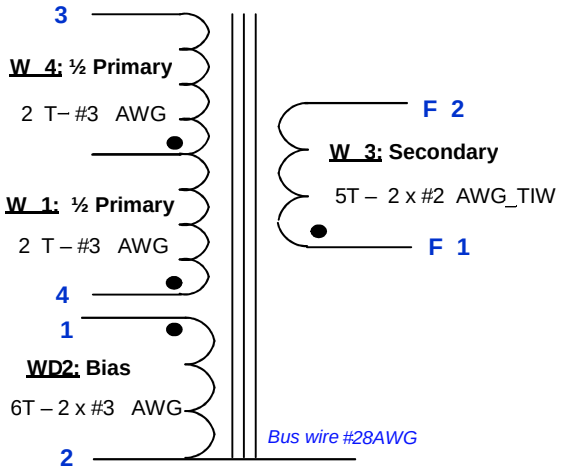

Figure 8 – Electrical Diagram.

7.2 *Electrical Specification*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 3 and 4, with all other windings open.	1187 µH ±5%
Resonant Frequency	Between pin 3 and 4, other windings open.	1,200 kHz (Min.)
Primary Leakage Inductance	Between pin 3 and 4, with pins: FL1-FL2 shorted.	7.0 µH (Max.)

7.3 *Transformer Build Diagram*

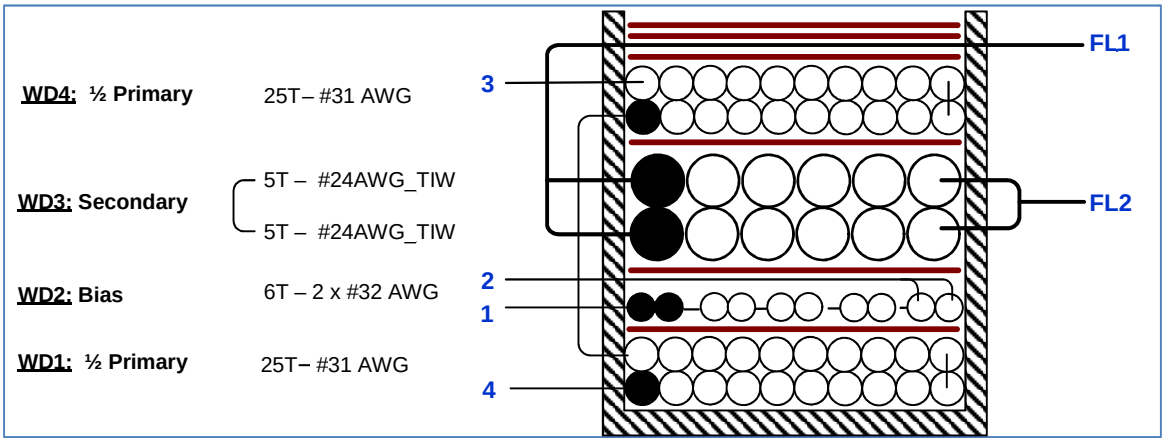

Figure 9 – Transformer Build Diagram.

7.4 *Material List*

Item	Description
[1]	Core: EQ27, ACP-95.
[2]	Bobbin: EQ2506 – Vertical – 4pins (4/0); PI#: 25-01095-00.
[3]	Magnet Wire: **#**31 AWG, Double Coated.
[4]	Magnet Wire: **#**32 AWG, Double Coated.
[5]	Magnet Wire: #24 AWG, Triple Insulated Wire.
[6]	Bus Wire: #28 AWG, Alpha Wire, Tinned Copper.
[7]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 4.25 mm Width.
[8]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 27.5 mm x 52 mm.
[9]	Varnish: Dolph BC-359.

7.5 *Transformer Instruction*

Winding Preparation	Make 2 slots with 2 mm width on flanges of secondary side of bobbin Item [2], (see illustration below). Position the bobbin on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.
WD1 1st Primary	Start at pin 4, wind 25 turns of wire Item [3] in 2 layers, with tight tension, from left to right and right to left. At the last turn, leave this wire with enough length for WD4 – 2nd Primary.
Insulation	1 layer of tape Item [7].
WD2: Bias	Start at pin1, wind 6 bifilar turns of wire Item [4] from left to right, spread wires evenly on the bobbin. At the last turn bring the wires back to the left and terminate at pin 2.
Insulation	1 layer of tape Item [7].
WD3 Secondary	Start at left slot of secondary side of bobbin, use wire Item [5] leaving ~ 1”, mark as FL1, and wind 5 turns with tight tension. At the last turn, exit the wire at the right slot, also leaving ~ 1” and mark as FL2. Repeat same winding above and on top, also start as FL1 and end FL2.
Insulation	1 layer of tape Item [7].
WD4 2nd Primary	Using wire floating from WD1, continue winding 25 turns in 2 layers, and terminate at pin 3.
Insulation	Place 1 layer of tape Item [7], bring 2 wires floating FL1 from Secondary – WD3 to right slot and continue placing another 2 layers of tape to secure these wires and all the windings.
Finish Assembly	Gap core halves to get 1187 μH. Use 50 mm of bus wire Item [6], solder to pin 2 then lean along core halves and secure with tape. Varnish with Item [9]. Places 2 layers of tape Item [8] at bottom of transformer, wrap up to the body, and 1 layer of tape Item [7] around the transformer, (see illustration below).

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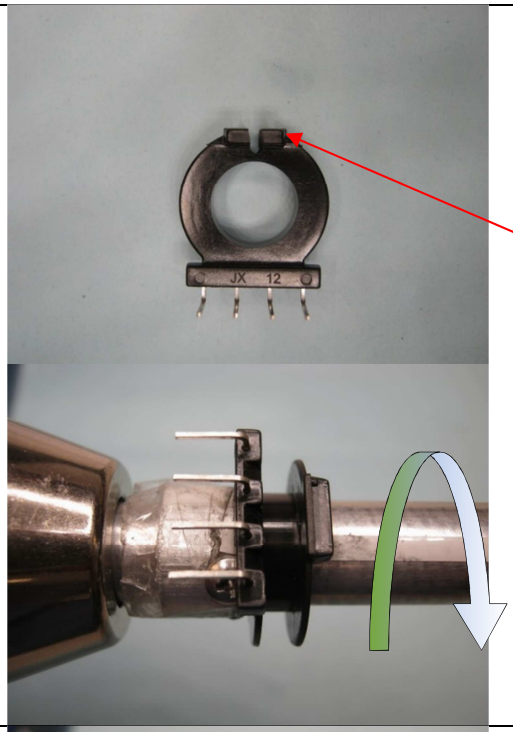
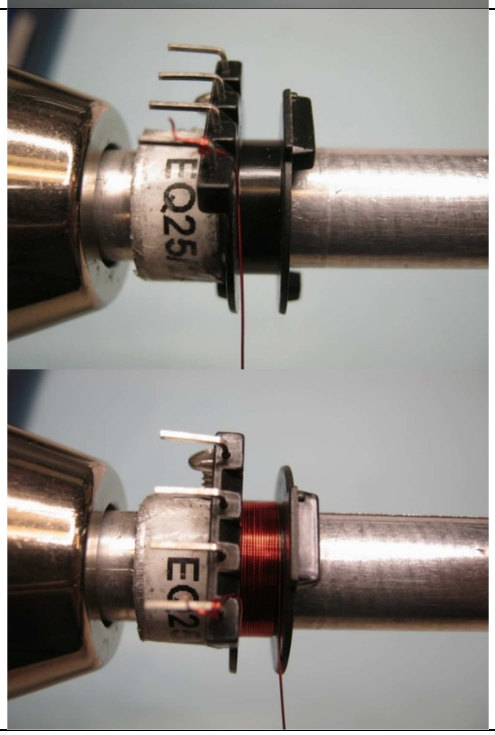
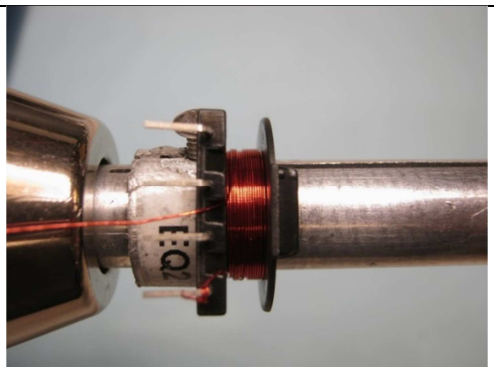
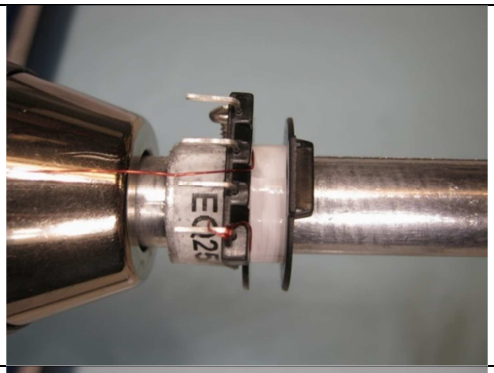
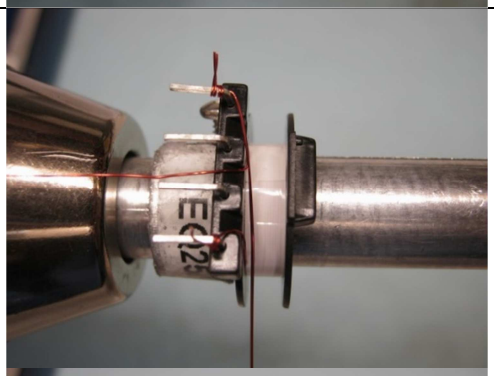
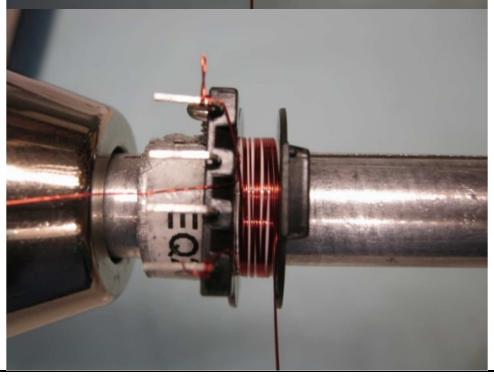
7.6 *Winding Illustrations*

Winding Preparation		Make 2 slots with 2 mm width on flanges of secondary side of bobbin Item [2], (see illustration beside). Position the bobbin on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.
WD1 **1st Primary**		Start at pin 4, wind 25 turns of wire Item [3] in 2 layers, with tight tension, from left to right and right to left. At the last turn, leave this wire with enough length for WD4 – 2nd Primary.

		
Insulation		1 layer of tape Item [7].
WD2: Bias	 	Start at pin1, wind 6 bifilar turns of wire Item [4] from left to right, spread wires evenly on the bobbin. At the last turn bring the wires back to the left and terminate at pin 2.

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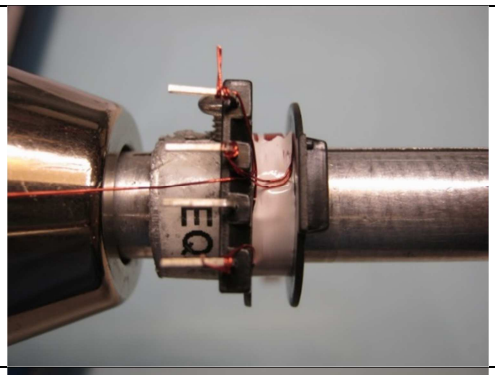
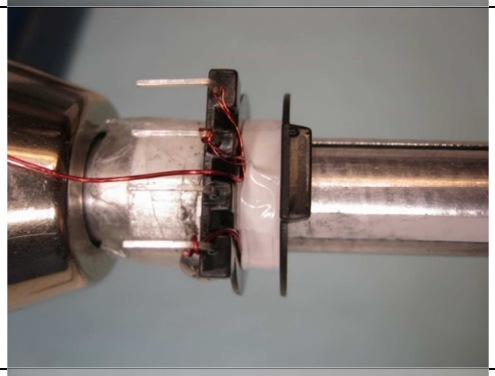
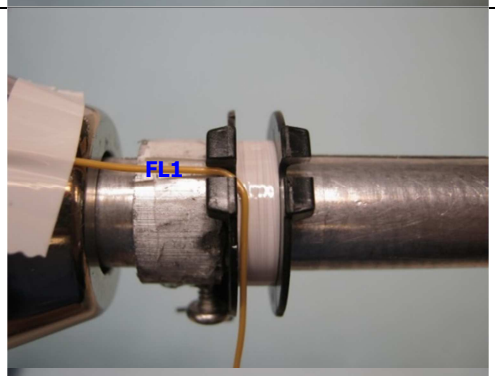
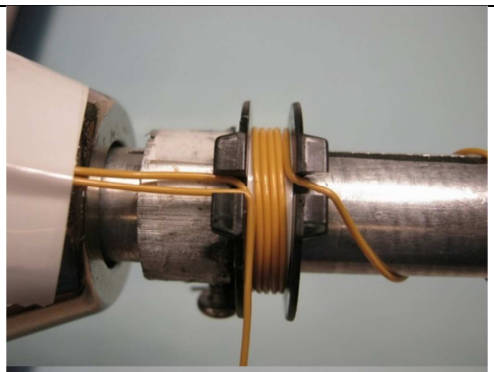
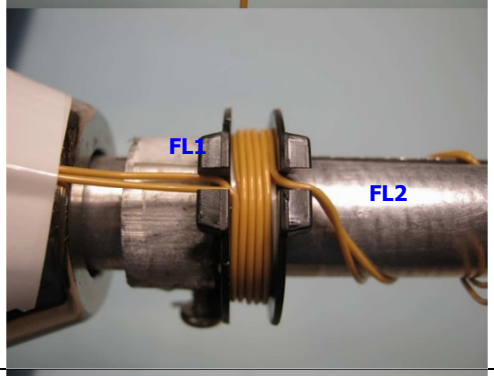
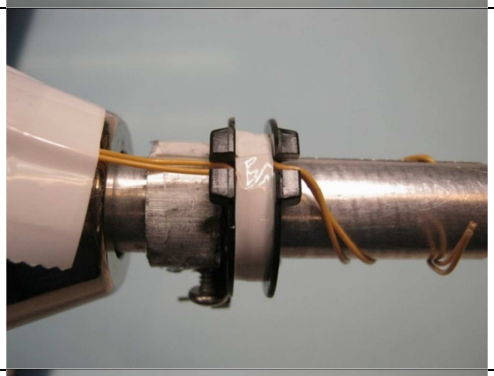
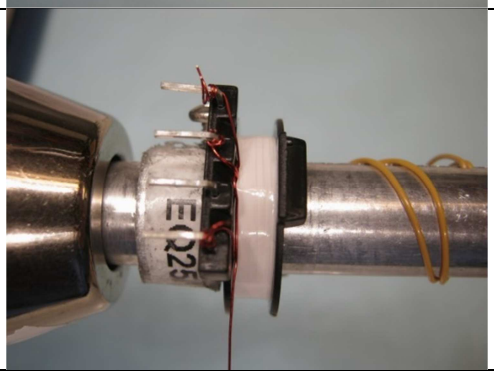
		
Insulation		1 layer of tape item [7].
WD3 **Secondary**	 	Start at left slot of secondary side of bobbin, use wire Item [5] leaving ~ 1”, mark as FL1, and wind 5 turns with tight tension. At the last turn, exit the wire at the right slot, also leaving ~ 1” and mark as FL2. Repeat same winding above and on top, also start as FL1 and end FL2.

	 	
Insulation		1 layer of tape Item [7].
WD4 **2nd Primary**		Using wire floating from WD1, continue winding 25 turns in 2 layers, and terminate at pin 3.

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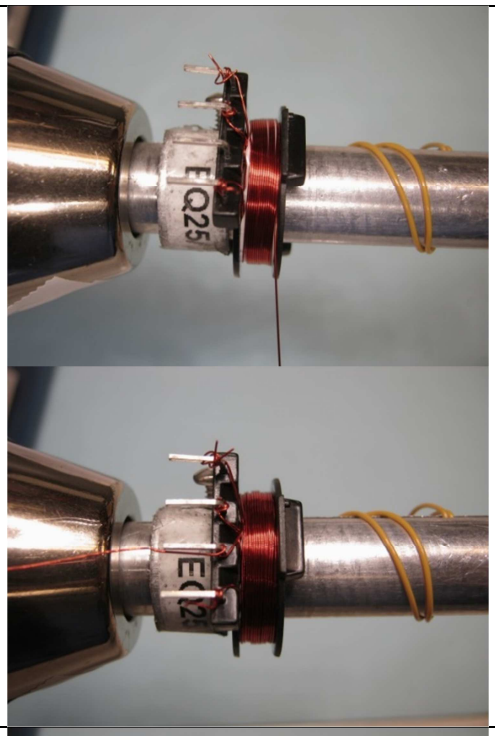
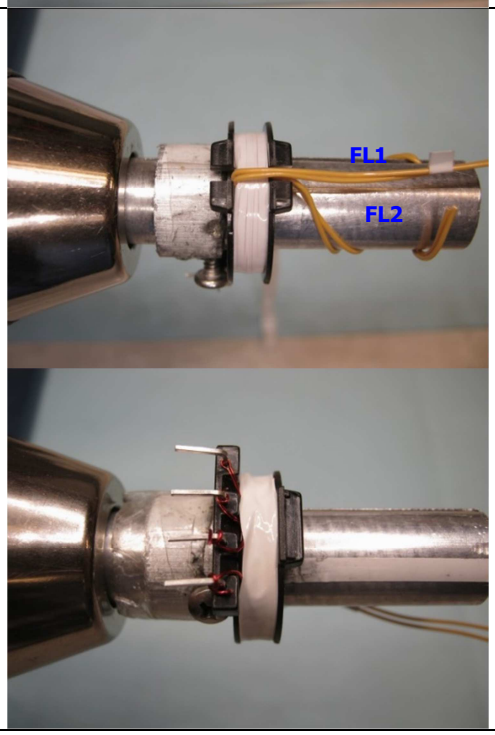
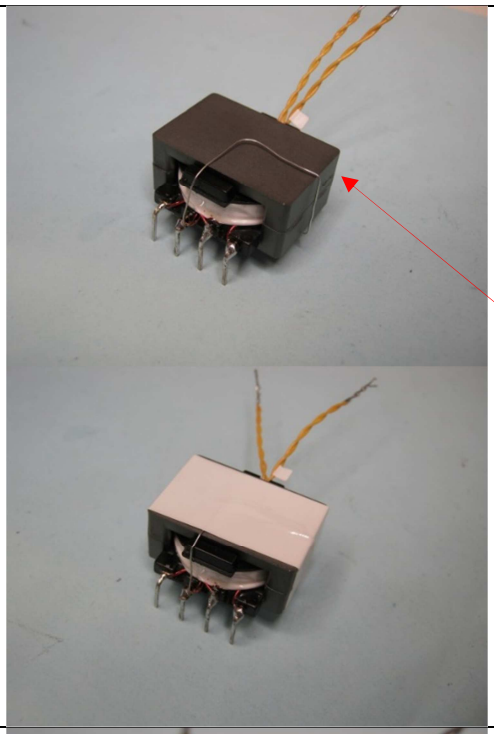
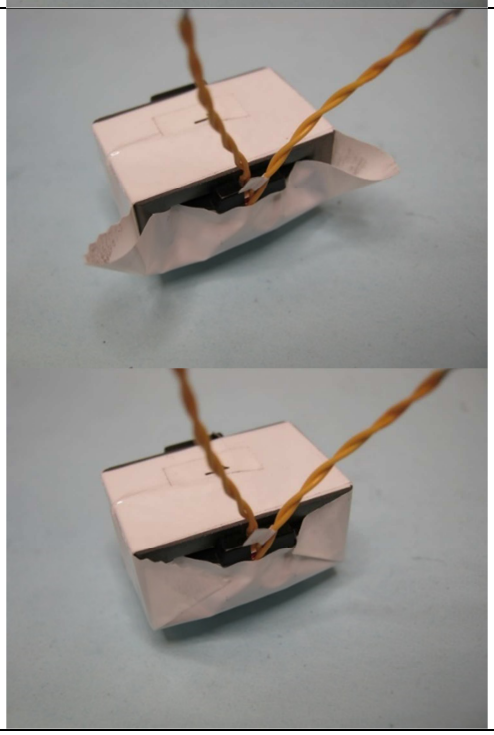
		
Insulation		Place 1 layer of tape Item [7], bring 2 wires floating FL1 from Secondary – WD3 to right slot and continue placing another 2 layers of tape to secure these wires and all the windings.

Finish		Gap core halves to get 1187 µH. Use 50 mm of bus wire Item [6], solder to pin 2 then lean along core halves and secure with tape. Varnish with Item [9].
Finish (Cont'd)		Places 2 layers of tape Item [8] at bottom of transformer, wrap up to the body, and 1 layer of tape Item [7] around the transformer, (see illustration below).

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	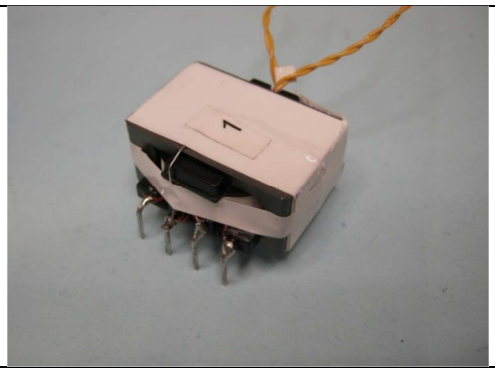	

8 Performance Data

All measurements performed with room ambient temperature. Measured at PCB output terminal.

8.1 *Efficiency vs. Load and Input Voltage*

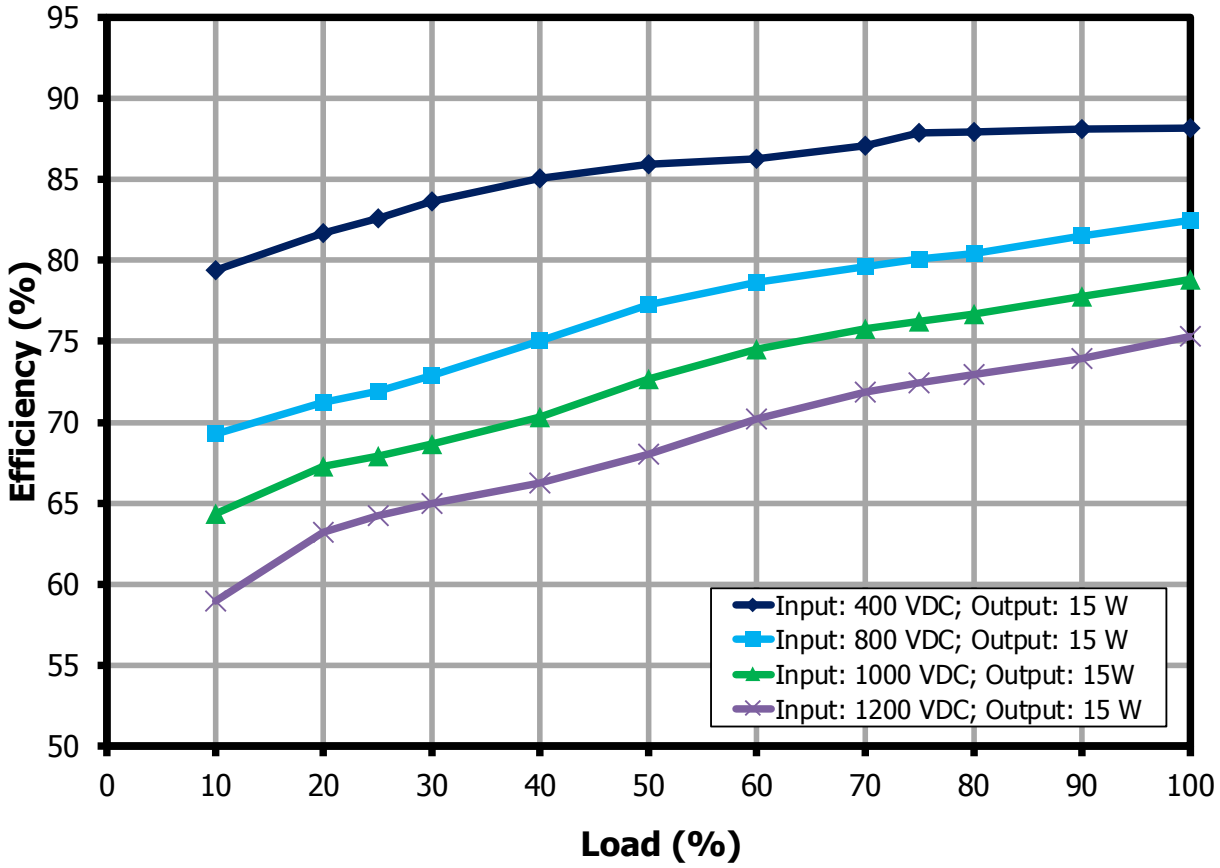

Figure 10 – Efficiency vs. Load and Input Voltage, Room Temperature.

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8.2 *Full Load Efficiency vs. Line*

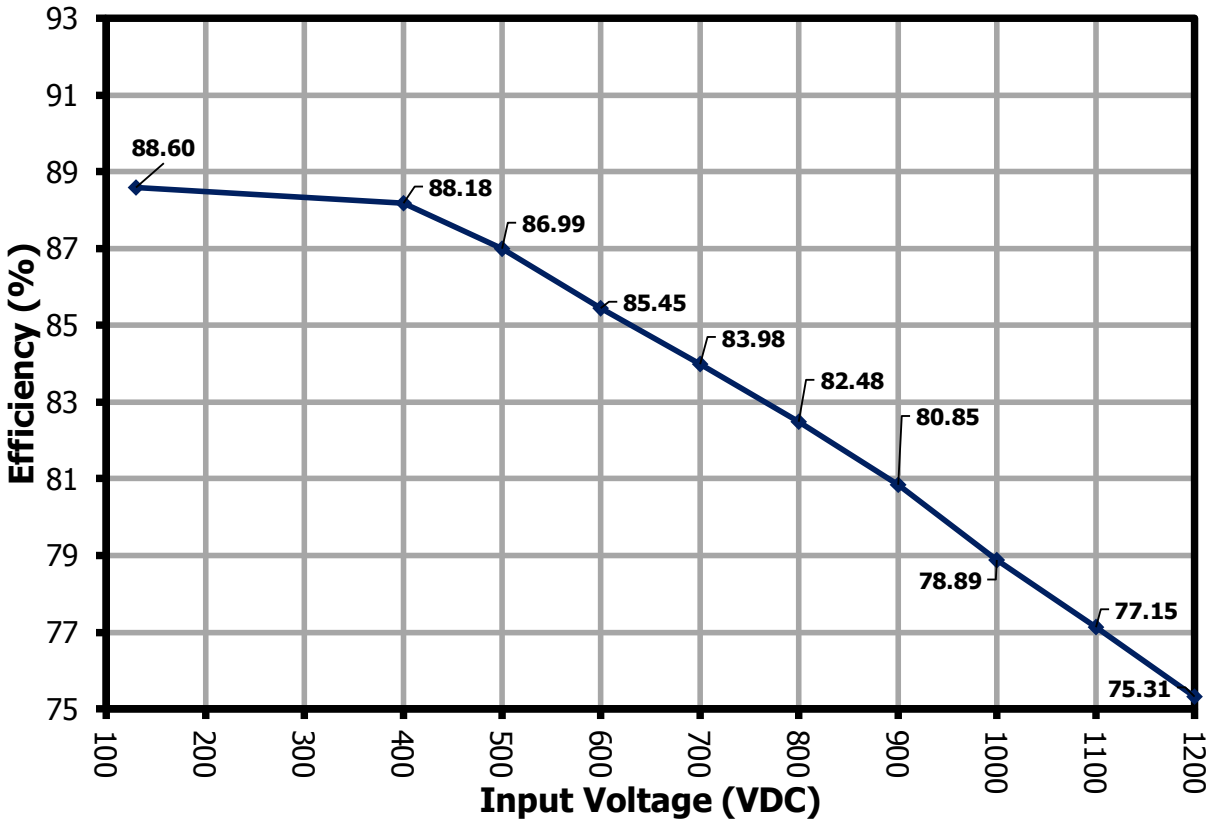

Figure 11 – Efficiency vs. Line (VDC), Room Temperature.

8.3 *Efficiency at Low Input Voltage*

V_{IN} (VDC)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
130	16.97	12.03	1.25	15.03	88.60
100	17.14	12	1.25	14.99	87.45
90	17.32	12.01	1.25	15.00	86.63
60	17.14	11.53	1.25	14.41	84.29
40	9.98	11.42	0.70	7.99	80.13
35	8.02	11.40	0.55	6.27	78.10
30	2.84	11.59	0.19	2.20	77.38

Note: 2 W Load at 30 VDC Input during power down only.

8.4 *No-Load Input Power*

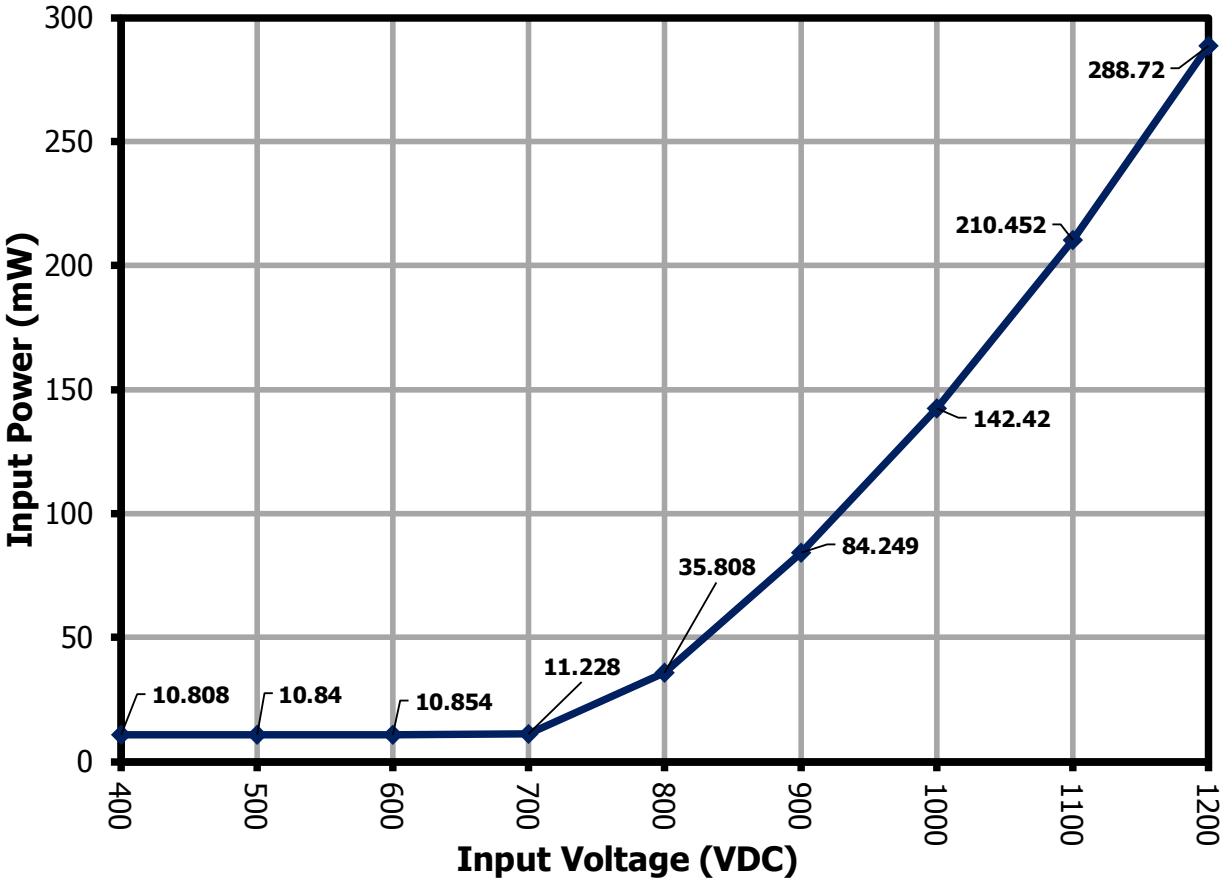

Figure 12 – No-Load Input Power, Room Temperature.

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8.5 *Load and Line Regulation*

Measurements taken at 0% to 100% of rated load

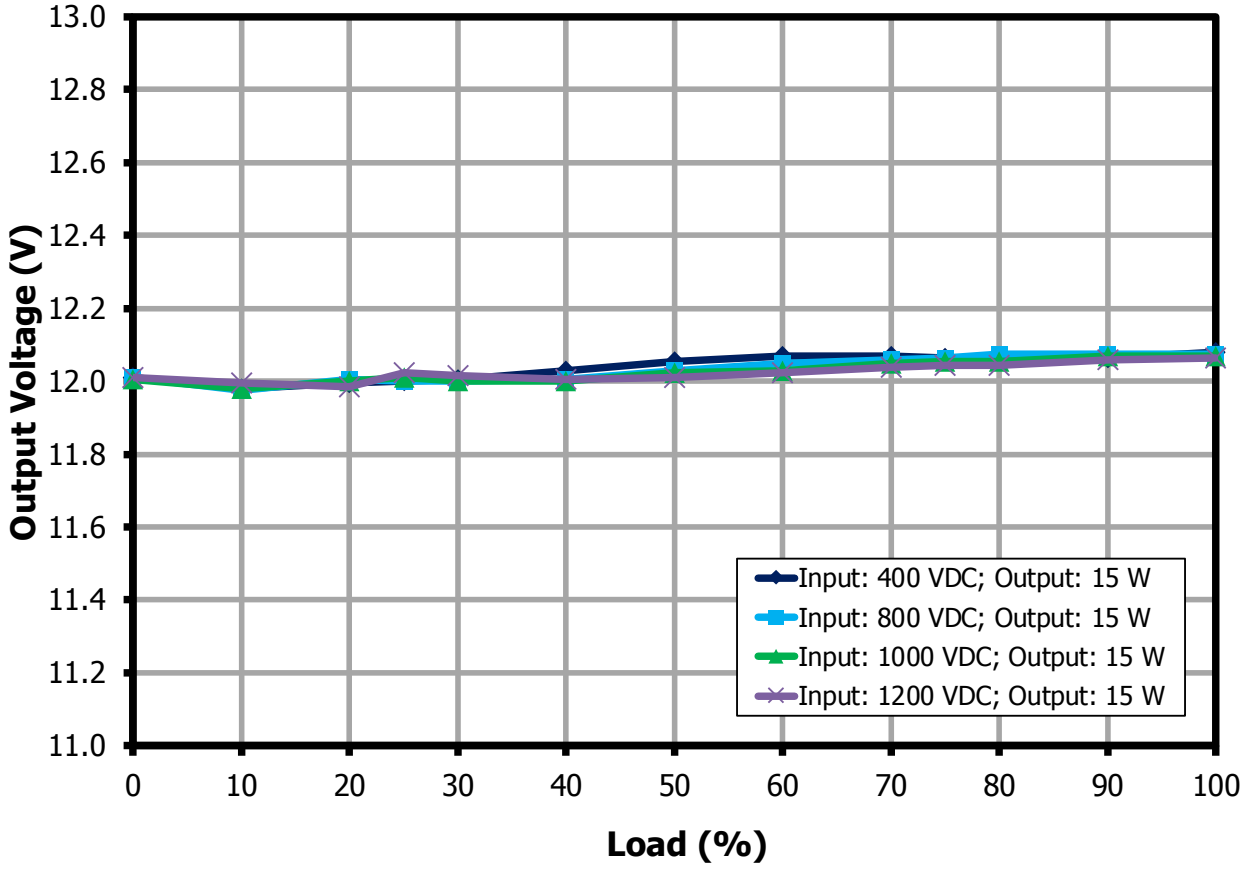

Figure 13 – Output Voltage vs. Output Current and Input Voltage (VDC), Room Temperature.

9 Waveforms

9.1 *INN3996CQ Drain Voltage and Current, Steady-State*

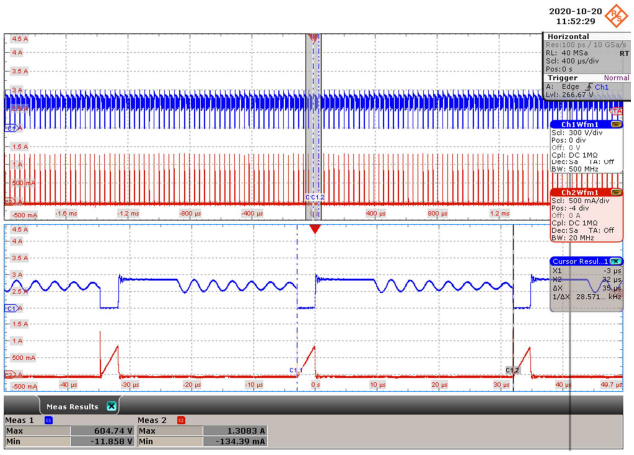

Figure 14 – Drain Voltage and Current Waveforms.
V_{IN} = 400 VDC, I_{OUT} = 1.25 A.
$V_{DS(MAX)}$ = 604 V.
Upper: V_{DRAIN}, 300 V, 400 µs / div.
Lower: I_{DRAIN}, 500 mA, 400 µs / div.
Bottom Half: Zoom @ 10 µs / div.

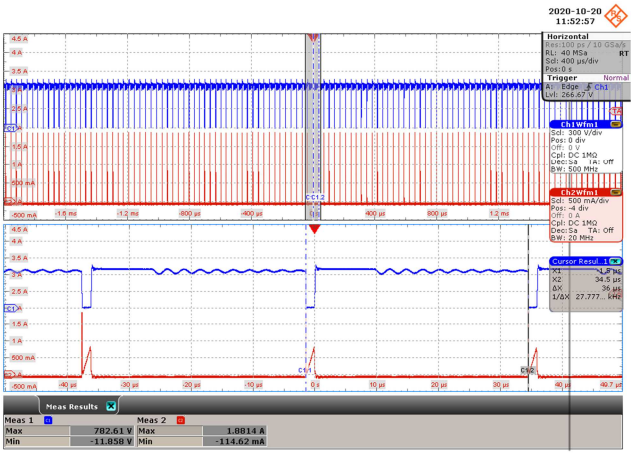

Figure 15 – Drain Voltage and Current Waveforms.
V_{IN} = 800 VDC, I_{OUT} = 1.25 A.
$V_{DS(MAX)}$ = 782 V.
Upper: V_{DRAIN}, 300 V, 400 µs / div.
Lower: I_{DRAIN}, 500 mA, 400 µs / div.
Bottom Half: Zoom @ 10 µs / div.

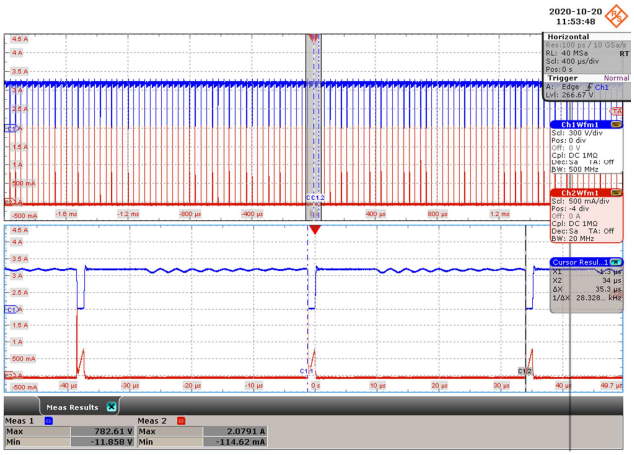

Figure 16 – Drain Voltage and Current Waveforms.
V_{IN} = 1000 VDC, I_{OUT} = 1.25 A.
$V_{DS(MAX)}$ = 782 V.
Upper: V_{DRAIN}, 300 V, 400 µs / div.
Lower: I_{DRAIN}, 500 mA, 400 µs / div.
Bottom Half: Zoom @ 10 µs / div.

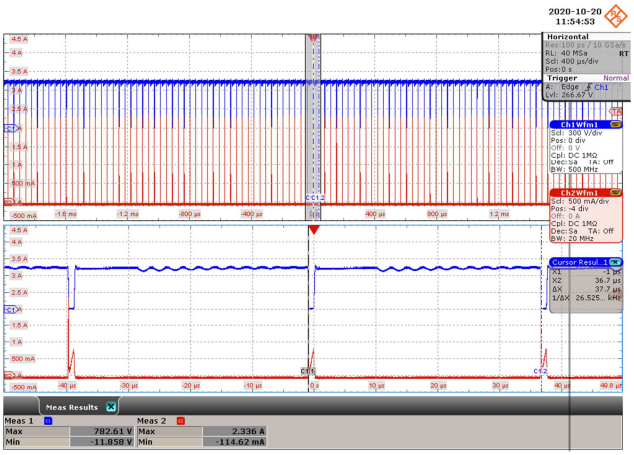

Figure 17 – Drain Voltage and Current Waveforms.
V_{IN} = 1200 VDC, I_{OUT} = 1.25 A.
$V_{DS(MAX)}$ = 782 V.
Upper: V_{DRAIN}, 300 V, 400 µs / div.
Lower: I_{DRAIN}, 500 mA, 400 µs / div.
Bottom Half: Zoom @ 10 µs / div.

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9.2 *INN3996CQ Drain Voltage and Current, Start-up*

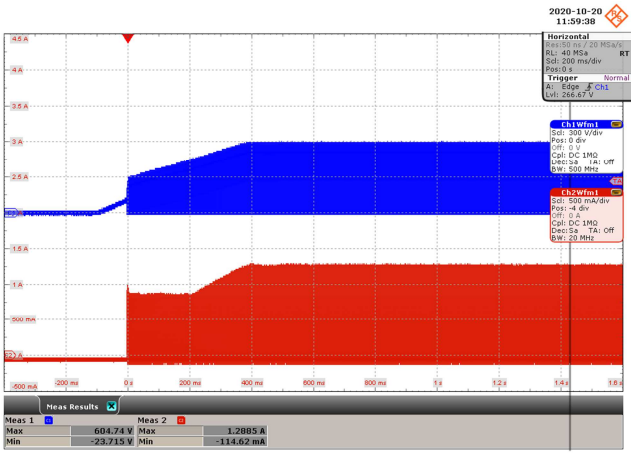

Figure 18 – Drain Voltage and Current Waveforms.
V_{IN} = 400 VDC, I_{OUT} = 1.25 A.
$V_{DS(MAX)}$ = 604 V.
Upper: V_{DRAIN}, 300 V, 200 ms / div.
Lower: I_{DRAIN}, 500 mA, 200 ms / div.

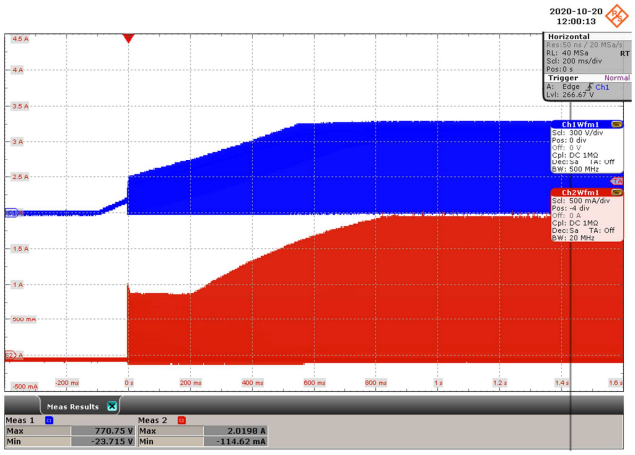

Figure 19 – Drain Voltage and Current Waveforms.
V_{IN} = 800 VDC, I_{OUT} = 1.25 A.
$V_{DS(MAX)}$ = 770 V.
Upper: V_{DRAIN}, 300 V, 200 ms / div.
Lower: I_{DRAIN}, 500 mA, 200 ms / div.

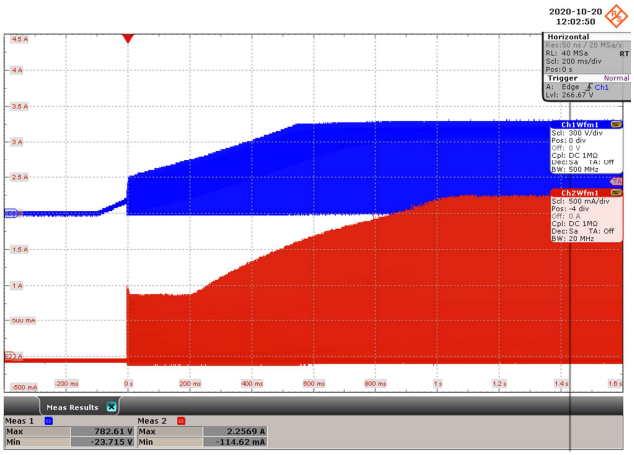

Figure 20 – Drain Voltage and Current Waveforms.
V_{IN} = 1000 VDC, I_{OUT} = 1.25 A.
$V_{DS(MAX)}$ = 782 V.
Upper: V_{DRAIN}, 300 V, 200 ms / div.
Lower: I_{DRAIN}, 500 mA, 200 ms / div.

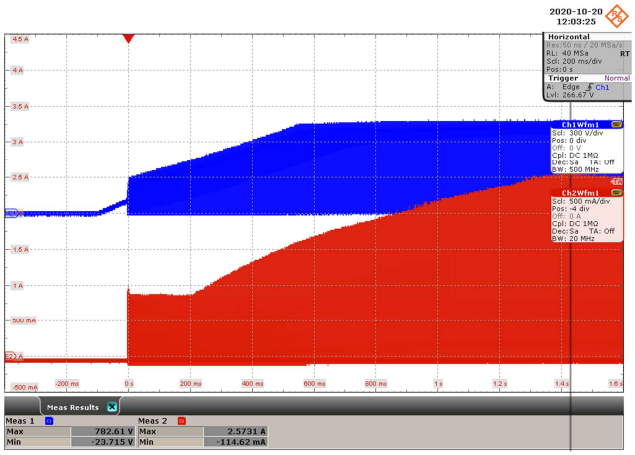

Figure 21 – Drain Voltage and Current Waveforms.
V_{IN} = 1200 VDC, I_{OUT} = 1.25 A.
$V_{DS(MAX)}$ = 782 V.
Upper: V_{DRAIN}, 300 V, 200 ms / div.
Lower: I_{DRAIN}, 500 mA, 200 ms / div.

9.3 *Total and StackFET Drain to Source Voltage, Steady-State*

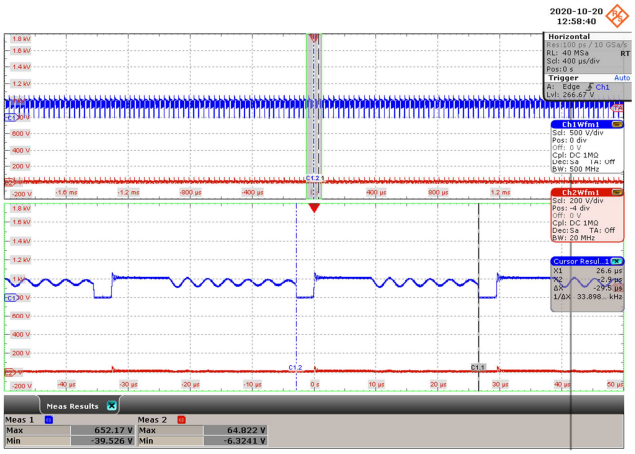

Figure 22 – Total and STACKFET Drain to Source Voltage Waveforms.
V_{IN} = 400 VDC, I_{OUT} = 1.25 A.
$V_{STACKFET(MAX)}$ = 65 V, $V_{DS\_TOTAL(MAX)}$ = 652 V.
Upper: V_{TOTAL}, 500 V, 400 µs / div.
Lower: $V_{STACKFET}$, 200 V, 400 µs / div.
Bottom Half: Zoom @ 10 µs / div.

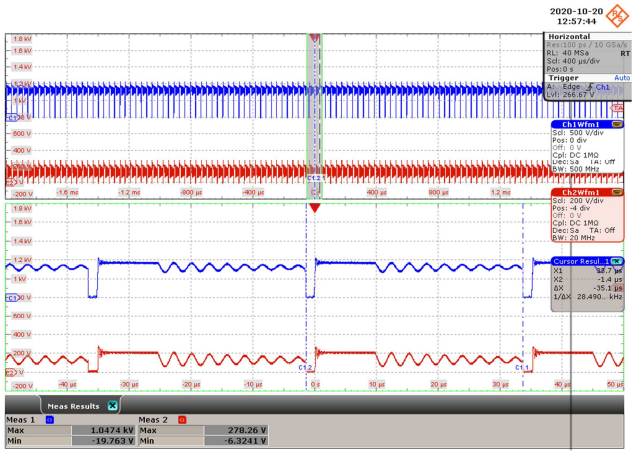

Figure 23 – Total and STACKFET Drain to Source Voltage Waveforms.
V_{IN} = 800 VDC, I_{OUT} = 1.25 A.
$V_{STACKFET(MAX)}$ = 278 V, $V_{TOTAL(MAX)}$ = 1047 V.
Upper: V_{TOTAL}, 500 V, 400 µs / div.
Lower: $V_{STACKFET}$, 200 V, 400 µs / div.
Bottom Half: Zoom @ 10 µs / div.

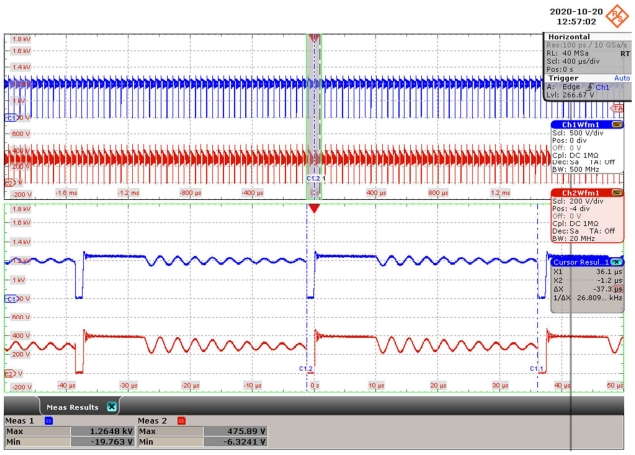

Figure 24 – Total and STACKFET Drain to Source Voltage Waveforms.
V_{IN} = 1000 VDC, I_{OUT} = 1.25 A.
$V_{STACKFET(MAX)}$ = 476 V, $V_{TOTAL(MAX)}$ = 1265 V.
Upper: V_{TOTAL}, 500 V, 400 µs / div.
Lower: $V_{STACKFET}$, 200 V, 400 µs / div.
Bottom Half: Zoom @ 10 µs / div.

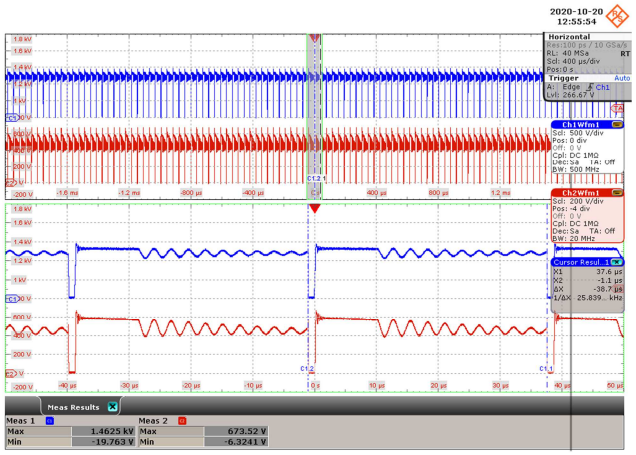

Figure 25 – Total and STACKFET Drain to Source Voltage Waveforms.
V_{IN} = 1200 VDC, I_{OUT} = 1.25 A.
$V_{STACKFET(MAX)}$ = 674 V, $V_{TOTAL(MAX)}$ = 1463 V.
Upper: V_{TOTAL}, 500 V, 400 µs / div.
Lower: $V_{STACKFET}$, 200 V, 400 µs / div.
Bottom Half: Zoom @ 10 µs / div.

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9.4 *Total and StackFET Drain to Source Voltage, Start-up*

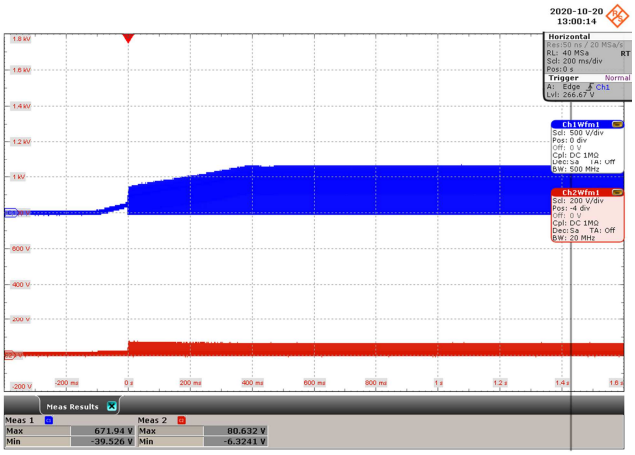

Figure 26 – Total and STACKFET Drain to Source Voltage Waveforms.
V_{IN} = 400 VDC, I_{OUT} = 1.25 A.
$V_{STACKFET(MAX)}$ = 81 V, $V_{DS\_TOTAL(MAX)}$ = 672 V.
Upper: V_{TOTAL}, 500 V, 200 ms / div.
Lower: $V_{STACKFET}$, 200 V, 200 ms / div.

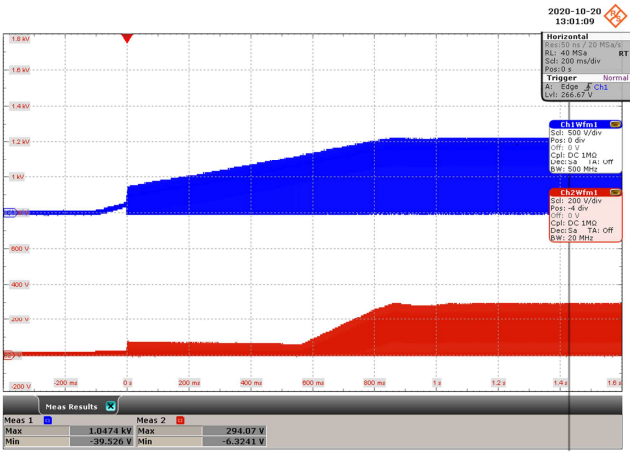

Figure 27 – Total and STACKFET Drain to Source Voltage Waveforms.
V_{IN} = 800 VDC, I_{OUT} = 1.25 A.
$V_{STACKFET(MAX)}$ = 294 V, $V_{TOTAL(MAX)}$ = 1047 V.
Upper: V_{TOTAL}, 500 V, 200 ms / div.
Lower: $V_{STACKFET}$, 200 V, 200 ms / div.

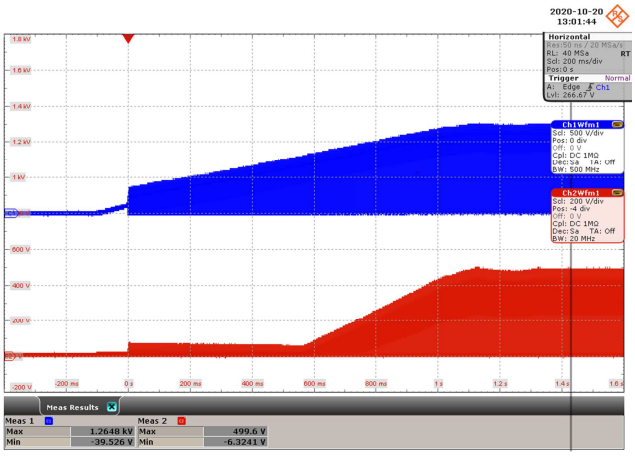

Figure 28 – Total and STACKFET Drain to Source Voltage Waveforms.
V_{IN} = 1000 VDC, I_{OUT} = 1.25 A.
$V_{STACKFET(MAX)}$ = 500 V, $V_{TOTAL(MAX)}$ = 1265 V.
Upper: V_{TOTAL}, 500 V, 200 ms / div.
Lower: $V_{STACKFET}$, 200 V, 200 ms / div.

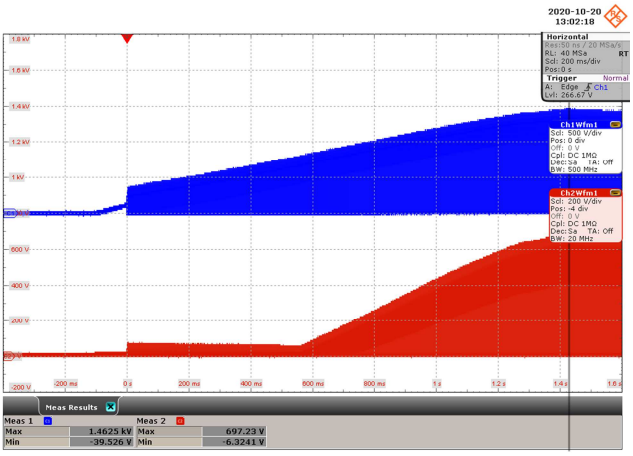

Figure 29 – Total and STACKFET Drain to Source Voltage Waveforms.
V_{IN} = 1200 VDC, I_{OUT} = 1.25 A.
$V_{STACKFET(MAX)}$ = 697 V, $V_{TOTAL(MAX)}$ = 1463 V.
Upper: V_{TOTAL}, 500 V, 200 ms / div.
Lower: $V_{STACKFET}$, 200 V, 200 ms / div.

9.5 *SR FET Waveforms, Steady-State*

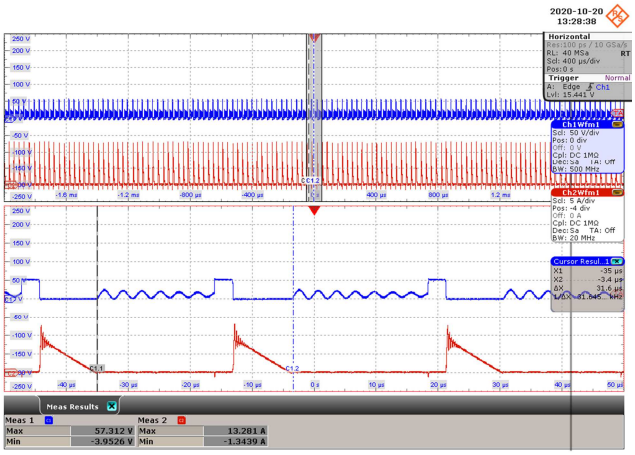

Figure 30 – SRFET Drain to Source Voltage Waveforms.
V_{IN} = 400 VDC, I_{OUT} = 1.25 A.
SRFET $V_{DS(MAX)}$ = 57.3 V.
SRFET $I_{DS(MAX)}$ = 13.3 A.
Upper: SRFET V_{DS}, 50 V, 400 µs / div.
Lower: SRFET I_{DS}, 5 A, 400 µs / div.
Bottom Half: Zoom @ 10 µs / div.

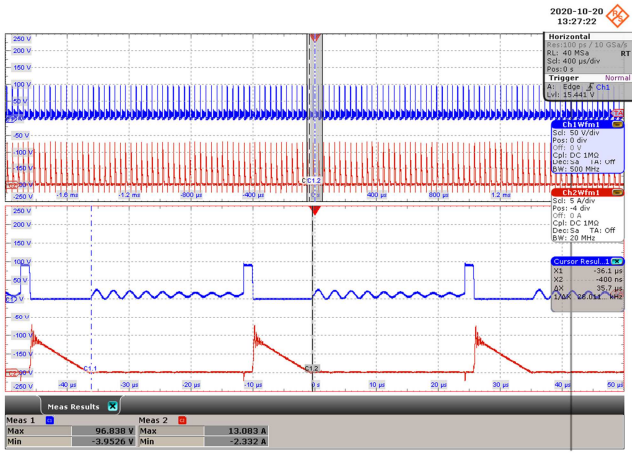

Figure 31 – SRFET Drain to Source Voltage Waveforms.
V_{IN} = 800 VDC, I_{OUT} = 1.25 A.
SRFET $V_{DS(MAX)}$ = 96.8 V.
SRFET $I_{DS(MAX)}$ = 13.1 A.
Upper: SRFET V_{DS}, 50 V, 400 µs / div.
Lower: SRFET I_{DS}, 5 A, 400 µs / div.
Bottom Half: Zoom @ 10 µs / div.

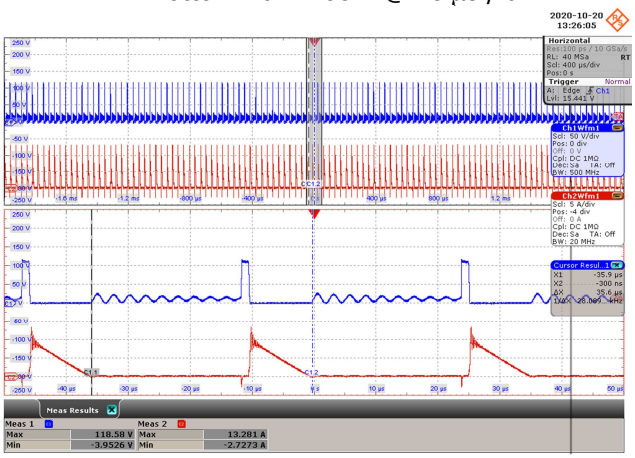

Figure 32 – SRFET Drain to Source Voltage Waveforms.
V_{IN} = 1000 VDC, I_{OUT} = 1.25 A.
SRFET $V_{DS(MAX)}$ = 118.6 V.
SRFET $I_{DS(MAX)}$ = 13.3 A.
Upper: SRFET V_{DS}, 50 V, 400 µs / div.
Lower: SRFET I_{DS}, 5 A, 400 µs / div.
Bottom Half: Zoom @ 10 µs / div.

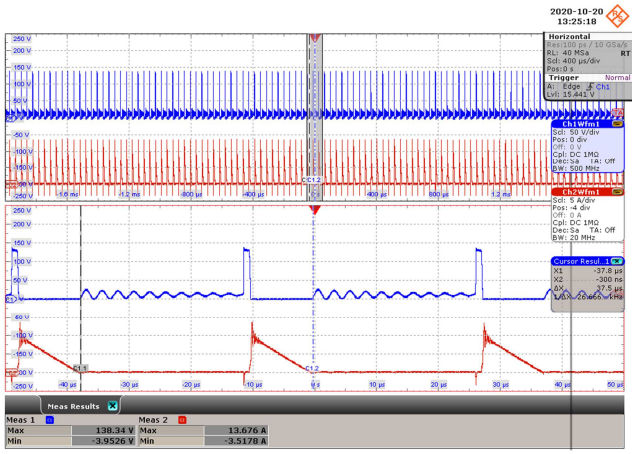

Figure 33 – SRFET Drain to Source Voltage Waveforms.
V_{IN} = 1200 VDC, I_{OUT} = 1.25 A.
SRFET $V_{DS(MAX)}$ = 138.3 V.
SRFET $I_{DS(MAX)}$ = 13.7 A.
Upper: SRFET V_{DS}, 50 V, 400 µs / div.
Lower: SRFET I_{DS}, 5 A, 400 µs / div.
Bottom Half: Zoom @ 10 µs / div.

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9.6 *SR FET Waveforms, Start-up*

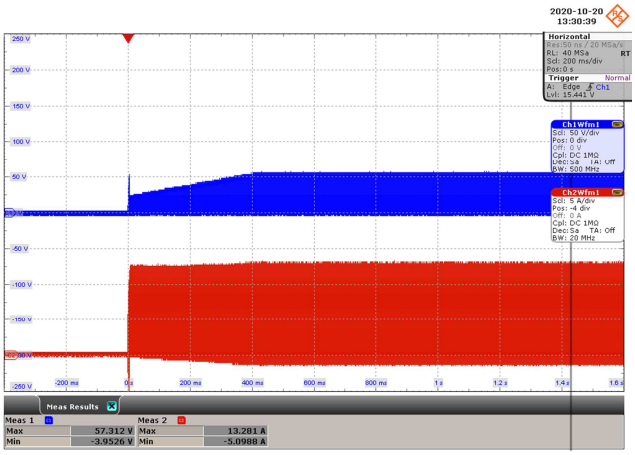

Figure 34 – SRFET Drain to Source Voltage Waveforms.
V_{IN} = 400 VDC, I_{OUT} = 1.25 A.
SRFET $V_{DS(MAX)}$ = 57.3 V.
SRFET $I_{DS(MAX)}$ = 13.3 A.
Upper: SRFET V_{DS}, 50 V, 200 ms / div.
Lower: SRFET I_{DS}, 5 A, 200 ms / div.

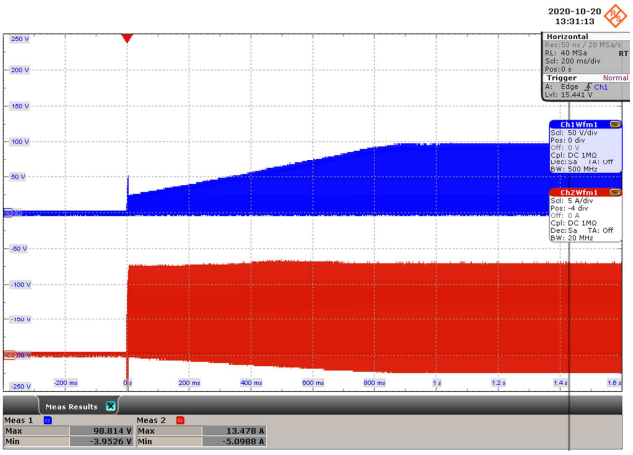

Figure 35 – SRFET Drain to Source Voltage Waveforms.
V_{IN} = 800 VDC, I_{OUT} = 1.25 A.
SRFET $V_{DS(MAX)}$ = 98.8 V.
SRFET $I_{DS(MAX)}$ = 13.5 A.
Upper: SRFET V_{DS}, 50 V, 200 ms / div.
Lower: SRFET I_{DS}, 5 A, 200 ms / div.

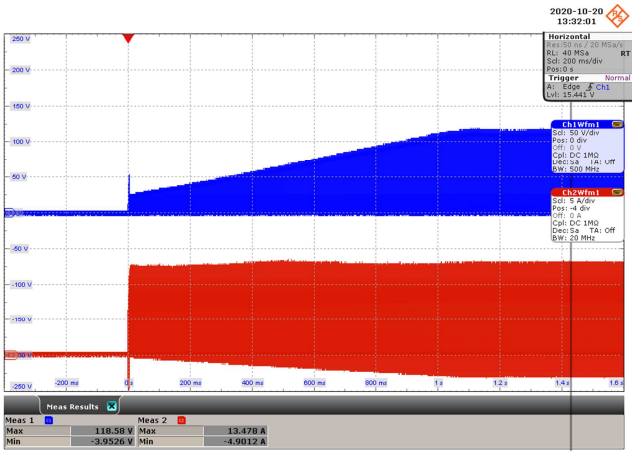

Figure 36 – SRFET Drain to Source Voltage Waveforms.
V_{IN} = 1000 VDC, I_{OUT} = 1.25 A.
SRFET $V_{DS(MAX)}$ = 118.6 V.
SRFET $I_{DS(MAX)}$ = 13.5 A.
Upper: SRFET V_{DS}, 50 V, 200 ms / div.
Lower: SRFET I_{DS}, 5 A, 200 ms / div.

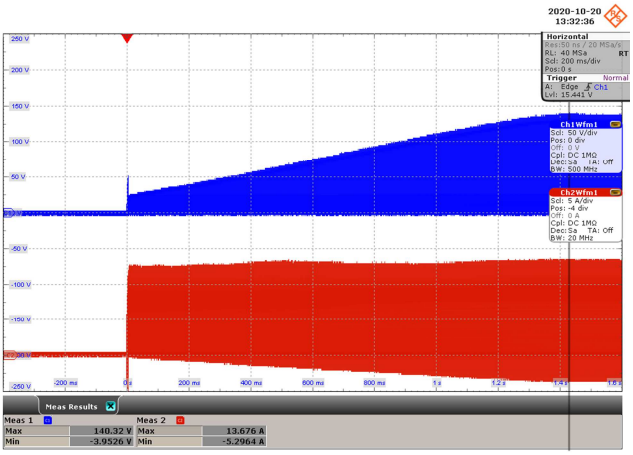

Figure 37 – SRFET Drain to Source Voltage Waveforms.
V_{IN} = 1200 VDC, I_{OUT} = 1.25 A.
SRFET $V_{DS(MAX)}$ = 140.3 V.
SRFET $I_{DS(MAX)}$ = 13.7 A.
Upper: SRFET V_{DS}, 50 V, 200 ms / div.
Lower: SRFET I_{DS}, 5 A, 200 ms / div.

9.7 *Output Ripple Measurements*

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with once capacitor tied in parallel across the probe tip. The capacitor includes one (1) 1 μF/50 V ceramic type.

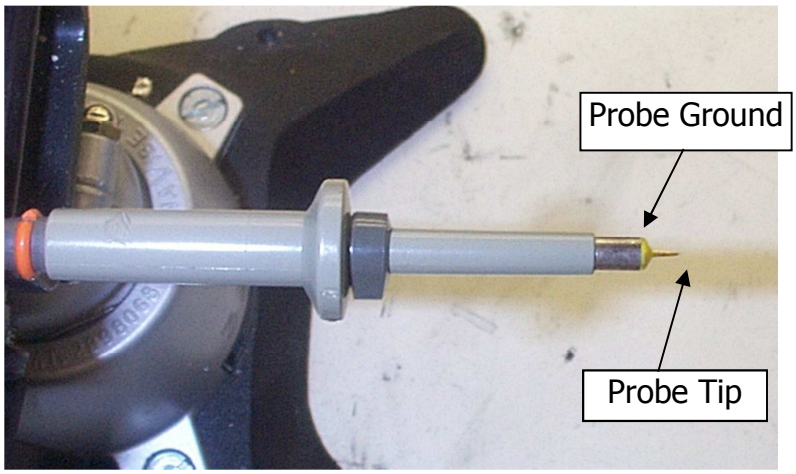

Figure 38 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

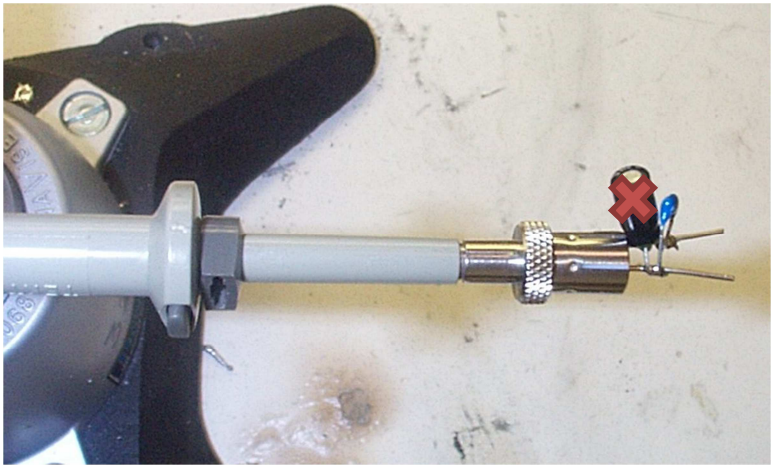

Figure 39 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and one parallel decoupling capacitor added)

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9.7.1 100% Loading Condition

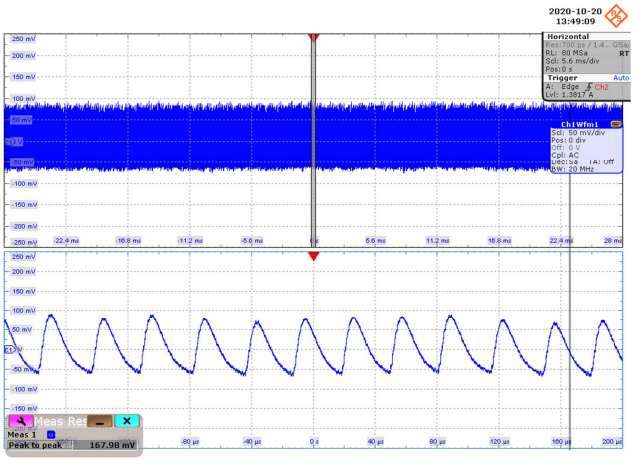

Figure 40 – Output Voltage Ripple.
V_{IN} = 400 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 168 mV_{P-P}.

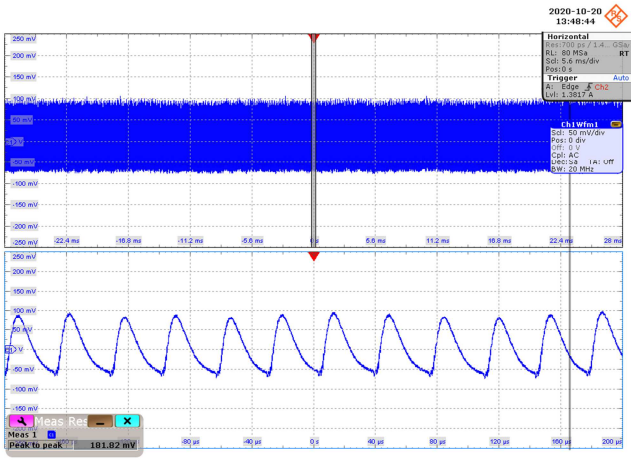

Figure 41 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 182 mV_{P-P}.

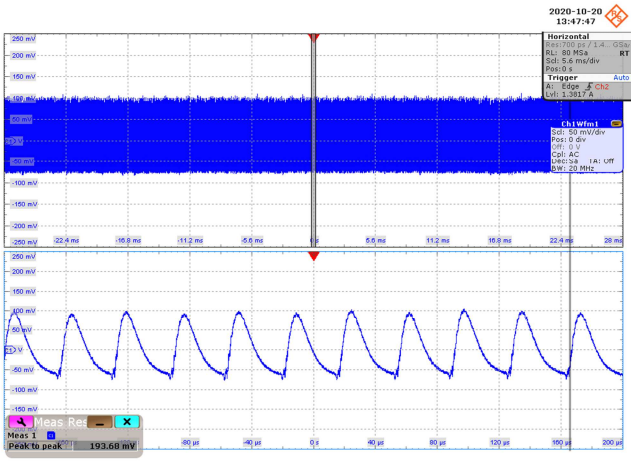

Figure 42 – Output Voltage Ripple.
V_{IN} = 1000 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 194 mV_{P-P}.

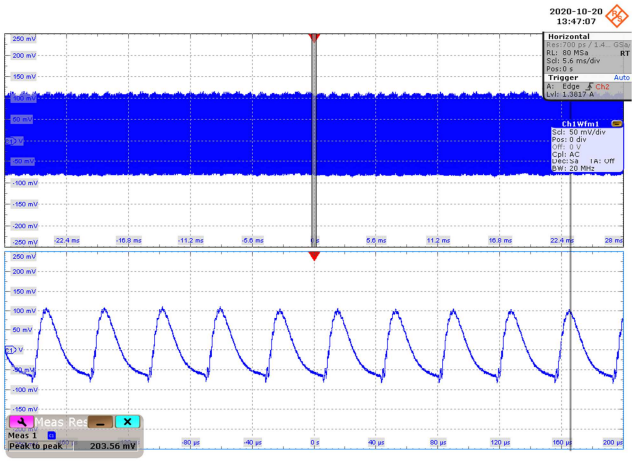

Figure 43 – Output Voltage Ripple.
V_{IN} = 1200 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 204 mV_{P-P}.

9.7.2 75% Loading Condition

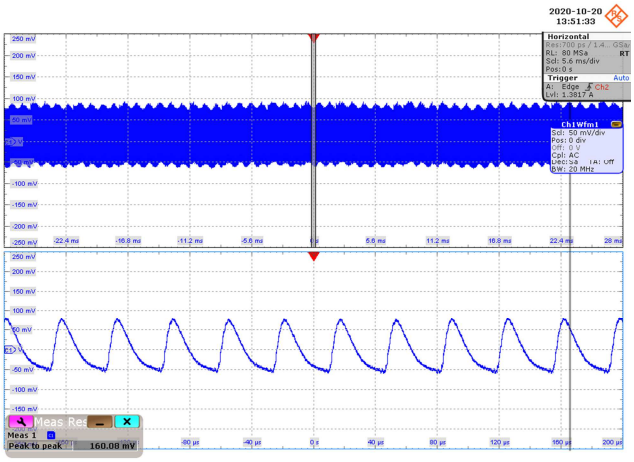

Figure 44 – Output Voltage Ripple.
V_{IN} = 400 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 160 mV_{P-P}.

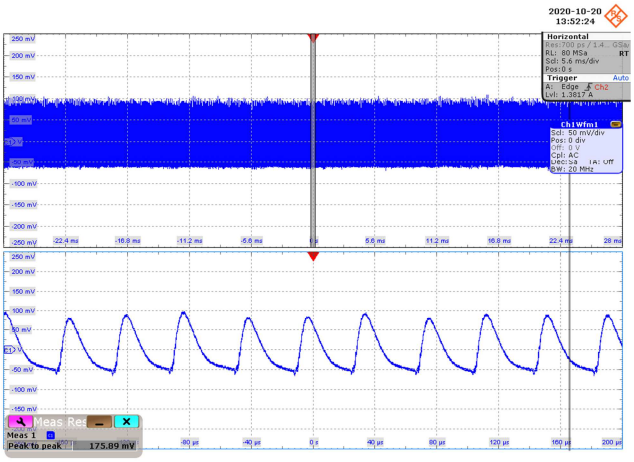

Figure 45 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 176 mV_{P-P}.

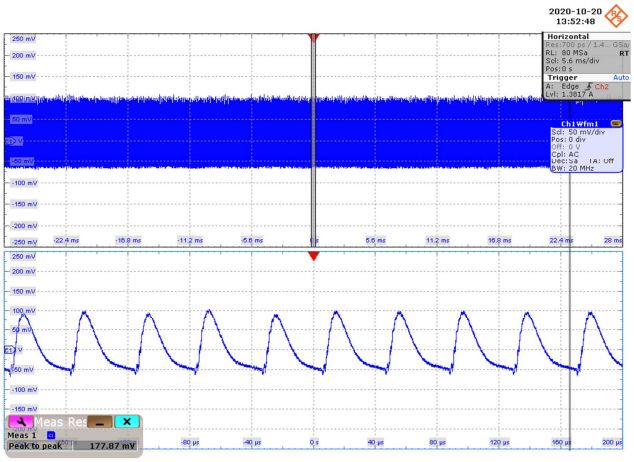

Figure 46 – Output Voltage Ripple.
V_{IN} = 1000 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 178 mV_{P-P}.

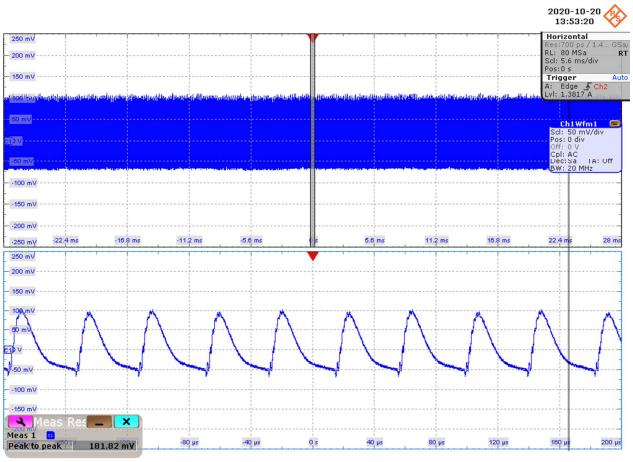

Figure 47 – Output Voltage Ripple.
V_{IN} = 1200 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 182 mV_{P-P}.

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9.7.3 50% Loading Condition

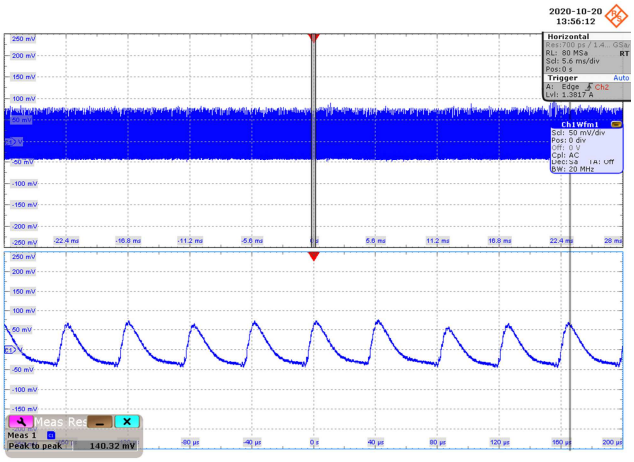

Figure 48 – Output Voltage Ripple.
V_{IN} = 400 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 140 mV_{P-P}.

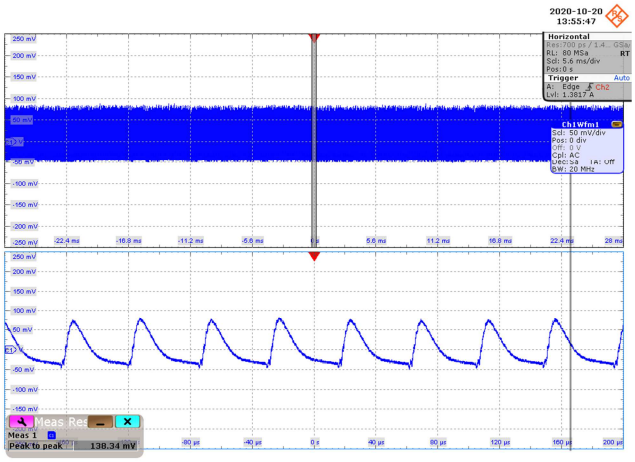

Figure 49 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 138 mV_{P-P}.

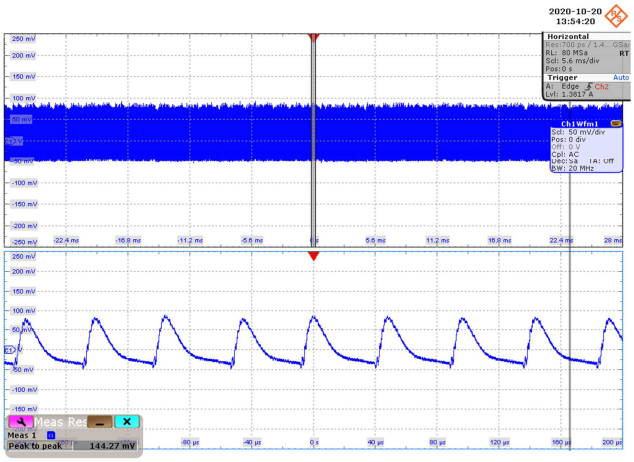

Figure 50 – Output Voltage Ripple.
V_{IN} = 1000 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 144 mV_{P-P}.

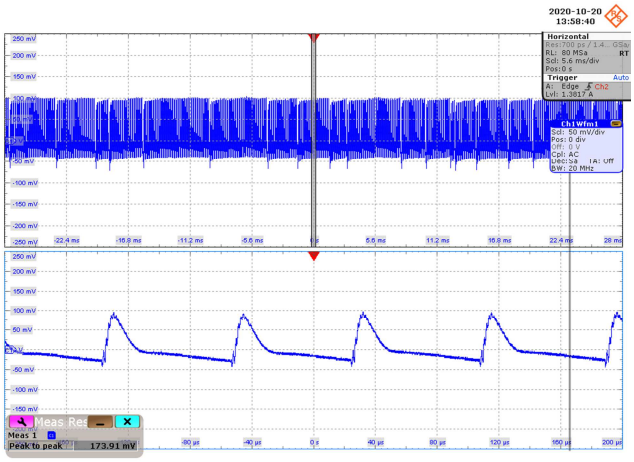

Figure 51 – Output Voltage Ripple.
V_{IN} = 1200 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 174 mV_{P-P}.

9.7.4 25% Loading Condition

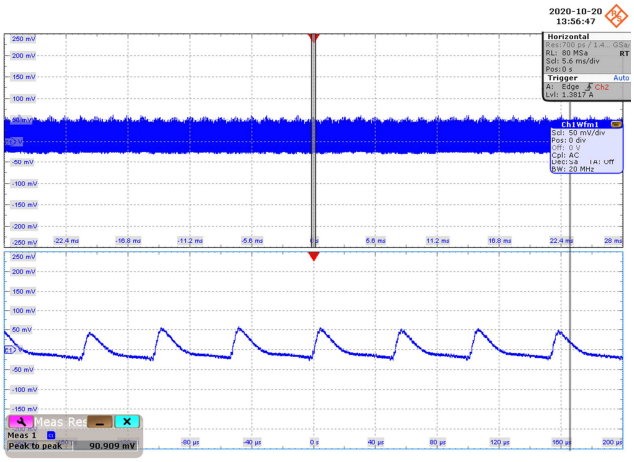

Figure 52 – Output Voltage Ripple.
V_{IN} = 400 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 99 mV_{P-P}.

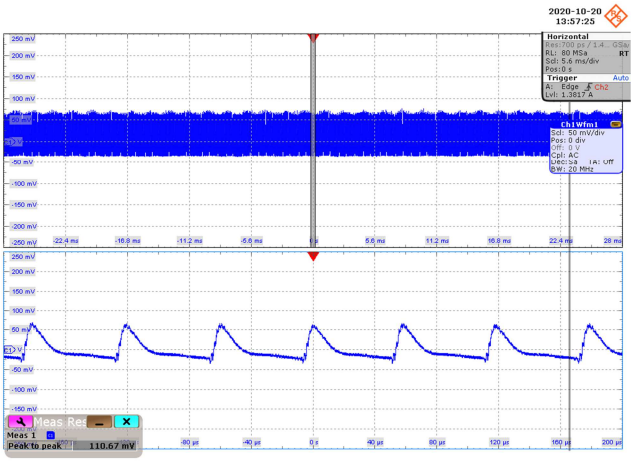

Figure 53 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 111 mV_{P-P}.

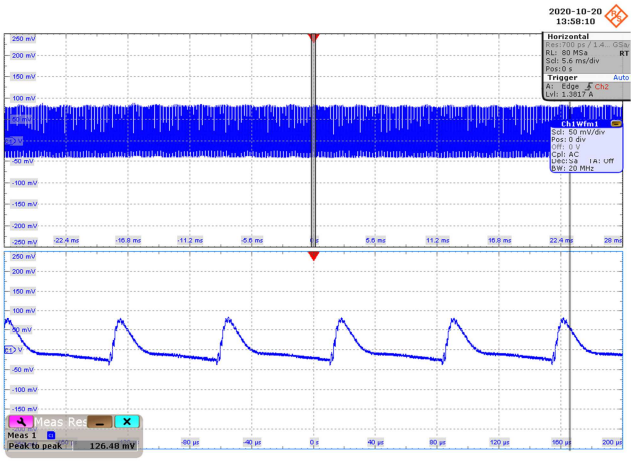

Figure 54 – Output Voltage Ripple.
V_{IN} = 1000 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 126 mV_{P-P}.

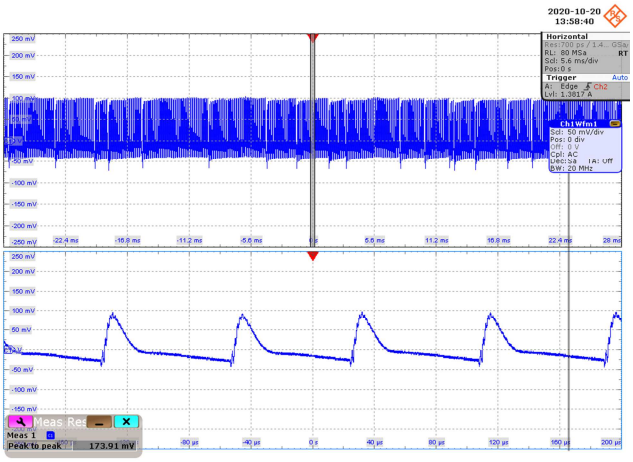

Figure 55 – Output Voltage Ripple.
V_{IN} = 1200 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 174 mV_{P-P}.

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9.7.5 0% Loading Condition

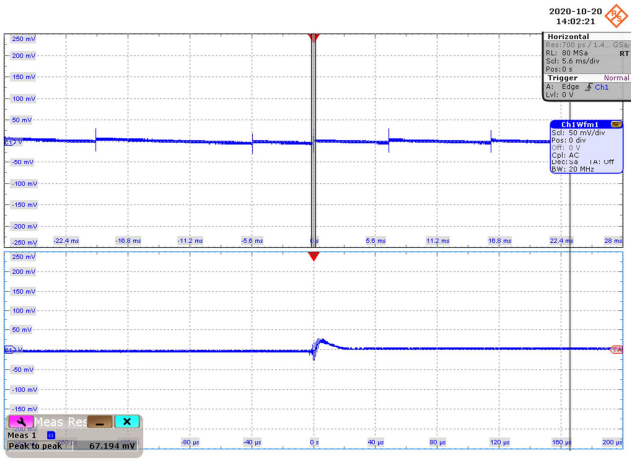

Figure 56 – Output Voltage Ripple.
V_{IN} = 400 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 67 mV_{P-P}.

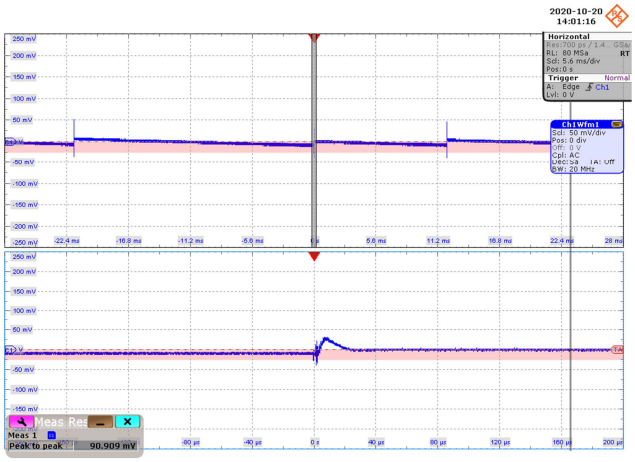

Figure 57 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 91 mV_{P-P}.

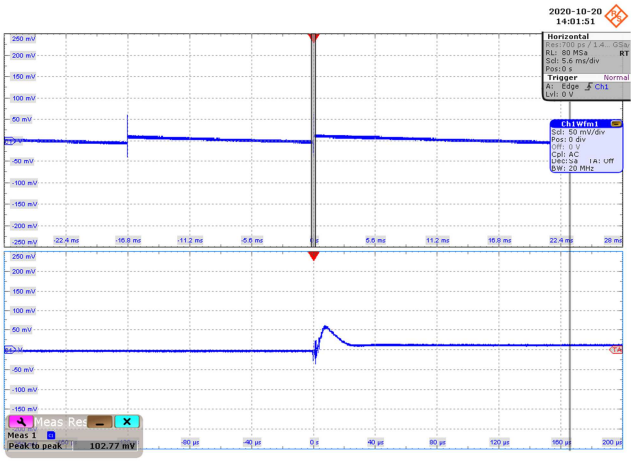

Figure 58 – Output Voltage Ripple.
V_{IN} = 1000 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 103 mV_{P-P}.

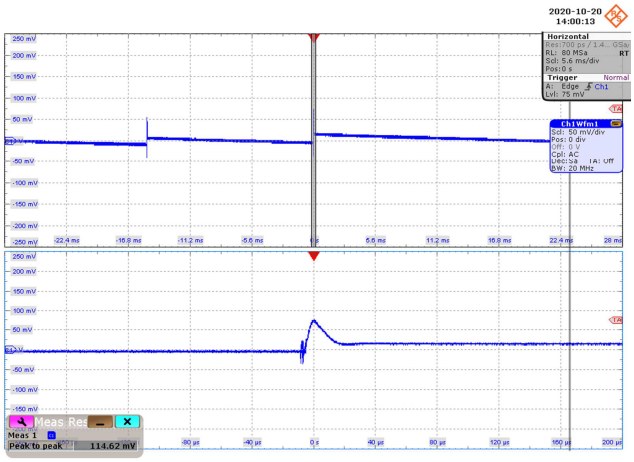

Figure 59 – Output Voltage Ripple.
V_{IN} = 1200 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
V_{RIPPLE} = 115 mV_{P-P}.

9.8 *Output Voltage Ripple (ATE)*

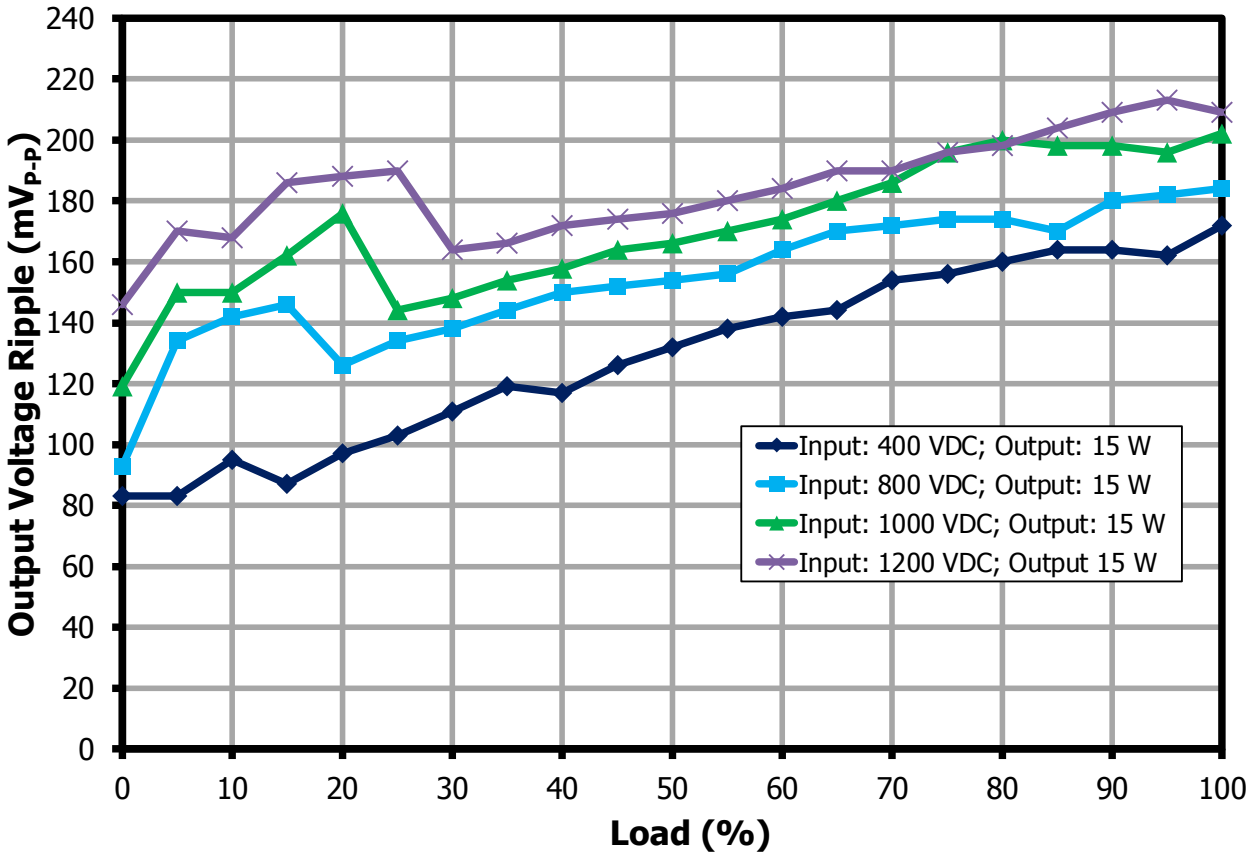

Figure 60 – Output Voltage Ripple.

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9.9 ***Output Load Transient***

9.9.1 Output Load Transient, 100% to 50% Load

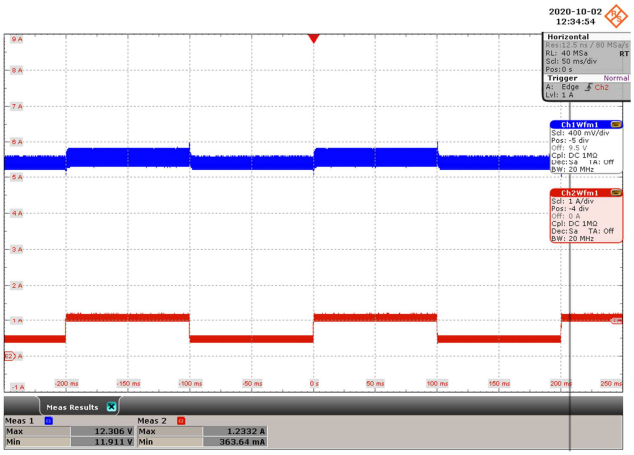

Figure 61 – Output Load Transient, 100% to 50% Load.
V_{IN} = 400 VDC, I_{OUT} = 1.25 A to 0.625 A.
$V_{OUT(MAX)}$ = 12.31 V, $V_{OUT(MIN)}$= 11.91 V.
Upper: V_{OUT}, 400 mV,50 ms / div.
Lower: $I_{OUT,}$ 1 A, 50 ms / div.

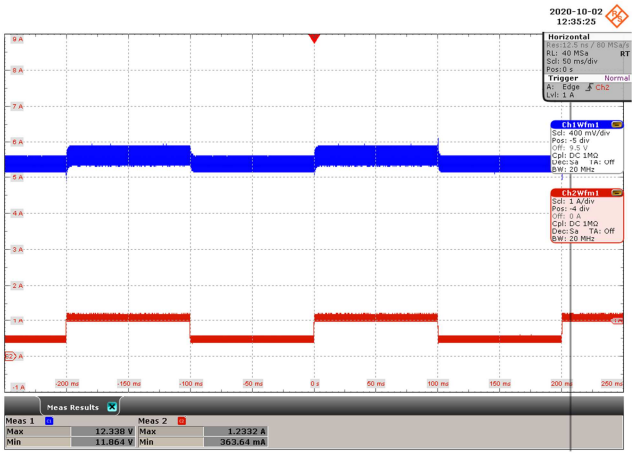

Figure 62 – Output Load Transient, 100 % to 50 % Load.
V_{IN} = 800 VDC, I_{OUT} = 1.25 A to 0.625 A.
$V_{OUT(MAX)}$ = 12.34 V, $V_{OUT(MIN)}$= 11.85 V.
Upper: V_{OUT}, 400 mV, 50 ms / div.
Lower: $I_{OUT,}$ 1 A, 50 ms / div.

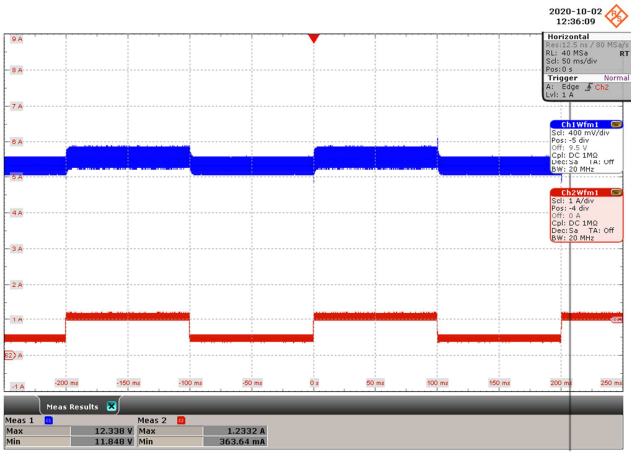

Figure 63 – Output Load Transient, 100% to 50% Load.
V_{IN} = 1000 VDC, I_{OUT} = 1.25 A to 0.625 A.
$V_{OUT(MAX)}$ = 12.34 V, $V_{OUT(MIN)}$= 11.85 V.
Upper: V_{OUT}, 400 mV, 50 ms / div.
Lower: $I_{OUT,}$ 1 A, 50 ms / div.

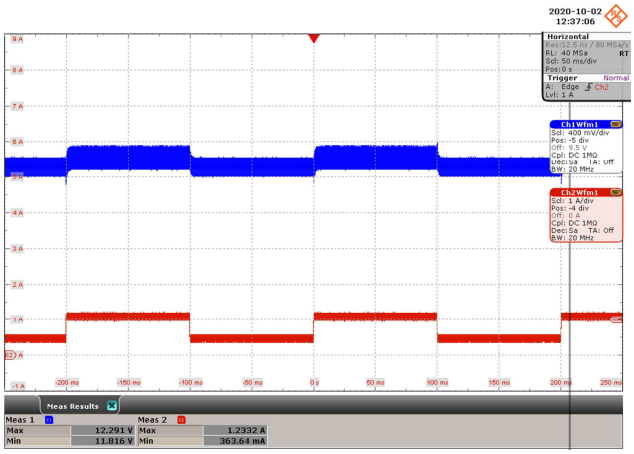

Figure 64 – Output Load Transient, 100 % to 50 % Load.
V_{IN} = 1200 VDC, I_{OUT} = 1.25 A to 0.625 A.
$V_{OUT(MAX)}$ = 12.29 V, $V_{OUT(MIN)}$= 11.82 V.
Upper: V_{OUT}, 400 mV, 50 ms / div.
Lower: $I_{OUT,}$ 1 A, 50 ms / div.

9.9.2 Output Load Transient, 100% to 0% Load

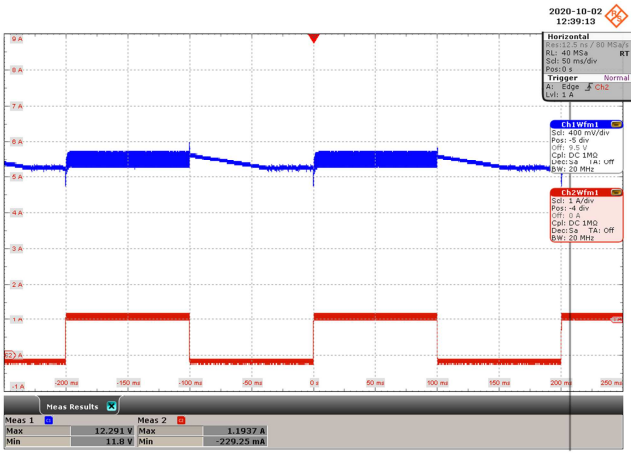

Figure 65 – Output Load Transient, 100% to 0% Load.
V_{IN} = 400 VDC, I_{OUT} = 1.25 A to 0 A.
$V_{OUT(MAX)}$ = 12.29 V, $V_{OUT(MIN)}$= 11.8 V.
Upper: V_{OUT}, 400 mV,50 ms / div.
Lower: $I_{OUT,}$ 1 A, 50 ms / div.

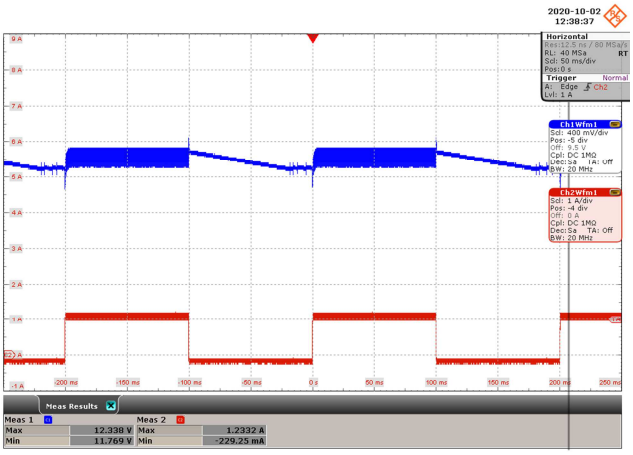

Figure 66 – Output Load Transient, 100 % to 0 % Load.
V_{IN} = 800 VDC, I_{OUT} = 1.25 A to 0 A.
$V_{OUT(MAX)}$ = 12.34 V, $V_{OUT(MIN)}$= 11.77 V.
Upper: V_{OUT}, 400 mV, 50 ms / div.
Lower: $I_{OUT,}$ 1 A, 50 ms / div.

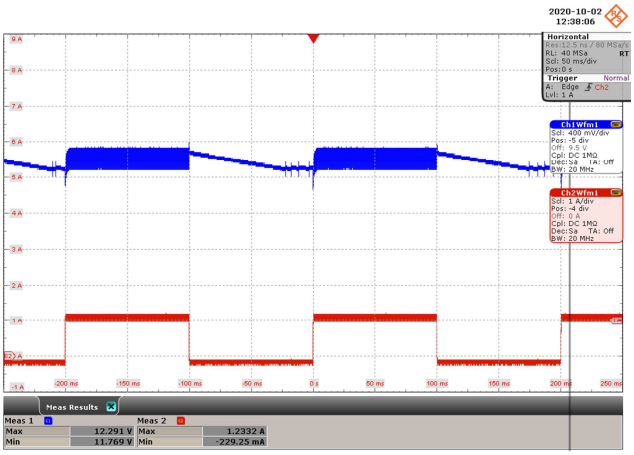

Figure 67 – Output Load Transient, 100% to 0% Load.
V_{IN} = 1000 VDC, I_{OUT} = 1.25 A to 0 A.
$V_{OUT(MAX)}$ = 12.29 V, $V_{OUT(MIN)}$= 11.77 V.
Upper: V_{OUT}, 400 mV, 50 ms / div.
Lower: $I_{OUT,}$ 1 A, 50 ms / div.

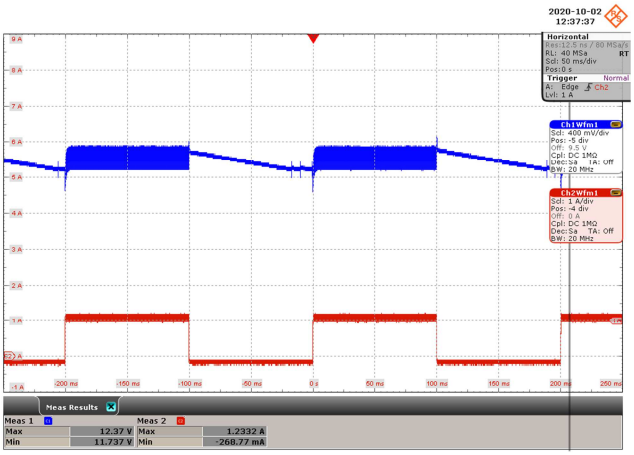

Figure 68 – Output Load Transient, 100 % to 0 % Load.
V_{IN} = 1200 VDC, I_{OUT} = 1.25 A to 0 A.
$V_{OUT(MAX)}$ = 12.37 V, $V_{OUT(MIN)}$= 11.74 V.
Upper: V_{OUT}, 400 mV, 50 ms / div.
Lower: $I_{OUT,}$ 1 A, 50 ms / div.

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9.10 *FWD Waveforms During Shorted Output*

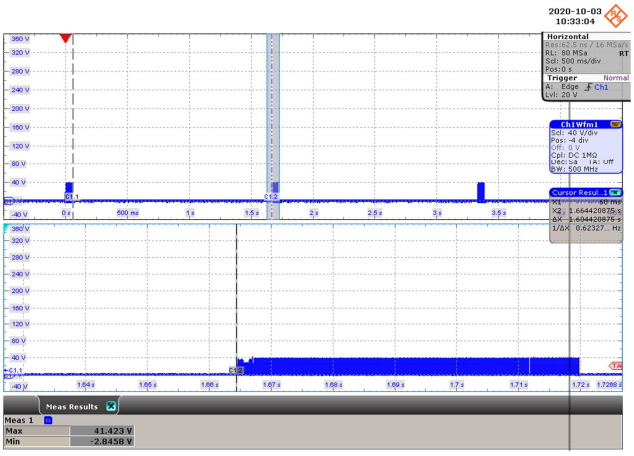

Figure 69 – FWD Voltage During Shorted Output.
V_{IN} = 400 VDC $V_{FWD(MAX)}$ = 41 V.
Upper: V_{FWD}, 40 V, 500 ms / div.
Lower: Zoom @ 10 µs / div.

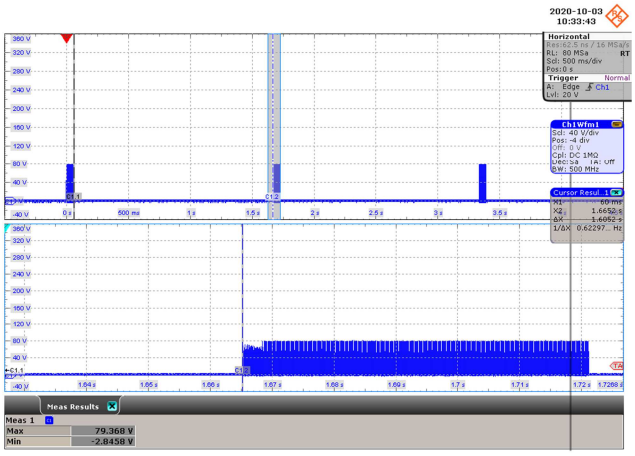

Figure 70 – FWD Voltage During Shorted Output.
V_{IN} = 800 VDC $V_{FWD(MAX)}$ = 79 V.
Upper: V_{FWD}, 40 V, 500 ms / div.
Lower: Zoom @ 10 µs / div.

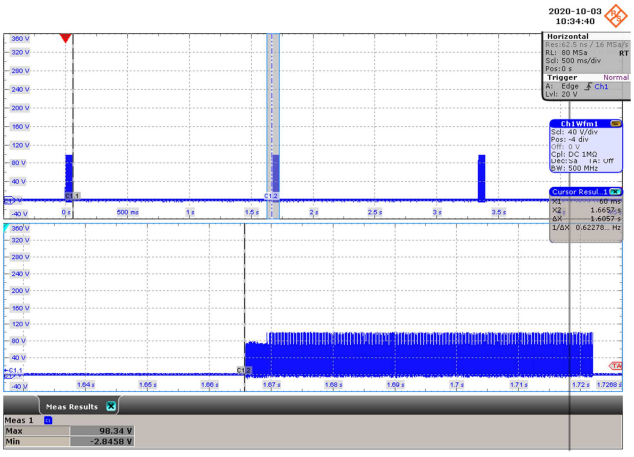

Figure 71 – FWD Voltage During Shorted Output.
V_{IN} = 1000 VDC $V_{FWD(MAX)}$ = 98 V.
Upper: V_{FWD}, 40 V, 500 ms / div.
Lower: Zoom @ 10 µs / div.

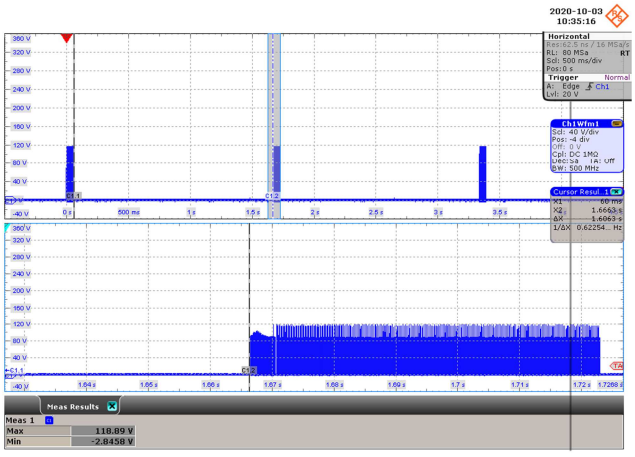

Figure 72 – FWD Voltage During Shorted Output.
V_{IN} = 1200 VDC $V_{FWD(MAX)}$ = 119 V.
Upper: V_{FWD}, 40 V, 500 ms / div.
Lower: Zoom @ 10 µs / div.

10 Thermal Performance

All measurements have been done at room ambient temperature after 1 hour of continuous operation.

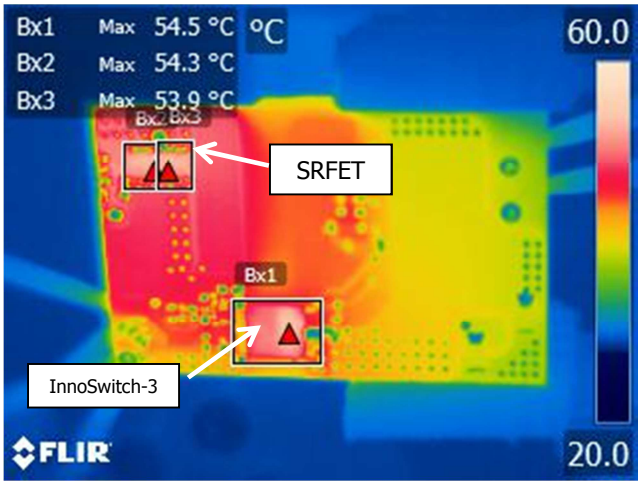

Figure 73 – 400 VDC 1.25 A Full Load.
Temperature of INN3996CQ: 54.5 ºC.
Temperature of SR FET1(Q2): 54.3 ºC.
Temperature of SR FET2(Q3): 53.9 ºC.
Ambient Temperature: 28.5 ºC.

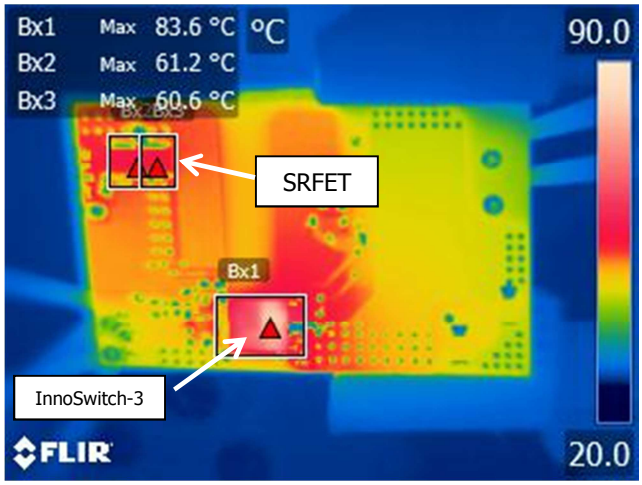

Figure 74 – 800 VDC 1.25 A Full Load.
Temperature of INN3996CQ: 83.6 ºC.
Temperature of SR FET1(Q2): 61.2 ºC.
Temperature of SR FET2(Q3): 60.6 ºC.
Ambient Temperature: 29 ºC.

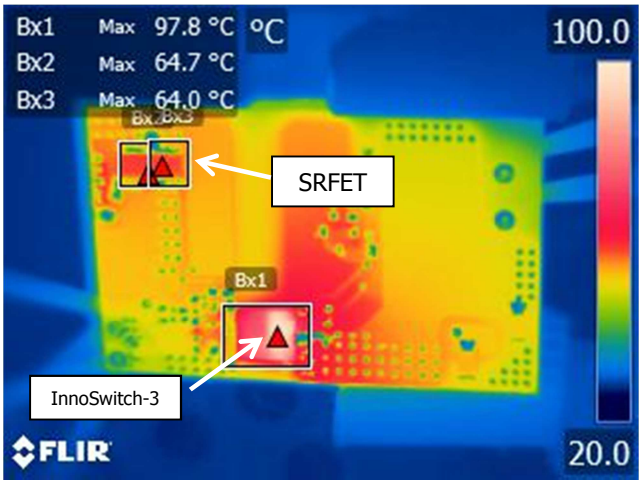

Figure 75 – 1000 VDC 1.25 A Full Load.
Temperature of INN3996CQ: 97.8 ºC.
Temperature of SR FET1(Q2): 64.7 ºC.
Temperature of SR FET2(Q3): 64.0 ºC.
Ambient Temperature: 29.3 ºC.

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10.1 *Temperature vs. Output Power*

400 VDC					
P_{OUT} (W)	INN3977CQ (ºC)	SR FET (ºC)	TVS (ºC)	STACKFET (ºC)	AMB (ºC)
15.07	54.5	54.3	41.1	41.7	28.5
11.31	49.9	47.6	38.2	39.9	28.3
7.53	49.6	42.8	37.5	38.9	28.3
3.74	43.6	36.3	34.7	35.4	27.8

800 VDC					
P_{OUT} (W)	INN3977CQ (ºC)	SR FET (ºC)	TVS (ºC)	STACKFET (ºC)	AMB (ºC)
15.05	83.6	61.2	52.4	52.5	29.3
11.31	78.9	54.4	49.6	50.7	27.9
7.51	71.6	48	46.2	47.1	27.9
3.74	59.3	40.2	41	42	27.8

1000 VDC					
P_{OUT} (W)	INN3977CQ (ºC)	SR FET (ºC)	TVS (ºC)	STACKFET (ºC)	AMB (ºC)
15.08	97.8	64.7	59.8	61.7	29.3
11.30	90.3	58.1	56.1	59.2	27.7
7.51	83.8	53.5	54.4	55.2	30.1
3.75	64.5	43.6	46.6	47.2	29.7

10.2 *Maximum Output Power vs. Ambient Temperature*

(Based on 125 ºC junction temperature of INN3996CQ)

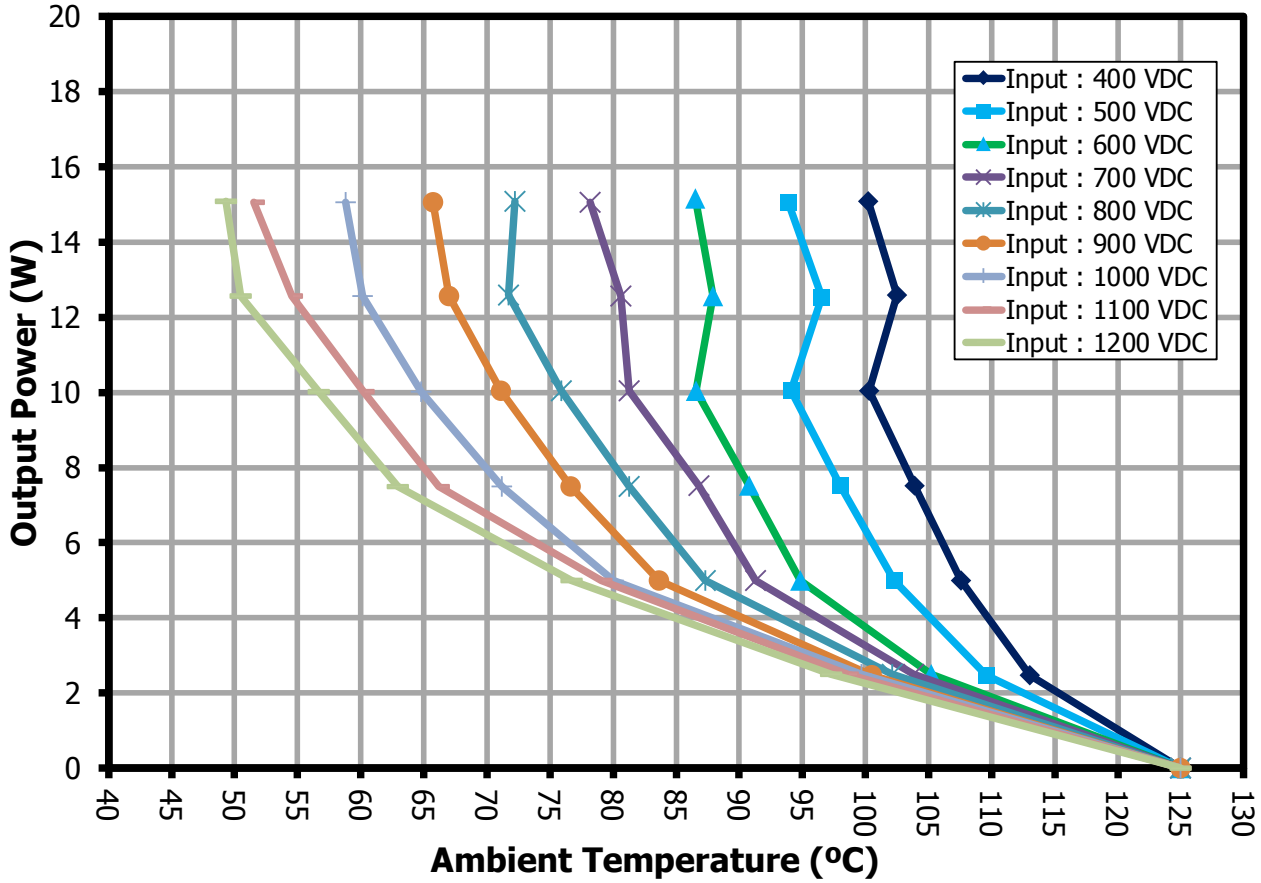

Figure 76 – Maximum Output Power vs. Ambient Temperature.

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11 Revision History

Date	Author	Revision	Description & Changes	Reviewed
08-Dec-20	MA	1.0	Initial Release.	Mktg & Apps
09-Apr-21	MA	1.1	Change Minimum Input Voltage from 300 VDC to 40 VDC.	Mktg & Apps
20-Apr-21	MA	1.2	Change Minimum Input Voltage from 40 VDC to 30 VDC.	Mktg & Apps

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