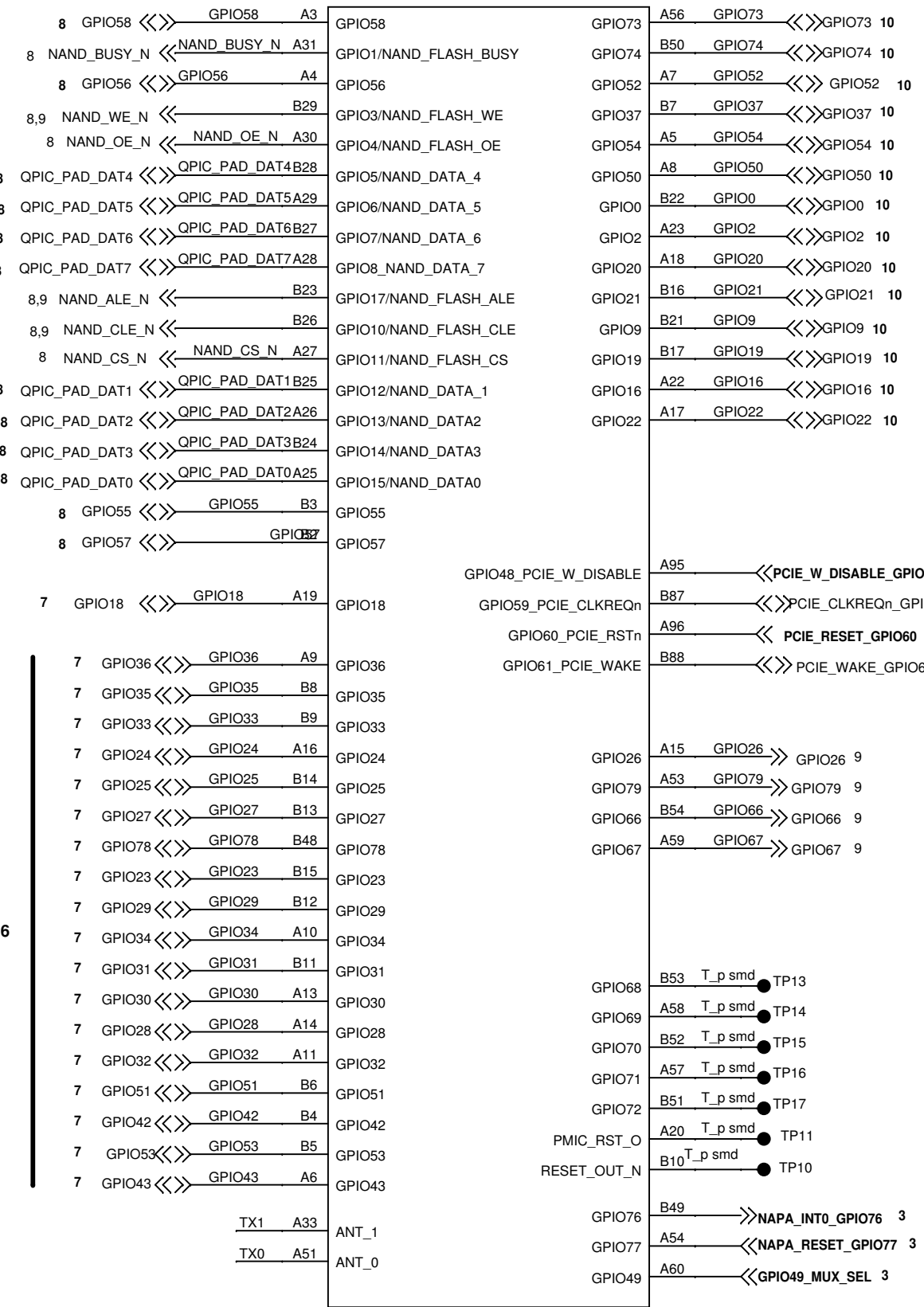
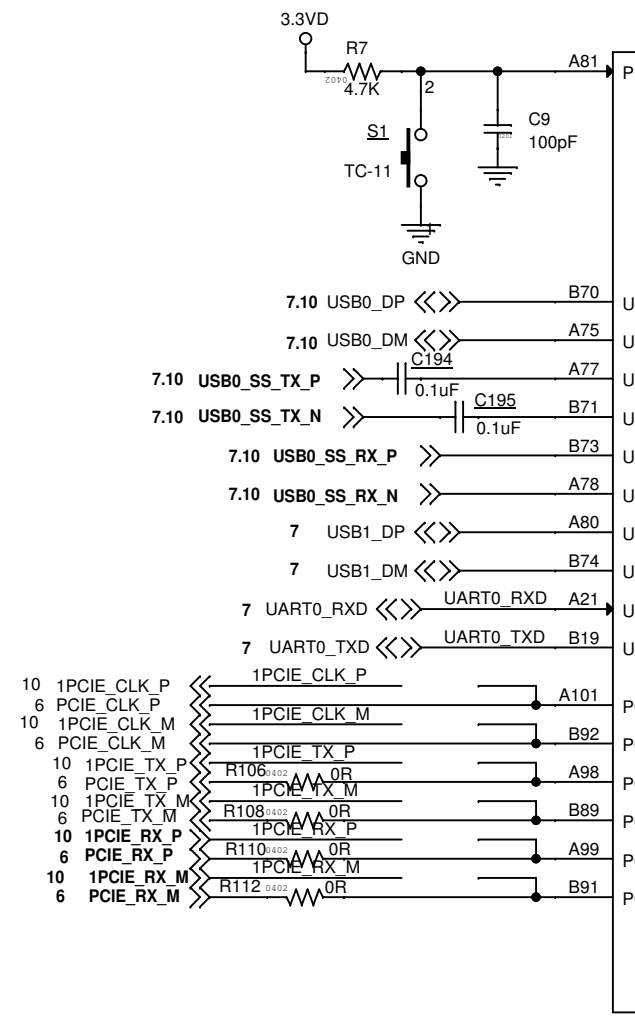
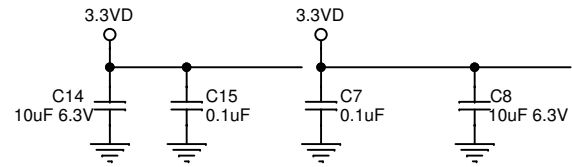


# MANGO Module

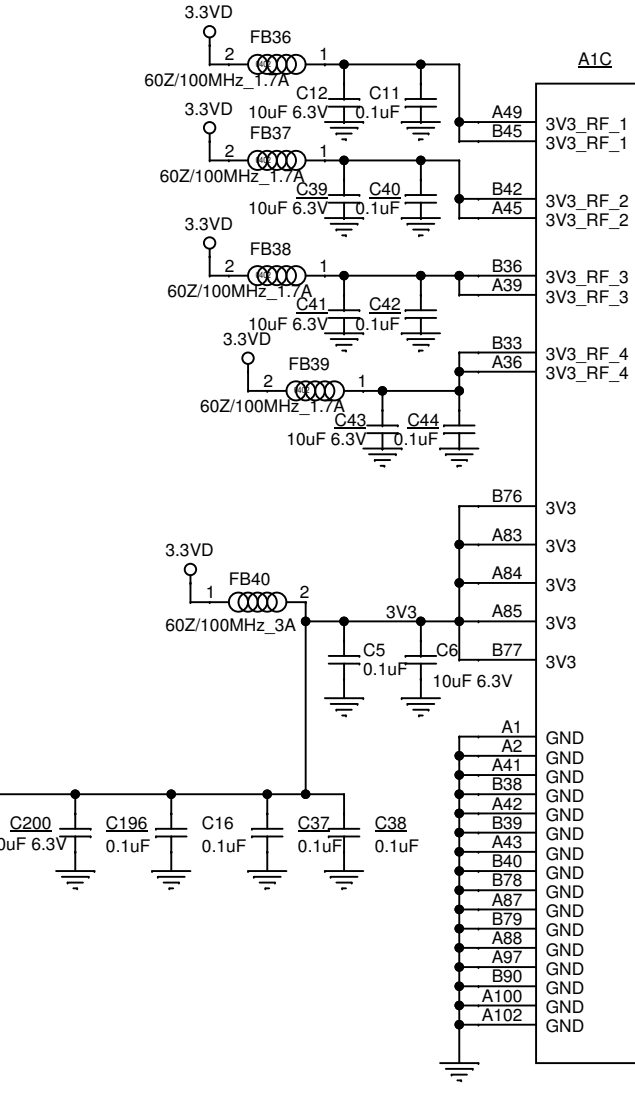
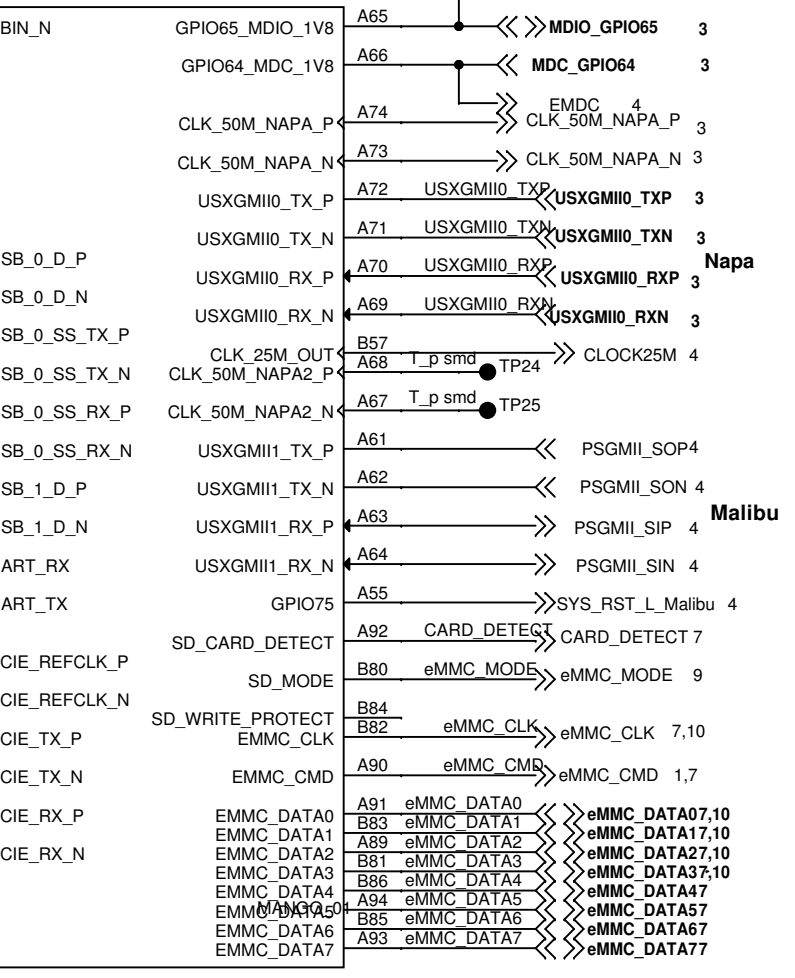
A1A



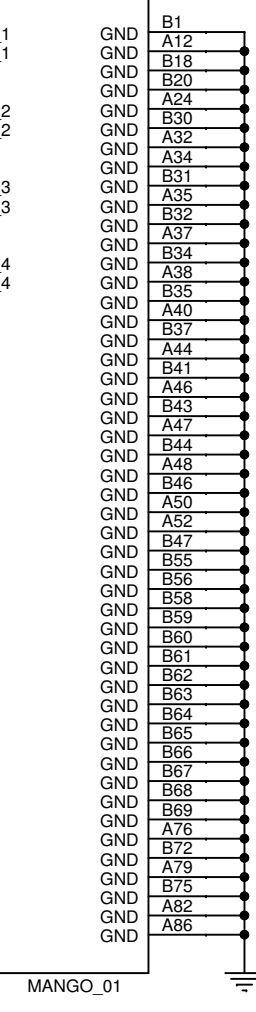
MANGO\_01



A1B

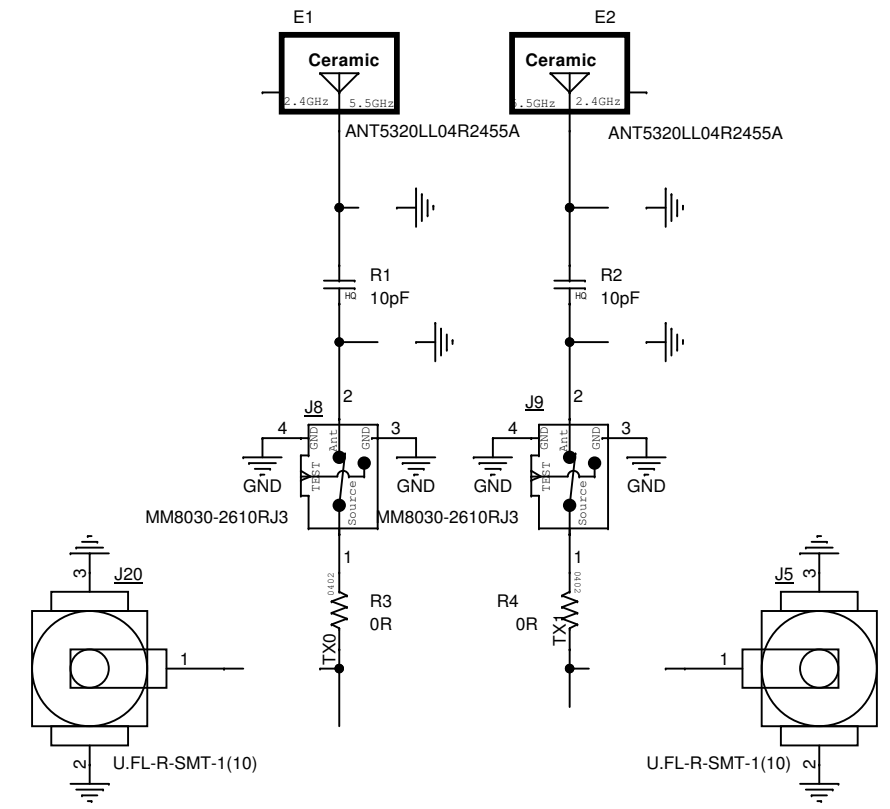


A1C



MANGO\_01

## Internal RF antenna

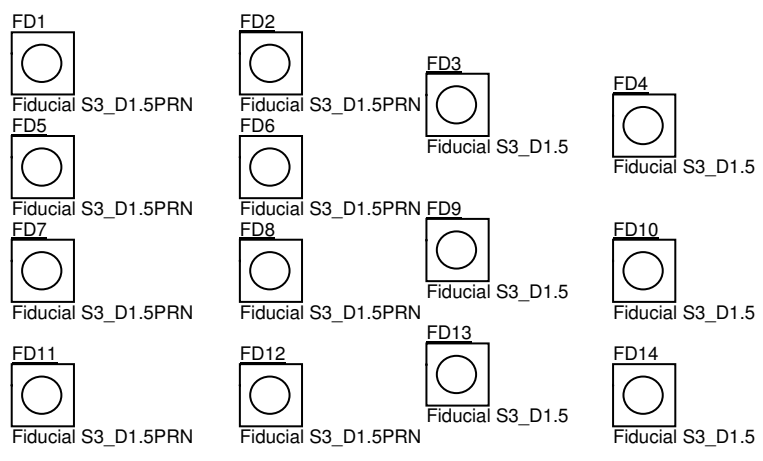
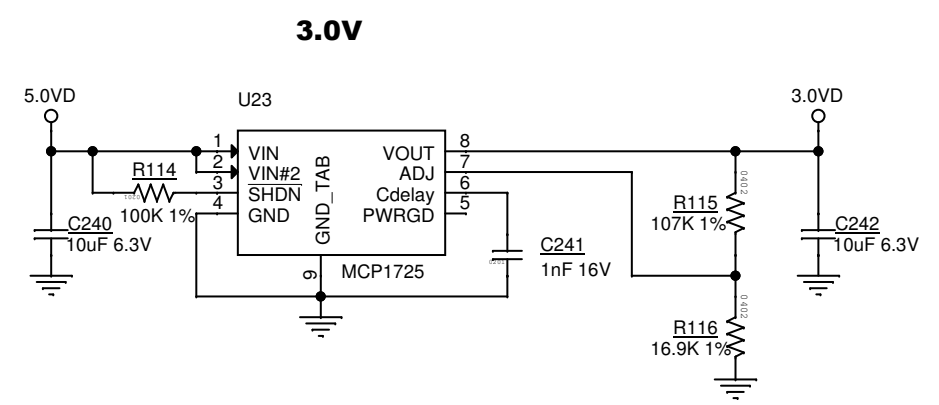
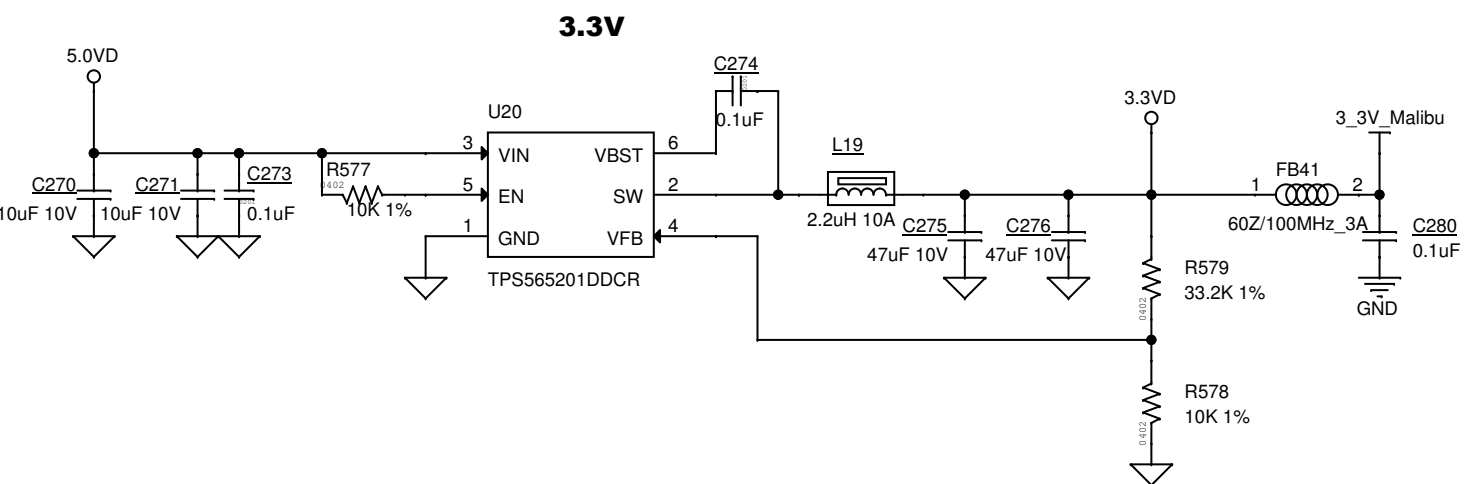
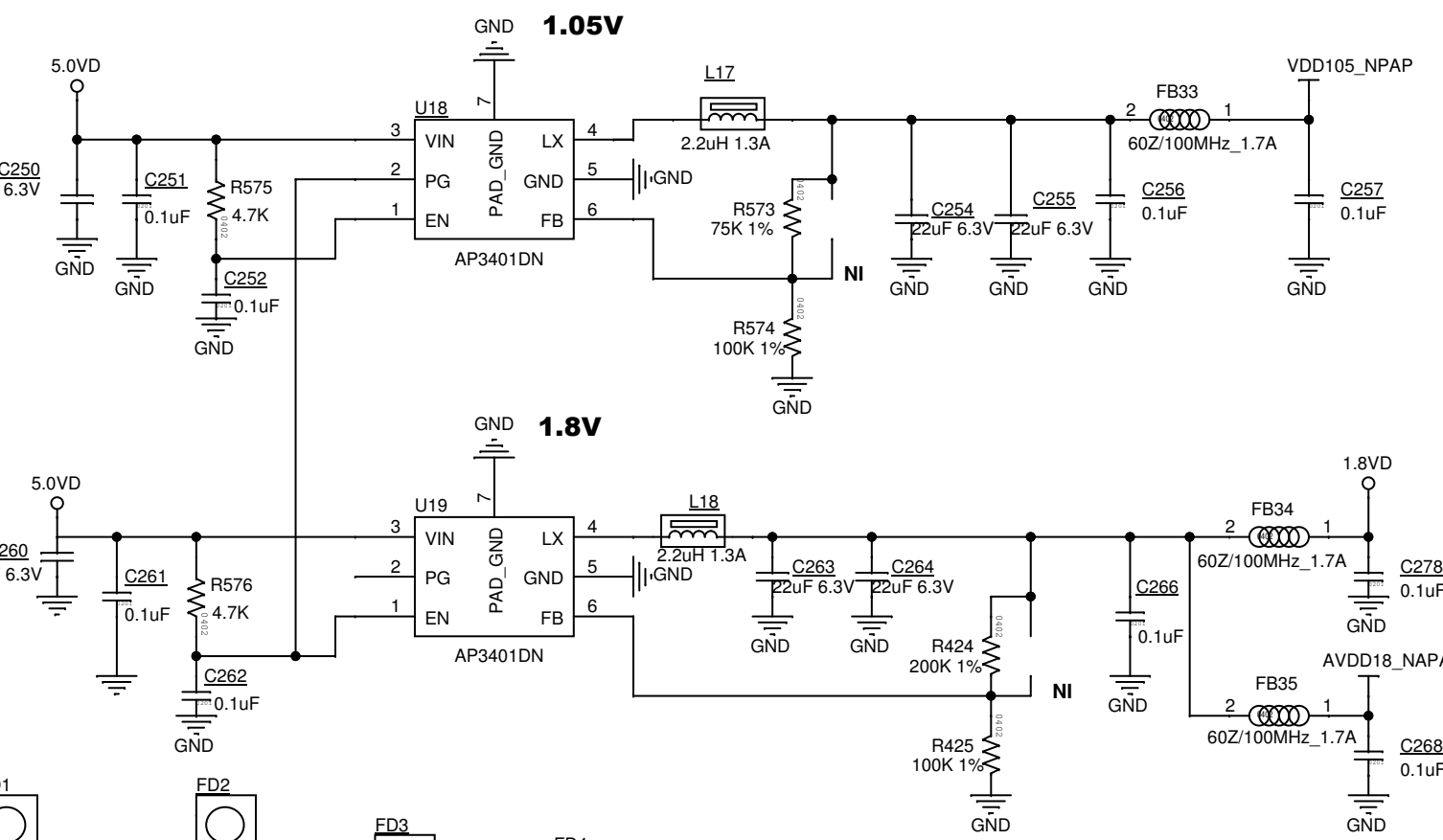
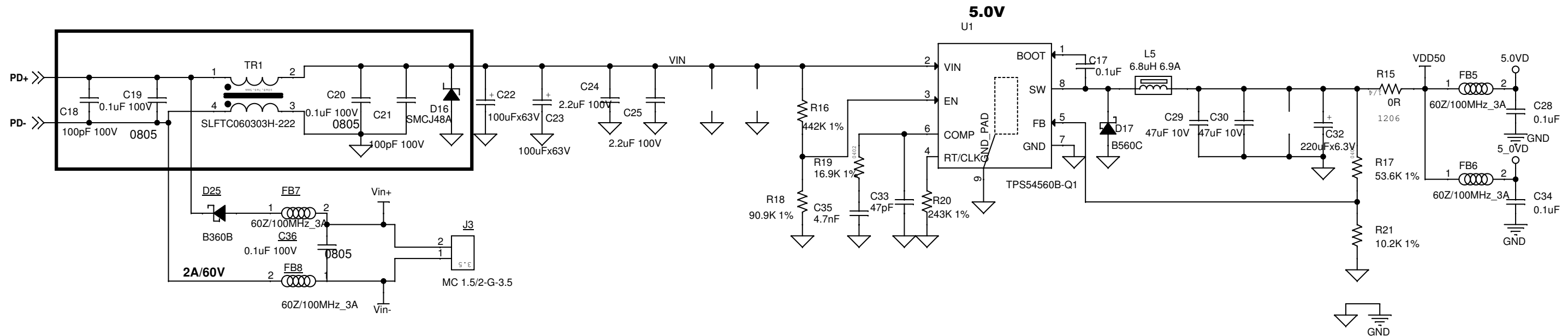



**8DEVICES**

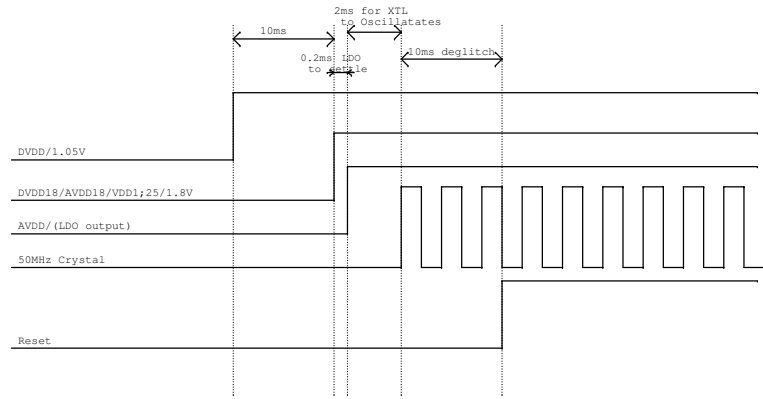
Approval

Drawing

Title: 01_MANGO		
Size: A3	Document Number: MAN_200_02_SB_DVK	Rev: 2.0
Date: Tuesday, December 01, 2020	Sheet: 1	of: 10



 <b>8Devices</b>	Approval	
	Drawing	
Title: 02_PowerSupply		
Size: B	Document Number: MAN_200_02_SB_DVK	Rev: 2.0
Date: Tuesday, December 01, 2020		Sheet 2 of 10

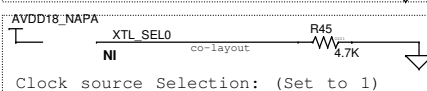
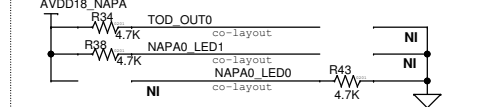
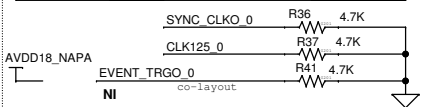


Mode Selection  
3'b000 -> function mode with MDIO  
3'b001 -> function mode with I2C

Mode	Pin	Signal	Default
Mode3	45	SYNC_CLKO_PTP	0
Mode2	27	CLK125_TDI	0
Mode1	26	EVENT_TRG_O	0

MDIO PHY address: 0x10/0x11  
1, Bit[1:0] 00 is NAPA PHY, 01 is NAPA SERDES

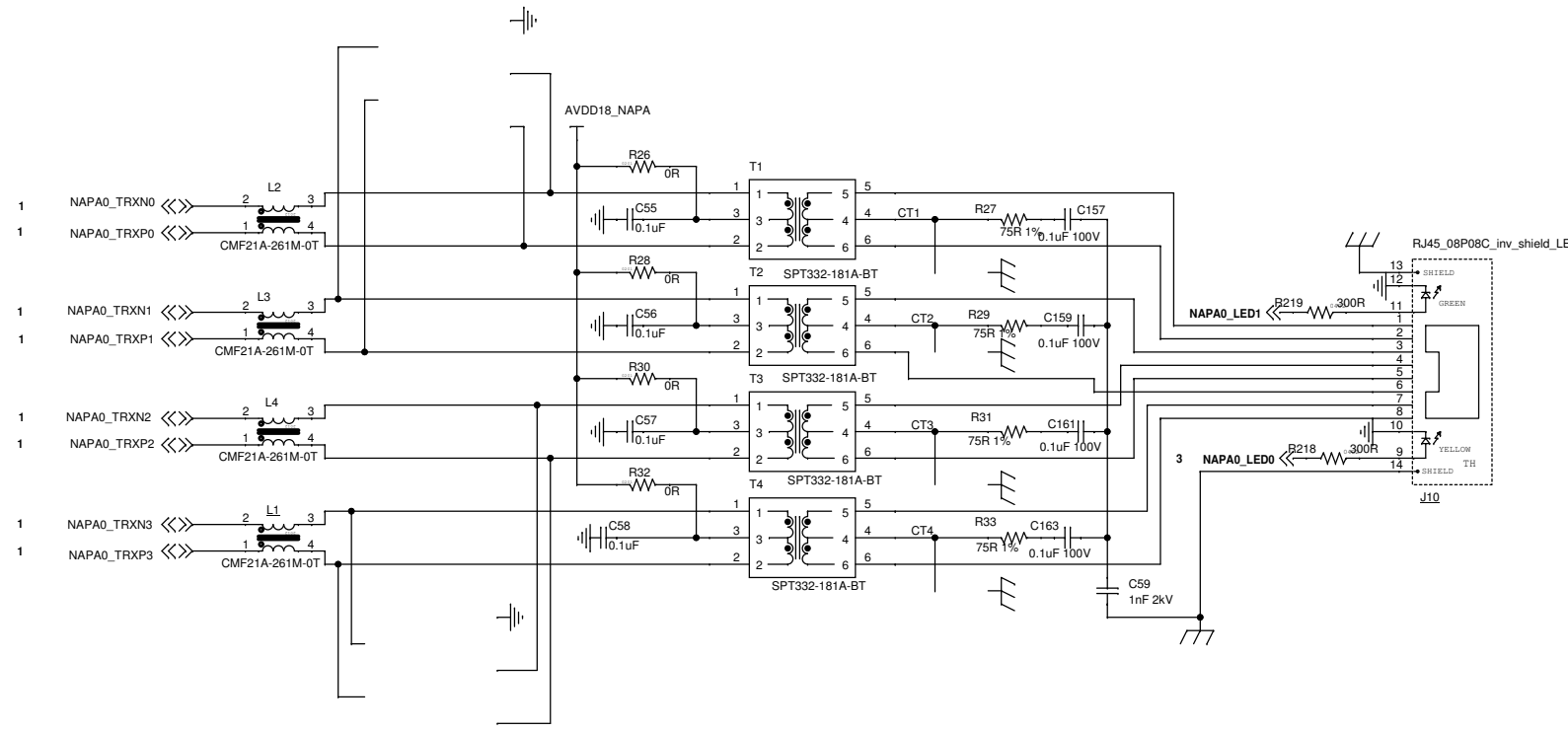
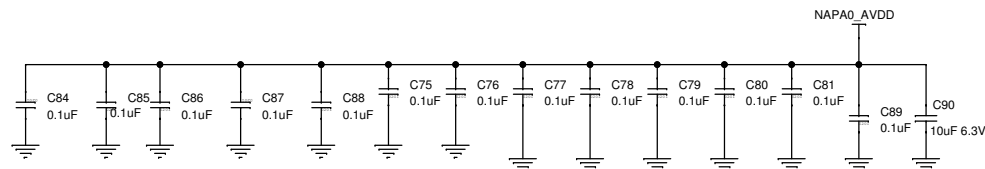
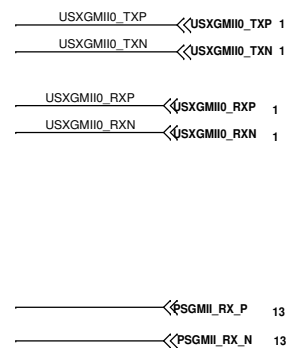
MDIO PHY Address	Pin	Signal	Default
phyaddr4	29	TOD_OUT	1
phyaddr3	49	LED1	0
phyaddr2	48	LED0	0



Pin	Signal	Setting	function
1	MDIO pad is OD	1	MDIO pad is OD
46	PPS_OUT	0	MDIO pad is CMOS

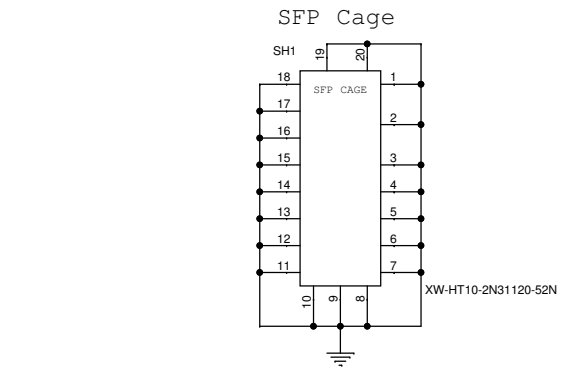
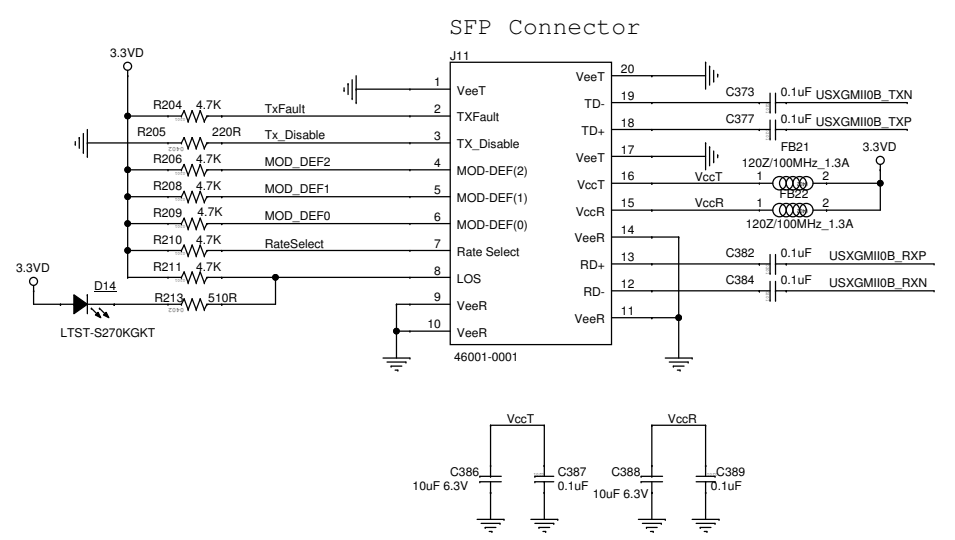
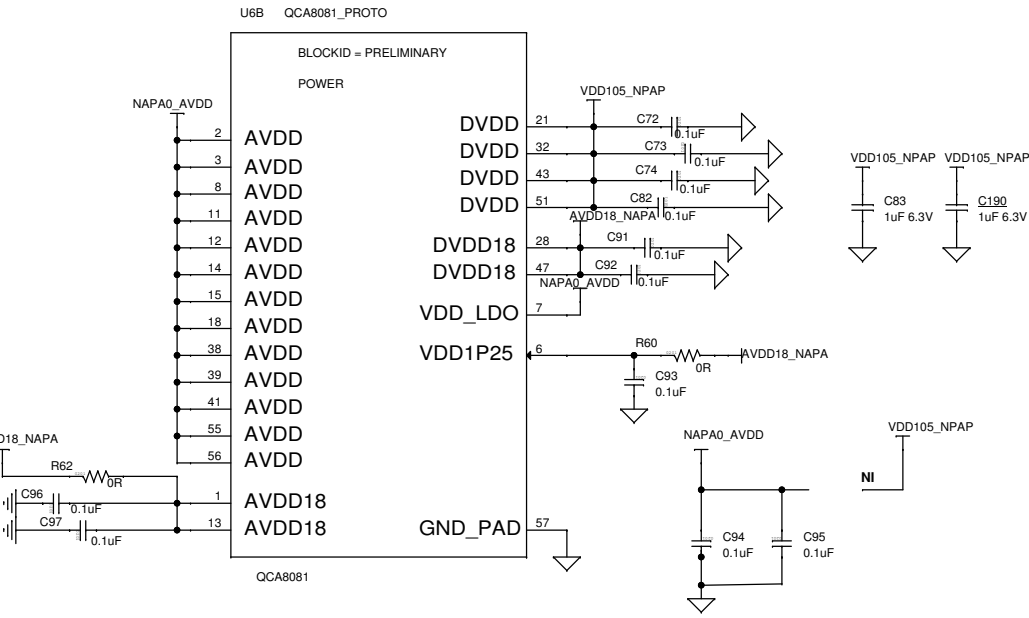
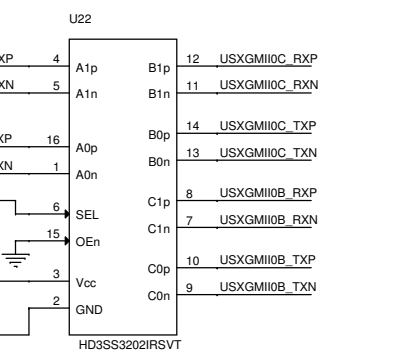
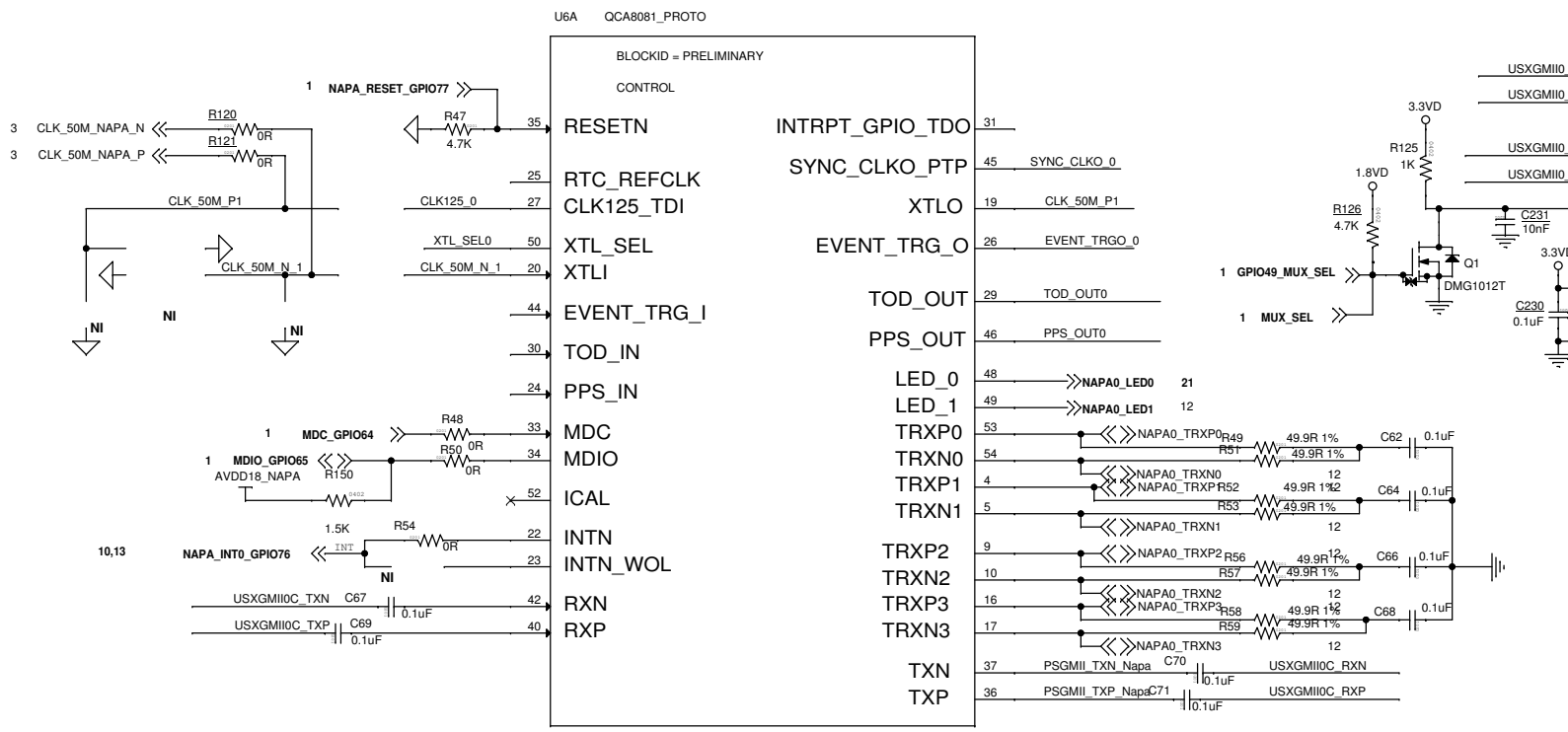
Clock source Selection: (Set to 1)

Pin	Signal	Setting	function
0	Use 50MHz LVDS source	0	Use 50MHz LVDS source
50	XTL_SEL	1	Use 50MHz crystal



2.5G Ethernet PHY

SGMII mux



8DEVICES

Approval

Drawing

File: 03\_2.5G PHY

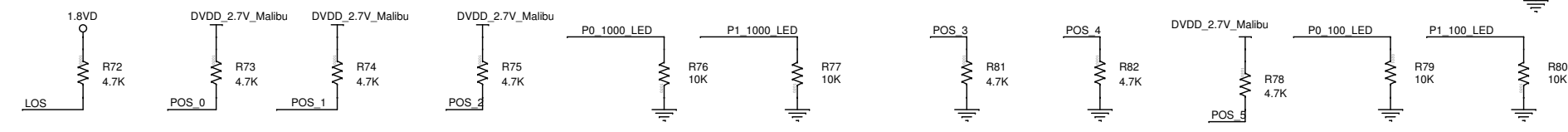
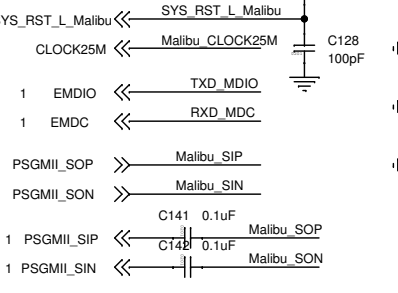
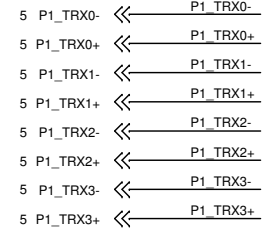
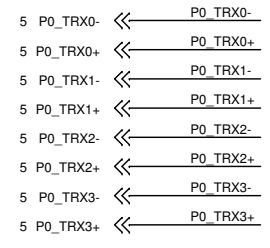
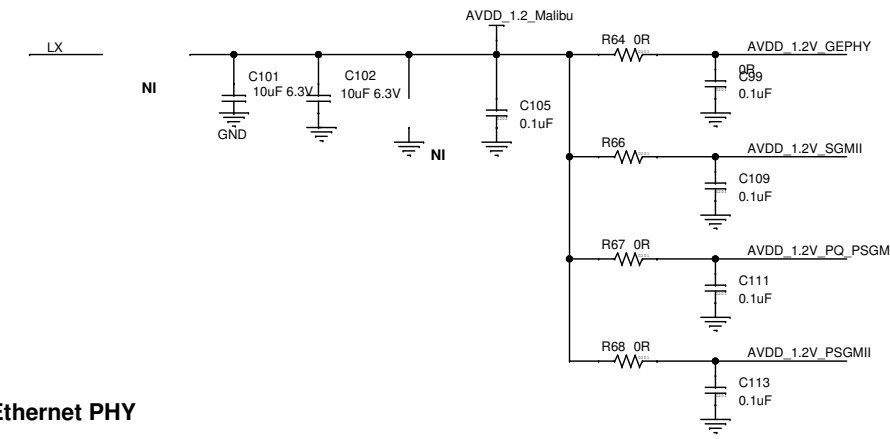
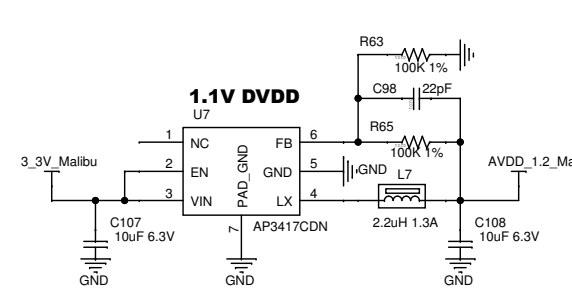
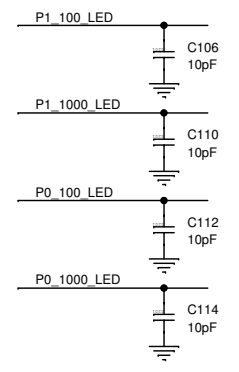
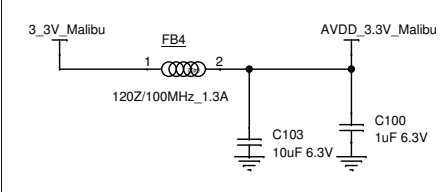
Size A2

Document Number: MAN\_200\_02\_SB\_DVK

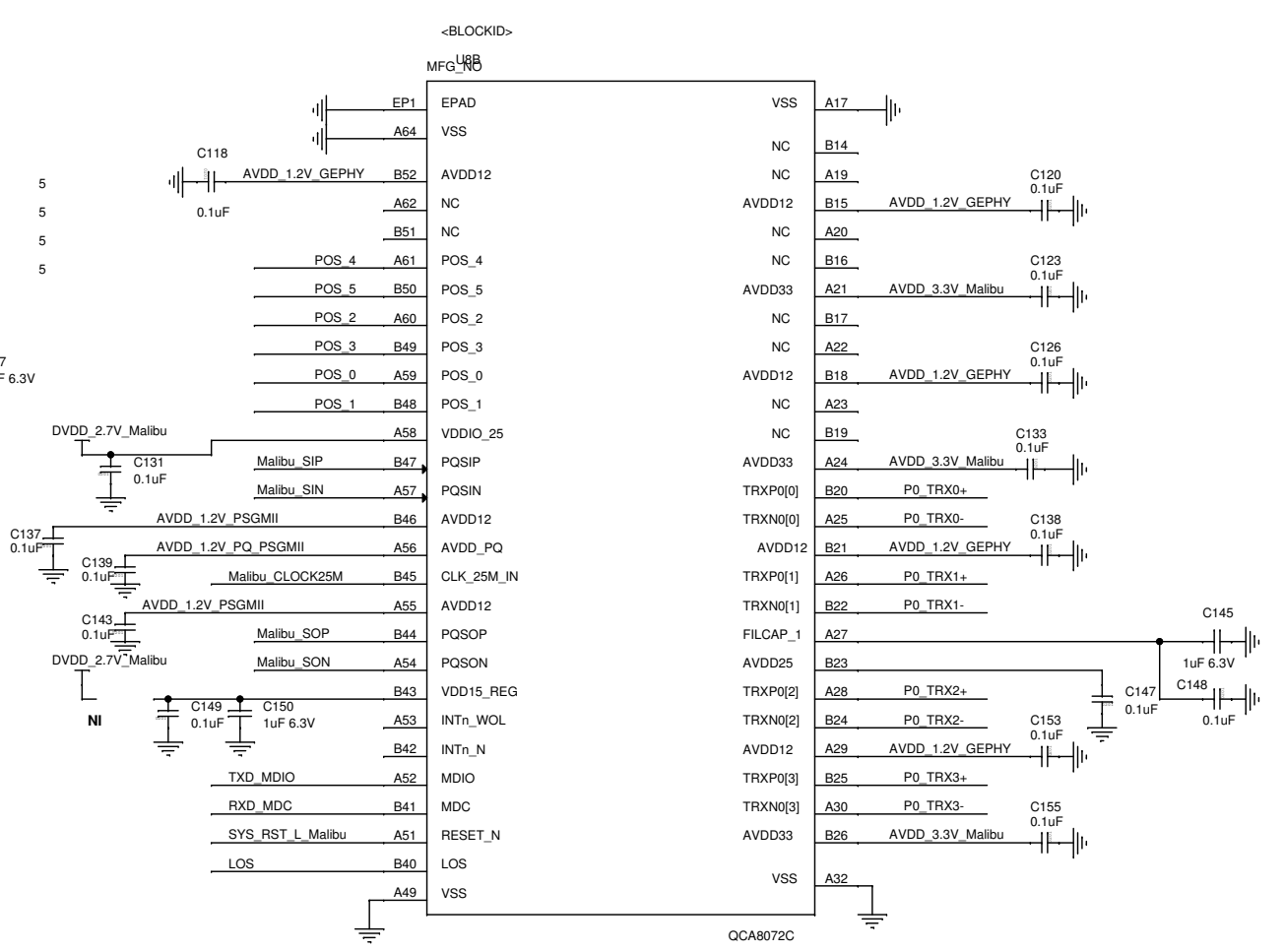
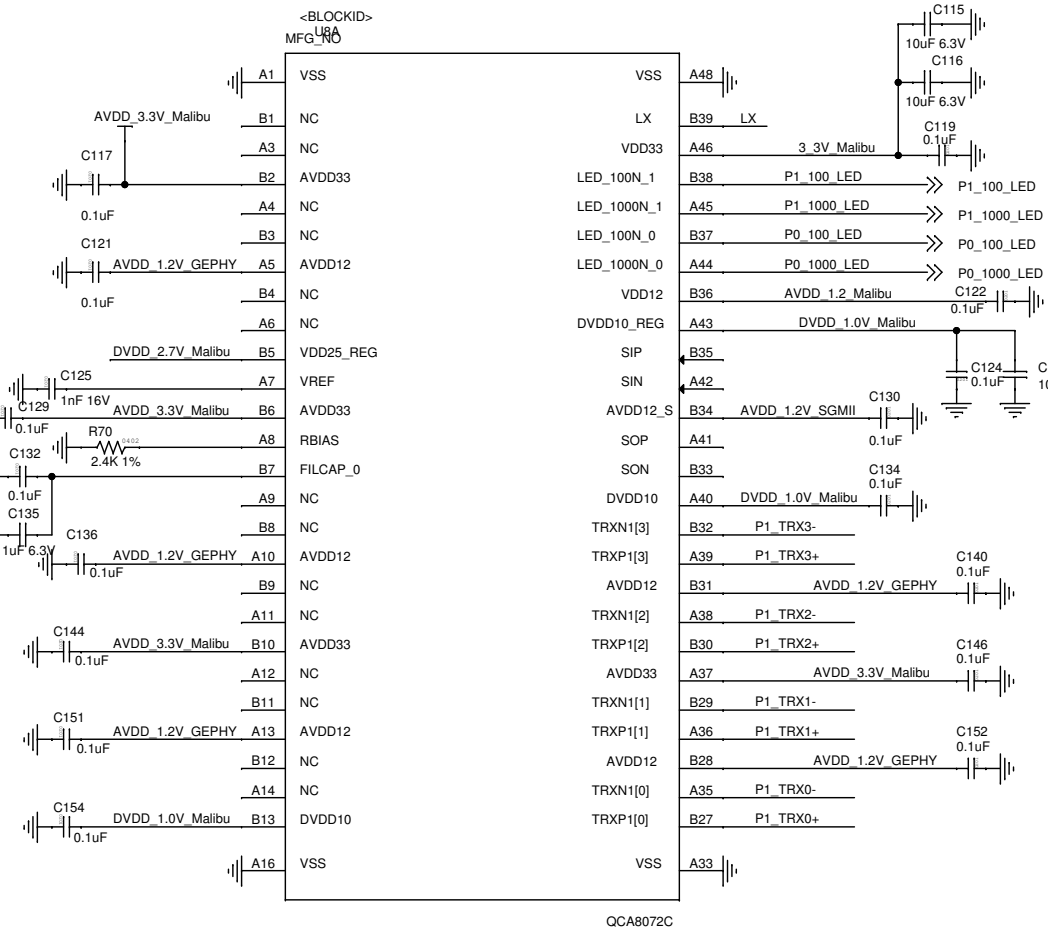
Date: Tuesday, December 01, 2020

Sheet 3 of 10

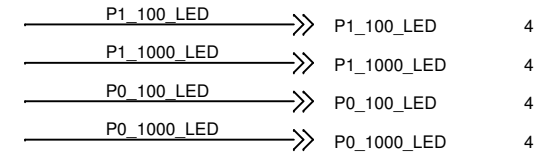
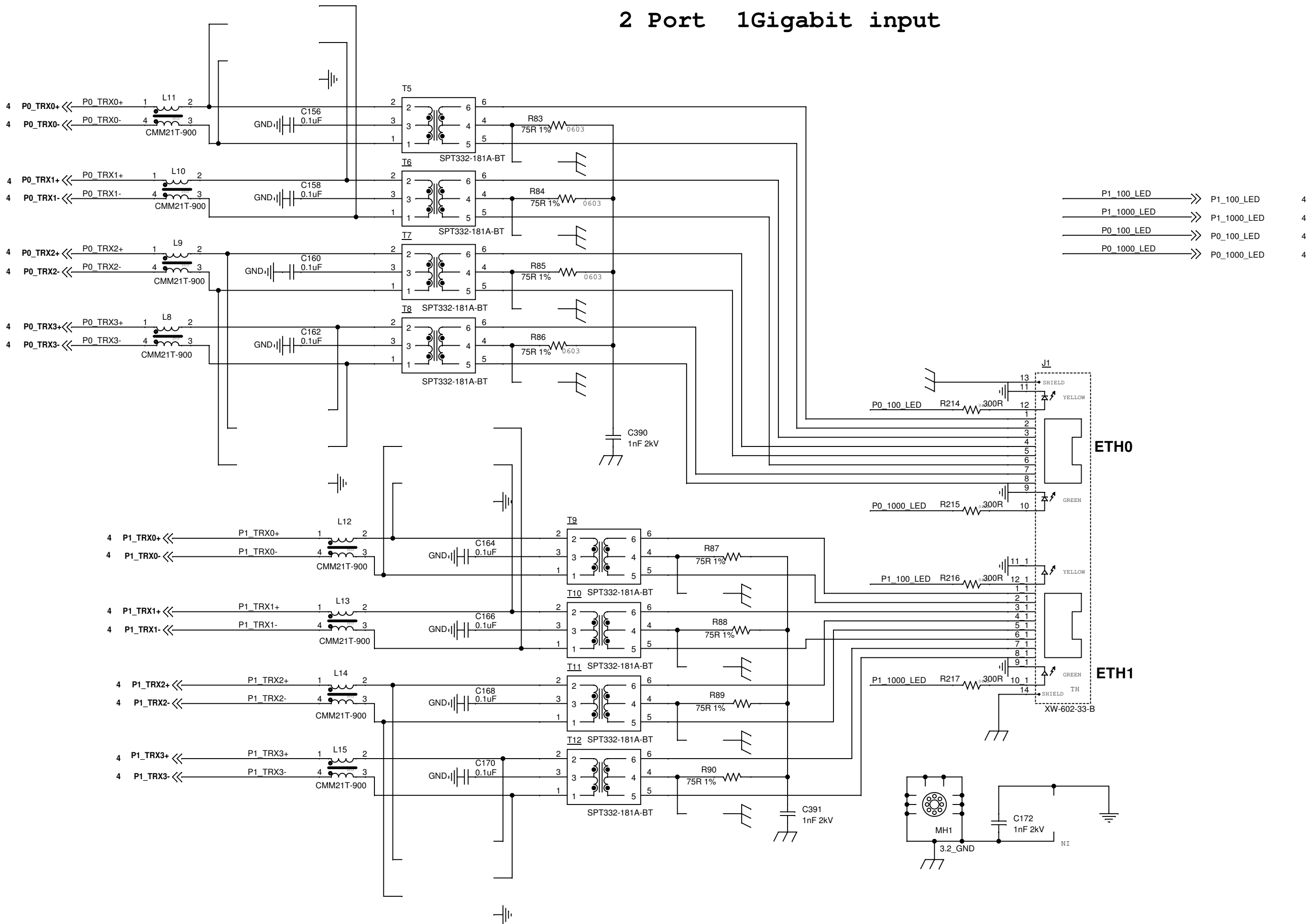
Rev 2.0




2 Port 1G Ethernet PHY

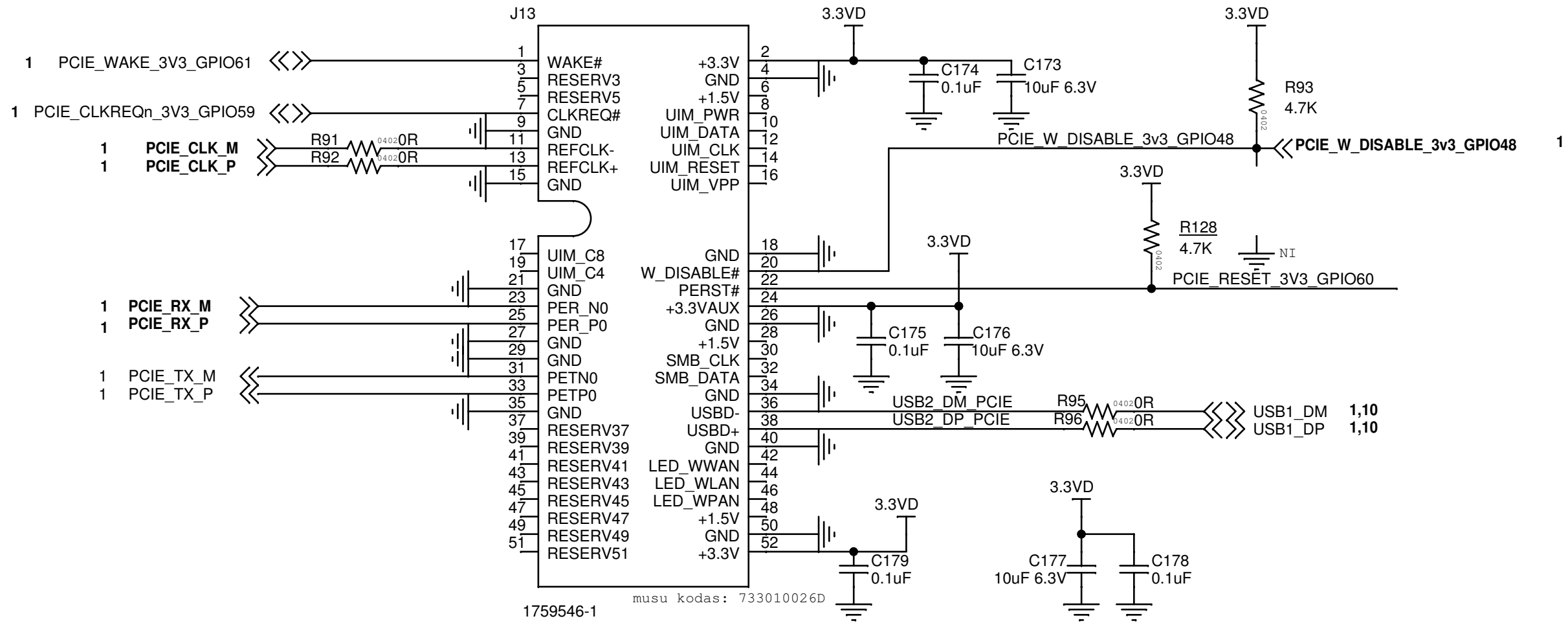


# 2 Port 1Gigabit input

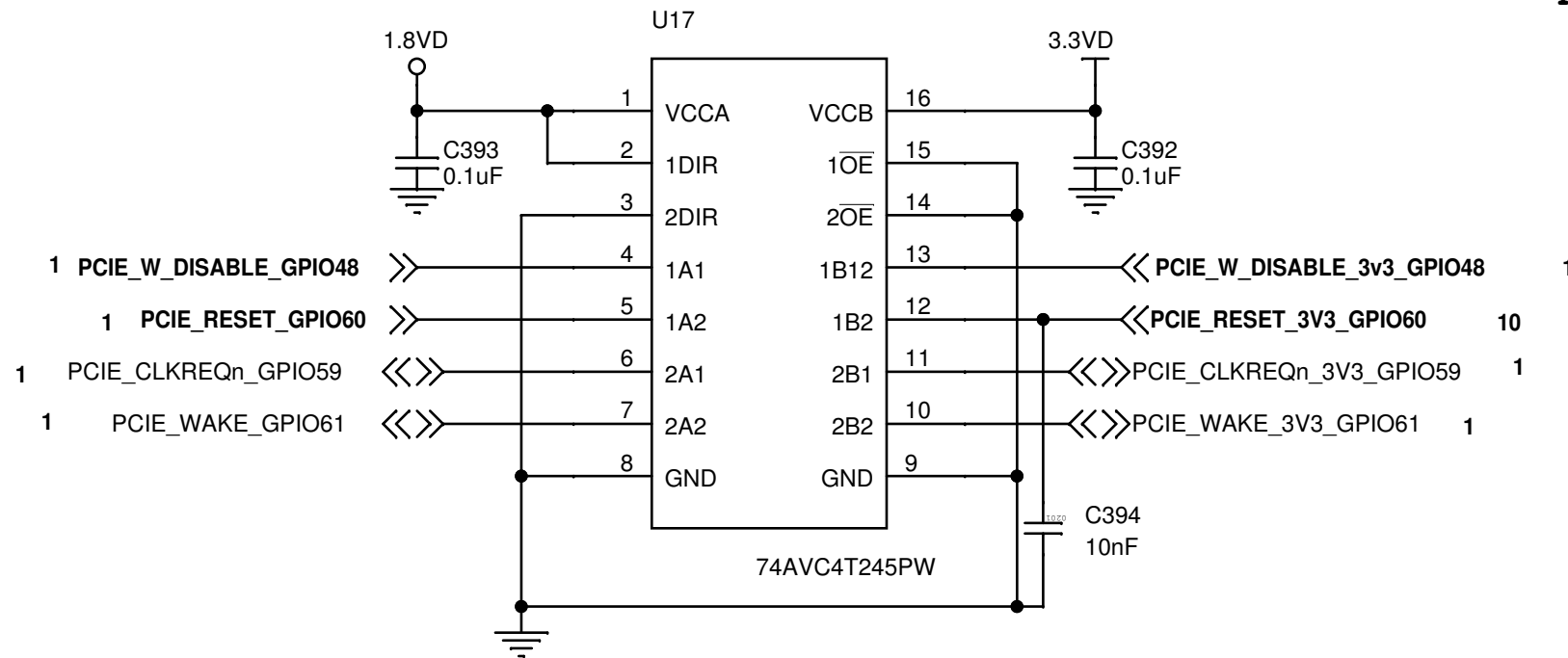


 8DEVICES	Approval	
	Drawing	
Title		
05_Phy transformer and RJ45		
Size	Document Number	Rev
A3	MAN_200_02_SB_DVK	2.0
Date:	Tuesday, December 01, 2020	Sheet 5 of 10

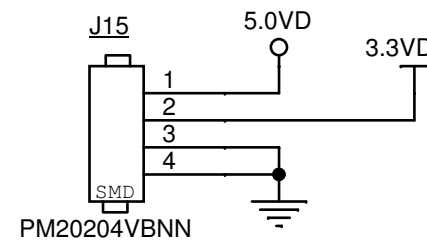
### M.2 PCIe connector



### Level Shifter 1V8 / 3V3: PCIe controll



### Header con. for PCIe Power



8DEVICES

Approval

Drawing

Title  
06-PCIE

Size  
A4

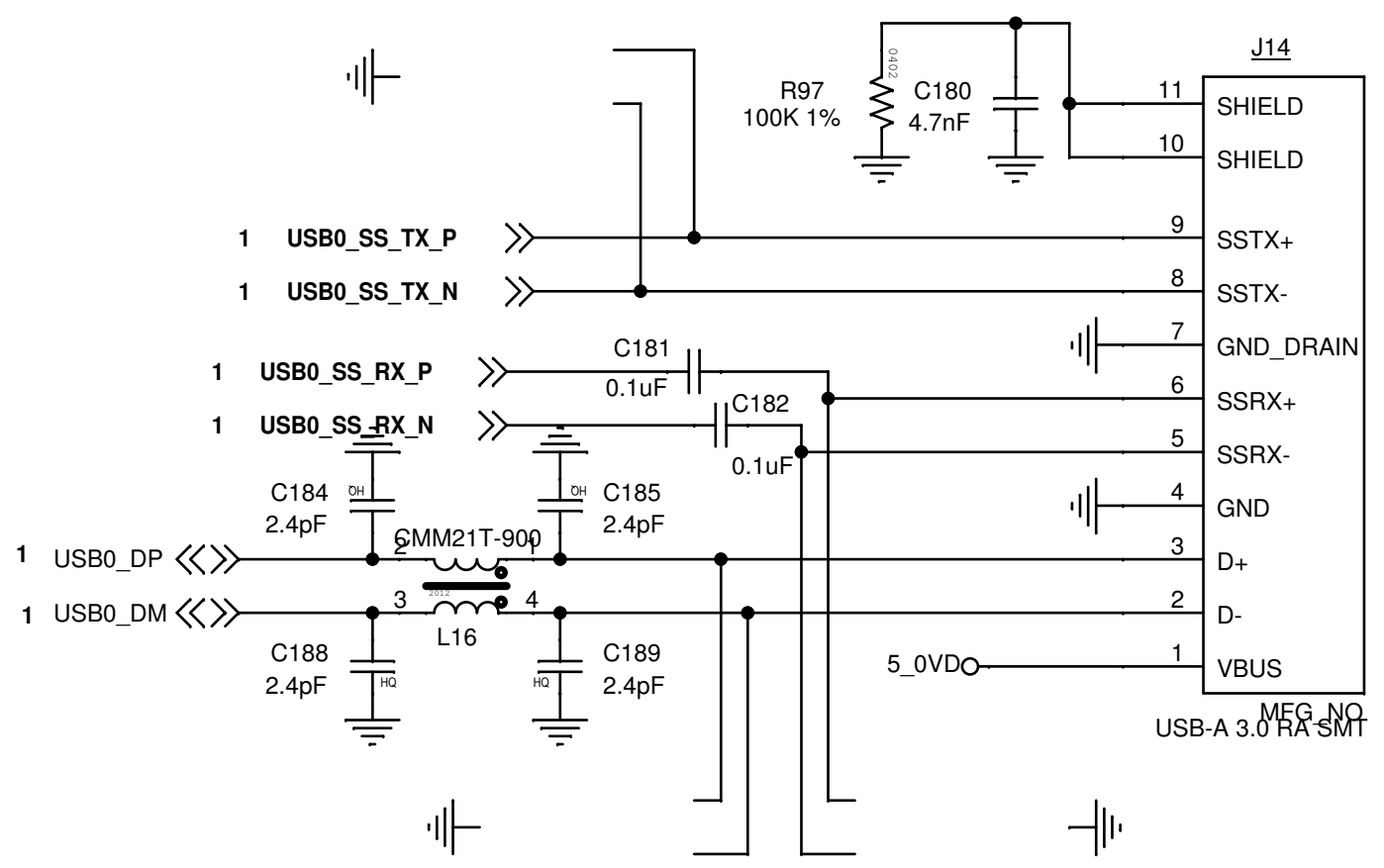
Document Number  
MAN\_200\_02\_SB\_DVK

Rev  
2.0

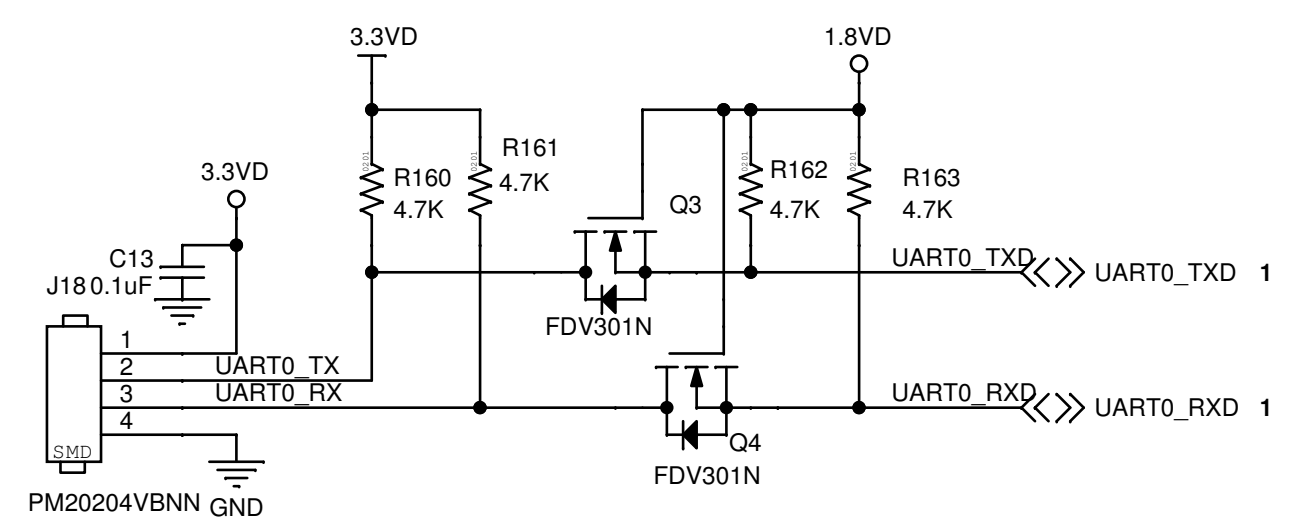
Date: Tuesday, December 01, 2020

Sheet 6 of 10

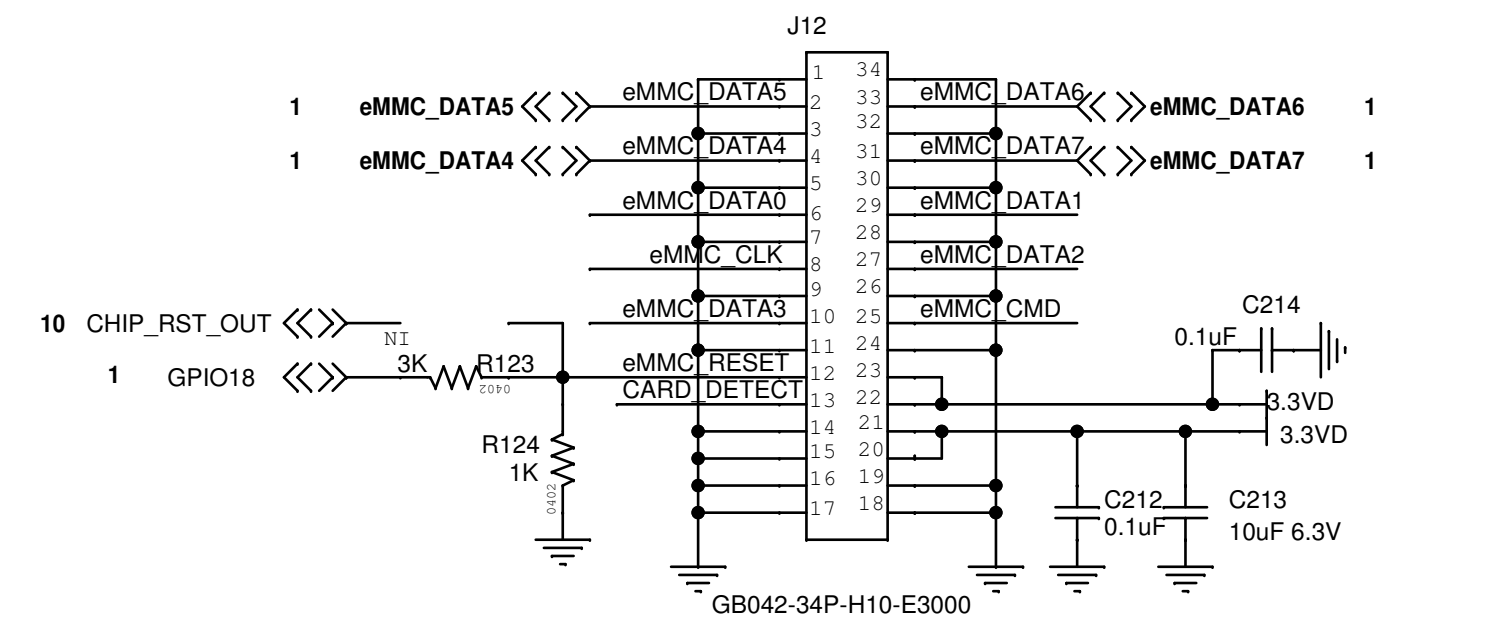
### USB 3.0



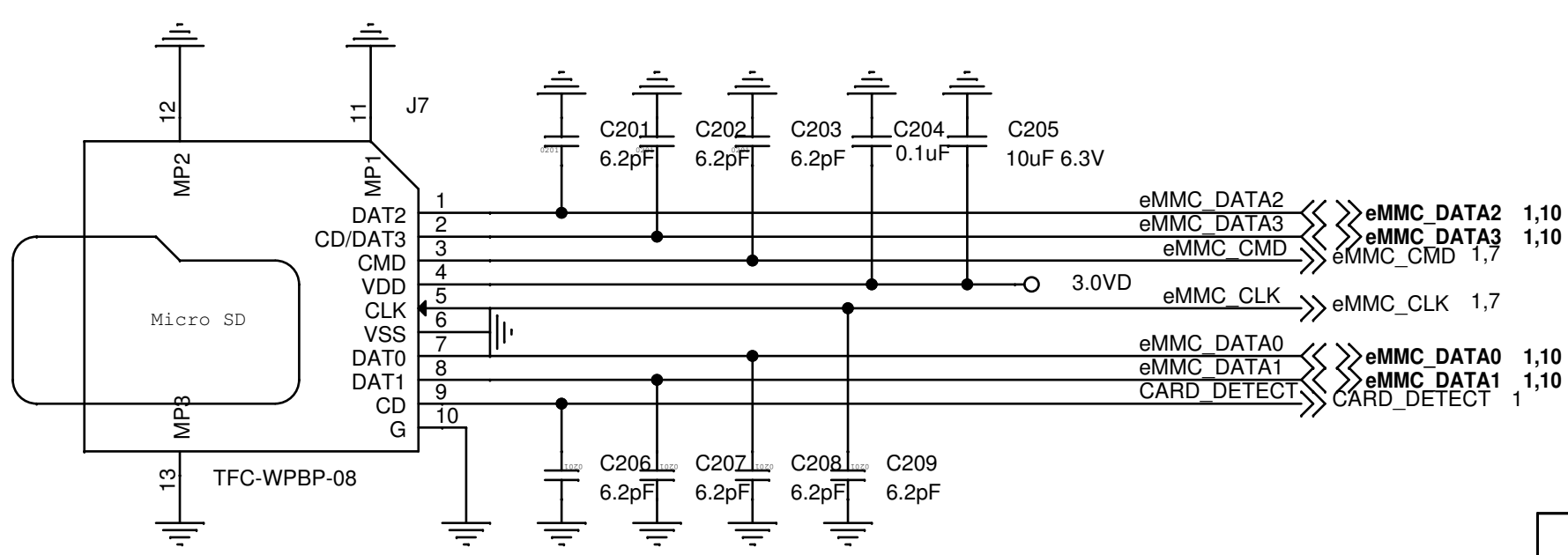
### Debug UART



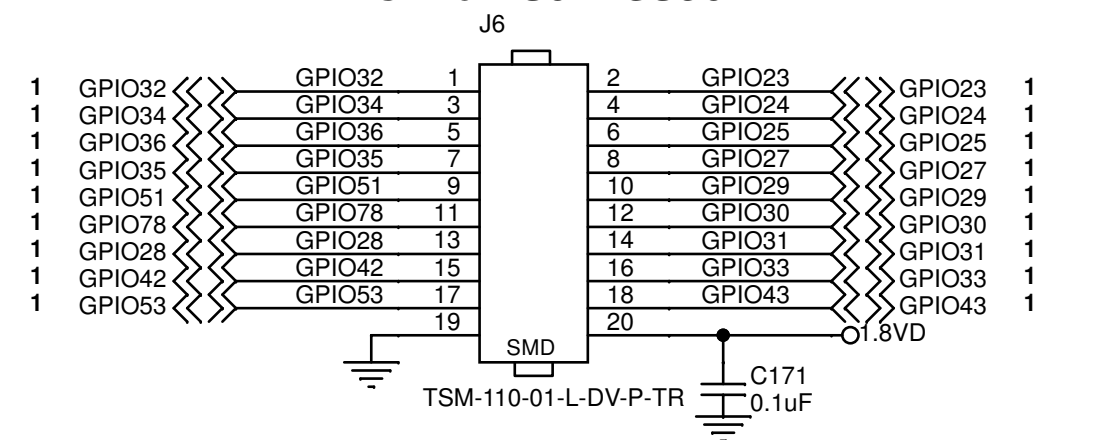
### eMMC Module connector



### SD Card

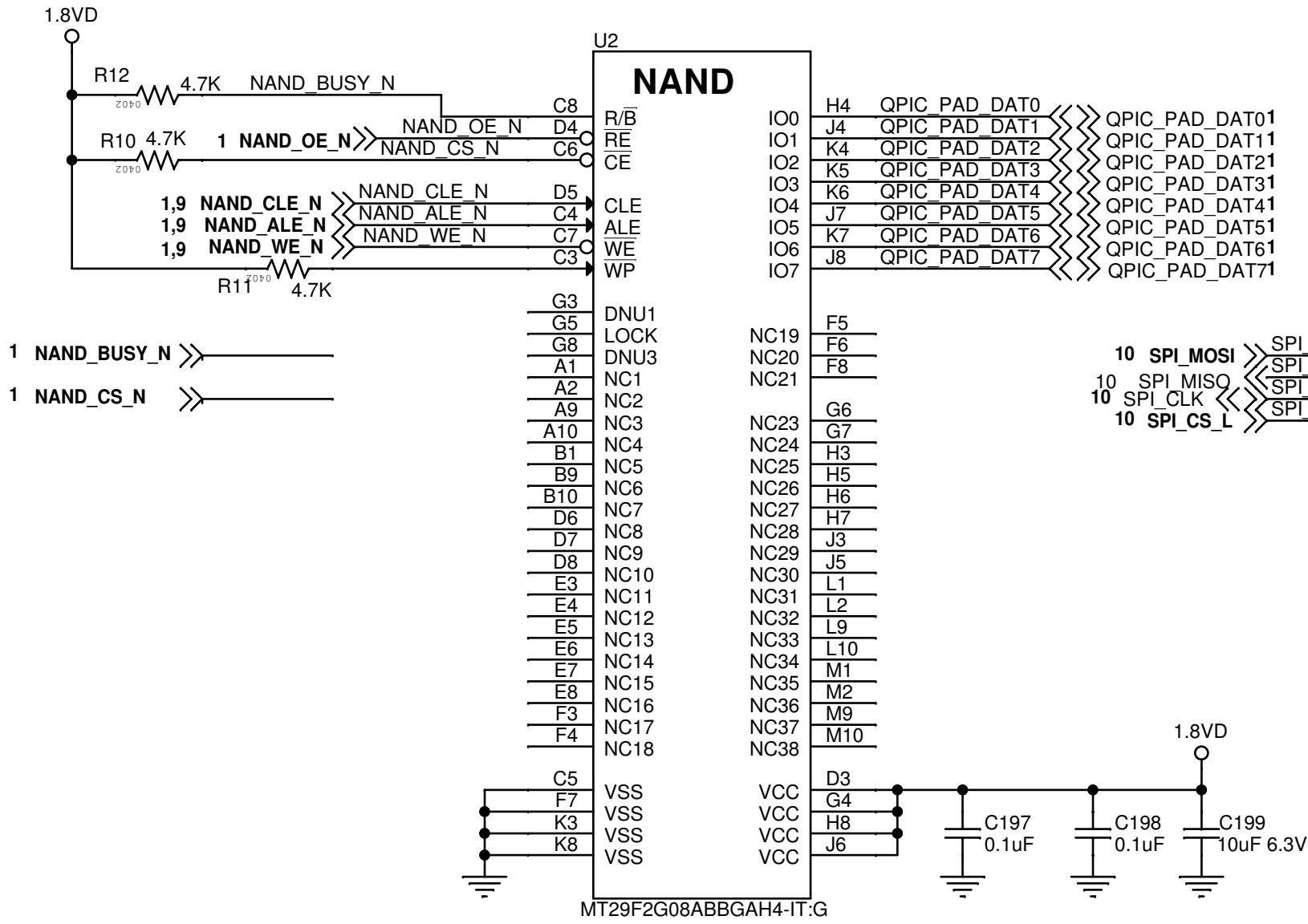


### GPIO connector

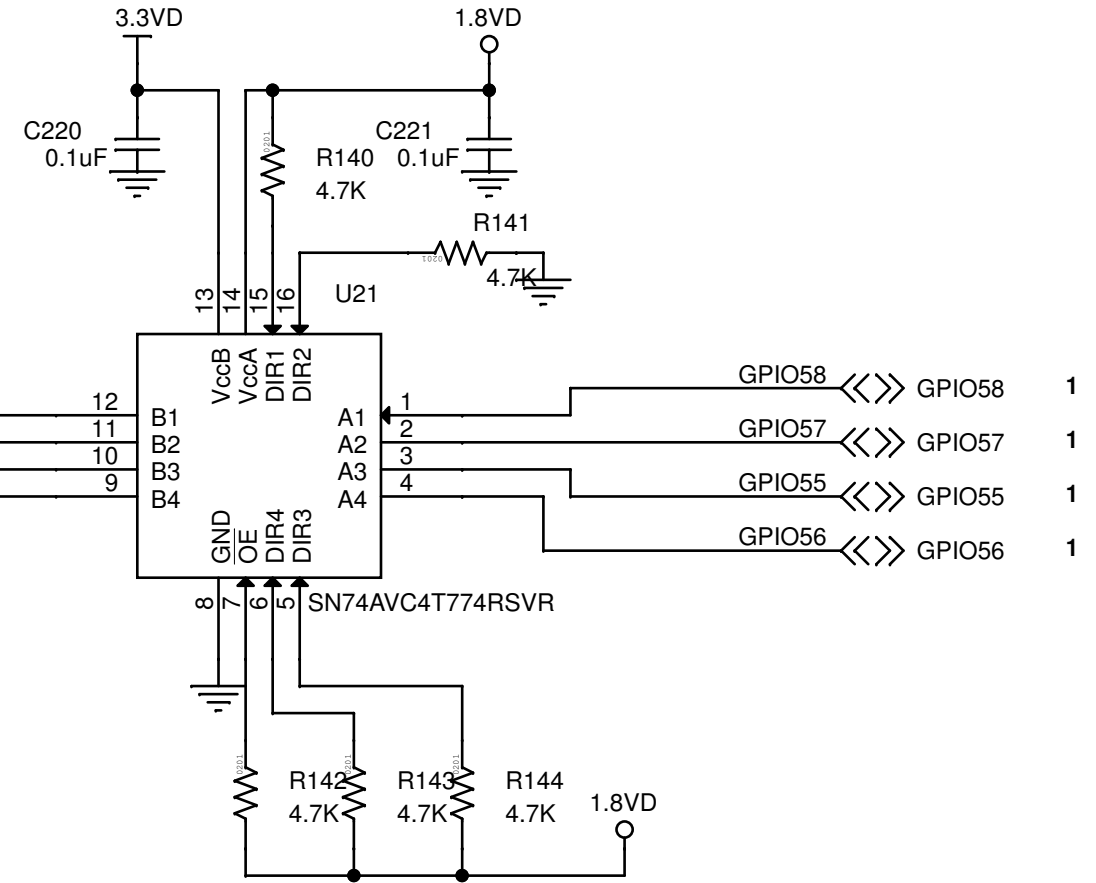


<b>8DEVICES</b>		Approval	
		Drawing	
Title 07-USB			
Size A4	Document Number MAN_200_02_SB_DVK		Rev 2.0
Date:	Tuesday, December 01, 2020	Sheet 7	of 10

### Flash - NAND



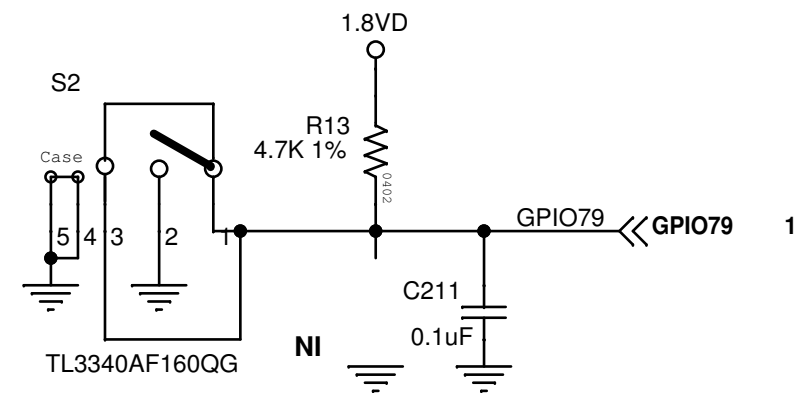
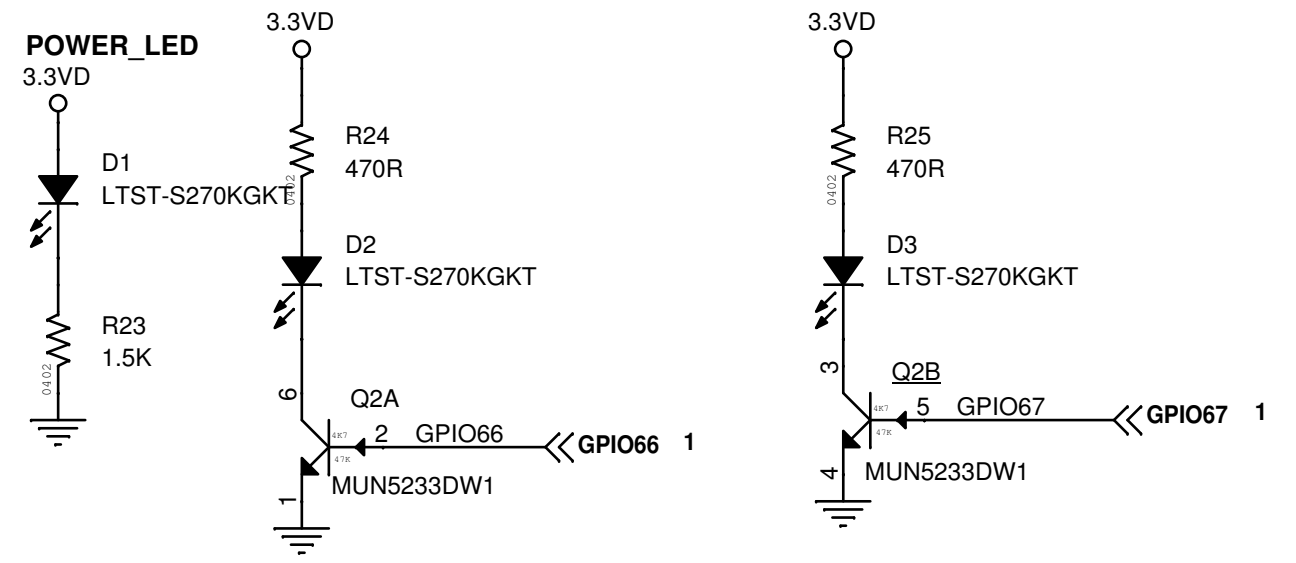
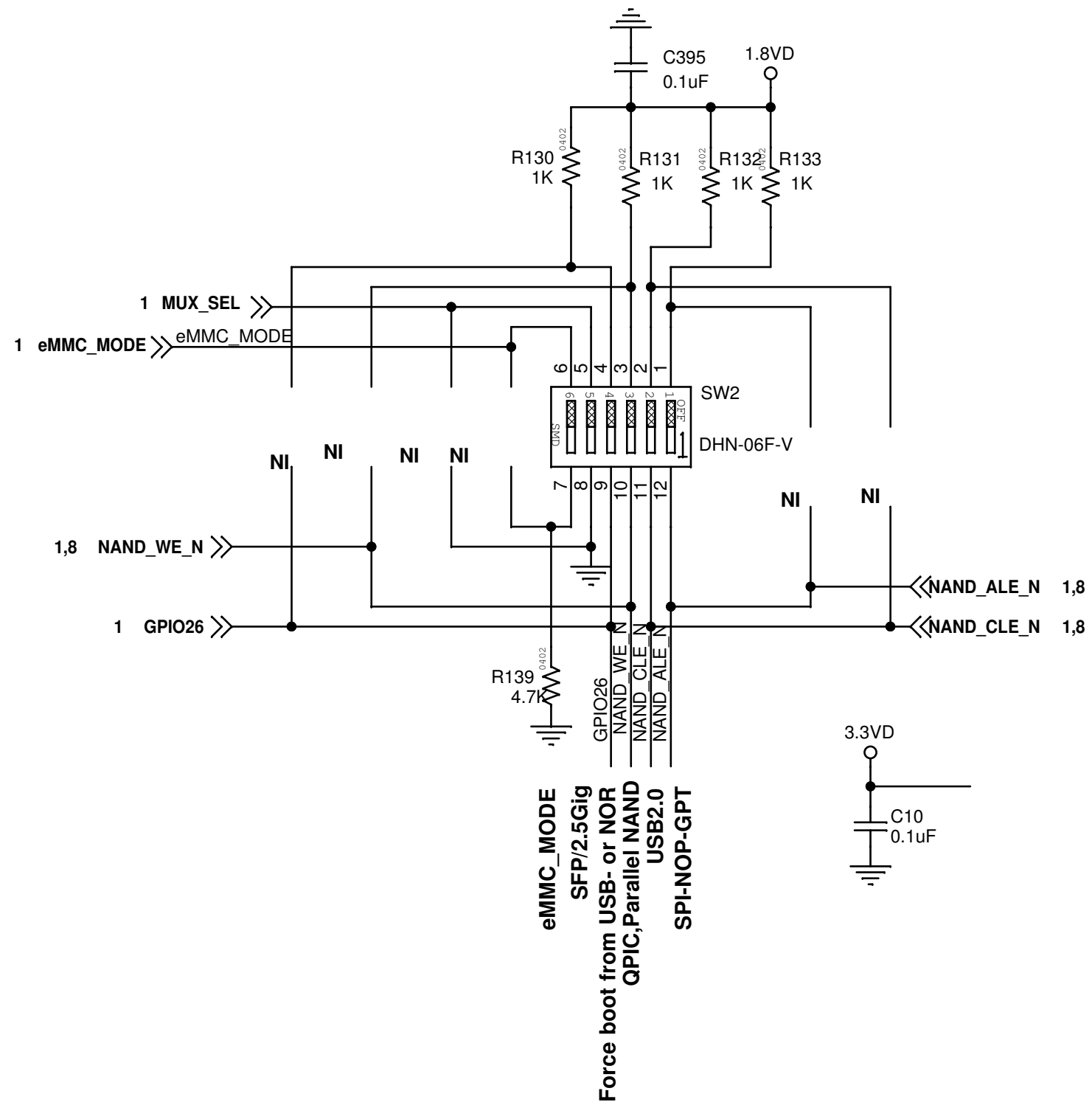
### SPI Level Shifter 1V8 / 3V3



<b>8DEVICES</b>		Approval	
		Drawing	
Title 08_FLASH			
Size A4	Document Number MAN_200_02_SB_DVK		Rev 2.0
Date:		Tuesday, December 01, 2020	Sheet 8 of 10

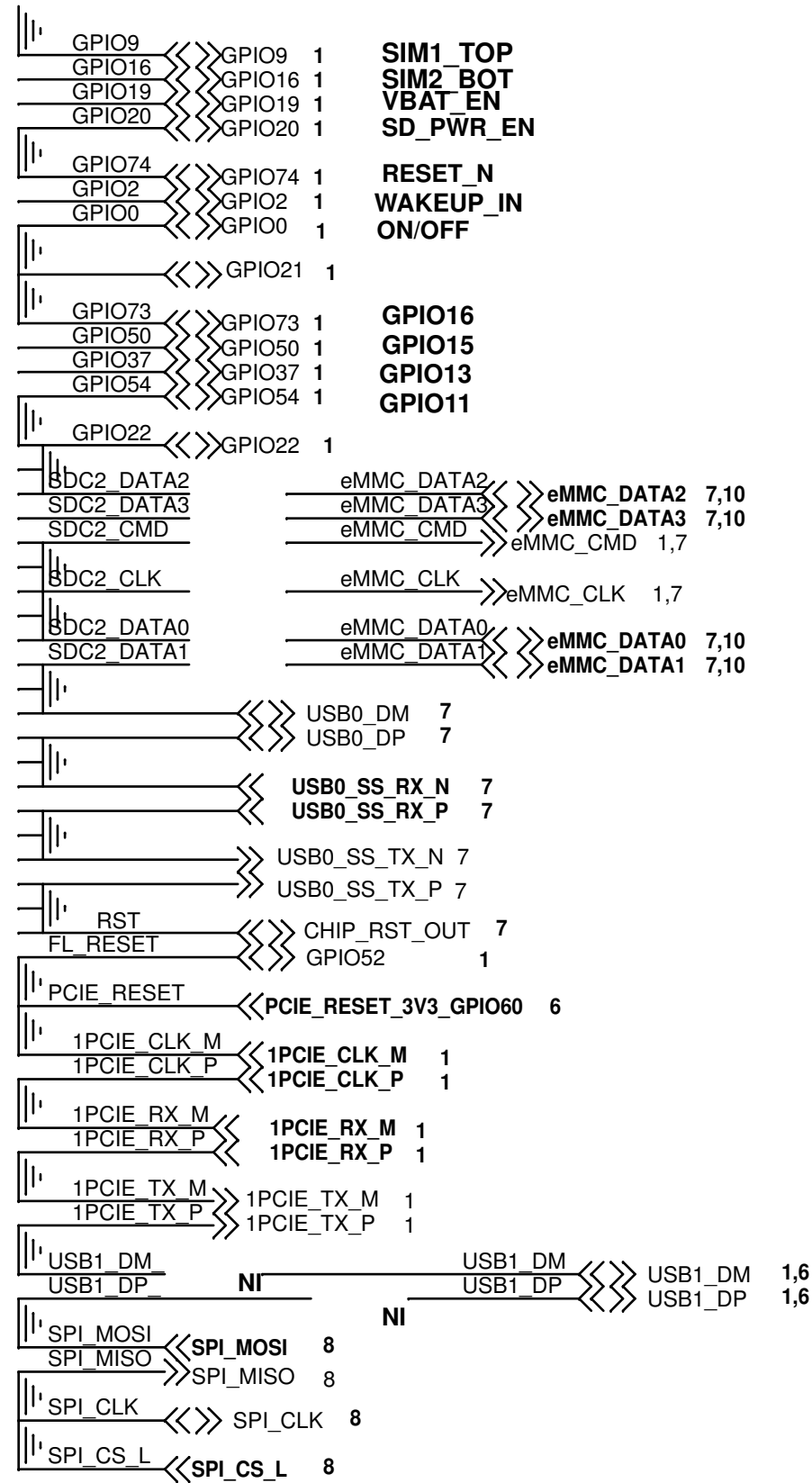


# Boot configuration switch



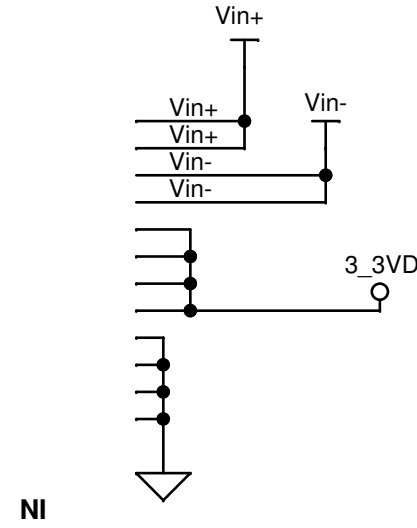
<b>8DEVICES</b>		Approval	
		Drawing	
Title 09_			
Size A4	Document Number MAN_200_02_SB_DVK		Rev 2.0
Date:	Tuesday, December 01, 2020	Sheet 9	of 10

# Flex connector



NI

# Flex connector Power



NI

<b>8DEVICES</b>		Approval	
		Drawing	
Title 10_Connectors			
Size A4	Document Number MAN_200_02_SB_DVK		Rev 2.0
Date:		Tuesday, December 01, 2020	Sheet 10 of 10