XD9263/XD9264 Series

ETR05066-001a

18V Operation 500mA Synchronous Step-Down DC/DC Converters

☆AEC-Q100 Grade2

■GENERAL DESCRIPTION

The XD9263/XD9264 series are synchronous step-down DC/DC converter ICs. The XD9263/64 series have operating voltage range of 3V~18V and switching frequency is 2.2 MHz and it can support 500mA as an output current with high-efficiency. Compatible with Low ESR capacitors such as ceramic capacitors for the output capacitor.

0.75V reference voltage source is incorporated in the IC, and the output voltage can be set to a value from 1.0V to 15.0V using external resistors.

XD9263/XD9264 has a fixed internal Soft Start time which is 1.0ms (TYP.), additionally the time can be extended by using an external resistor and capacitor.

UVLO and over current protection and short-circuit protection and thermal shutdown are embedded and they secure a safety operation. As an option, timer latch off over current protection (Integral Latch Method) can be selected.

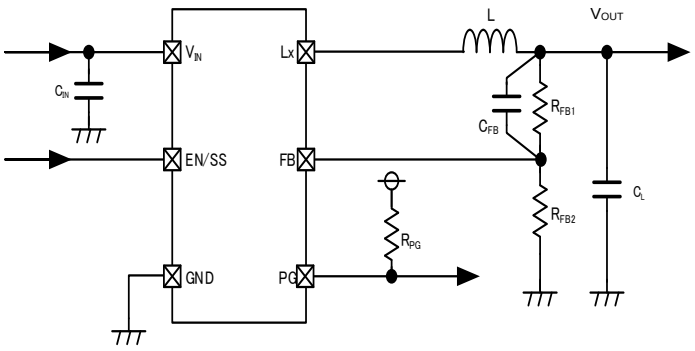
■APPLICATIONS

- Automotive Body Control ECU
- Automotive Infotainment
- Automotive accessories
  - ・Drive recorder
  - ・Car-mounted camera
  - ・ETC
- Industrial Equipment

■FEATURES

Input Voltage Range	:	3.0V ~ 18.0V (Absolute Max 20V)
Output Voltage Range		1.0V ~ 15.0V
FB Voltage	:	0.75V ± 1.5% (Ta=25℃)
Oscillation Frequency	:	2.2MHz
Output Current		500mA
Quiescent Current	:	13.5μA
Control Methods	:	PWM control (XD9263) PWM/PFM Auto (XD9264) Efficiency 85%@12V→5V, 300mA
Function	:	Soft-Start External settings Power Good (USP-6C Package only)
Protect Function	:	Over Current Protection ・Automatic Recovery (XD9263D/XD9264D) ・Integral Latch Method (XD9263C/XD9264C) UVLO Thermal Shutdown
Output Capacitor	:	Ceramic Capacitor
Operating Ambient Temperature	:	-40℃ ~ 105℃
Package	:	SOT-25 (Without Power Good) USP-6C (With Power Good)
Environmentally Friendly	:	EU RoHS Compliant, Pb Free

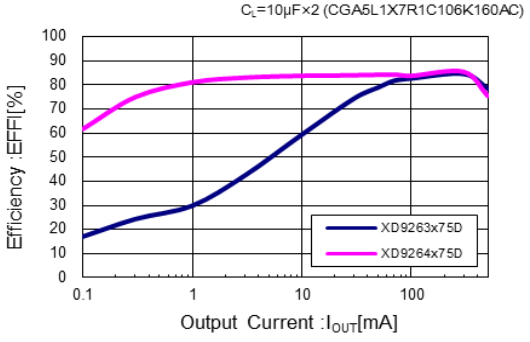
■TYPICAL APPLICATION CIRCUIT



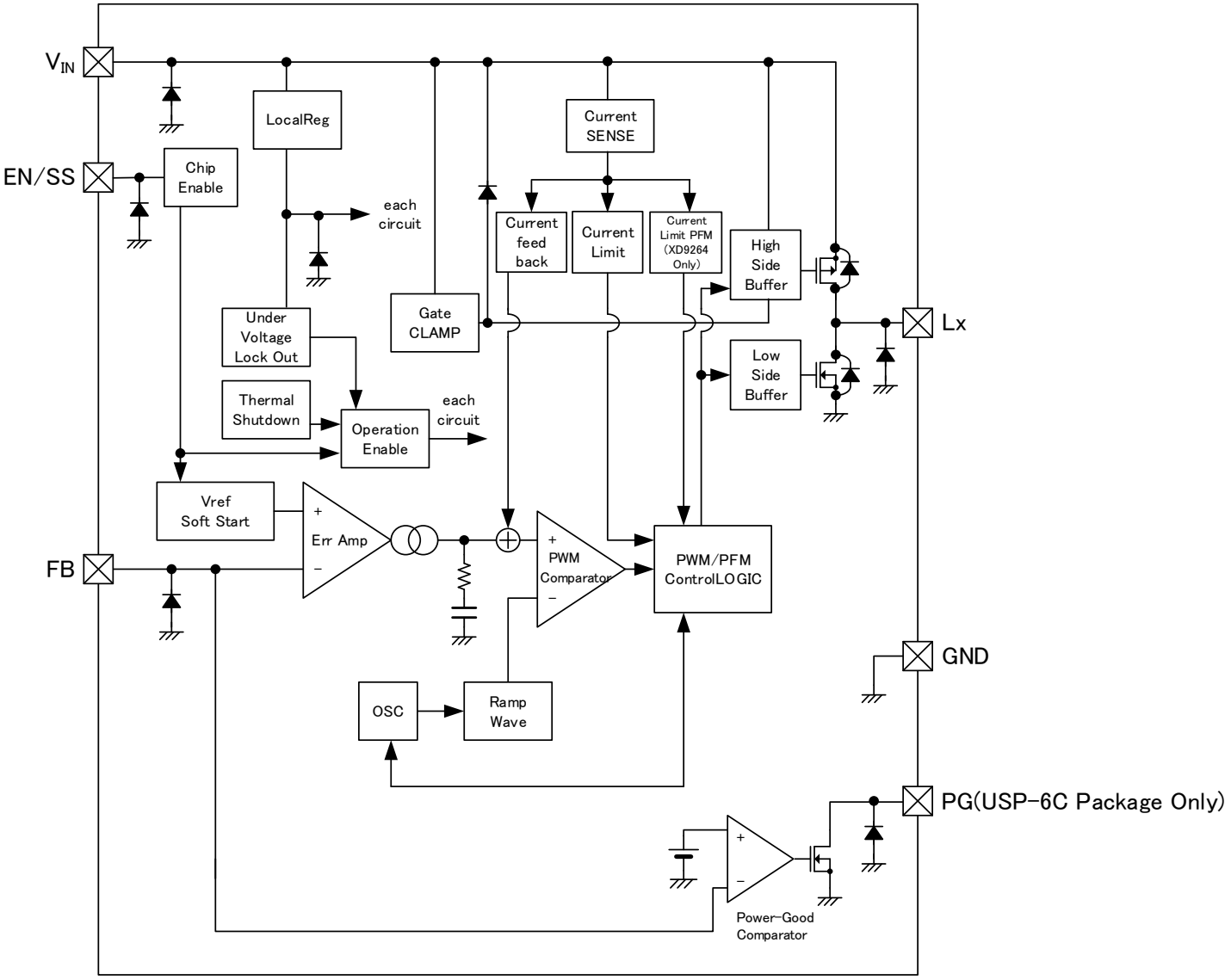
■TYPICAL PERFORMANCE CHARACTERISTICS

XD9263x75D/XD9264x75D
(V_{IN}=12V, V_{OUT}=5V)

L=2.2μH(CLF6045NIT-2R2N-D), C_{IN}=2.2μF(CGA4J3X7R1E225K125AB),
C_L=10μF×2 (CGA5L1X7R1C106K160AC)



■BLOCK DIAGRAM



*Diodes inside the circuit are an ESD protection diodes and a parasitic diodes.

■PRODUCT CLASSIFICATION

●Ordering Information

XD9263①②③④⑤⑥-⑦(*1) PWM control
XD9264①②③④⑤⑥-⑦(*1) PWM/PFM Auto

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	C	Refer to Selection Guide
		D	
②③	FB Voltage	75	Output voltage can be adjusted in 1V to 15V
④	Oscillation Frequency	D	2.2MHz
⑤⑥-⑦	Packages (Order Unit)	MR-Q (*1)	SOT-25 (3,000pcs/Reel)
		ER-Q (*1)	USP-6C (3,000pcs/Reel)

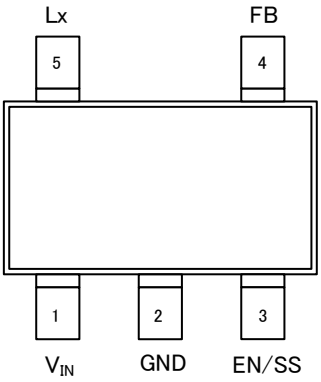
(*1) The “-Q” suffix denotes “AEC-Q100” and “Halogen and Antimony free” as well as being fully EU RoHS compliant.

●Selection Guide

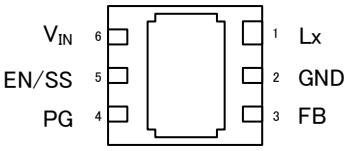
FUNCTION	C TYPE		D TYPE	
	SOT-25	USP-6C	SOT-25	USP-6C
Chip Enable	Yes	Yes	Yes	Yes
UVLO	Yes	Yes	Yes	Yes
Thermal Shutdown	Yes	Yes	Yes	Yes
Soft Start	Yes	Yes	Yes	Yes
Power-Good	-	Yes	-	Yes
Current Limiter (Automatic Recovery)	-	-	Yes	Yes
Current Limiter (Latch Protection (*2))	Yes	Yes	-	-

(*2) The over-current protection latch is an integral latch type.

■PIN CONFIGURATION



SOT-25
(TOP VIEW)



USP-6C
(BOTTOM VIEW)

* The dissipation pad for the USP-6C package should be solder-plated in recommended mount pattern and metal masking so as to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to the GND (No. 2) pin.

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
SOT-25	USP-6C		
1	6	V_{IN}	Power Input
3	5	EN/SS	Enable Soft-Start
-	4	PG	Power-Good Output
4	3	FB	Output Voltage Sense
2	2	GND	Ground
5	1	Lx	Switching Output

■FUNCTION CHART

PIN NAME	SIGNAL	STATUS
EN/SS	L	Stand-by
	H	Active
	OPEN	Undefined State(*1)

(*1) Please do not leave the EN/SS pin open. Each should have a certain voltage.

PIN NAME	CONDITION		SIGNAL
PG	EN/SS = H	$V_{FB} > V_{PGDET}$	H (High impedance)
		$V_{FB} \leqq V_{PGDET}$	L (Low impedance)
		Thermal Shutdown	L (Low impedance)
		UVLO ($V_{IN} < V_{UVLO1}$)	Undefined State
	EN/SS = L	Stand-by	L (Low impedance)

■ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNITS
V_{IN} Pin Voltage		V_{IN}	-0.3 ~ 20	V
EN/SS Pin Voltage		$V_{EN/SS}$	-0.3 ~ 20	V
FB Pin Voltage		V_{FB}	-0.3 ~ 6.2	V
PG Pin Voltage (*1)		V_{PG}	-0.3 ~ 6.2	V
PG Pin Current (*1)		I_{PG}	8	mA
Lx Pin Voltage		V_{Lx}	-0.3 ~ V_{IN} + 0.3 or 20 (*2)	V
Lx Pin Current		I_{Lx}	1800	mA
Power Dissipation (Ta=25℃)	SOT-25	Pd	760 (JESD51-7 Board) (*3)	mW
	USP-6C		1250 (JESD51-7 Board) (*3)	
Operating Ambient Temperature		Topr	-40 ~ 105	℃
Storage Temperature		Tstg	-55 ~ 125	℃

* All voltages are described based on the GND pin.
(*1) For the USP-6C Package only.
(*2) The maximum value should be either V_{IN}+0.3V or 20V in the lowest.
(*3) The power dissipation figure shown is PCB mounted and is for reference only.
The mounting condition is please refer to PACKAGING INFORMATION.

■ELECTRICAL CHARACTERISTICS

XD9263/XD9264 Series

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	CIRCUIT
FB Voltage	V_{FB}	V_{FB}=0.731V → 0.769V V_{FB} Voltage when Lx pin voltage changes from "H" level to "L" level		0.739	0.750	0.761	V	②
			-40℃≦Ta≦105℃	0.731	0.750	0.769		
Output Voltage Setting Range(*1)	V_{OUTSET}	-	-40℃≦Ta≦105℃	1.0	-	15.0	V	−
Operating Voltage Range	V_{IN}	-	-40℃≦Ta≦105℃	3.0	-	18.0	V	−
UVLO Detect Voltage	V_{UVLO1}	V_{IN}=2.87V→2.53V, V_{FB}=0.675V, V_{IN} Voltage when Lx pin voltage changes from "H" level to "L" level		2.60	2.70	2.80	V	②
			-40℃≦Ta≦105℃	2.53	-	2.87		
UVLO Release Voltage	V_{UVLO2}	V_{IN}=2.63V→2.97V, V_{FB}=0.675V V_{IN} Voltage when Lx pin voltage changes from "L" level to "H" level		2.70	2.80	2.90	V	②
			-40℃≦Ta≦105℃	2.63	-	2.97		
Quiescent Current	I_q	V_{FB}=0.825V	XD9263	-	145	238	μA	④
			-40℃≦Ta≦105℃	-	-	257		
			XD9264	-	13.5	18.5		
			-40℃≦Ta≦105℃	-	-	20.0		
Stand-by Current	I_{STB}	$V_{EN/SS}$=0V		-	1.65	2.50	μA	⑤
			-40℃≦Ta≦105℃	-	-	2.80		
Oscillation Frequency	f_{OSC}	Connected to external components I_{OUT}=100mA		2013	2200	2387	kHz	①
			-40℃≦Ta≦105℃	1813	-	2531		
Minimum Duty Cycle	D_{MIN}	V_{FB}=0.825V	-40℃≦Ta≦105℃	-	-	0	%	②
Maximum Duty Cycle	D_{MAX}	V_{FB}=0.675V	-40℃≦Ta≦105℃	100	-	-	%	②
Lx SW "H" On Resistance	R_{LxH}	V_{FB}=0.675V, I_{LX}=200mA	USP-6C	-	0.95	1.10	Ω	②
			SOT-25	-	0.99	1.14		
Lx SW "L" On Resistance	R_{LxL}	V_{FB}=0.825V, I_{LX}=200mA	USP-6C	-	0.69(*2)	-	Ω	②
			SOT-25	-	0.73(*2)	-		
PFM Switch Current	I_{PFM}	XD9264 only Connected to external components, I_{OUT}=1mA		-	370	-	mA	①
Highside Current Limit(*3)	I_{LIMH}	V_{FB}=0.675V		920	1100	-	mA	②
Latch Time	t_{LAT}	Type C only Connected to external components, V_{FB}=0V		0.5	1.0	1.7	ms	⑥
Internal Soft-Start Time	t_{SS1}	$V_{EN/SS}$=0V→12V, V_{FB}=0.675V Time until Lx pin oscillates		0.5	1.0	1.7	ms	②
External Soft-Start Time	t_{SS2}	$V_{EN/SS}$=0V→12V, V_{FB}=0.675V R_{SS}=430kΩ, C_{SS}=0.47μF Time until Lx pin oscillates		17	26	35	ms	③

Test Condition: Unless otherwise stated, V_{IN}=12V, $V_{EN/SS}$=12V.

The ambient temperature range (-40℃≦Ta≦105℃) is design Value.

(*1) Please use within the range of V_{OUT}/V_{IN}≧0.17.

(*2) Design reference value. This parameter is provided only for reference.

(*3) Current limit denotes the level of detection at peak of coil current.

■ELECTRICAL CHARACTERISTICS (Continued)

XD9263/XD9264 Series

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	CIRCUIT
PG Detect Voltage(*4)	V_{PGDET}	V_{FB}=0.720V→0.630V, R_{PG}:100kΩ pull-up to 5V V_{FB} Voltage when PG pin voltage changes from "H" level to "L" level		0.638	0.675	0.712	V	②
			-40℃≦Ta≦105℃	0.630	-	0.720		
PG Output Voltage(*4)	V_{PG}	V_{FB}=0.6V, I_{PG}=1mA	-40℃≦Ta≦105℃	-	-	0.3	V	②
Efficiency	EFFI (*5)	Connected to external components V_{OUTSET}=5V, I_{OUT}=300mA		-	85(*2)	-	%	①
FB "H" Current	I_{FBH}	V_{IN}=$V_{EN/SS}$=18V, V_{FB}=3.0V	-40℃≦Ta≦105℃	-0.1	0.0	0.1	μA	④
FB "L" Current	I_{FBL}	V_{IN}=$V_{EN/SS}$=18V, V_{FB}=0V	-40℃≦Ta≦105℃	-0.1	0.0	0.1	μA	④
EN/SS "H" Current	$I_{EN/SSH}$	V_{IN}=$V_{EN/SS}$=18V, V_{FB}=0.825V	-40℃≦Ta≦105℃	-	0.1	0.3	μA	④
EN/SS "L" Current	$I_{EN/SSL}$	V_{IN}=18V, $V_{EN/SS}$=0V, V_{FB}=0.825V	-40℃≦Ta≦105℃	-0.1	0.0	0.1	μA	④
EN/SS "H" Voltage	$V_{EN/SSH}$	$V_{EN/SS}$=0.3V→2.5V, V_{FB}=0.71V $V_{EN/SS}$ Voltage when Lx pin voltage changes from "L" level to "H" level	-40℃≦Ta≦105℃	2.5	-	18.0	V	②
EN/SS "L" Voltage	$V_{EN/SSL}$	$V_{EN/SS}$=2.5V→0.3V, V_{FB}=0.71V $V_{EN/SS}$ Voltage when Lx pin voltage changes from "H" level to "L" level	-40℃≦Ta≦105℃	GND	-	0.3	V	②
Thermal Shutdown Temperature	T_{TSD}	Junction Temperature		-	150	-	℃	−
Hysteresis Width	T_{HYS}	Junction Temperature		-	25	-	℃	−

Test Condition: Unless otherwise stated, V_{IN}=12V, $V_{EN/SS}$=12V.

The ambient temperature range (-40℃≦Ta≦105℃) is design Value.

(*1) Please use within the range of V_{OUT}/V_{IN}≧0.17/

(*2) Design reference value. This parameter is provided only for reference.

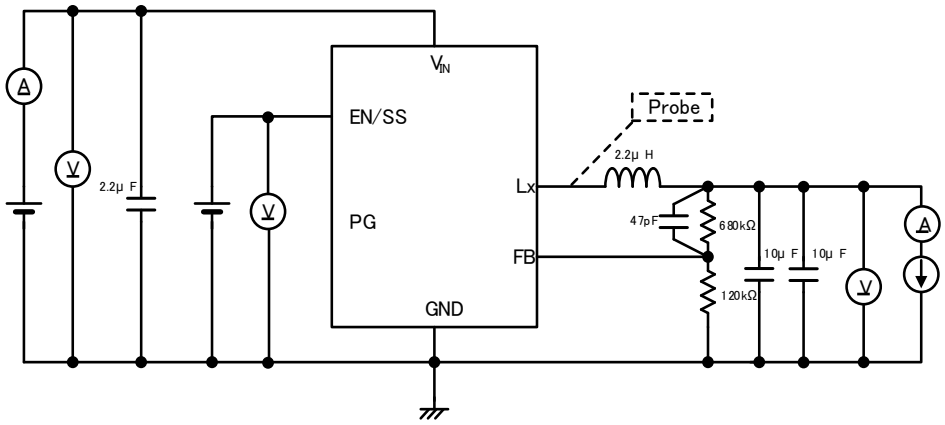
(*3) Current limit denotes the level of detection at peak of coil current.

(*4) For the USP-6C Package only.

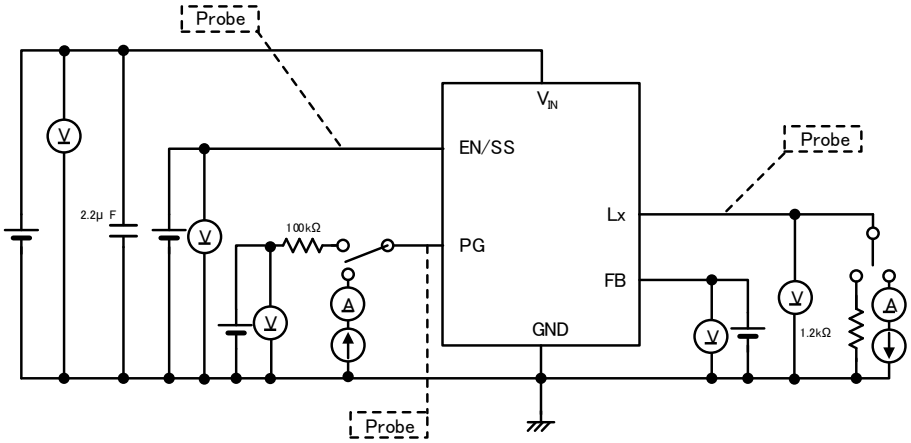
(*5) EFFI = {(output voltage) x (output current)} / {(input voltage) x (input current)} x 100

■TEST CIRCUITS

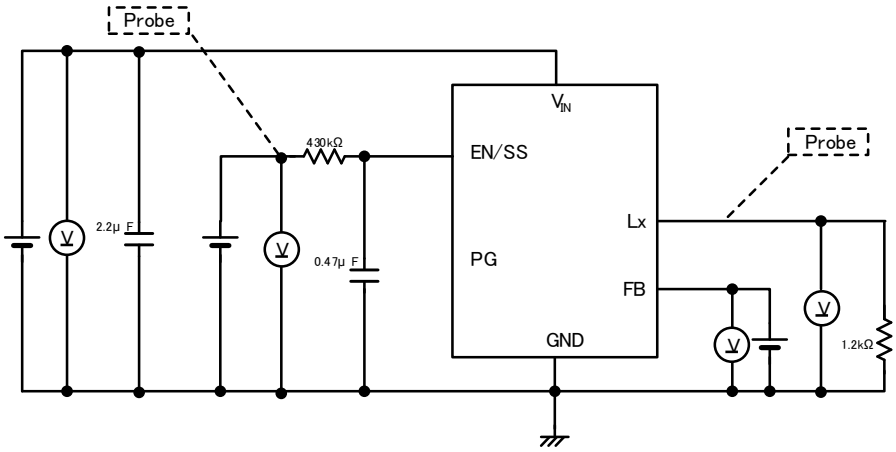
CIRCUIT①



CIRCUIT②



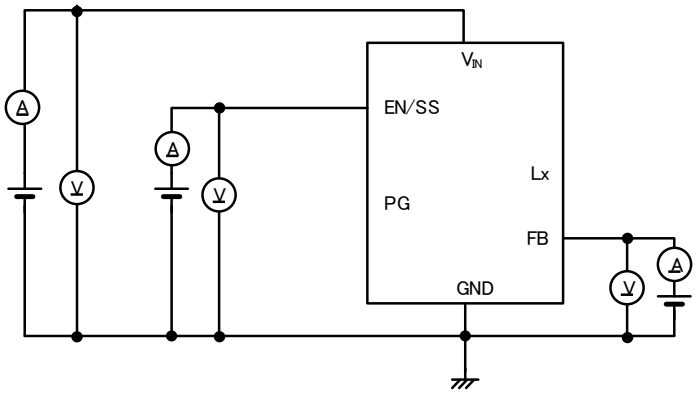
CIRCUIT③



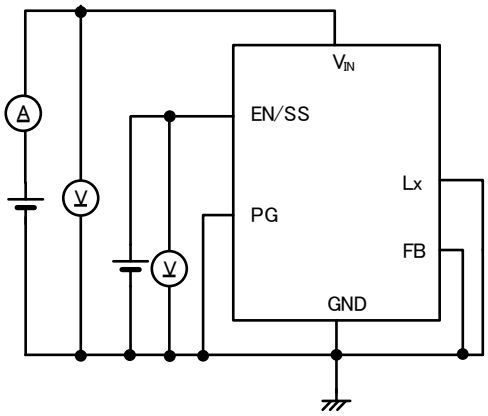
* PG Pin is USP-6C Package only.

■TEST CIRCUITS (Continued)

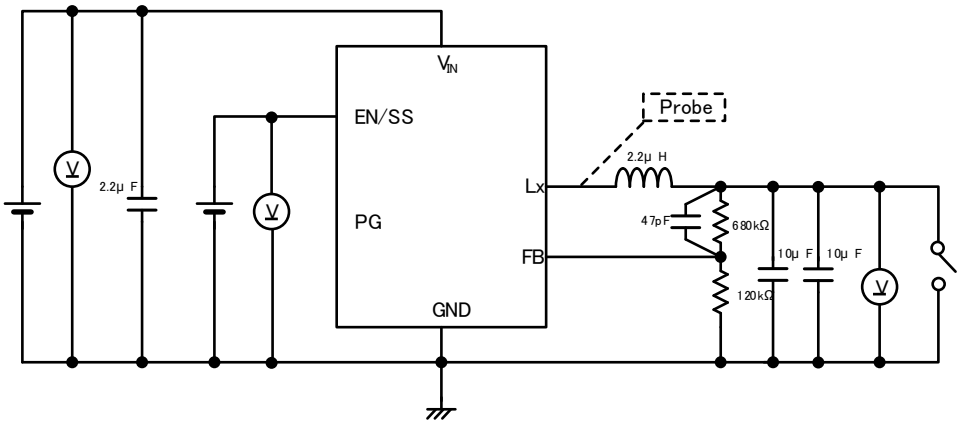
CIRCUIT④



CIRCUIT⑤

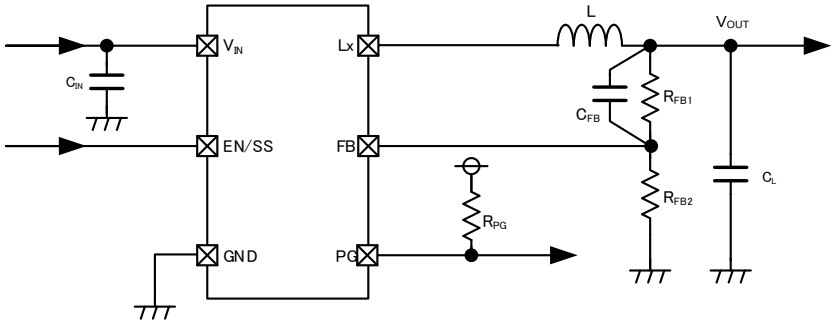


CIRCUIT⑥



* PG Pin is USP-6C Package only.

■TYPICAL APPLICATION CIRCUIT / PARTS SELECTION METHOD



【Typical Examples】

	MANUFACTURER	PRODUCT NUMBER	VALUE
L	TDK	CLF6045NIT-2R2N-D	2.2µH
C_{IN}(*1)	TDK	CGA4J3X7R1E225K125AB	2.2µF/25V
C_L(*2)	Murata	GRT21BR71A106KE13	10µF/10V 2parallel
	TDK	CGA5L1X7R1C106K160AC	10µF/16V 2parallel
	Murata	GRT32DC81E106KE01	10µF/25V 2parallel

Select parts considering the DC bias characteristics and rated voltage of ceramic capacitors.

(*1) For C_{IN}, use a capacitor with the same or higher effective capacity value as the recommended components.
(*2) For C_L, use a capacitor with the same or higher effective capacity value as the recommended components.
If a capacitor with a low effective capacity value is used, the output voltage may become unstable.
However, if large capacity capacitors, such as electrolytic capacitors, are connected in parallel,
the inrush current during startup could increase or the output could become unstable.

■TYPICAL APPLICATION CIRCUIT / PARTS SELECTION METHOD

<Output voltage setting Value V_{OUTSET} Setting >

The output voltage can be set by adding an external dividing resistor.

The output voltage is determined by the equation below based on the values of R_{FB1} and R_{FB2}.

$$V_{OUT}=V_{FB}\times(R_{FB1}+R_{FB2})/R_{FB2}$$

With $R_{FB1}+R_{FB2} \leqq 1M\Omega$

<C_{FB} setting>

Adjust the value of the phase compensation speed-up capacitor C_{FB} using the equation below.

$$C_{FB}=\frac{1}{2\pi\times fzfb\times R_{FB1}}$$

* A target value for fzfb of about 5kHz is optimum.

【Output voltage Setting Example】

To set output voltage to 5V.

When R_{FB1}=680kΩ, R_{FB2}=120kΩ, V_{OUTSET}=0.75V×(680kΩ+120kΩ) / 120kΩ=5.0V,

and fzfb is set to a target of 5kHz using the above equation,

C_{FB}=1/(2×π×5kHz×680kΩ)=46.8pF.

* The setting range for the output voltage is 1.0V to 15.0V.

The condition $V_{OUT}/V_{IN} \geqq 0.17$ must be satisfied.

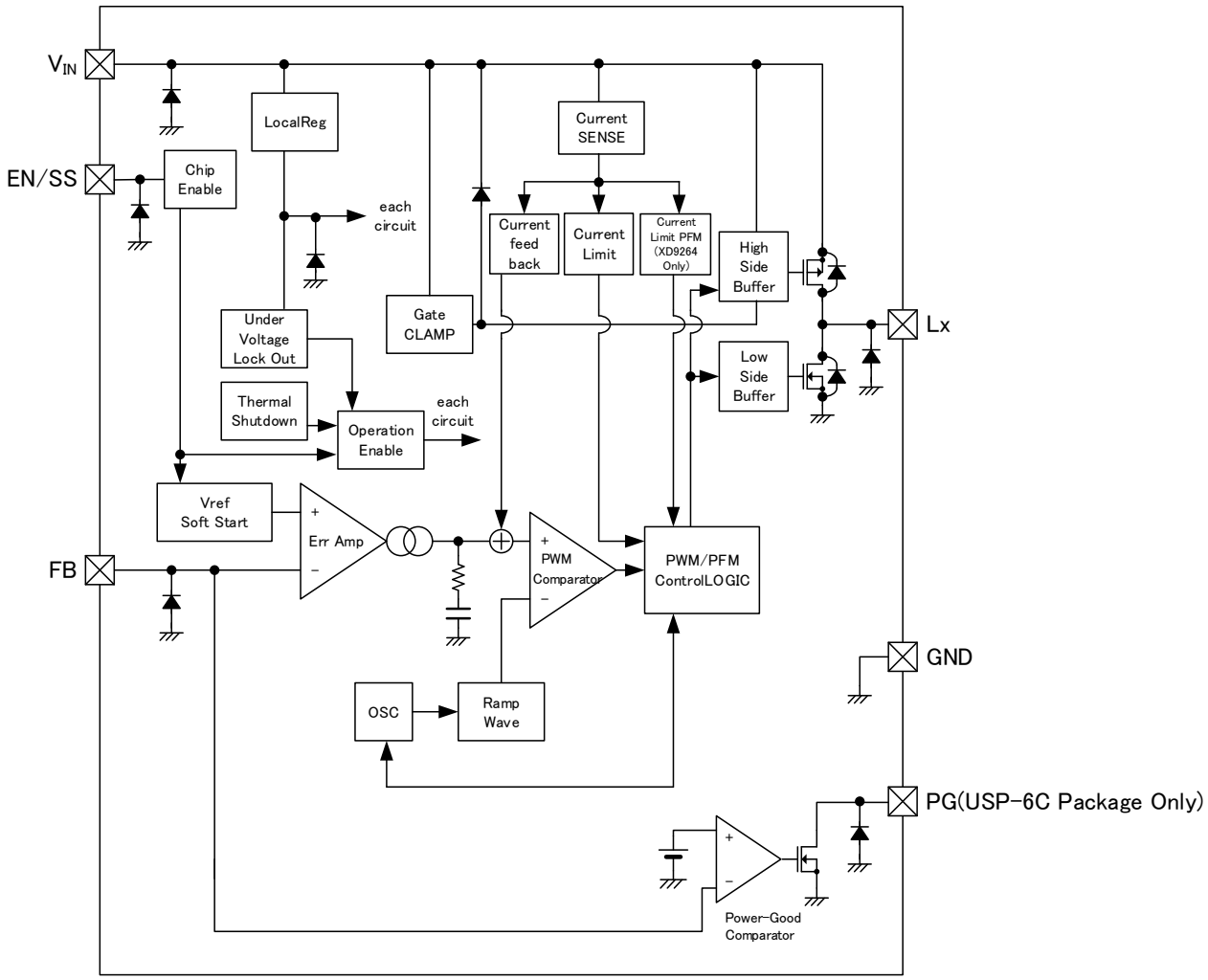
【Setting Example】

V_{OUTSET}	R_{FB1}[kΩ]	R_{FB2}[kΩ]	C_{FB}[pF]
1.2	91	150	360
3.3	510	150	62
5.0	680	120	47
12	360	24	91

■OPERATIONAL EXPLANATION

The XD9263/XD9264 series consist internally of a reference voltage supply with Soft Start function, a ramp wave circuit, an error amp, a PWM comparator, a High side driver FET, a Low side driver FET, a High side buffer circuit, a Low side buffer circuit, a current sense circuit, a phase compensation (Current feedback) circuit, a current limiting circuit, an under voltage lockout (UVLO) circuit, an internal power supply (Local Reg) circuit, a gate clamp (CLAMP) circuit and other elements.

The control method is the current mode control method for handling low ESR ceramic capacitors.



*Diodes inside the circuit are ESD protection diodes and parasitic diodes.

■OPERATIONAL EXPLANATION(Continued)

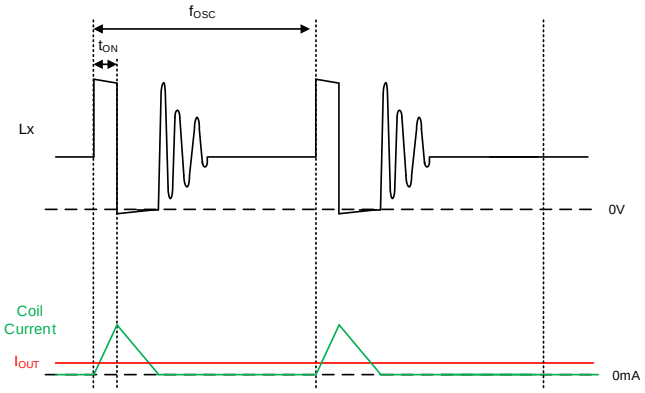
< Normal Operation >

The standard voltage Vref and FB pin voltage are compared using an error amplifier and then the control signal to which phase compensation has been added to the error amplifier output is input to the PWM comparator. The PWM comparator compares the above control signal and lamp wave to control the duty width during PWM control. Continuously conducting these controls stabilizes the output voltage.

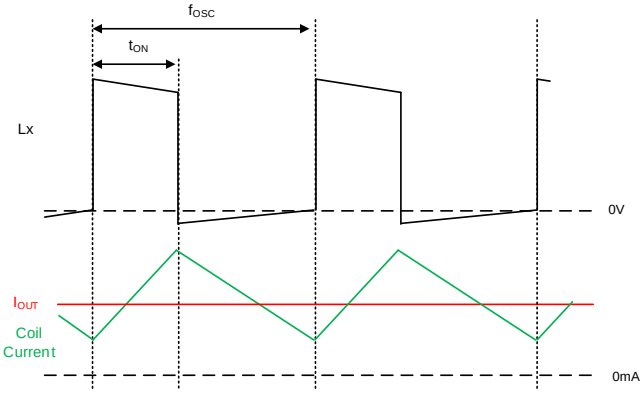
In addition, the current detecting circuit monitors the driver FET current for each switching and modulates the error amplifier output signal into a multiple feedback signal (current feedback circuit). This achieves stable feedback control even when low ESR capacitors, such as ceramic capacitors, are used to stabilize the output voltage.

XD9263 Series

The XD9263 Series (PWM control) performs switching at a set switching frequency f_{OSC} regardless of the output current. At light loads the on time is short and the circuit operates in discontinuous mode, and as the output current increases, the on time becomes longer and the circuit operates in continuous mode.



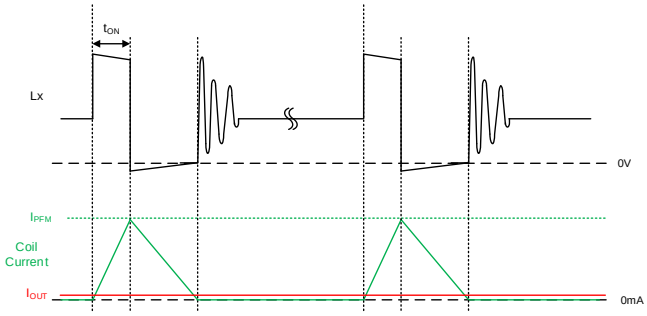
XD9263 Series: Example of light load operation



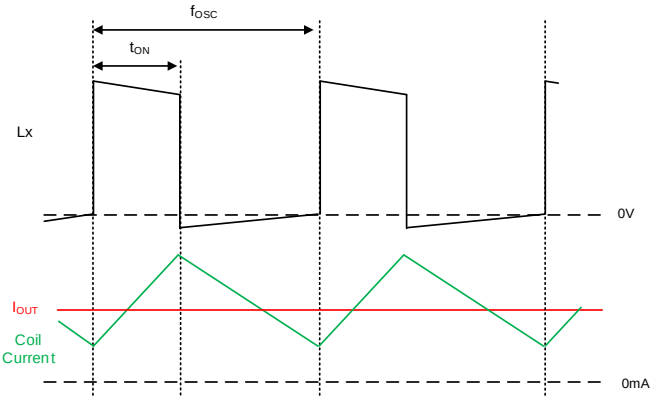
XD9263 Series: Example of heavy load operation

XD9264 Series

The XD9264 Series (PWM/PFM automatic switching control) lowers the switching frequency during light loads by turning on the High side driver FET when the coil current reaches the PFM current (I_{PFM}). This operation reduces the loss during light loads and achieves high efficiency from light to heavy loads. As the output current increases, the switching frequency increases proportional to the output current, and when the switching frequency increases f_{OSC}, the circuit switches from PFM control to PWM control and the switching frequency becomes fixed.



XD9264 Series: Example of light load operation



XD9264 Series: Example of heavy load operation

< 100% Duty Cycle Mode >

When the dropout voltage is low or there is a transient response, the circuit might change to the 100% Duty cycle mode where the High side driver FET is continuously on.

The 100% Duty cycle mode operation makes it possible to maintain the output current even when the dropout voltage is low such as when the input voltage declines due to cranking, etc.

■OPERATIONAL EXPLANATION(Continued)

< CE Function >

When an “H” voltage ($V_{EN/SSH}$) is input to the EN/SS pin, normal operation is performed after the output voltage is started up by the Soft Start function, normal operation is performed. When the “L” voltage ($V_{EN/SSL}$) is input to the EN/SS pin, the circuit enters the standby state, the supply current is suppressed to the standby current I_{STB} (TYP. 1.65μA), and the High side driver FET and Low side driver FET are turned off.

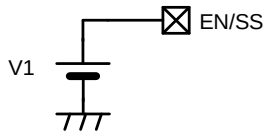
< Soft Start Function >

This function gradually starts up the output voltage to suppress the inrush current.

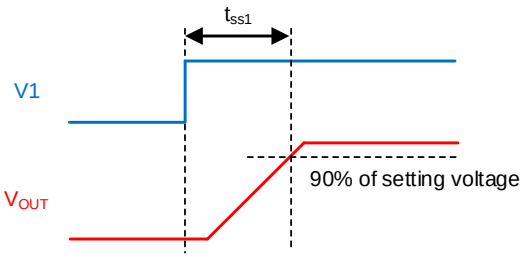
The Soft Start time is the time until the output voltage from $V_{EN/SSH}$ reaches 90% of the output voltage set value, and when the output voltage increases further, the Soft Start function is cancelled to switch to normal operation.

Internal Soft Start Time

The internal Soft Start time (t_{SS1}) is configured so that after the “H” voltage ($V_{EN/SSH}$) is input to the EN/SS pin, the standard voltage connected to the error amplifier increases linearly during the Soft Start period. This causes the output voltage to increase proportionally to the standard voltage increase. This operation suppresses the inrush current and smoothly increases the output voltage.



< Internal Soft Start EN/SS circuit >



< Overview of internal Soft Start >

External Setting Soft Start Time

The external setting Soft Start time (t_{SS2}) can adjust the increase speed of the standard voltage in the IC by adjusting the EN/SS pin voltage inclination during startup using externally connected component R_{SS} and C_{SS}. This makes it possible to externally adjust the Soft Start time.

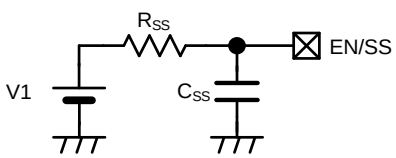
Soft Start time (t_{SS2}) is approximated by the equation below according to values of V1, R_{SS}, and C_{SS}.
When t_{ss2} is shorter than t_{ss1}, the output voltage rises at the internal Soft Start time.

$$t_{SS2}=C_{SS}\times R_{SS}\times \ln (V1 / (V1-1.45V))$$

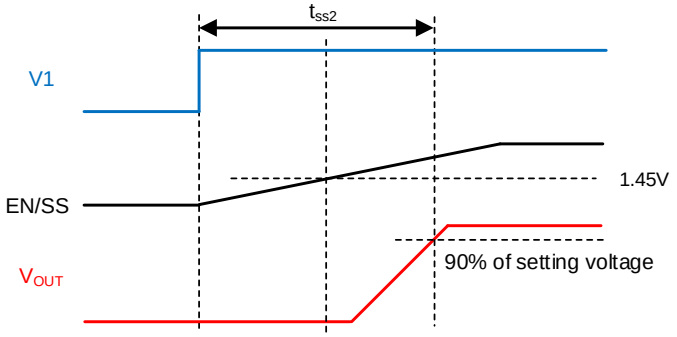
【Setting Example】

C_{SS} = 0.47μF, R_{SS} = 430kΩ, V1 = 12V

t_{SS2} = 0.47μF x 430kΩ x (ln (12V/(12V-1.45V)) = 26ms



< External Soft Start EN/SS circuit >



< Overview of external Soft Start >

■OPERATIONAL EXPLANATION (Continued)

< Power Good >

The output state can be monitored using the power good function. The PG pin is an Nch open drain output, therefore a pull-up resistor (approx. 100kΩ) must be connected to the PG pin.

The pull-up voltage should be 5.5V or less. When not using the power good function, connect the PG terminal to GND or leave it open.

CONDITION		SIGNAL
EN/SS = H	$V_{FB} > V_{PGDET}$	H (High impedance)
	$V_{FB} \leqq V_{PGDET}$	L (Low impedance)
	Thermal Shutdown	L (Low impedance)
	UVLO ($V_{IN} < V_{UVLOD}$)	Undefined State
EN/SS = L	Stand-by	L (Low impedance)

< UVLO Function >

When the V_{IN} pin voltage falls below V_{UVLOD} (TYP. 2.7V), the high side driver FET and low side driver FET are forcibly turned off to prevent false pulse output due to instable operation of the internal circuits. When the V_{IN} pin voltage rises above V_{UVLOR} (TYP. 2.8V), the UVLO function is released, the Soft Start function activates, and output start operation begins. Stopping by UVLO is not shutdown; only pulse output is stopped and the internal circuits continue to operate.

< Thermal Shutdown Function >

A thermal shutdown (TSD) function is built in for protection from overheating. When the junction temperature reaches the thermal shutdown detection temperature T_{TSD}, the High side driver FET and Low side driver FET are compulsorily turned off.

If the driver FET continues in the off state, the junction temperature declines, and when the junction temperature falls to the thermal shutdown cancel temperature, the thermal shutdown function is cancelled and the Soft Start function operates to start up the output voltage.

■OPERATIONAL EXPLANATION (Continued)

<Current limiting>

The current limiting circuit of the XD9263/XD9264 series monitor the current that flows through the High side driver transistor and Low side driver transistor, and when over-current is detected, the current limiting function activates.

① High side driver Tr. current limiting

The current in the High side driver Tr. is detected to equivalently monitor the peak value of the coil current. The High side driver Tr. current limiting function forcibly turns off the High side driver Tr. when the peak value of the coil current reaches the High side driver current limit value I_{LIMH}.

High side driver Tr. current limit value I_{LIMH}=1.1A (TYP.)

② Low side driver Tr. current limiting

The current in the Low side driver Tr. is detected to equivalently monitor the bottom value of the coil current. The Low side driver Tr. current limiting function operates when the High side driver Tr. current limiting value reaches I_{LIMH}. The Low side driver Tr. current limiting function prohibits the High side driver Tr. from turning on in an over current state where the bottom value of the coil current is higher than the Low side driver Tr. current limit value I_{LIML}.

Low side driver Tr. current limit value I_{LIML}=0.9A (TYP.)

When the output current increases and reaches the current limit value, the current foldback circuit operates and lowers the output voltage and FB voltage. The I_{LIMH} and I_{LIML} decline accompanying the FB voltage decrease to restrict the output current.

When the overcurrent state is removed, the foldback circuit operation increases the I_{LIMH} and I_{LIML} together with output voltage to return the output to the output voltage set value.

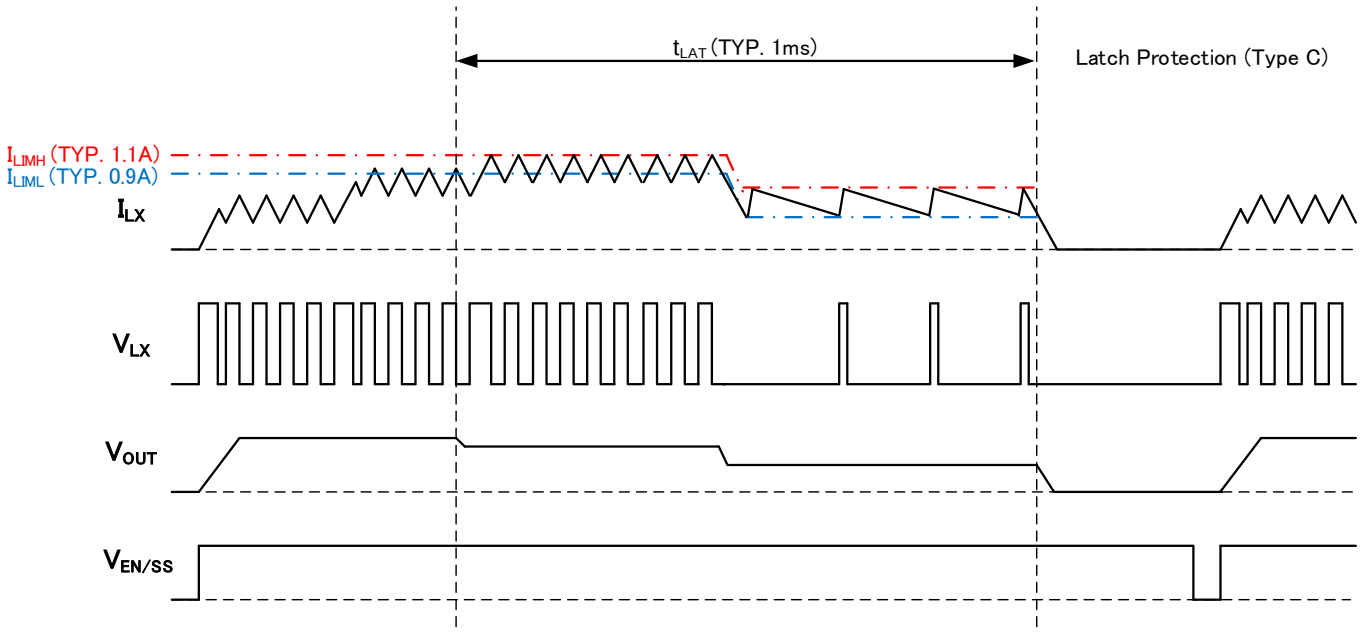
③ Over current latch (Type C)

Type C turns off the High side and Low side driver Tr. when state ① or ② continues for t_{LAT} (TYP. 1.0ms). The Lx pin is latch stopped at the GND level (0V).

The latch stopped state only stops the pulse output from the Lx pin; the internal circuitry of the IC continues to operate. To restart after latch stopping, L level and then H level must be input into the EN/SS pin, or V_{IN} pin re-input must be performed (after lowering the voltage below the UVLO detection voltage) to resume operation by Soft-Start.

The over current latch function may occasionally be released from the current limit detection state by the effects of ambient noise, and it may also happen that the latch time becomes longer or latching does not take place due to board conditions. For this reason, place the input capacitor as close as possible to the IC.

Type D is an automatic recovery type that performs the operation of ① or ② until the over current state is released.



Current limiting timing chart

■NOTES ON USE

1) In the case of a temporary and transient voltage drop or voltage rise.
If the absolute maximum ratings are exceeded, the IC may be deteriorate or destroyed.

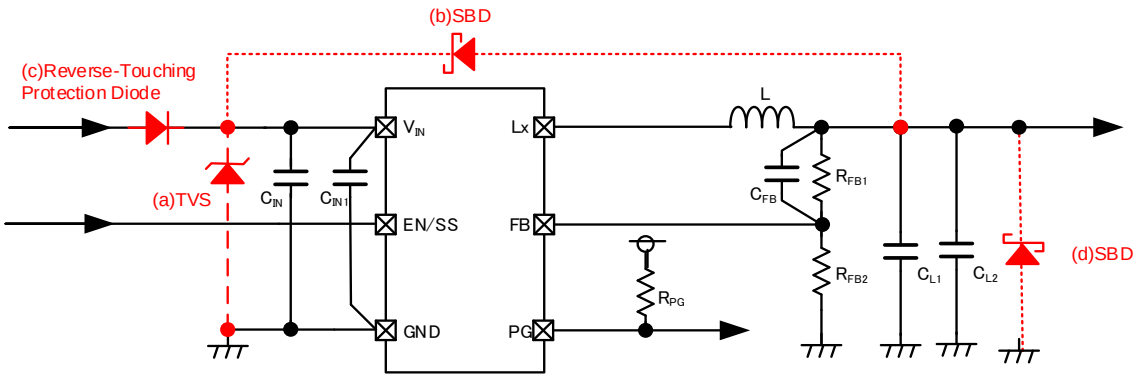
If a voltage exceeding the absolute maximum voltage is applied to the IC due to chattering caused by a mechanical switch or an external surge voltage, please use a protection element such as a TVS and a protection circuit as a countermeasure. Please see the countermeasures from (a) to (d) shown below.

(a) When voltage exceeding the absolute maximum ratings comes into the V_{IN} pin due to the transient change on the power line, there is a possibility that the IC breaks down in the end.
To prevent such a failure, please add a TVS between V_{IN} and GND as a countermeasure.

(b) When the input voltage decreases below the output voltage, there is a possibility that an overcurrent will flow in the IC's Internal parasitic diode and exceed the absolute maximum rating of the Lx pin.
If the current is pulled into the input side by the low impedance between V_{IN} and GND, then countermeasures, such as adding an SBD between V_{OUT} and V_{IN}, should be taken.

(c) When a negative voltage is applied to the input voltage by a reverse connection or chattering, an overcurrent could flow in the IC's parasitic diode and damage the IC. Take countermeasures, such as adding a reverse touching protection diode.

(d) When a sudden surge of electrical current travels along the V_{OUT} pin and GND due to a short-circuit, electrical resonance of a circuit involving parasitic inductor of cable related to short circuit and an output capacitor (C_L) and impedance such as V_{OUT} line generates a negative voltage exceeding the breakdown voltage and may damage the device.
Take countermeasures, such as connecting a schottky diode between the V_{OUT} and GND.



■NOTES ON USE(Continued)

2) Make sure that the absolute maximum ratings of the external components and of this IC are not exceeded.

3) The DC/DC converter characteristics depend greatly on the externally connected components as well as on the characteristics of this IC, so refer to the specifications and standard circuit examples of each component when carefully considering which components to select.
Be especially careful of the capacitor characteristics and use X7R or X5R (EIA standards) ceramic capacitors.
The capacitance decrease caused by the bias voltage may become large depending on the external size of the capacitor.

4) The current limit value is the coil current peak value when switching is not conducted.
The coil current peak value when the actual current limit function begins to operate may exceed the current limit of the electrical characteristics due to the effect of the propagation delay inside the circuit.

5) When the On time is less than the Minimum On Time (t_{ONMIN}) and the dropout voltage is large or the load is low, the PWM control operates intermittently and the V_{OUT} ripple voltage may become large or the output voltage may become unstable.

6) The V_{OUT} ripple voltage could be increased when switching from discontinuous conduction mode to continuous conduction mode and when switching to 100% Duty cycle.

7) The PWM/PFM auto series may cause superimposed V_{OUT} ripple voltage by continuous pulses if used in high temperature and no load conditions. It is necessary to set an idle current of higher than 100μA from V_{OUT} if used at no load.
It can have the same effect as when R_{FB2} is lower than 7.5kΩ. Please refer to the
< Output Voltage Setting Value V_{OUTSET} Setting > section under TYPICAL APPLICATION CIRCUIT.

8) If the voltage at the EN/SS Pin does not start from 0V but it is at the midpoint potential when the power is switched on, the Soft Start function may not work properly and it may cause larger inrush current and bigger V_{OUT} ripple voltages.

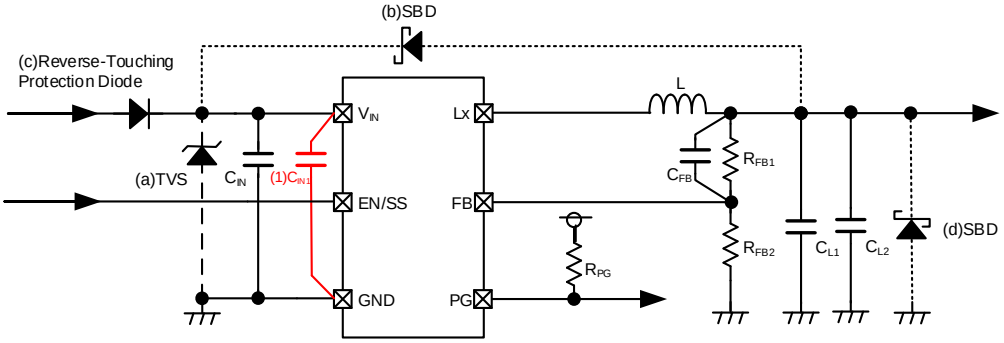
9) The effects of ambient noise and the state of the circuit board may cause release from the current limiting state, and the latch time may lengthen or latch operation may not take place. Please evaluate IC well on customer's PCB.

10) Torex places an importance on improving our products and their reliability. We request that users incorporate fail safe designs and post aging protection treatment when using Torex products in their systems.

■NOTES ON USE(Continued)

11) Instructions of pattern layouts.
The operation may become unstable due to noise and/or phase lag from the output current when the wire impedance is high, please place the input capacitor(C_{IN}) and the output capacitor (C_L) as close to the IC as possible.

(1) In order to stabilize V_{IN} voltage level, we recommend that a by-pass capacitor (C_{IN1}) be connected as close as possible to the V_{IN} and GND pins.



(2) Please mount each external component as close to the IC as possible.
Please place the external parts on the same side of the PCB as the IC, not on the reverse side of the PCB and elsewhere.

(3) Wire external components as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.

(4) Make sure that the GND traces are as thick as possible, as variations in ground potential caused by high ground currents at the time of switching may result in instability of the IC.

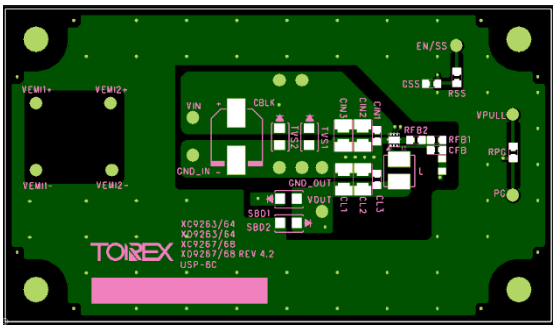
(5) This product has a built in driver FET, which causes heat generation from the on resistance, so take measures to dissipate the heat when necessary.

■NOTE ON USE (Continued)

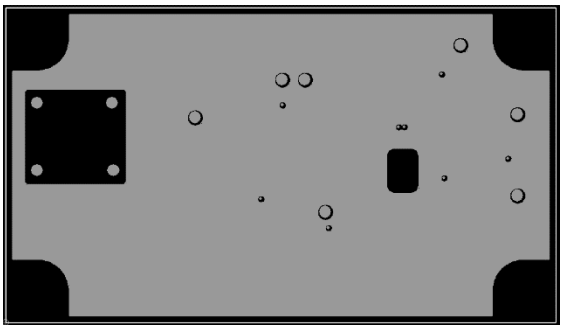
<Reference Pattern Layout>

●USP-6C

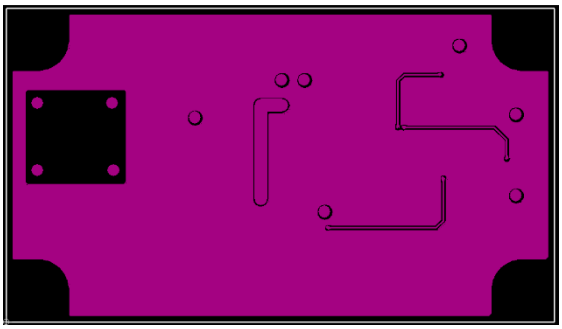
Layer 1



Layer 2



Layer 3



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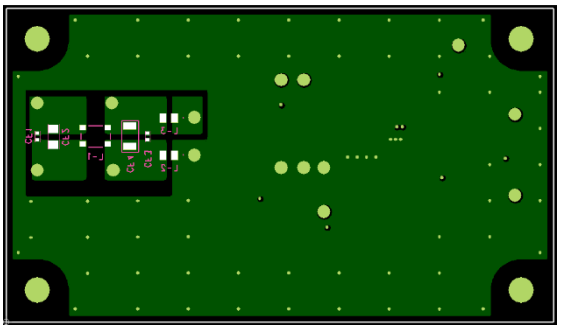
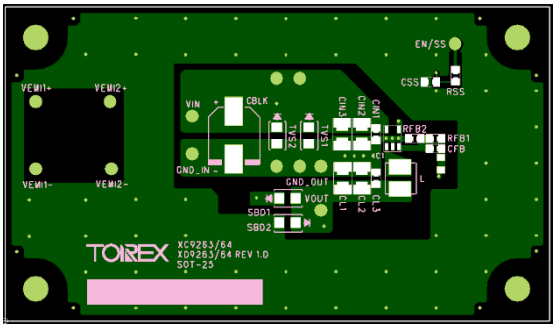


●SOT-25

Layer 1



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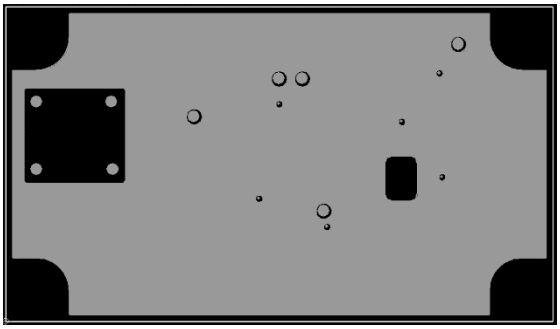
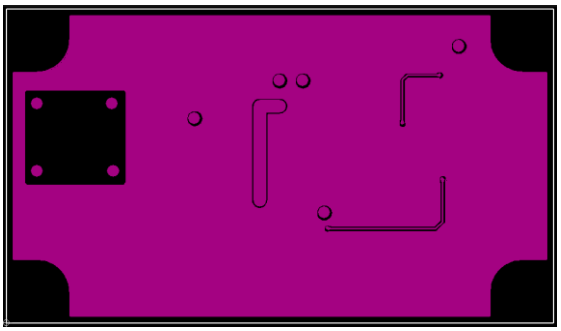


Layer 3



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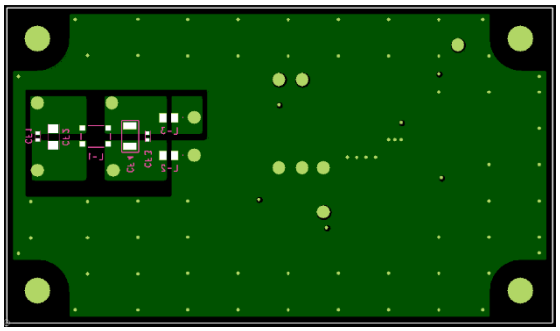
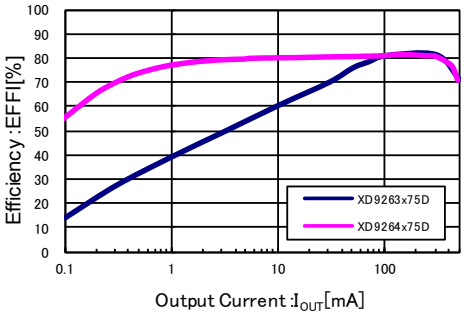


■TYPICAL PERFORMANCE CHARACTERISTICS

(1) Efficiency vs. Output current

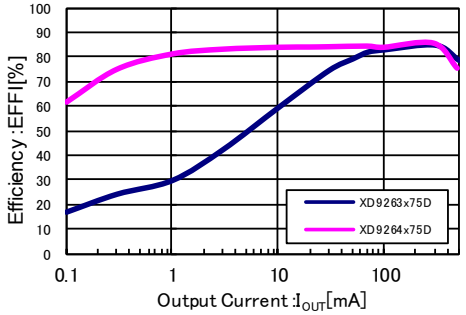
XD9263x75D/XD9264x75D
(V_{IN}=12V, V_{OUT}=3.3V)

L=2.2μ H(CLF6045NIT-2R2), C_{IN}=2.2μ F(GRT31CC81H225KE01),
C_L=10μ F×2 (GRT32DC81E106KE01)



XD9263x75D/XD9264x75D
(V_{IN}=12V, V_{OUT}=5V)

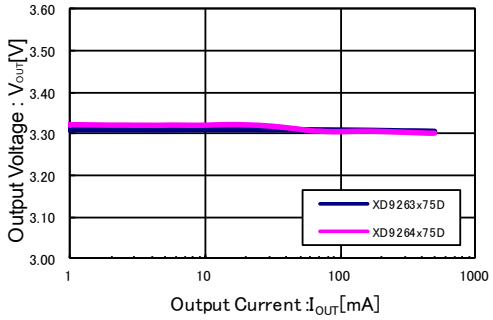
L=2.2μH(CLF6045NIT-2R2), CIN=2.2μF(GRT31CC81H225KE01),
CL=10μF×2 (GRT32DC81E106KE01)



(2) Output Voltage vs. Output Current

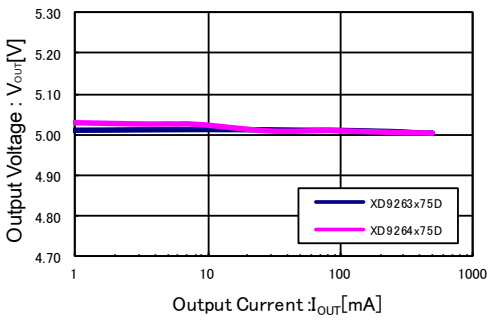
XD9263x75D/XD9264x75D
(V_{IN}=12V, V_{OUT}=3.3V)

L=2.2μ H(CLF6045NIT-2R2), C_{IN}=2.2μ F(GRT31CC81H225KE01),
C_L=10μ F×2 (GRT32DC81E106KE01)



XD9263x75D/XD9264x75D
(V_{IN}=12V, V_{OUT}=5V)

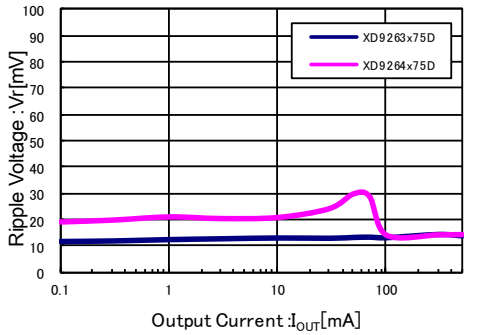
L=2.2μ H(CLF6045NIT-2R2), C_{IN}=2.2μ F(GRT31CC81H225KE01),
C_L=10μ F×2 (GRT32DC81E106KE01)



(3) Ripple Voltage vs. Output Current

XD9263x75D/XD9264x75D
(V_{IN}=12V, V_{OUT}=5V)

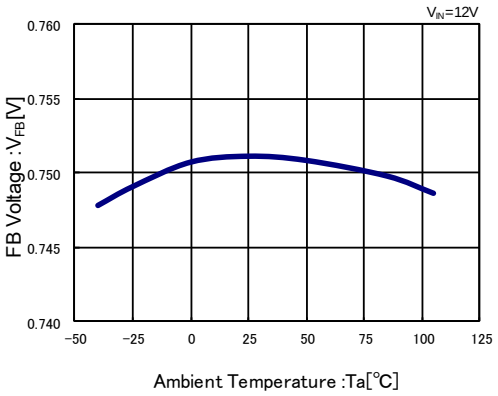
L=2.2μ H(CLF6045NIT-2R2), C_{IN}=2.2μ F(GRT31CC81H225KE01),
C_L=10μ F×2 (GRT32DC81E106KE01)



(4) FB Voltage vs. Ambient Temperature

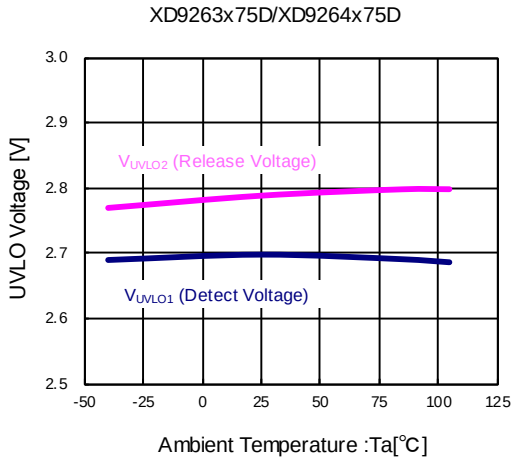
XD9263/XD9264

V_{IN}=12V

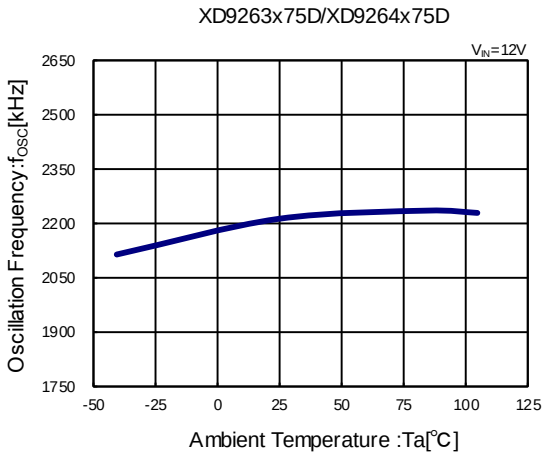


■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

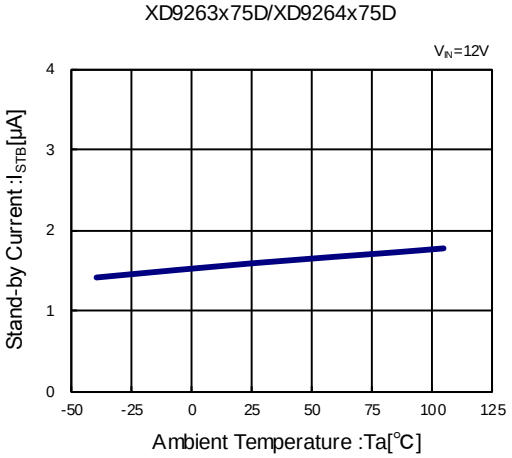
(5) UVLO Voltage vs. Ambient Temperature



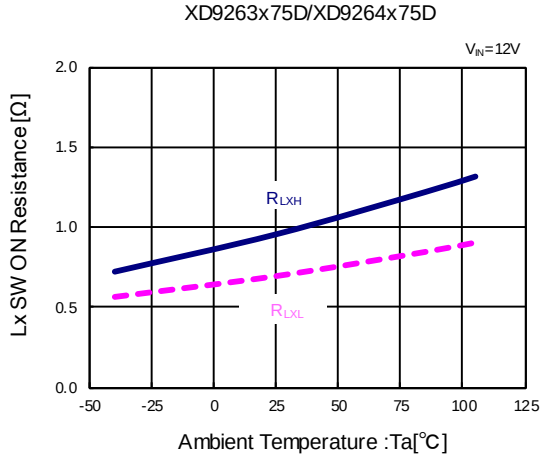
(6) Oscillation Frequency vs. Ambient Temperature



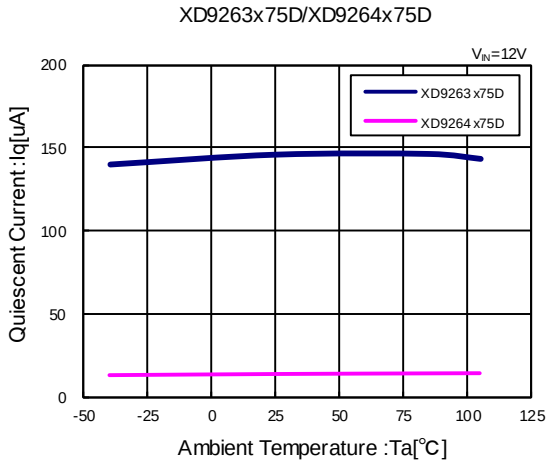
(7) Stand-by Current vs. Ambient Temperature



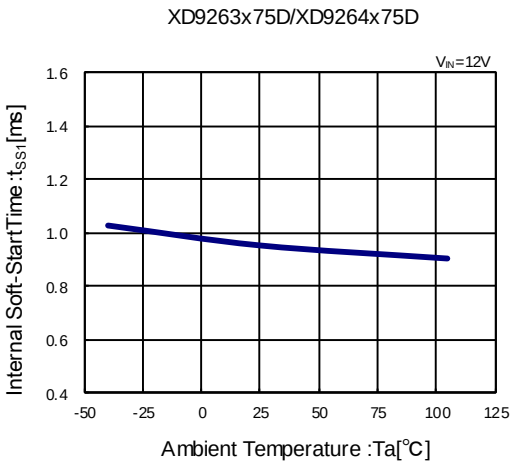
(8) Lx SW ON Resistance vs. Ambient Temperature



(9) Quiescent Current vs. Ambient Temperature

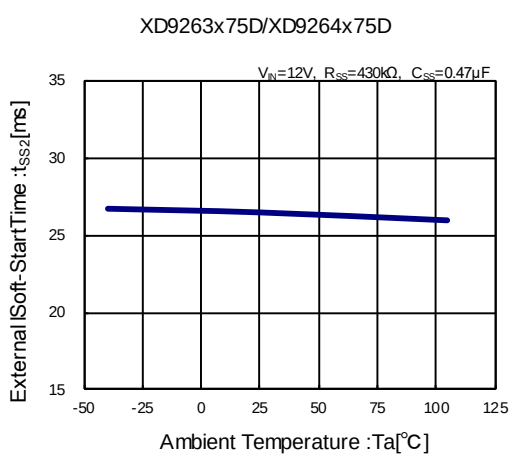


(10) Internal Soft-Start Time vs. Ambient Temperature

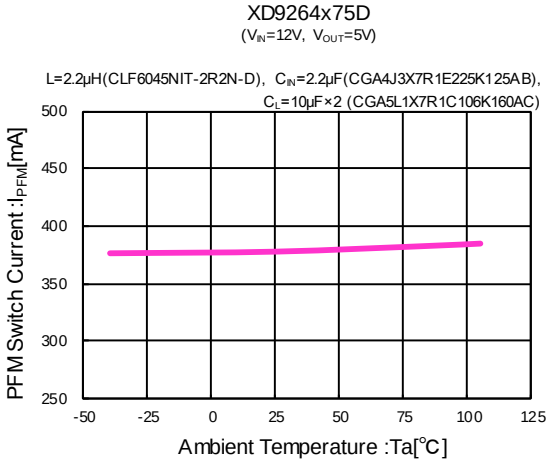


■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

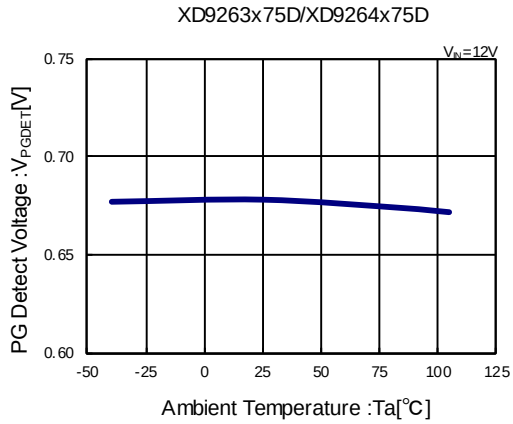
(11) External Soft-Start Time vs. Ambient Temperature



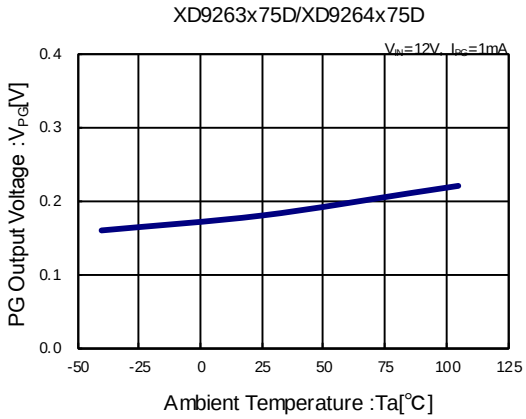
(12) PFM Switch Current vs. Ambient Temperature



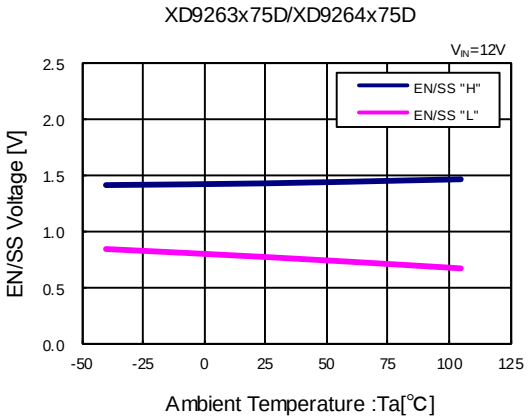
(13) PG Detect Voltage vs. Ambient Temperature



(14) PG Output Voltage vs. Ambient Temperature

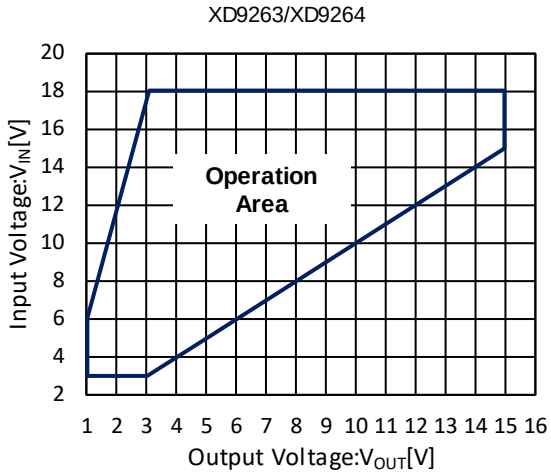


(15) EN/SS Voltage vs. Ambient Temperature

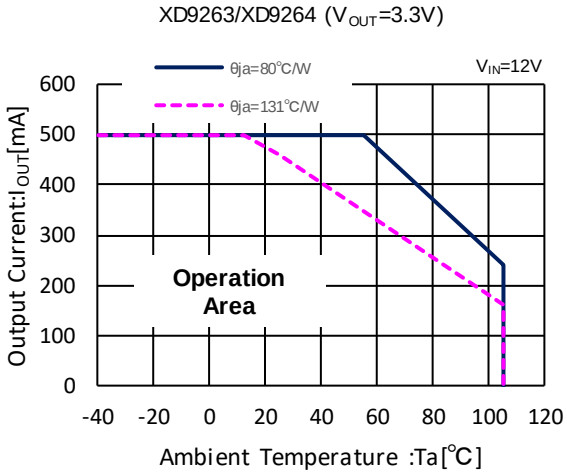


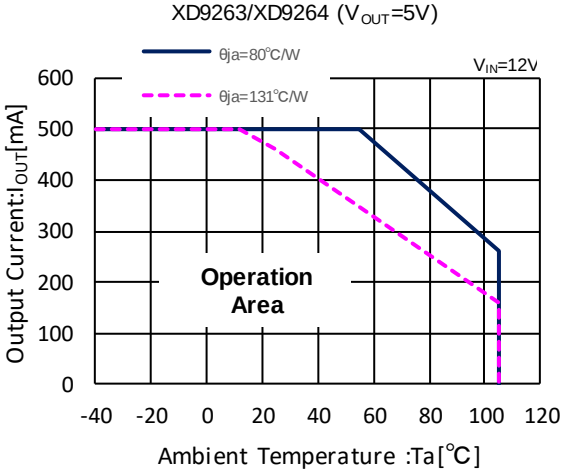
■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

(16) V_{IN}-V_{OUT} Operation Area



(17) Output Current Operation Area





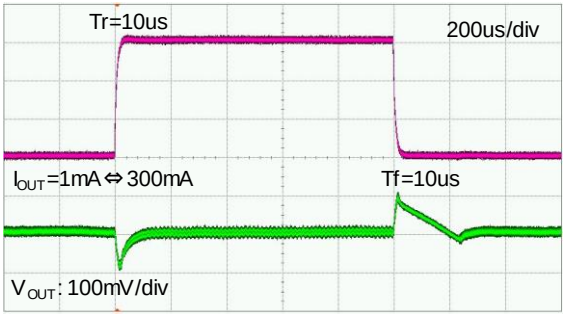
■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

(18) Load Transient Response

XD9263x75D

V_{IN}=12V, V_{OUT}=5.0V, I_{OUT}=1mA⇔300mA

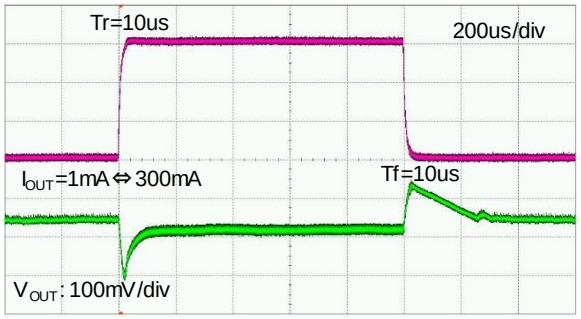
L=2.2μH(CLF6045NIT-2R2N-D), C_{IN}=2.2μF(CGA4J3X7R1E225K125AB),
C_L=10μF×2 (CGA5L1X7R1C106K160AC)



XD9264x75D

V_{IN}=12V, V_{OUT}=5.0V, I_{OUT}=1mA⇔300mA

L=2.2μH(CLF6045NIT-2R2N-D), C_{IN}=2.2μF(CGA4J3X7R1E225K125AB),
C_L=10μF×2 (CGA5L1X7R1C106K160AC)

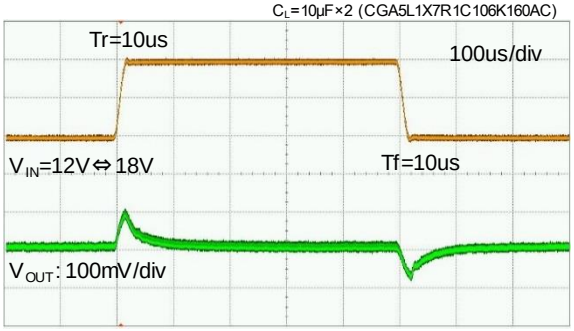


(19) Input Transient Response

XD9263x75D

V_{IN}=12V⇔18V, V_{OUT}=5V, I_{OUT}=300mA

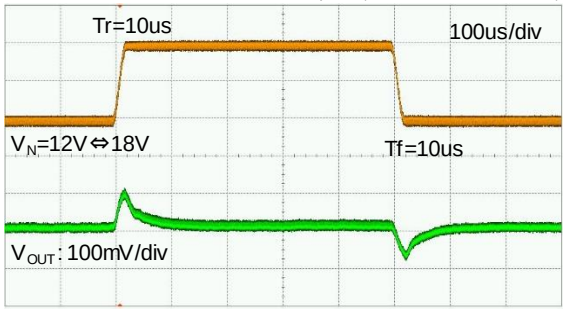
L=2.2μH(CLF6045NIT-2R2N-D), C_{IN}=2.2μF(CGA4J3X7R1E225K125AB),
C_L=10μF×2 (CGA5L1X7R1C106K160AC)



XD9264x75D

V_{IN}=12V⇔18V, V_{OUT}=5V, I_{OUT}=300mA

L=2.2μH(CLF6045NIT-2R2N-D), C_{IN}=2.2μF(CGA4J3X7R1E225K125AB),
C_L=10μF×2 (CGA5L1X7R1C106K160AC)

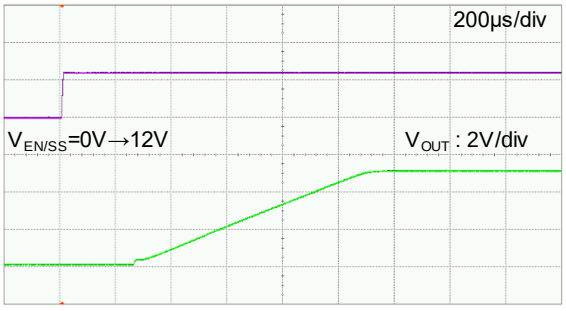


(20) EN/SS Rising Response

XD9263x75D

V_{IN}=12V, $V_{EN/SS}$=0V→12V, V_{OUT}=5V, I_{OUT}=300mA

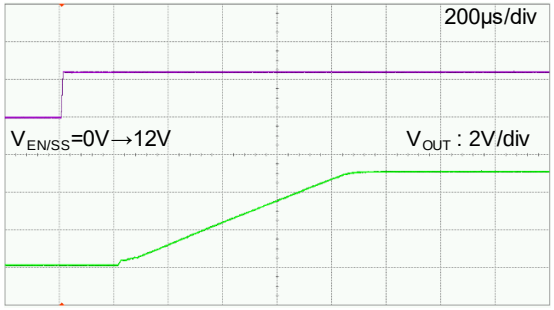
L=2.2μH(CLF6045NIT-2R2N-D), C_{IN}=2.2μF(CGA4J3X7R1E225K125AB),
C_L=10μF×2 (CGA5L1X7R1C106K160AC)



XD9264x75D

V_{IN}=12V, $V_{EN/SS}$=0V→12V, V_{OUT}=5V, I_{OUT}=300mA

L=2.2μH(CLF6045NIT-2R2N-D), C_{IN}=2.2μF(CGA4J3X7R1E225K125AB),
C_L=10μF×2 (CGA5L1X7R1C106K160AC)



■PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages/

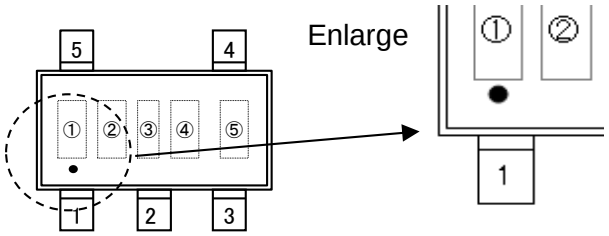
PACKAGE	OUTLIN / LAND PATTERN	THERMAL CHARACTERISTICS	
SOT-25	SOT-25 PKG	JESD51-7 Board	SOT-25 Power Dissipation
USP-6C	USP-6C PKG	JESD51-7 Board	USP-6C Power Dissipation

■MARKING RULE

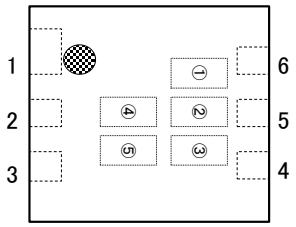
●SOT-25 / USP-6C

(*) SOT-25 has a dot mark, which is printed under MARK ① (refer to drawings below).

●SOT-25 (Under dot)



●USP-6C



①②③represents products series, products type, Oscillation Frequency

MARK			SERIES	TYPE	OSCILLATION FREQUENCY	PRODUCT SERIES
①	②	③				
L	4	1	XD9263	C	D	XD9263C75D**-Q
L	4	2	XD9263	D	D	XD9263D75D**-Q
L	4	3	XD9264	C	D	XD9264C75D**-Q
L	4	4	XD9264	D	D	XD9264D75D**-Q

④,⑤ represents production lot number
01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ, B1～ZZ in order.
(G, I, J, O, Q, W excluded)
* No character inversion used.

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.

2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.

3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.

4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions, excluding when specified for in-vehicle use or other uses.
   Do not use the product for in-vehicle use or other uses unless agreed by us in writing in advance.

5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.

6. Our products are not designed to be Radiation-resistant.

7. Please use the product listed in this datasheet within the specified ranges.

8. We assume no responsibility for damage or loss due to abnormal use.

9.

TOREX SEMICONDUCTOR LTD.