XC9267 Series

36V Operation 0.6A Synchronous Step-Down DC/DC Converters

■GENERAL DESCRIPTION

The XC9267 series are 36V operation synchronous step-down DC/DC converter ICs with a built-in P-channel MOS driver transistor and N-channel MOS switching transistor.

The XC9267 series has operating voltage range of 3.0V～36.0V and high-efficiency power supply up to an output current of 0.6A. Low ESR capacitors such as ceramic capacitors can be used for the load capacitor (C_L).

A 0.75V reference voltage source is incorporated in the IC, and the output voltage can be set to a value from 1.0V to 25.0V using external resistors (R_{FB1}, R_{FB2}).

1.2MHz or 2.2MHz can be selected for the switching frequency.

The soft-start time is internally set to 2.0ms (TYP.), but can be adjusted to set a longer time using an external resistor and capacitor.

With the built-in UVLO function, the driver transistor is forced OFF when input voltage becomes 2.7V or lower.
The output state can be monitored using the power good function.
Internal protection circuits include over current protection, short-circuit protection, and thermal shutdown circuits to enable safe use.

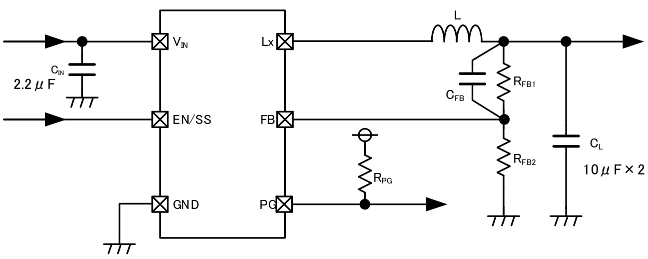
■APPLICATIONS

- Electric Meter
- Gas Detector
- Various Sensor
- Industrial Equipment
- Home appliance

■FEATURES

Input Voltage Range	:	3～36V(Absolute Max 40V)
Output Voltage Range		1.0～25V
FB Voltage	:	0.75V±1.5%
Oscillation Frequency	:	1.2MHz、2.2MHz
Output Current	:	0.6A
Control Methods	:	PWM control
		Efficiency88%@12V→5V、300mA
Soft-start Time	:	Adjustable by RC
Protection Circuits	:	Over Current Protection
	:	Thermal Shutdown
		Short-circuit Protection
Low ESR Ceramic Capacitor	:	Ceramic Capacitor
Packages	:	SOT-89-5 (Without Power Good)
	:	USP-6C (With Power Good)
Environmentally Friendly		EU RoHS Compliant, Pb Free

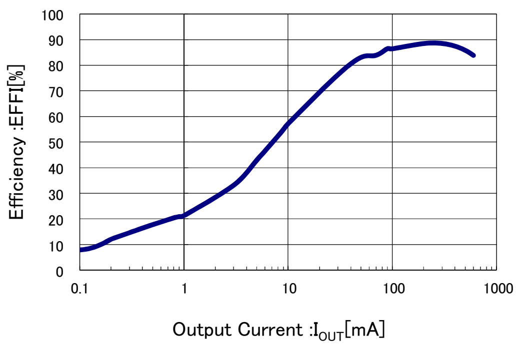
■TYPICAL APPLICATION CIRCUIT



■TYPICAL PERFORMANCE CHARACTERISTICS

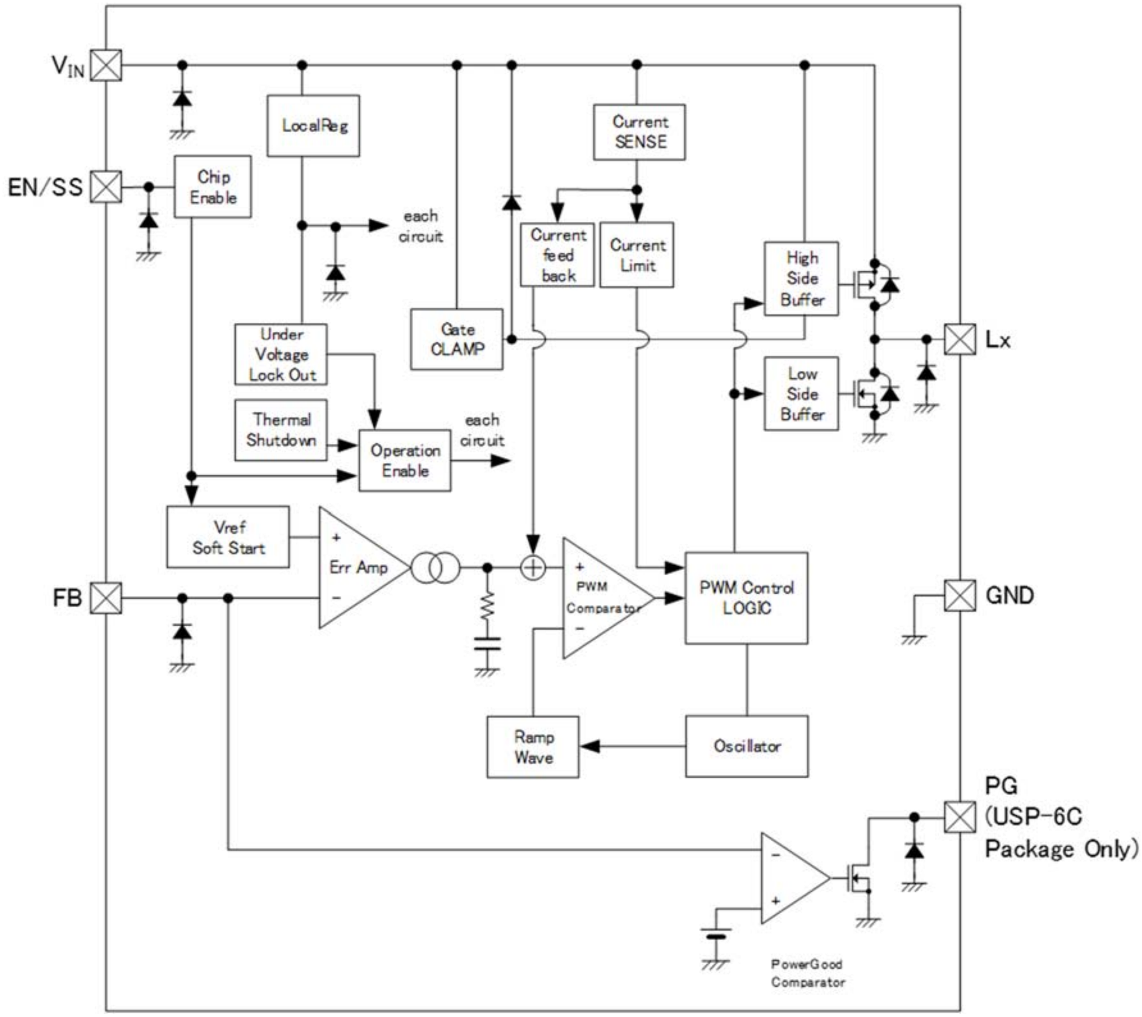
XC9267B75Cxx
(V_{IN}=12V, V_{OUT}=5V, f_{OSC}=1.2MHz)

L=6.8μH(CLF5030NIT-6R8), C_{IN}=4.7μF×2(C2012X6S1H475K)
C_L=10μF×2 (C3216X7R1E106K)



■BLOCK DIAGRAM

XC9267 Series



Diodes inside the circuit are an ESD protection diodes and a parasitic diodes.

■PRODUCT CLASSIFICATION

●Ordering Information

XC9267①②③④⑤⑥-⑦(*1) PWM control

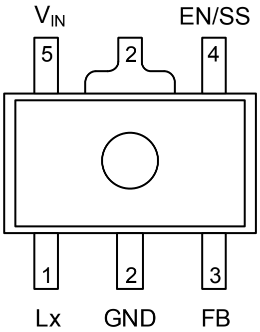
DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	B	Refer to Selection Guide
②③	Adjustable Output Voltage	75	Output voltage can be adjusted in 1.0V to 25V
④	Oscillation Frequency	C	1.2MHz
		D	2.2MHz
⑤⑥-⑦	Packages	PR-G(*1)	SOT-89-5 (1000pcs/Reel)
		ER-G(*1)	USP-6C (3000pcs/Reel)

(*1) The "-G" suffix denotes Halogen and Antimony free as well as being fully RoHS compliant.

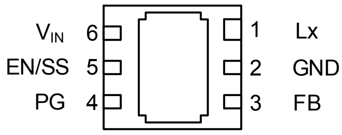
●Selection Guide

TYPE	Packages	Chip Enable	UVLO	Thermal Shutdown	Power Good (USP-6C)	Soft Start	Current Limiter	Automatic Recovery (Current Limiter)
B	SOT-89-5	YES	YES	YES	NO	YES	YES	YES
	USP-6C	YES	YES	YES	YES	YES	YES	YES

■PIN CONFIGURATION



SOT-89-5
(TOP VIEW)



USP-6C
(BOTTOM VIEW)

* The dissipation pad for the USP-6C package should be solder-plated in recommended mount pattern and metal masking so as to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to the GND (No. 2) pin.

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
SOT-89-5	USP-6C		
5	6	V_{IN}	Power Input
4	5	EN/SS	Enable Soft-start
-	4	PG	Power-good Output
3	3	FB	Output Voltage Sense
2	2	GND	Ground
1	1	Lx	Switching Output

■FUNCTION CHART

PIN NAME	SIGNAL	STATUS
EN/SS	L	Stand-by
	H	Active
	OPEN	Undefined State(*1)

(*1) Please do not leave the EN/SS pin open. Each should have a certain voltage.

■ABSOLUTE MAXIMUM RATINGS

Ta=25℃

PARAMETER		SYMBOL	RATINGS	UNITS
V_{IN} Pin Voltage		V_{IN}	-0.3 ～ +40	V
EN/SS Pin Voltage		$V_{EN/SS}$	-0.3 ～ +40	V
FB Pin Voltage		V_{FB}	-0.3 ～ +6.2	V
PG Pin Voltage(*1)		V_{PG}	-0.3 ～ +6.2	V
PG Pin Current(*1)		I_{PG}	8	mA
Lx Pin Voltage		V_{Lx}	-0.3 ～ V_{IN} + 0.3 or +40 (*2)	V
Lx Pin Current		I_{Lx}	1800	mA
Power Dissipation	SOT-89-5	Pd	1750(JEDEC board) (*4)	mW
	USP-6C(DAF)		1250(JEDEC board) (*4)	
Surge Voltage		V_{SURGE}	+46(*3)	V
Operating Ambient Temperature		Topr	-40 ～ +105	℃
Storage Temperature		Tstg	-55 ～ +125	℃

* All voltages are described based on the GND pin.

(*1) For the USP-6C Package only.

(*2) The maximum value should be either V_{IN}+0.3 or 40 in the lowest.

(*3) Applied Time≦400ms

(*4) The power dissipation figure shown is PCB mounted and is for reference only.
Please see the power dissipation page for the mounting condition.

■ELECTRICAL CHARACTERISTICS

XC9267series Ta=25℃

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	CIRCUIT
FB Voltage	V_{FBE}	V_{FB}=0.739V→0.761V, V_{FB} Voltage when Lx pin voltage changes from"H" level to "L" level		0.739	0.750	0.761	V	②
Setting Output Voltage Range (*1)	V_{OUTSET}	-		1	-	25	V	-
Operating Input Voltage Range (*1)	V_{IN}	-		3	-	36	V	-
UVLO Detect Voltage	V_{UVLOD}	$V_{EN/SS}$=12V,V_{IN}:2.8V→2.6V,V_{FB}=0V V_{IN} Voltage which Lx pin voltage holding "H" level		2.6	2.7	2.8	V	②
UVLO Release Voltage	V_{UVLOR}	$V_{EN/SS}$=12V,V_{IN}:2.7V→2.9V,V_{FB}=0V V_{IN} Voltage which Lx pin voltage holding "L" level		2.7	2.8	2.9	V	②
Quiescent Current	I_q	V_{FB}=0.825V	XC9267B75C	-	180	350	μA	④
			XC9267B75D	-	290	500		
Stand-by Current	I_{STBY}	V_{IN}=12V, $V_{EN/SS}$=V_{FB}=0V		-	1.65	2.50	μA	④
Oscillation Frequency	f_{OSC}	Connected to external components, I_{OUT}=200mA	XC9267B75C	1.098	1.200	1.302	MHz	①
			XC9267B75D	2.013	2.200	2.387		
Minimum On Time	t_{ONMIN}	Connected to external components		-	85 (*2)	-	ns	①
Minimum Duty Cycle	D_{MIN}	V_{FB}=0.825V		-	-	0	%	②
Maximum Duty Cycle	D_{MAX}	V_{FB}=0.675V		100	-	-	%	②
Lx SW "H" On Resistance	R_{LxH}	V_{FB}=0.675V, I_{Lx}=200mA		-	1.20	1.38	Ω	⑤
Lx SW "L" On Resistance	R_{LxL}			-	0.60 (*2)	-	Ω	⑤
Highside Current Limit (*3)	I_{LIMH}	V_{FB}=V_{FBE}×0.98		1.00	1.30	-	A	⑤
Internal Soft-Start Time	t_{SS1}	V_{FB}=0.675V		1.6	2.0	2.4	ms	②
External Soft-Start Time	t_{SS2}	V_{FB}=0.675V R_{SS}=430KΩ, C_{SS}=0.47μF		21	26	33	ms	③
PG detect voltage (*4)	V_{PGDET}	V_{FB}=0.712V→0.638V, R_{PG}:100kΩ pull-up to 5V V_{FB} Voltage when PG pin voltage changes from"H" level to "L" level		0.638	0.675	0.712	V	⑤
PG Output voltage (*4)	V_{PG}	V_{FB}=0.6V, I_{PG}=1mA		-	-	0.3	V	②
Efficiency (*5)	EFFI	Connected to external components, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=300mA		-	88	-	%	①
FB Voltage Temperature Characteristics	$\Delta V_{FB}/(\Delta T_{opr}\cdot V_{FBE})$	-40℃≦T_{opr}≦105℃		-	±100	-	ppm/℃	②

Test Condition: Unless otherwise stated, V_{IN}=12V, $V_{EN/SS}$=12V, V_{PG}:OPEN (*4)
Peripheral parts connection conditions：
L=6.8μH,R_{FB1}=680kΩ,R_{FB2}=120kΩ,C_{FB}=18pF,C_L=10μF×2parallel, C_{IN}=2.2μF
(*1) Please use within the range of $V_{OUT}/V_{IN} \geqq t_{ONMIN}[ns] \times f_{OSC}[MHz] \times 10^{-3}$
(*2) Design reference value. This parameter is provided only for reference.
(*3) Current limit denotes the level of detection at peak of coil current.
(*4) For the USP-6C Package only.
(*5) EFFI = {(output voltage) x (output current)} / {(input voltage) x (input current)} x 100

■ELECTRICAL CHARACTERISTICS(Continued)

XC9267 series Ta=25℃

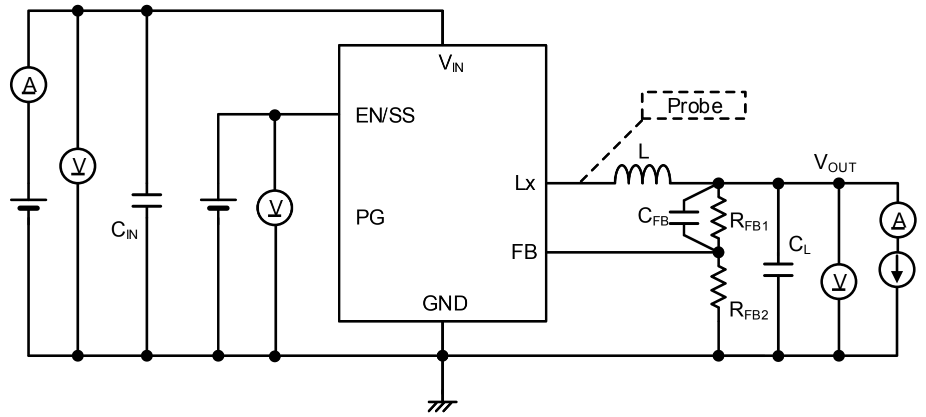
ARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	CIRCUIT
FB "H" Current	I_{FBH}	$V_{IN}=V_{EN/SS}$=36V, V_{FB}=3.0V	-0.1	-	0.1	μA	④
FB "L" Current	I_{FBL}	$V_{IN}=V_{EN/SS}$=36V, V_{FB}=0V	-0.1	-	0.1	μA	④
EN/SS "H" Voltage	$V_{EN/SSH}$	$V_{EN/SS}$=0.3V→2.5V, V_{FB}=0.71V $V_{EN/SS}$ Voltage when Lx pin voltage changes from "L" level to "H" level	2.5	-	36	V	②
EN/SS "L" Voltage	$V_{EN/SSL}$	$V_{EN/SS}$=2.5V→0.3V, V_{FB}=0.71V $V_{EN/SS}$ Voltage when Lx pin voltage changes from "H" level to "L" level	-	-	0.3	V	②
EN/SS "H" Current	$I_{EN/SSH}$	$V_{IN}=V_{EN/SS}$=36V, V_{FB}=0.825V	-	0.1	0.3	μA	④
EN/SS "L" Current	$I_{EN/SSL}$	V_{IN}=36V, $V_{EN/SS}$=0V, V_{FB}=0.825V	-0.1	-	0.1	μA	④
Thermal Shutdown Temperature	T_{TSD}	Junction Temperature	-	150	-	℃	−
Hysteresis Width	T_{HYS}	Junction Temperature	-	25	-	℃	−

Test Condition: Unless otherwise stated, V_{IN}=12V, $V_{EN/SS}$=12V, V_{PG}:OPEN [*4]

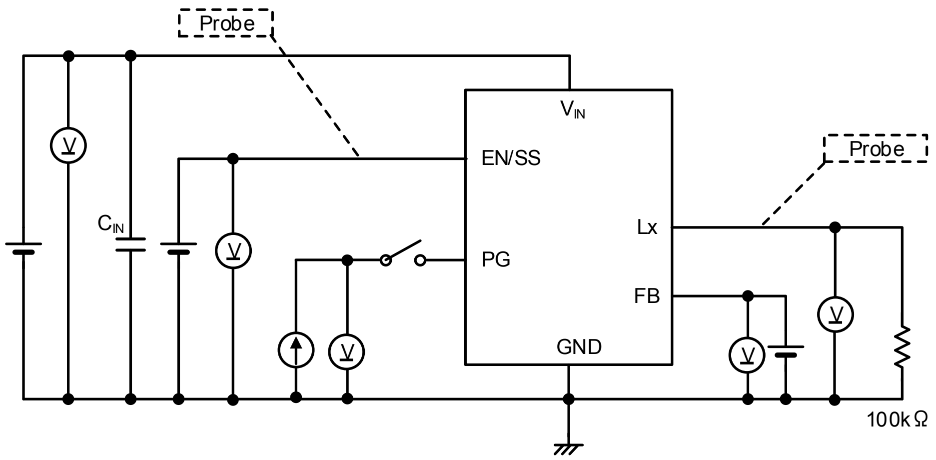
[*4] For the USP-6C Package only.

■TEST CIRCUITS

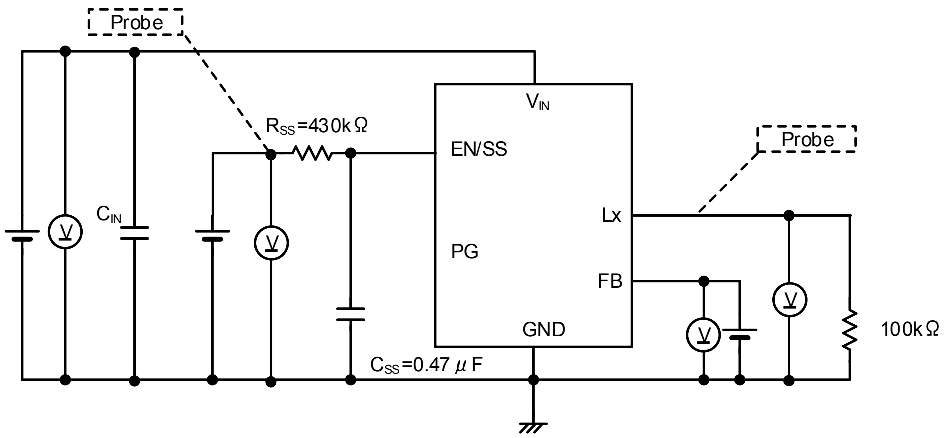
CIRCUIT①



CIRCUIT②



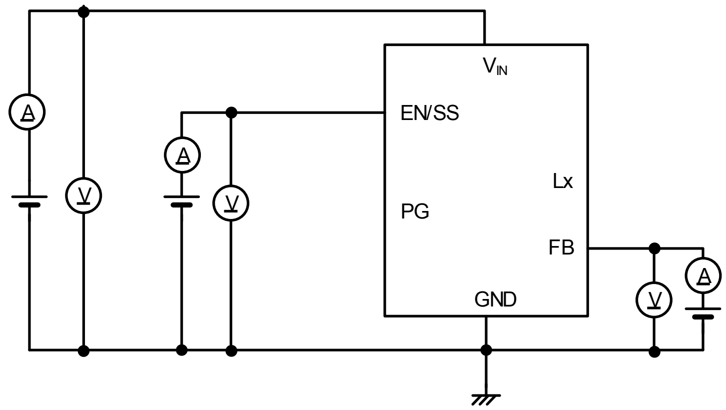
CIRCUIT③



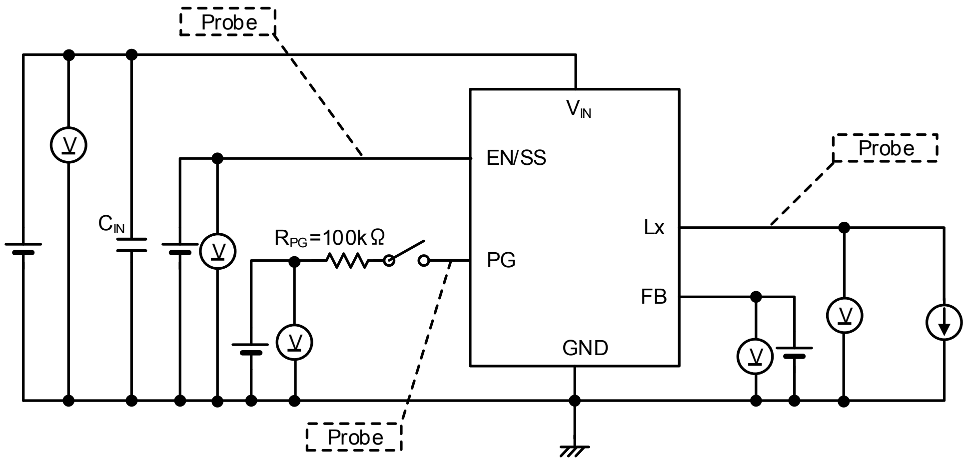
* PG Pin is USP-6C Package only.

■TEST CIRCUITS(Continued)

CIRCUIT④

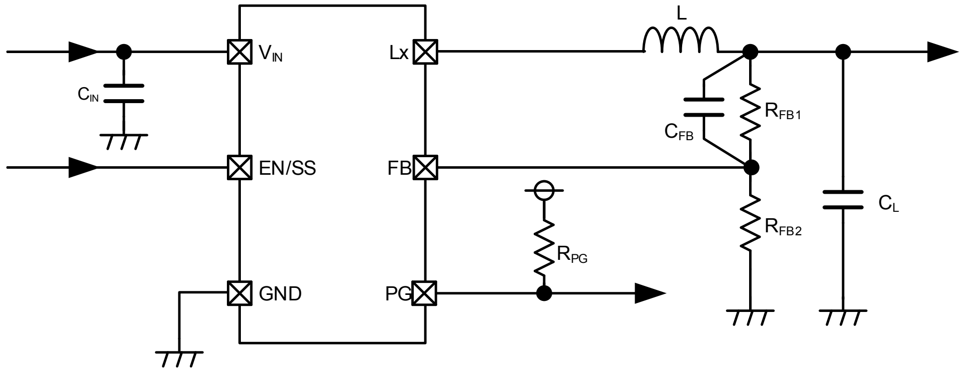


CIRCUIT⑤



* PG Pin is USP-6C Package only.

■TYPICAL APPLICATION CIRCUIT



＜Inductance value setting＞

For the XC9267 Series, operation is optimized by setting the following inductance value according to the set frequency and setting output voltage.

F_{OSCSET}: Frequency setting　 V_{OUTSET}: Output voltage setting

【Typical Examples】

	F_{OSCSET}	conditions	MANUFACTURER	PRODUCT NUMBER	VALUE
L	1.2MHz	$1V < V_{OUTSET} \leqq 2V$	TDK	CLF5030NIT-3R3N	3.3μH
			Coilcraft	XEL4030-332ME	
		$2V < V_{OUTSET} \leqq 3.3V$	TDK	CLF5030NIT-4R7N	4.7μH
			Coilcraft	XEL4030-472ME	
		$3.3V < V_{OUTSET} \leqq 6V$	TDK	CLF5030NIT-6R8N	6.8μH
			Coilcraft	XEL4030-682ME	
		$6V < V_{OUTSET} \leqq 25V$	TDK	CLF5030NIT-100N	10μH
	2.2MHz	$1V < V_{OUTSET} \leqq 2V$	TDK	CLF5030NIT-1R5N	1.5μH
			Coilcraft	XEL4030-152ME	
		$2V < V_{OUTSET} \leqq 3.3V$	TDK	CLF5030NIT-2R2N	2.2μH
			Coilcraft	XEL4030-222ME	
		$3.3V < V_{OUTSET} \leqq 6V$	TDK	CLF5030NIT-3R3N	3.3μH
			Coilcraft	XEL4030-332ME	
		$6V < V_{OUTSET} \leqq 25V$	TDK	CLF5030NIT-4R7N	4.7μH
			Coilcraft	XEL4030-472ME	
C_{IN}	1.2MHz	$V_{IN} < 20V$	TDK	C2012X6S1H475K125AC	4.7μF/50V
		$V_{IN} \geqq 20V$	TDK	C2012X6S1H475K125AC	4.7μF/50V 2parallel
	2.2MHz	$V_{IN} < 20V$	TDK	C2012X7R1H225K125AC	2.2μF/50V
		$V_{IN} \geqq 20V$	TDK	C2012X7R1H225K125AC	2.2μF/50V 2parallel
C_L	-	-	TDK	C2012X7R1A106K125AC	10μF/10V 2parallel
				C3216X7R1E106K160AB	10μF/35V 2parallel
				C3225X7R1H106M250AC	10μF/50V 2parallel

■TYPICAL APPLICATION CIRCUIT(Continued)

< Output voltage setting >
The output voltage can be set by adding an external dividing resistor.
The output voltage is determined by the equation below based on the values of R_{FB1} and R_{FB2}.

$$V_{OUT}=0.75V\times(R_{FB1}+R_{FB2})/R_{FB2}$$
$$\text{With } R_{FB2}\leqq 400k\Omega$$

<C_{FB} setting>
Adjust the value of the phase compensation speed-up capacitor C_{FB} using the equation below.

$$C_{FB}=\frac{1}{2\pi\times fzfb\times R_{FB1}}$$

A target value for fzfb of about $fzfb=\dfrac{1}{2\pi\sqrt{C_L\times L}}$ is optimum.

【Setting Example】
To set output voltage to 5V with fosc=1.2MHz, C_L=10μF×2, L=6.8μH

When R_{FB1}=680kΩ, R_{FB2}=120kΩ, V_{OUTSET}=0.75V× (680kΩ+120kΩ) / 120kΩ=5.0V
And fzfb is set to a target of 13.65 kHz using the above equation,
C_{FB}=1/ (2×π×13.65 kHz×680kΩ) =17.15pF. A capacitor of E24 series is 18pF.

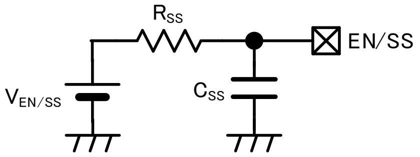
XC9267B75Cxx / f_{OSC}=1.2MHz					
V_{OUTSET}	R_{FB1}	R_{FB2}	L	C_{FB}	fzfb
1.2V	120kΩ	200kΩ	3.3μH	68pF	19.6kHz
3.3V	510kΩ	150kΩ	4.7μH	18pF	16.4kHz
5.0V	680kΩ	120kΩ	6.8μH	18pF	13.7kHz
12V	1500kΩ	100kΩ	10μH	9pF	11.3kHz

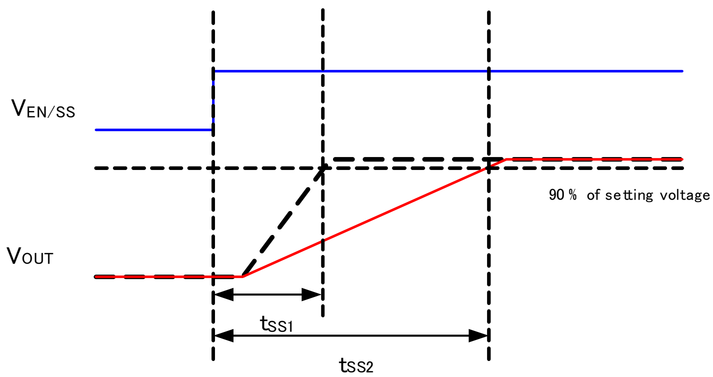
XC9267B75Dxx / f_{OSC}=2.2MHz					
V_{OUTSET}	R_{FB1}	R_{FB2}	L	C_{FB}	fzfb
1.2V	120kΩ	200kΩ	1.5μH	47pF	29.1kHz
3.3V	510kΩ	150kΩ	2.2μH	12pF	24.0kHz
5.0V	680kΩ	120kΩ	3.3μH	12pF	19.6kHz
12V	1500kΩ	100kΩ	4.7μH	6.2pF	16.4kHz

<Soft-start Time Setting>
The soft-start time can be adjusted by adding a capacitor and a resistor to the EN/SS pin.
Soft-start time (t_{SS2}) is approximated by the equation below according to values of $V_{EN/SS}$, R_{SS}, and C_{SS}.

$$t_{ss2}=C_{ss}\times R_{ss}\times \ln\left(V_{EN/SS}/(V_{EN/SS}-1.45)\right)$$

【Setting Example】
When C_{SS}=0.47μF, R_{SS}=430kΩ and $V_{EN/SS}$=12V, $t_{SS2}=0.47\times10^{-6}\times430\times10^{3}\times(\ln(12/(12-1.45)))$ =26ms (Approx.)
*The soft-start time is the time from the start of $V_{EN/SS}$ until the output voltage reaches 90% of the set voltage.
If the EN/SS pin voltage rises steeply without connecting C_{SS} and R_{SS} (R_{SS}=0Ω), Output rises with taking the soft-start time of t_{SS1}=2.0ms (TYP.) which is fixed internally.

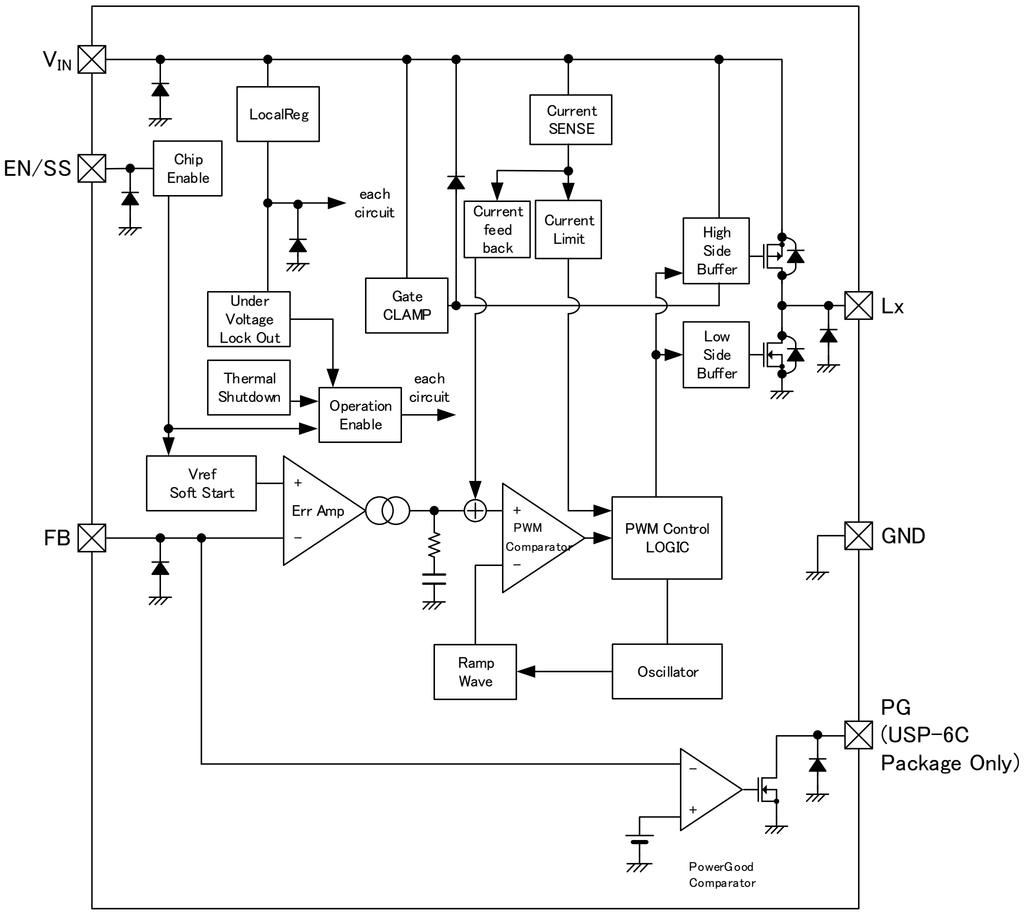




■OPERATIONAL EXPLANATION

The XC9267 series consists internally of a reference voltage supply with soft-start function, error amp, PWM comparator,ramp wave circuit, oscillator circuit, phase compensation (Current feedback) circuit, current limiting circuit, current limit PFM circuit, High-side driver Tr., Low-side driver Tr., buffer drive circuit, internal power supply (LocalReg) circuit, under-voltage lockout (UVLO) circuit, gate clamp (CLAMP) circuit, thermal shutdown (TSD) circuit, power good comparator, PWM control block and other elements.
The voltage feedback from the FB pin is compared to the internal reference voltage by the error amp, the output from the error amp is phase compensated, and the signal is input to the PWM comparator to determine the ON time of switching during PWM operation. The output signal from the error amp is compared to the ramp wave by the PWM comparator, and the output is sent to the buffer drive circuit and output from the LX pin as the duty width of switching. This operation is performed continuously to stabilize the output voltage.
The driver transistor current is monitored at each switching by the phase compensation (Current feedback) circuit, and the output signal from the error amp is modulated as a multi-feedback signal. This allows a stable feedback system to be obtained even when a low ESR capacitor such as a ceramic capacitor is used, and this stabilizes the output voltage.

XC9267 Series



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

<Reference voltage source>
The reference voltage source provides the reference voltage to ensure stable output voltage of the DC/DC converter.

<Oscillator circuit>
The oscillator circuit determines switching frequency.1.2MHz or 2.2MHz is available for the switching frequency.
Clock pulses generated in this circuit are used to produce ramp waveforms needed for PWM operation.

<Error amplifier>
The error amplifier is designed to monitor output voltage. The amplifier compares the reference voltage with the feedback voltage divided by the internal voltage divider, R_{FB1} and R_{FB2}. When a voltage is lower than the reference voltage, then the voltage is fed back, the output voltage of the error amplifier increases. The error amplifier output is fixed internally to deliver an optimized signal to the mixer.

■OPERATIONAL EXPLANATION(Continued)

<Current limiting>
The current limiting circuit of the XC9267 series monitors the current that flows through the High-side driver transistor and Low-side driver transistor, and when over-current is detected, the current limiting function activates.

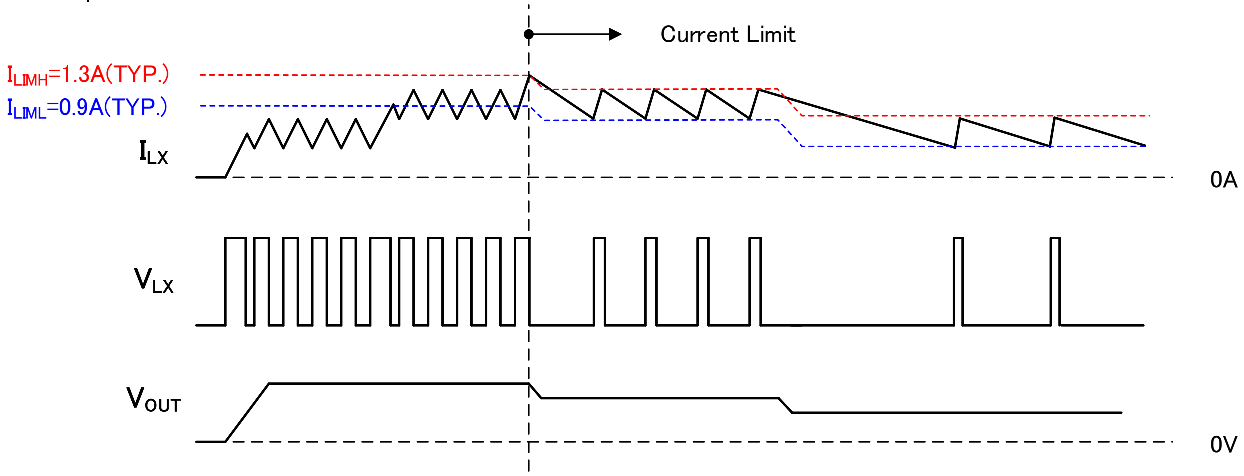
(1) High-side driver Tr. current limiting
The current in the High-side driver Tr. is detected to equivalently monitor the peak value of the coil current. The High-side driver Tr. current limiting function forcibly turns off the High-side driver Tr. when the peak value of the coil current reaches the High-side driver current limit value I_{LIMH}.

High-side driver Tr. current limit value I_{LIMH}=1.3A (TYP.)

(2) Low-side driver Tr. current limiting
The current in the Low-side driver Tr. is detected to equivalently monitor the bottom value of the coil current. The Low-side driver Tr. current limiting function operates when the High-side driver Tr. current limiting value reaches I_{LIMH}. The Low-side driver Tr. current limiting function prohibits the High-side driver Tr. from turning on in an over-current state where the bottom value of the coil current is higher than the Low-side driver Tr. current limit value I_{LIML}.

Low side driver Tr. current limit value I_{LIML}=0.9A (TYP.)

The current foldback circuit operates control to lower the switching frequency f_{OSC}. When the over-current state is released, normal operation resumes.



<Soft-start function>
The output voltage of XC9267 rises with soft start by slowly raising the reference voltage. The rise time of this reference voltage is the soft start time. The soft-start time is set to 2.0ms (TYP.) which is fixed internally or to the time set by adding a capacitor and a resistor to the EN / SS pin whichever is later.

<Thermal shutdown>
The thermal shutdown (TSD) as an over temperature limit is built in the XC9267 series.
When the junction temperature reaches the detection temperature, the driver transistor is forcibly turned off. When the junction temperature falls to the release temperature while in the output stop state, restart takes place by soft-start.

<UVLO>
When the V_{IN} pin voltage falls below 2.7V (TYP.), the driver transistor is forcibly turned off to prevent false pulse output due to instable operation of the internal circuits. When the V_{IN} pin voltage rises above 2.8V (TYP.), the UVLO function is released, the soft-start function activates, and output start operation begins. Stopping by UVLO is not shutdown; only pulse output is stopped and the internal circuits continue to operate.

<Power good>
On USP-6C Package, the output state can be monitored using the power good function. When the FB voltage drops below 90% (TYP.), the PG pin outputs an "L" signal. The PG pin is an Nch open drain output, therefore a pull-up resistance (approx. 100kΩ) must be connected to the PG pin.

■NOTE ON USE

1) For the phenomenon of temporal and transitional voltage decrease or voltage increase, the IC may be damaged or deteriorated if IC is used beyond the absolute MAX. specifications.

2) Make sure that the absolute maximum ratings of the external components and of this IC are not exceeded.

3) The DC/DC converter characteristics depend greatly on the externally connected components as well as on the characteristics of this IC, so refer to the specifications and standard circuit examples of each component when carefully considering which components to select.
Be especially careful of the capacitor characteristics and use X7R or X5R (EIA standard) ceramic capacitors.
The capacitance decrease caused by the bias voltage may become remarkable depending on the external size of the capacitor.

4) The DC/DC converter of this IC uses a current-limiting circuit to monitor the coil peak current. If the potential dropout voltage is large or the load current is large, the peak current will increase, which makes it easier for current limitation to be applied which in turn could cause the operation to become unstable. When the peak current becomes large, adjust the coil inductance and sufficiently check the operation.

The following formula is used to show the peak current.
Peak Current: $I_{pk} = (V_{IN} - V_{OUT}) \times V_{OUT} / V_{IN} / (2 \times L \times f_{OSC}) + I_{OUT}$

L: Coil Inductance [H]
f_{OSC}: Oscillation Frequency [Hz]
I_{OUT}: Load Current [A]

5) If there is a large dropout voltage, a circuit delay could create the ramp-up of coil current with staircase waveform exceeding the current limit.

6) Even in the PWM control, the intermittent operation occurs and the ripple voltage becomes higher, when the minimum On Time is faster than 85ns (typ.) as well as the dropout voltage is large and output current is small.

7) The ripple voltage could be increased when switching from discontinuous conduction mode to continuous conduction mode and at switching to 100% Duty cycle. Please evaluate IC well on customer's PCB.

8) If the voltage at the EN/SS Pin does not start from 0V but it is at the midpoint potential when the power is switched on, the soft start function may not work properly and it may cause the larger inrush current and bigger ripple voltages.

9) Torex places an importance on improving our products and their reliability. We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems.

■NOTE ON USE(Continued)

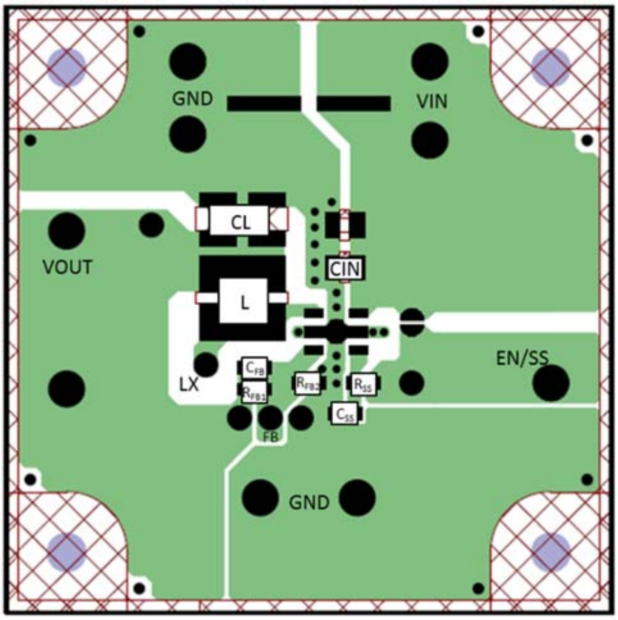
10) Instructions of pattern layouts

The operation may become unstable due to noise and/or phase lag from the output current when the wire impedance is high, please place the input capacitor(C_{IN}) and the output capacitor (C_L) as close to the IC as possible.

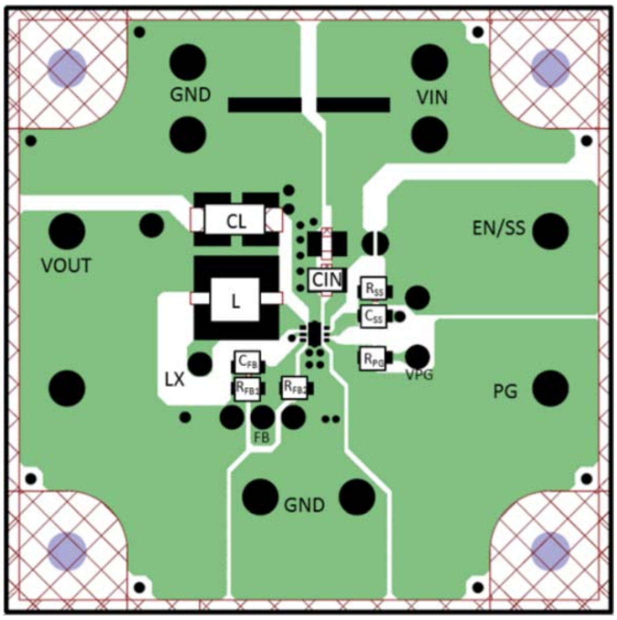
(1) In order to stabilize V_{IN} voltage level, we recommend that a by-pass capacitor (C_{IN}) be connected as close as possible to the V_{IN} and GND pins.
(2) Please mount each external component as close to the IC as possible.
(3) Wire external components as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.
(4) Make sure that the GND traces are as thick as possible, as variations in ground potential caused by high ground currents at the time of switching may result in instability of the IC.
(5) Please note that internal driver transistors bring on heat because of the load current and ON resistance of Highside driver transistor, Lowside driver transistor. Please make sure that the heat is dissipated properly, especially at higher temperatures.

<Reference Pattern Layout>

SOT-89-5



USP-6C

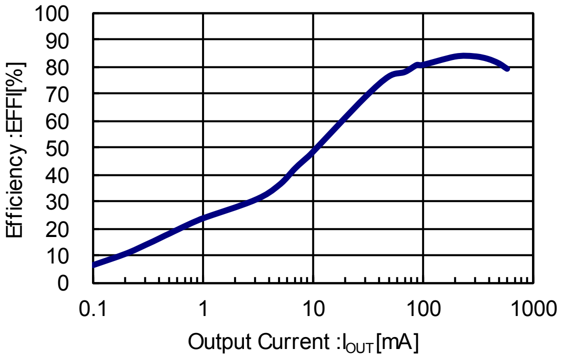


■TYPICAL PERFORMANCE CHARACTERISTICS

(1) Efficiency vs. Output Current

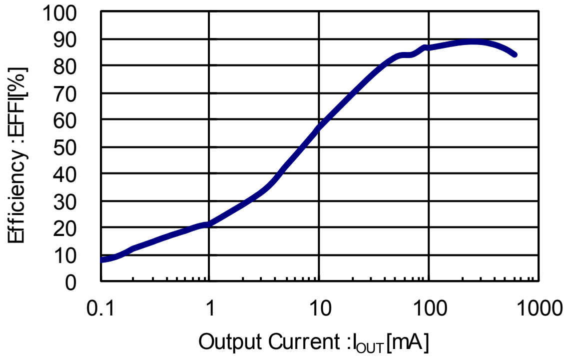
XC9267B75Cxx
(V_{IN}=12V, V_{OUT}=3.3V, f_{OSC}=1.2MHz)

L=4.7μH(CLF5030NIT-4R7), C_{IN}=4.7μF×2(C2012X6S1H475K)
C_L=10μF×2 (C3216X7R1E106K)



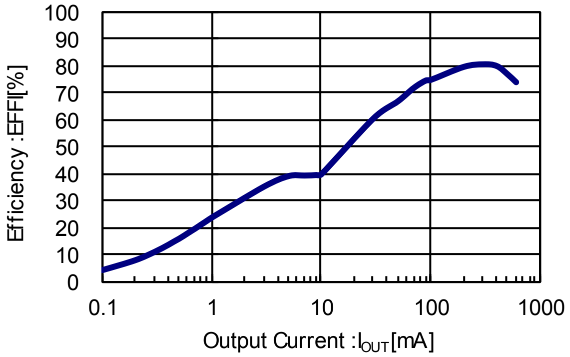
XC9267B75Cxx
(V_{IN}=12V, V_{OUT}=5V, f_{OSC}=1.2MHz)

L=6.8μH(CLF5030NIT-6R8), C_{IN}=4.7μF×2(C2012X6S1H475K)
C_L=10μF×2 (C3216X7R1E106K)



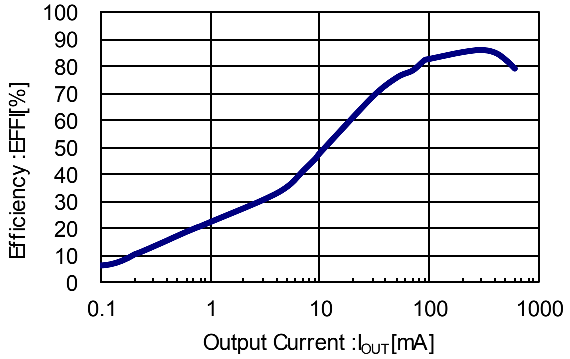
XC9267B75Dxx
(V_{IN}=12V, V_{OUT}=3.3V, f_{OSC}=2.2MHz)

L=2.2μH(CLF5030NIT-2R2), C_{IN}=2.2μF×2(C2012X7R1H225K)
C_L=10μF × 2 (C3216X7R1E106K)



XC9267B75Dxx
(V_{IN}=12V, V_{OUT}=5V, f_{OSC}=2.2MHz)

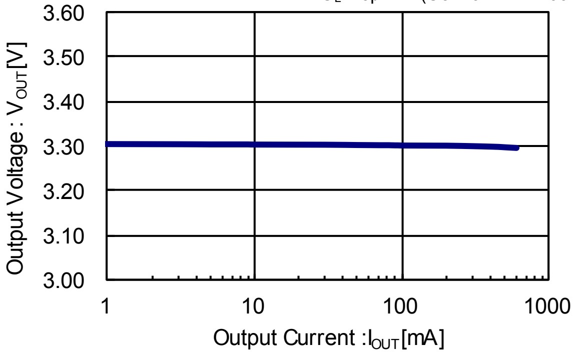
L=3.3μH(CLF5030NIT-3R3), C_{IN}=2.2μF×2(C2012X7R1H225K)
C_L=10μF×2 (C3216X7R1E106K)



(2) Output Voltage vs. Output Current

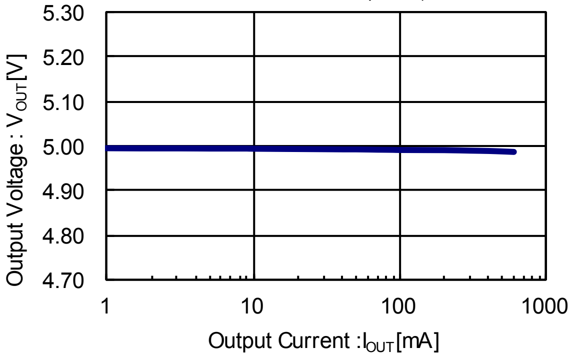
XC9267B75Cxx
(V_{IN}=12V, V_{OUT}=3.3V, f_{OSC}=1.2MHz)

L=4.7μH(CLF5030NIT-4R7), C_{IN}=4.7μF×2(C2012X6S1H475K)
C_L=10μF×2 (C3216X7R1E106K)



XC9267B75Cxx
(V_{IN}=12V, V_{OUT}=5V, f_{OSC}=1.2MHz)

L=6.8μH(CLF5030NIT-6R8), C_{IN}=4.7μF×2(C2012X6S1H475K)
C_L=10μF×2 (C3216X7R1E106K)

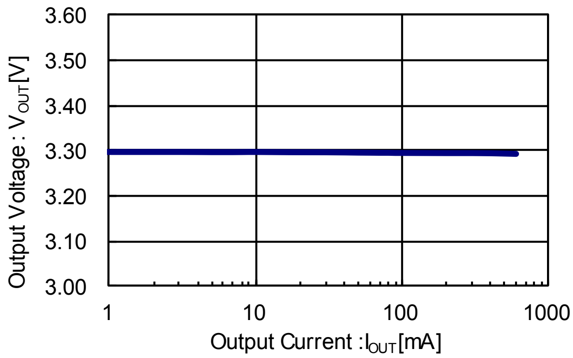


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(2) Output Voltage vs. Output Current

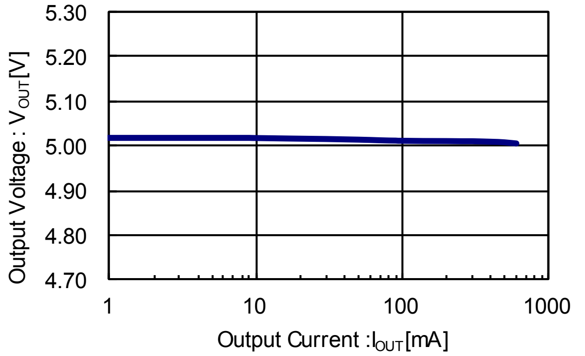
XC9267B75Dxx
(V_{IN}=12V, V_{OUT}=3.3V, f_{OSC}=2.2MHz)

L=2.2μH(CLF5030NIT-2R2), C_{IN}=2.2μF×2(C2012X7R1H225K)
C_L=10μF×2 (C3216X7R1E106K)



XC9267B75Dxx
(V_{IN}=12V, V_{OUT}=5V, f_{OSC}=2.2MHz)

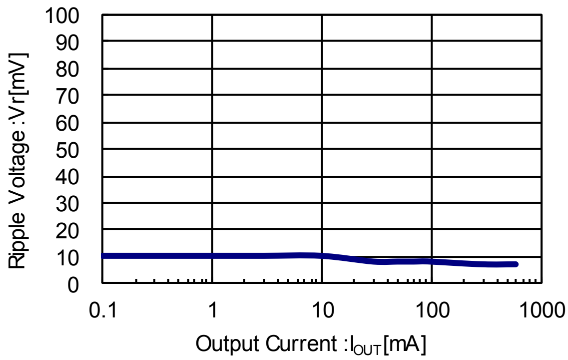
L=3.3μH(CLF5030NIT-3R3), C_{IN}=2.2μF×2(C2012X7R1H225K)
C_L=10μF×2 (C3216X7R1E106K)



(3) Ripple Voltage vs. Output Current

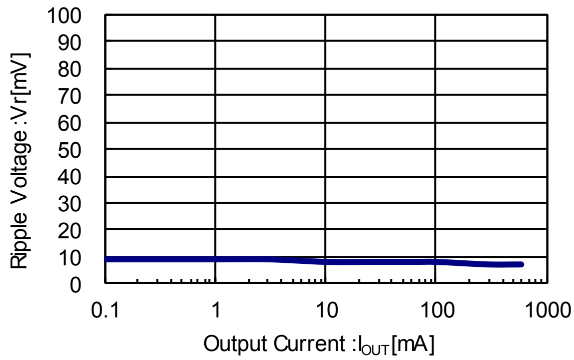
XC9267B75Cxx
(V_{IN}=12V, V_{OUT}=5V, f_{OSC}=1.2MHz)

L=6.8μH(CLF5030NIT-6R8), C_{IN}=4.7μF×2(C2012X6S1H475K)
C_L=10μF×2 (C3216X7R1E106K)



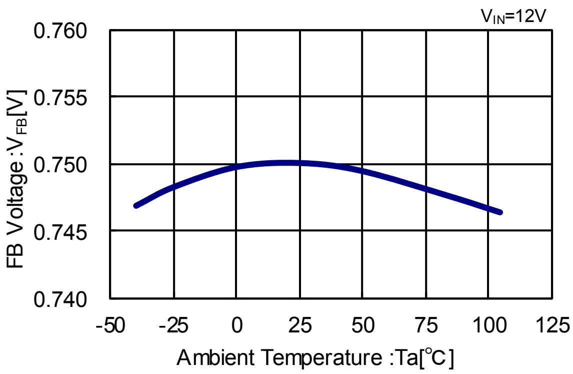
XC9267B75Dxx
(V_{IN}=12V, V_{OUT}=5V, f_{OSC}=2.2MHz)

L=3.3μH(CLF5030NIT-3R3), C_{IN}=2.2μF×2(C2012X7R1H225K)
C_L=10μF×2 (C3216X7R1E106K)



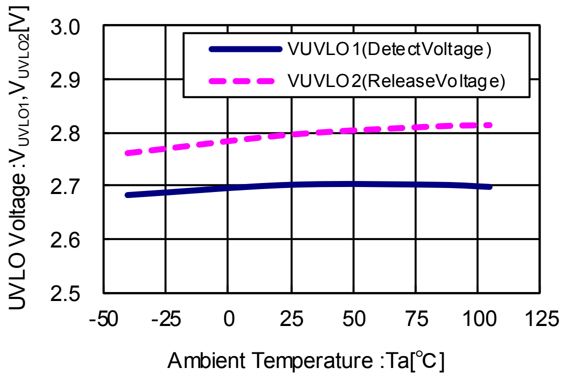
(4) FB Voltage vs. Ambient Temperature

XC9267B75xxx



(5) UVLO Voltage vs. Ambient Temperature

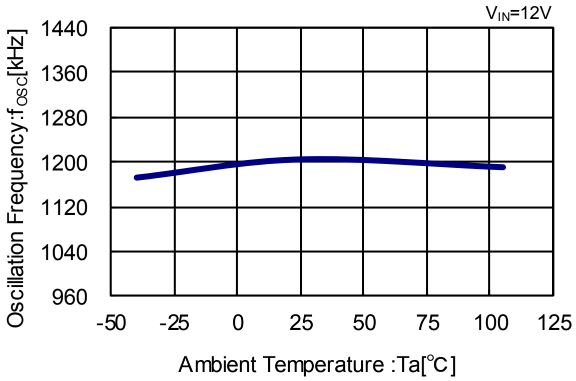
XC9267B75xxx



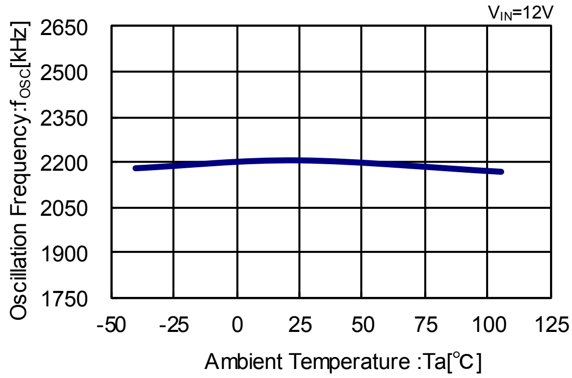
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(6) Oscillation Frequency vs. Ambient Temperature

XC9267B75Cxx
(f_{OSC}=1.2MHz)

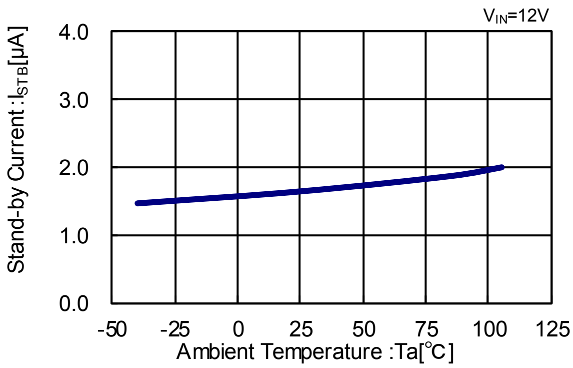


XC9267B75Dxx
(f_{OSC}=2.2MHz)



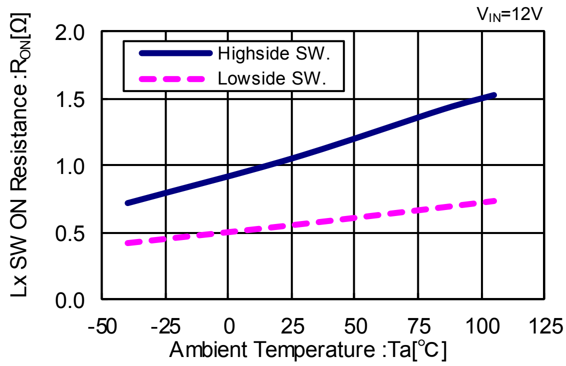
(7) Stand-by Current vs. Ambient Temperature

XC9267B75xxx



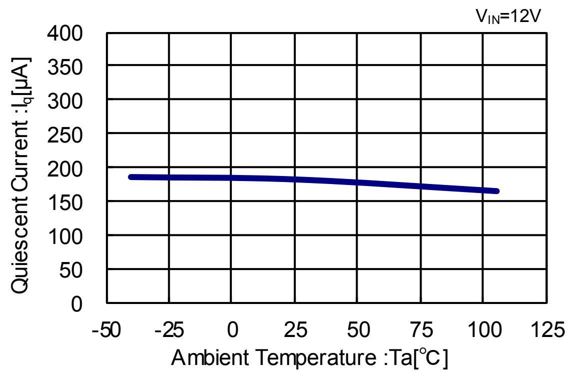
(8) Lx SW ON Resistance vs. Ambient Temperature

XC9267B75xxx

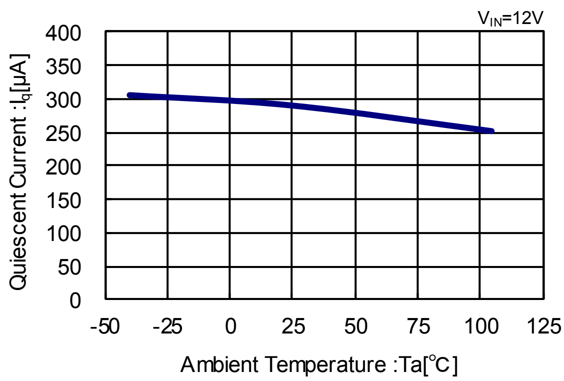


(9) Quiescent Current vs. Ambient Temperature

XC9267B75Cxx
(f_{OSC}=1.2MHz)

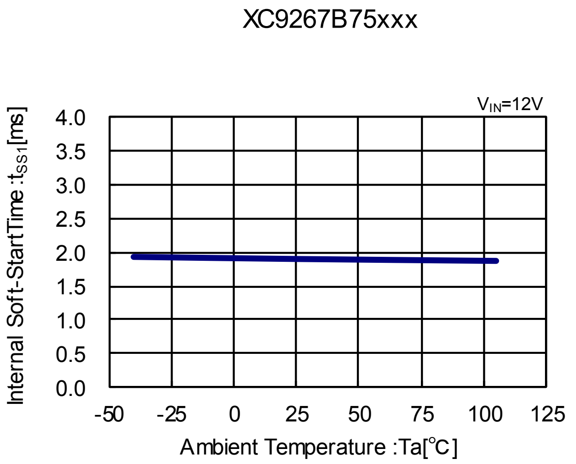


XC9267B75Dxx
(f_{OSC}=2.2MHz)

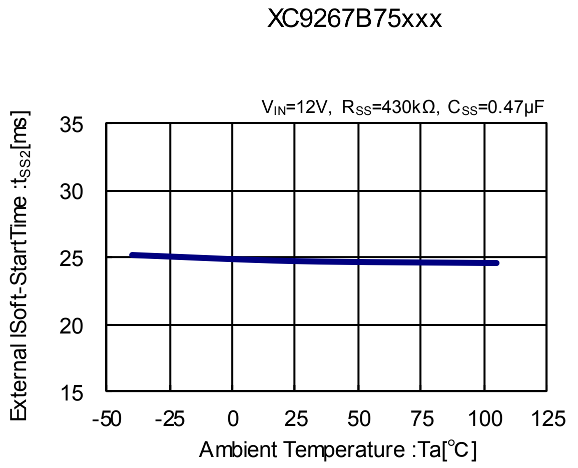


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

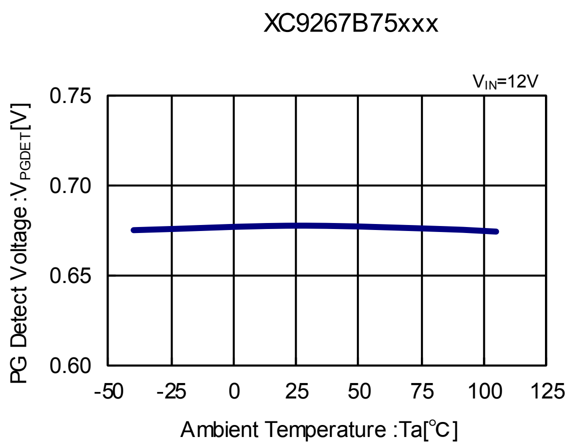
(10) Internal Soft-Start Time vs. Ambient Temperature



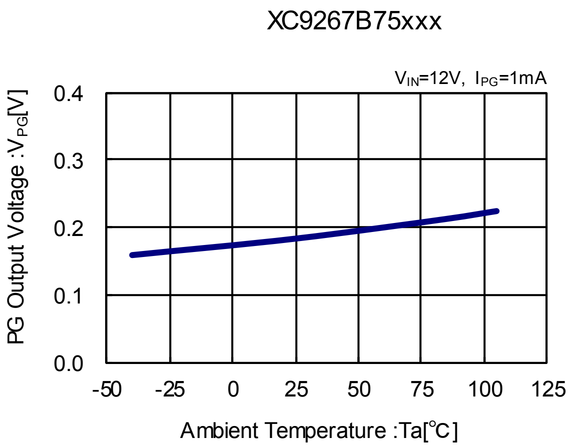
(11) External Soft-Start Time vs. Ambient Temperature



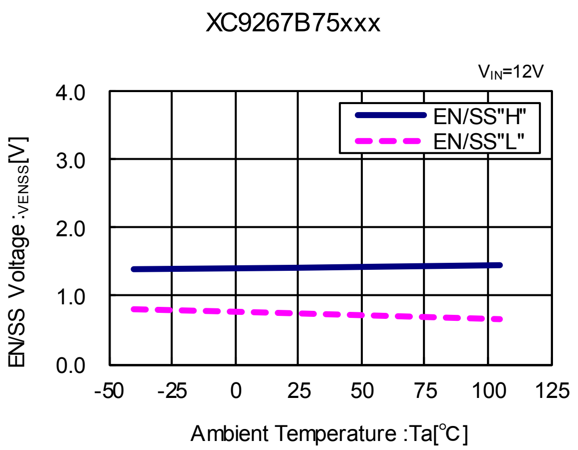
(12) PG Detect Voltage vs. Ambient Temperature



(13) PG Output Voltage vs. Ambient Temperature



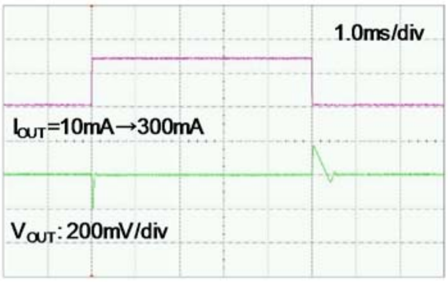
(14) EN/SS Voltage vs. Ambient Temperature



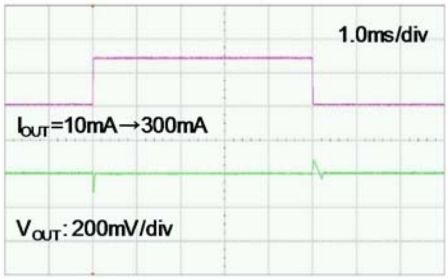
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(15) Load Transient Response

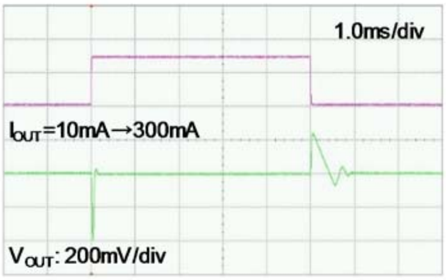
XC9267B75Cxx、f_{OSC}=1.2MHz
V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=10mA→300mA
L=4.7μH(CLF5030NIT-4R7), C_{IN}=4.7μF×2(C2012X6S1H475K)
C_L=10μF×2 (C3216X7R1E106K)



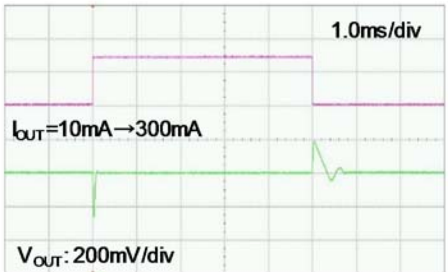
XC9267B75Cxx、f_{OSC}=1.2MHz
V_{IN}=24V, V_{OUT}=3.3V, I_{OUT}=10mA→300mA
L=4.7μH(CLF5030NIT-4R7), C_{IN}=4.7μF×2(C2012X6S1H475K)
C_L=10μF×2 (C3216X7R1E106K)



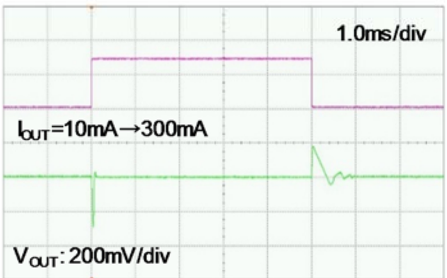
XC9267B75Cxx、f_{OSC}=1.2MHz
V_{IN}=12V, V_{OUT}=5.0V, I_{OUT}=10mA→300mA
L=6.8μH(CLF5030NIT-6R8), C_{IN}=4.7μF×2(C2012X6S1H475K)
C_L=10μF×2 (C3216X7R1E106K)



XC9267B75Cxx、f_{OSC}=1.2MHz
V_{IN}=24V, V_{OUT}=5.0V, I_{OUT}=10mA→300mA
L=6.8μH(CLF5030NIT-6R8), C_{IN}=4.7μF×2(C2012X6S1H475K)
C_L=10μF×2 (C3216X7R1E106K)



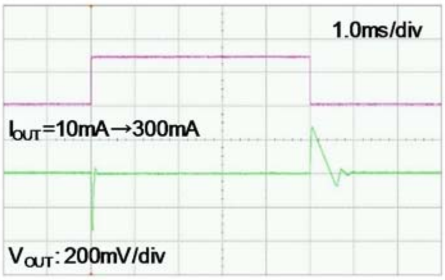
XC9267B75Dxx、f_{OSC}=2.2MHz
V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=10mA→300mA
L=2.2μH(CLF5030NIT-2R2), C_{IN}=2.2μF×2(C2012X7R1H225K)
C_L=10μF×2 (C3216X7R1E106K)



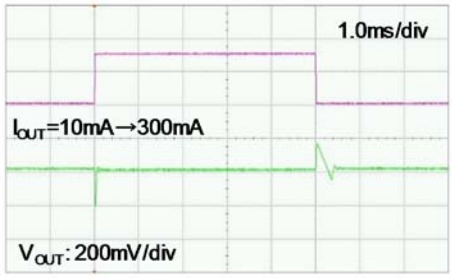
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(15) Load Transient Response

XC9267B75Dxx、f_{OSC}=2.2MHz
V_{IN}=12V, V_{OUT}=5.0V, I_{OUT}=10mA→300mA
L=3.3μH(CLF5030NIT-3R3), C_{IN}=2.2μF×2(C2012X7R1H225K)
C_L=10μF×2 (C3216X7R1E106K)

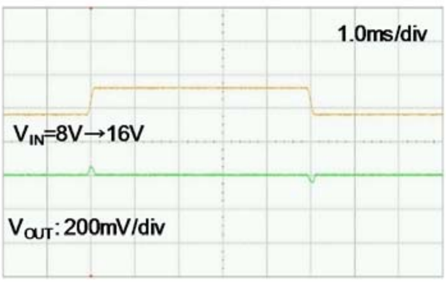


XC9267B75Dxx、f_{OSC}=2.2MHz
V_{IN}=24V, V_{OUT}=5.0V, I_{OUT}=10mA→300mA
L=3.3μH(CLF5030NIT-3R3), C_{IN}=2.2μF×2(C2012X7R1H225K)
C_L=10μF×2 (C3216X7R1E106K)



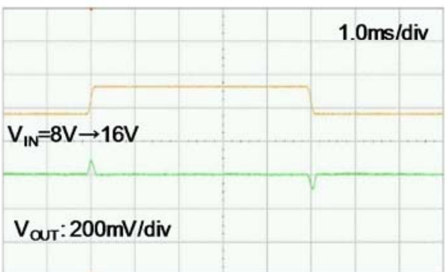
(16) Input Transient Response

XC9267B75Cxx、f_{OSC}=1.2MHz
V_{IN}=8V→16V, V_{OUT}=3.3V, I_{OUT}=300mA
L=4.7μH(CLF5030NIT-4R7), C_{IN}=4.7μF×2(C2012X6S1H475K)
C_L=10μF×2 (C3216X7R1E106K)



XC9267B75Cxx、f_{OSC}=1.2MHz
V_{IN}=16V→32V, V_{OUT}=3.3V, I_{OUT}=300mA
L=4.7μH(CLF5030NIT-4R7), C_{IN}=4.7μF×2(C2012X6S1H475K)
C_L=10μF×2 (C3216X7R1E106K)

XC9267B75Cxx、f_{OSC}=1.2MHz
V_{IN}=8V→16V, V_{OUT}=5.0V, I_{OUT}=300mA
L=6.8μH(CLF5030NIT-6R8), C_{IN}=4.7μF×2(C2012X6S1H475K)
C_L=10μF×2 (C3216X7R1E106K)



XC9267B75Cxx、f_{OSC}=1.2MHz
V_{IN}=16V→32V, V_{OUT}=5.0V, I_{OUT}=300mA
L=6.8μH(CLF5030NIT-6R8), C_{IN}=4.7μF×2(C2012X6S1H475K)
C_L=10μF×2 (C3216X7R1E106K)

■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(16) Input Transient Response

XC9267B75Dxx、f_{OSC}=2.2MHz

L=2.2μH(CLF5030NIT-2R2), C_{IN}=2.2μF×2(C2012X7R1H225K)
C_L=10μF×2 (C3216X7R1E106K)

XC9267B75Dxx、f_{OSC}=2.2MHz

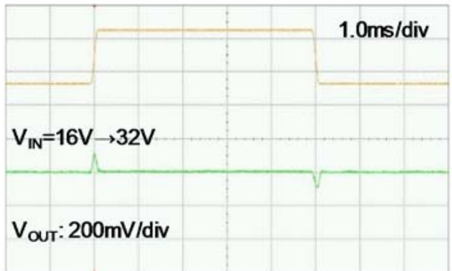
V_{IN}=8V→16V, V_{OUT}=5.0V, I_{OUT}=300mA

L=3.3μH(CLF5030NIT-3R3), C_{IN}=2.2μF×2(C2012X7R1H225K)
C_L=10μF×2 (C3216X7R1E106K)

XC9267B75Dxx、f_{OSC}=2.2MHz

V_{IN}=16V→32V, V_{OUT}=5.0V, I_{OUT}=300mA

L=3.3μH(CLF5030NIT-3R3), C_{IN}=2.2μF×2(C2012X7R1H225K)
C_L=10μF×2 (C3216X7R1E106K)

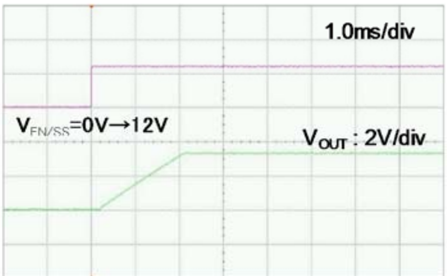


(17) EN/SS Rising Response

XC9267B75Cxx、f_{OSC}=1.2MHz

V_{IN}=12V, V_{ENSS}=0→12V, V_{OUT}=3.3V, I_{OUT}=300mA

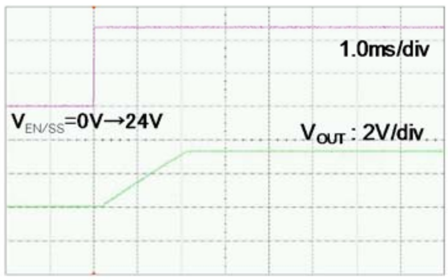
L=4.7μH(CLF5030NIT-4R7), C_{IN}=4.7μF×2(C2012X6S1H475K)
C_L=10μF×2 (C3216X7R1E106K)



XC9267B75Cxx、f_{OSC}=1.2MHz

V_{IN}=24V, V_{ENSS}=0→24V, V_{OUT}=3.3V, I_{OUT}=300mA

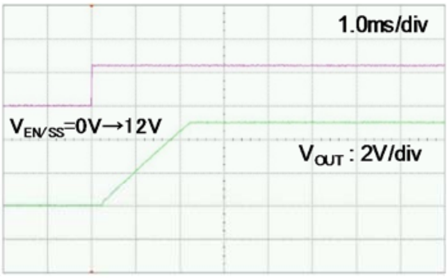
L=4.7μH(CLF5030NIT-4R7), C_{IN}=4.7μF×2(C2012X6S1H475K)
C_L=10μF×2 (C3216X7R1E106K)



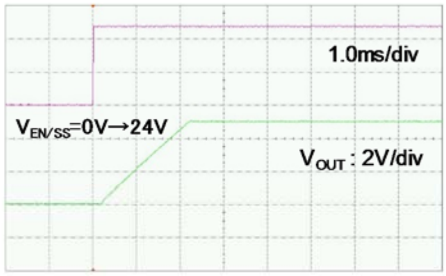
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(17) EN/SS Rising Response

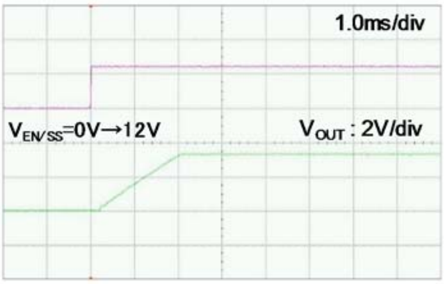
XC9267B75Cxx、f_{OSC}=1.2MHz
V_{IN}=12V, V_{ENSS}=0→12V, V_{OUT}=5V, I_{OUT}=300mA
L=6.8μH(CLF5030NIT-6R8), C_{IN}=4.7μF×2(C2012X6S1H475K)
C_L=10μF×2 (C3216X7R1E106K)



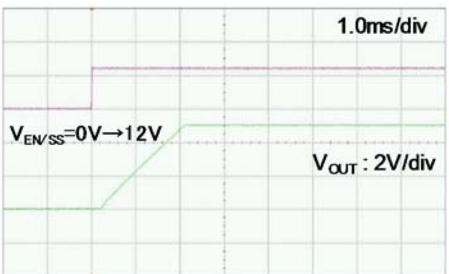
XC9267B75Cxx、f_{OSC}=1.2MHz
V_{IN}=24V, V_{ENSS}=0→24V, V_{OUT}=5V, I_{OUT}=300mA
L=6.8μH(CLF5030NIT-6R8), C_{IN}=4.7μF×2(C2012X6S1H475K)
C_L=10μF×2 (C3216X7R1E106K)



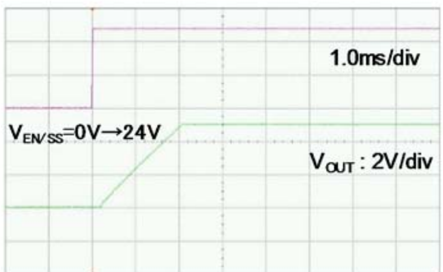
XC9267B75Dxx、f_{OSC}=2.2MHz
V_{IN}=12V, V_{ENSS}=0→12V, V_{OUT}=3.3V, I_{OUT}=300mA
L=2.2μH(CLF5030NIT-2R2), C_{IN}=2.2μF×2(C2012X7R1H225K)
C_L=10μF×2 (C3216X7R1E106K)



XC9267B75Dxx、f_{OSC}=2.2MHz
V_{IN}=12V, V_{ENSS}=0→12V, V_{OUT}=5V, I_{OUT}=300mA
L=3.3μH(CLF5030NIT-3R3), C_{IN}=2.2μF×2(C2012X7R1H225K)
C_L=10μF×2 (C3216X7R1E106K)



XC9267B75Dxx、f_{OSC}=2.2MHz
V_{IN}=24V, V_{ENSS}=0→24V, V_{OUT}=5V, I_{OUT}=300mA
L=3.3μH(CLF5030NIT-3R3), C_{IN}=2.2μF×2(C2012X7R1H225K)
C_L=10μF×2 (C3216X7R1E106K)



■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

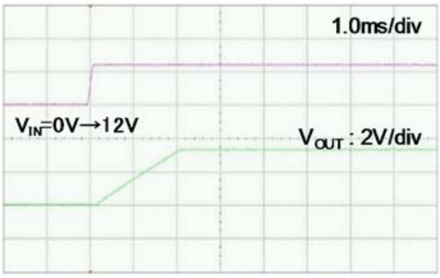
(18) VIN Rising Response

XC9267B75Cxx、f_{OSC}=1.2MHz

V_{IN}=0→12V, V_{ENSS}=0→12V, V_{OUT}=3.3V, I_{OUT}=300mA

L=4.7μH(CLF5030NIT-4R7), C_{IN}=4.7μF×2(C2012X6S1H475K)

C_L=10μF×2 (C3216X7R1E106K)

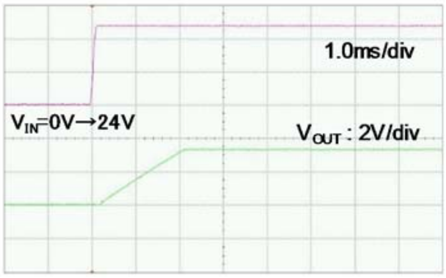


XC9267B75Cxx、f_{OSC}=1.2MHz

V_{IN}=0→24V, V_{ENSS}=0→24V, V_{OUT}=3.3V, I_{OUT}=300mA

L=4.7μH(CLF5030NIT-4R7), C_{IN}=4.7μF×2(C2012X6S1H475K)

C_L=10μF×2 (C3216X7R1E106K)

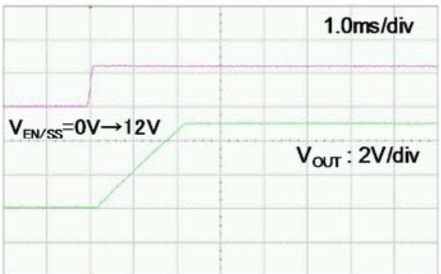


XC9267B75Cxx、f_{OSC}=1.2MHz

V_{IN}=0→12V, V_{ENSS}=0→12V, V_{OUT}=5V, I_{OUT}=300mA

L=6.8μH(CLF5030NIT-6R8), C_{IN}=4.7μF×2(C2012X6S1H475K)

C_L=10μF×2 (C3216X7R1E106K)

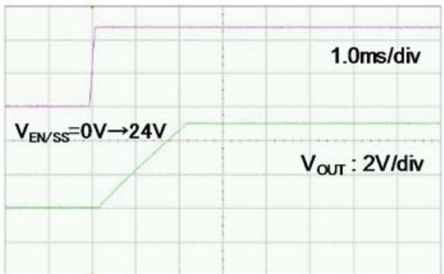


XC9267B75Cxx、f_{OSC}=1.2MHz

V_{IN}=0→24V, V_{ENSS}=0→24V, V_{OUT}=5V, I_{OUT}=300mA

L=6.8μH(CLF5030NIT-6R8), C_{IN}=4.7μF×2(C2012X6S1H475K)

C_L=10μF×2 (C3216X7R1E106K)

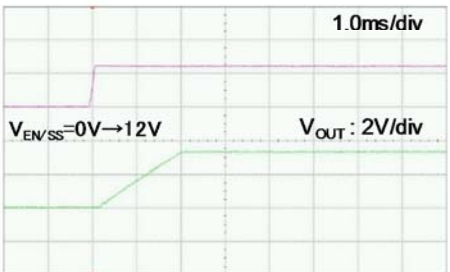


XC9267B75Dxx、f_{OSC}=2.2MHz

V_{IN}=0→12V, V_{ENSS}=0→12V, V_{OUT}=3.3V, I_{OUT}=300mA

L=2.2μH(CLF5030NIT-2R2), C_{IN}=2.2μF×2(C2012X7R1H225K)

C_L=10μF×2 (C3216X7R1E106K)



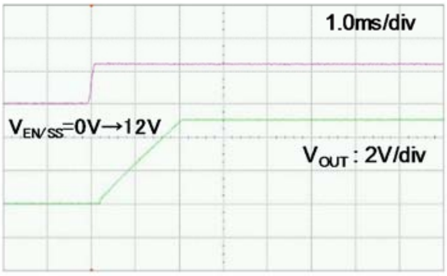
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(18) VIN Rising Response

XC9267x75D、f_{OSC}=2.2MHz

V_{IN}=0→12V, V_{ENSS}=0→12V, V_{OUT}=5V, I_{OUT}=300mA

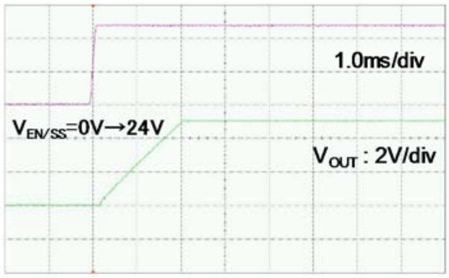
L=3.3μH(CLF5030NIT-3R3N-D), C_{IN}=2.2μF×2(C2012X7R1H225K)
C_L=10μF×2 (C3216X7R1E106K)



XC9267B75Dxx、f_{OSC}=2.2MHz

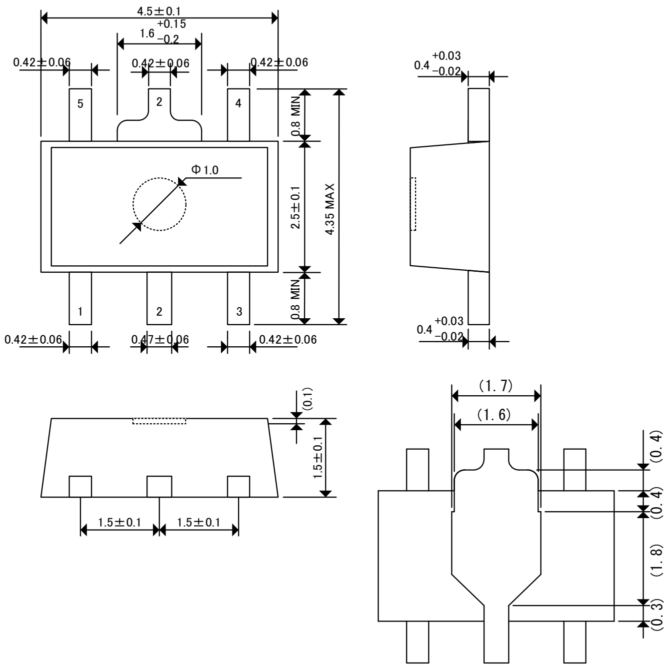
V_{IN}=0→24V, V_{ENSS}=0→24V, V_{OUT}=5V, I_{OUT}=300mA

L=3.3μH(CLF5030NIT-3R3N-D), C_{IN}=2.2μF×2(C2012X7R1H225K)
C_L=10μF×2 (C3216X7R1E106K)

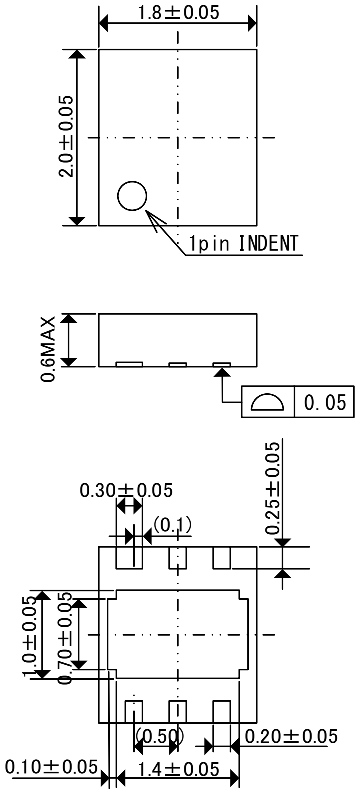


■PACKAGING INFORMATION

●SOT-89-5(unit : mm)

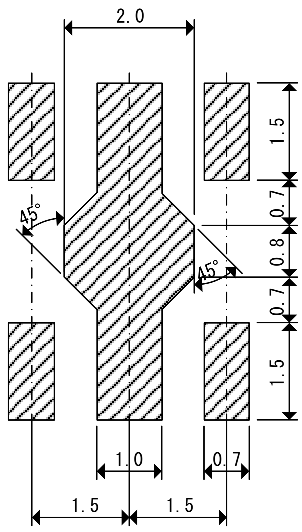


●USP-6C (unit:mm)

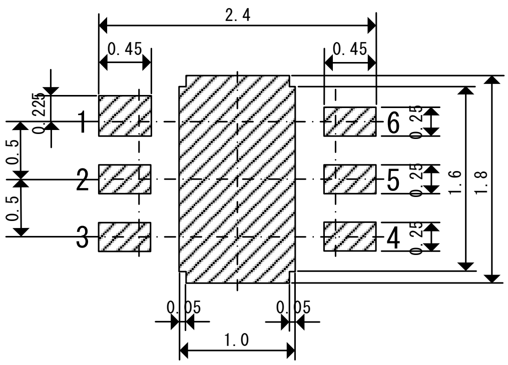


■PACKAGING INFORMATION (Continued)

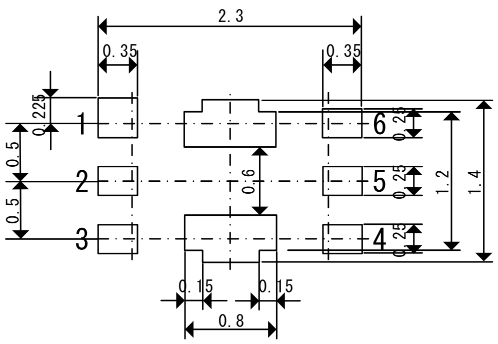
●SOT-89-5 Reference Pattern Layout (unit: mm)



●USP-6C Reference Pattern Layout (unit: mm)



●USP-6C Reference Metal Mask Design (unit: mm)

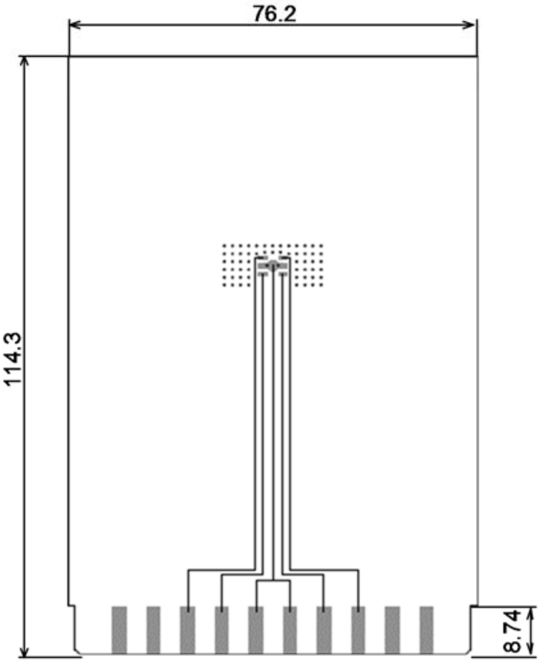


●SOT-89-5 Power Dissipation (JEDEC)

Power dissipation data for the SOT-89-5 is shown in this page.
The value of power dissipation varies with the mount board conditions.
Please use this data as one of reference data taken in the described condition.

1. Measurement Condition (Reference data)

Condition : Mount on a board
Ambient : Natural convection
Soldering : Lead (Pb) free
Board : The board using 4 copper layer.
(76.2mm×114.3mm･･･Area: about 8700mm^2)
1st layer : No copper foil (Signal layer)
2nd layer : 70mm×70mm_Connected to heat-sink.
3rd layer : 70mm×70mm_Connected to heat-sink.
4th layer : No copper foil (Signal layer)
Material : Glass Epoxy (FR-4)
Thickness : 1.6mm
Through-hole : φ0.2mm x 60pcs

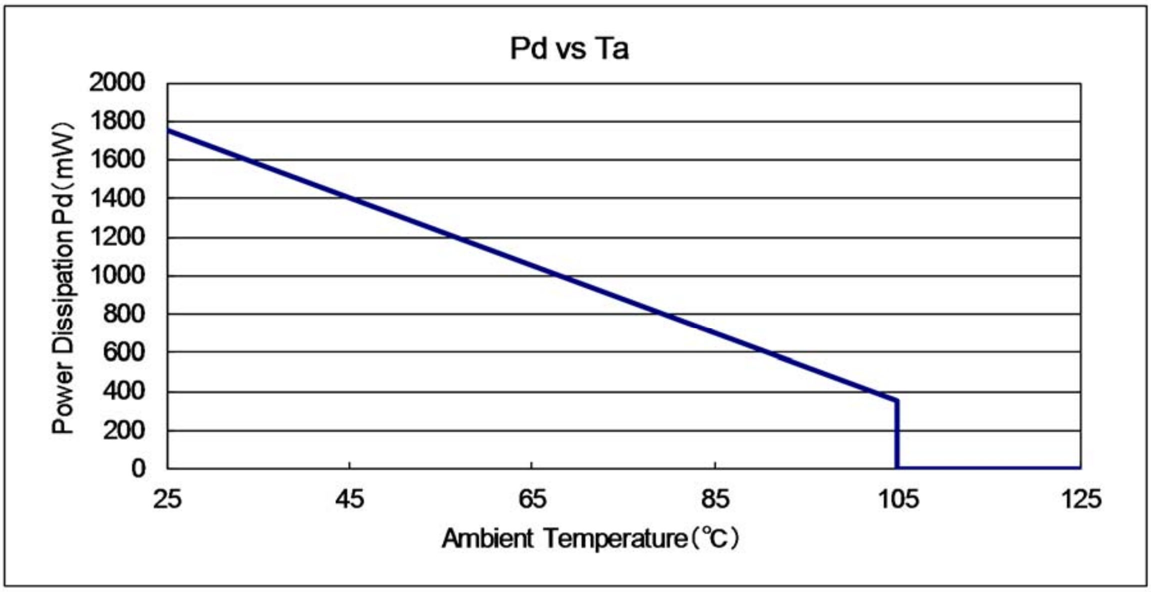


Evaluation Board (Unit: mm)

2.Power Dissipation vs. Ambient Temperature

Board Mount (Tj max = 125℃)

Ambient Temperature (℃)	Power Dissipation Pd (mW)	Thermal Resistance (℃/W)
25	1750	57.14
105	350	

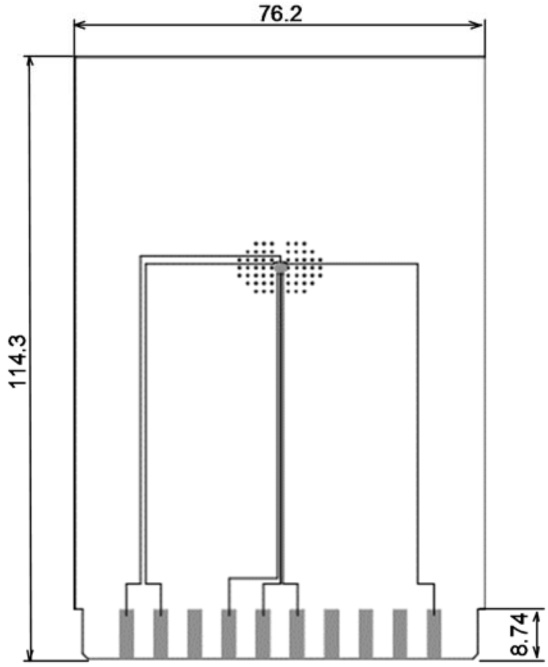


●USP-6C(Insulation Paste/DAF) Power Dissipation (JEDEC)

Power dissipation data for the USP-6C(Insulation Paste/DAF) is shown in this page.
The value of power dissipation varies with the mount board conditions.
Please use this data as one of reference data taken in the described condition.

1. Measurement Condition (Reference data)

Condition : Mount on a board
Ambient : Natural convection
Soldering : Lead (Pb) free
Board : The board using 4 copper layer.
(76.2mm×114.3mm･･･Area: about 8700mm^2)
1st layer : No copper foil (Signal layer)
2nd layer : 70mm×70mm_Connected to heat-sink.
3rd layer : 70mm×70mm_Connected to heat-sink.
4th layer : No copper foil (Signal layer)
Material : Glass Epoxy (FR-4)
Thickness : 1.6mm
Through-hole : φ0.2mm x 60pcs

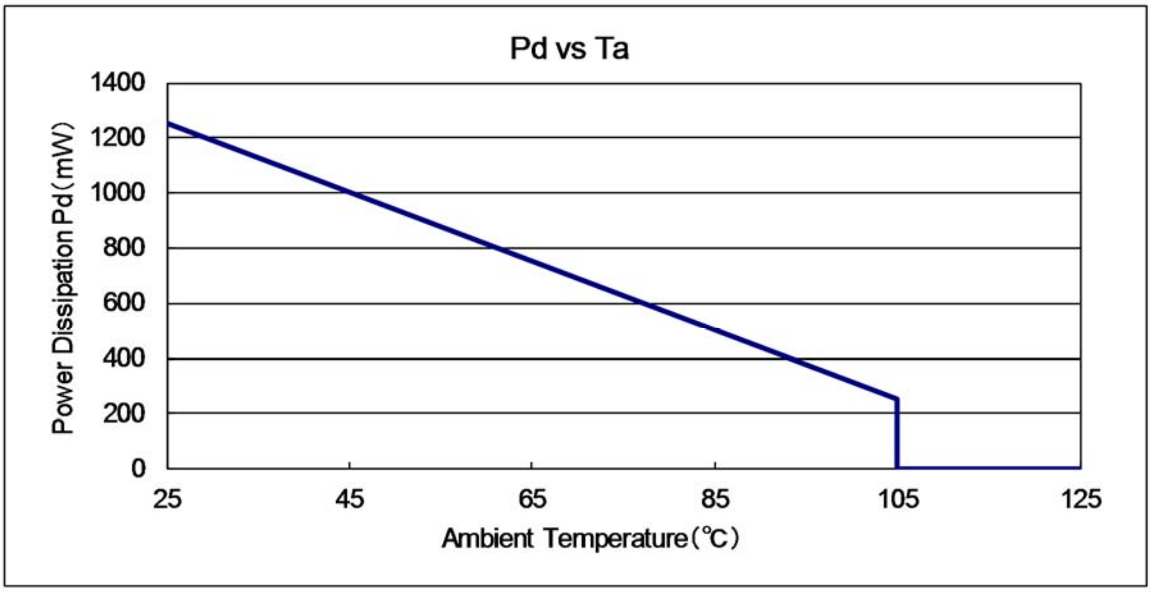


Evaluation Board (Unit: mm)

2.Power Dissipation vs. Ambient Temperature

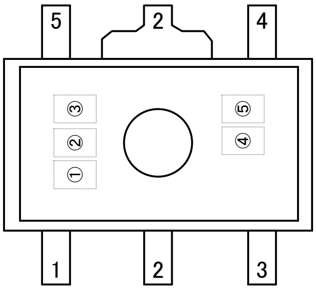
Board Mount (Tj max = 125℃)

Ambient Temperature (℃)	Power Dissipation Pd (mW)	Thermal Resistance (℃/W)
25	1250	80.00
105	250	

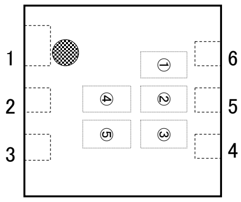


■MARKING RULE

●SOT-89-5



●USP-6C(Under dot)



①② represents product series、products type,

MARK		PRODUCT SERIES
①	②	
5	1	XC9267B75***-G

※USP-6C Under dot

③ represents Oscillation Frequency

MARK	Oscillation Frequency	PRODUCT SERIES
N	1.2MHz	XC9267B75C**-G
U	2.2MHz	XC9267B75D**-G

④⑤ represents production lot number
01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ, B1～ZZ repeated
(G, I, J, O, Q, W excluded)* No character inversion used.

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.

2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.

3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.

4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions. Do not use the product for the above use unless agreed by us in writing in advance.

5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.

6. Our products are not designed to be Radiation-resistant.

7. Please use the product listed in this datasheet within the specified ranges.

8. We assume no responsibility for damage or loss due to abnormal use.

9.

TOREX SEMICONDUCTOR LTD.