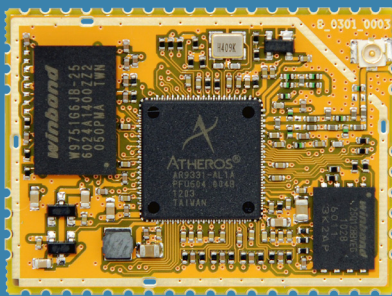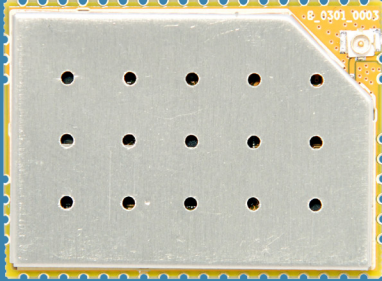# Carambola 2

8devices Carambola 2 is a member of Carambola wireless modules family and is based on Qualcomm/Atheros AR9331 SoC.
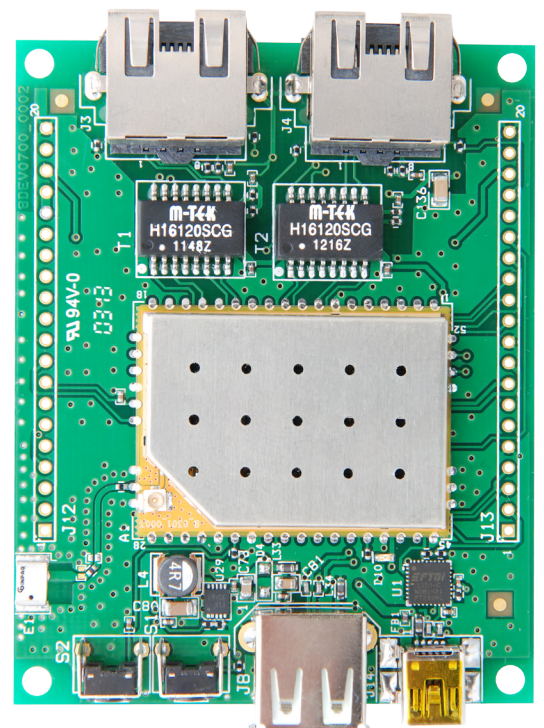
Carambola 2 is a surface mountable, single sided, Wi-Fi enabled Linux module, featuring the lowest power consumption in the industry.

Module comes bundled with an open source development board for a quick start of your new Internet of Things era project.

8devices is providing OpenWRT linux distribution source code with necessary patches on GitHub *https://github.com/8devices* and is supported by our growing community on *http://www.8devices.com/community* forum.
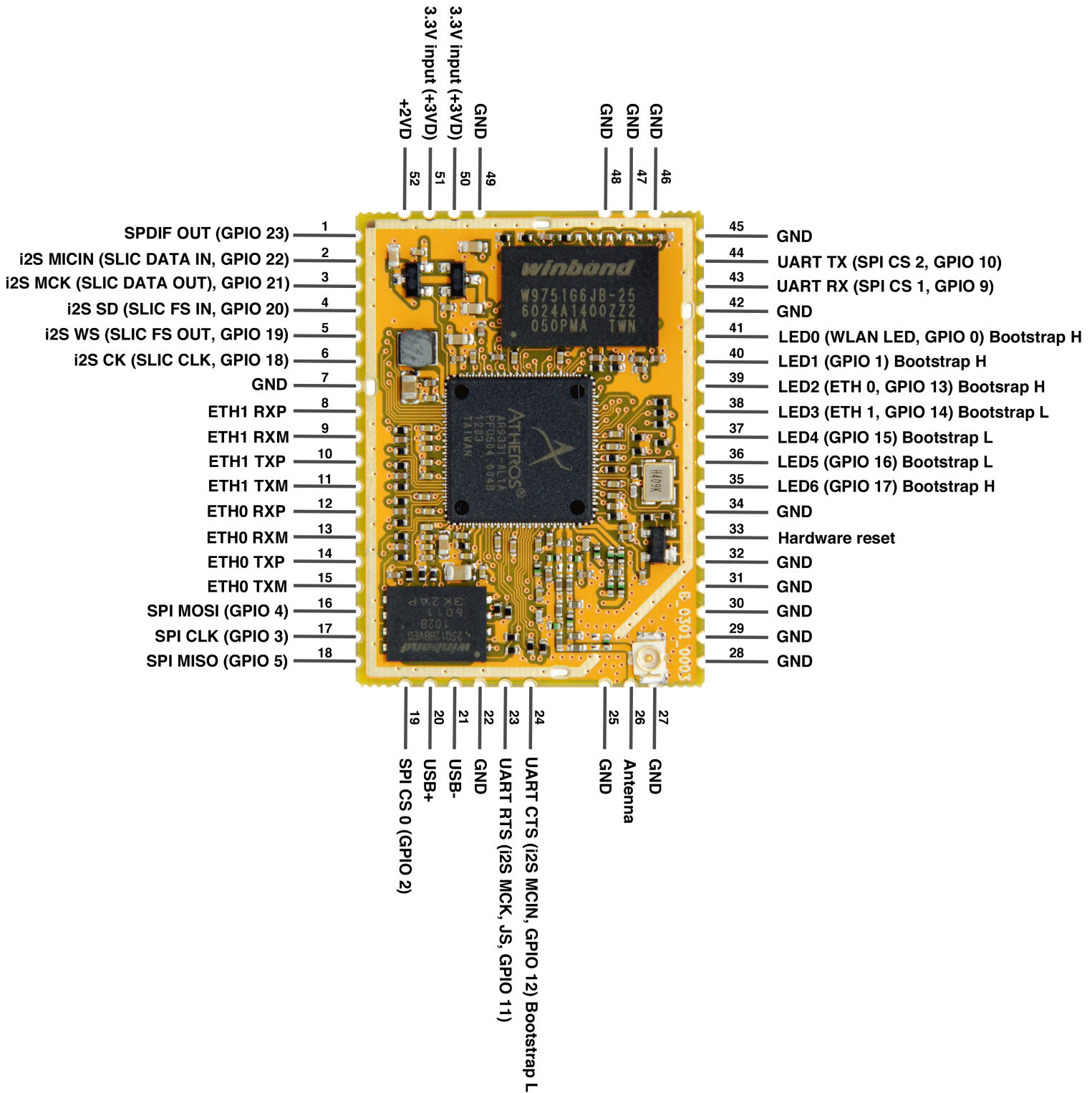
Quick specs

- 802.11 b/g/n, 2.4 GHz, 1x1 SISO, 150MBps max data rate, 21 dB output power
- U.FL connector or external pin for external antenna
- 16 MB FLASH, 64 MB DDR2 RAM
- Linux friendly , OpenWRT flash image and source code are available for download on www.8devices.com/wiki_carambola
- CPU – AR9331, 400 MHz clock speed
- 28 by 38 mm Size – small and easy to embed
- Surface mountable
- Power supply - 3.3 V, power consumption 0.5 W
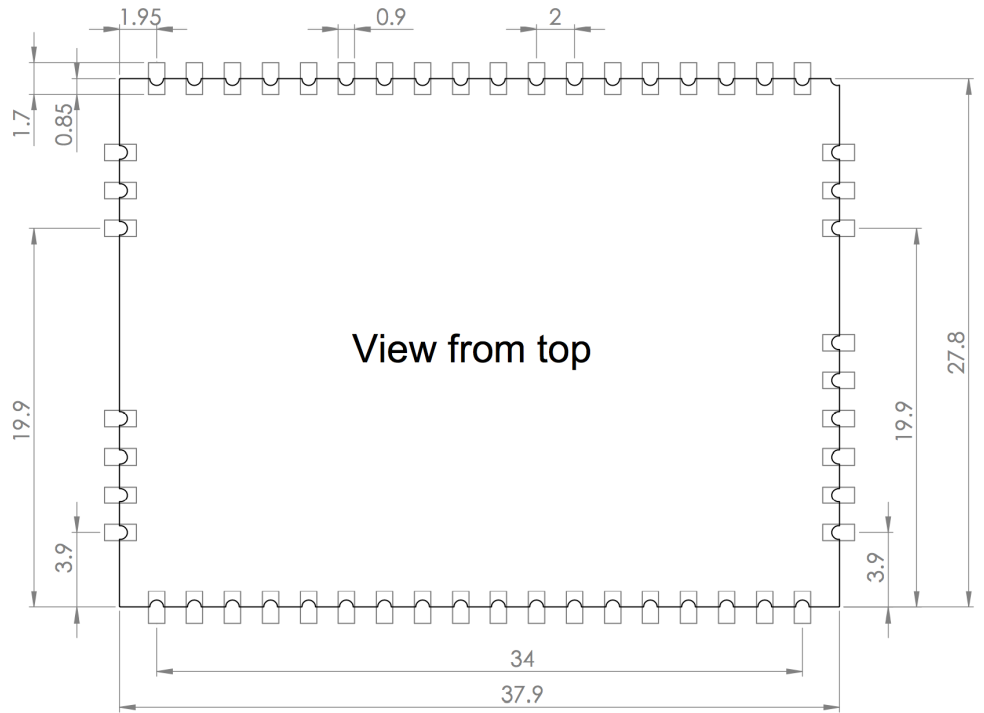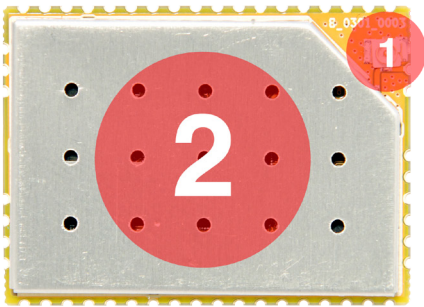- Available interfaces - USB host/slave, serial port, 2 x Ethernet, i2S, SLIC, SPDIF, 23 x GPIO
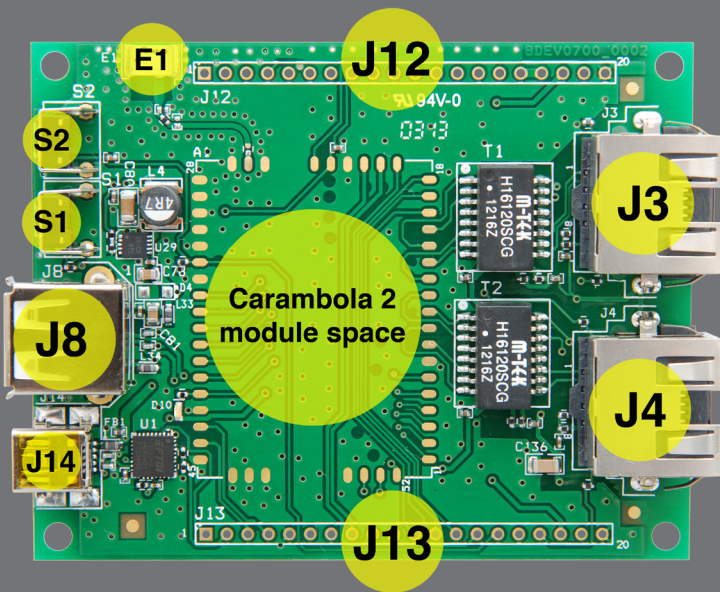
Pinout information

Top pins (left to right): +2VD (52), 3.3V input (+3VD) (51), 3.3V input (+3VD) (50), GND (49), GND (48), GND (47), GND (46)

Left side pins:
- 1 — SPDIF OUT (GPIO 23)
- 2 — i2S MICIN (SLIC DATA IN, GPIO 22)
- 3 — i2S MCK (SLIC DATA OUT), GPIO 21)
- 4 — i2S SD (SLIC FS IN, GPIO 20)
- 5 — i2S WS (SLIC FS OUT, GPIO 19)
- 6 — i2S CK (SLIC CLK, GPIO 18)
- 7 — GND
- 8 — ETH1 RXP
- 9 — ETH1 RXM
- 10 — ETH1 TXP
- 11 — ETH1 TXM
- 12 — ETH0 RXP
- 13 — ETH0 RXM
- 14 — ETH0 TXP
- 15 — ETH0 TXM
- 16 — SPI MOSI (GPIO 4)
- 17 — SPI CLK (GPIO 3)
- 18 — SPI MISO (GPIO 5)

Right side pins:
- 45 — GND
- 44 — UART TX (SPI CS 2, GPIO 10)
- 43 — UART RX (SPI CS 1, GPIO 9)
- 42 — GND
- 41 — LED0 (WLAN LED, GPIO 0) Bootstrap H
- 40 — LED1 (GPIO 1) Bootstrap H
- 39 — LED2 (ETH 0, GPIO 13) Bootsrap H
- 38 — LED3 (ETH 1, GPIO 14) Bootstrap L
- 37 — LED4 (GPIO 15) Bootstrap L
- 36 — LED5 (GPIO 16) Bootstrap L
- 35 — LED6 (GPIO 17) Bootstrap H
- 34 — GND
- 33 — Hardware reset
- 32 — GND
- 31 — GND
- 30 — GND
- 29 — GND
- 28 — GND

Bottom pins (left to right): SPI CS 0 (GPIO 2) (19), USB+ (20), USB- (21), GND (22), UART RTS (i2S MCK, JS, GPIO 11) (23), UART CTS (i2S MCIN, GPIO 12) Bootstrap L (24), GND (25), Antenna (26), GND (27)

Carambola 2 details

1) Male UFL connector for external antenna

2) RF shield

View from top

1.95 0.9 2
1.7 0.85
19.9 27.8
19.9
3.9 3.9
34
37.9

Carambola 2 development board

Carambola 2 module space

E1
S2
S1
J8
J14
J12
J3
J4
J13

E1 - Integrated 2.4 GHz chip antenna
J12, J13 - 2 x 10 2.54 mm pitch prototyping area holes
J3 - ETH0 LAN port
J4 - ETH1 LAN port
J8 - Type A USB socket
J14 - Mini - A USB socket (console + power 5V)
S1 - Hardware reset button
S2 - GPIO programable button