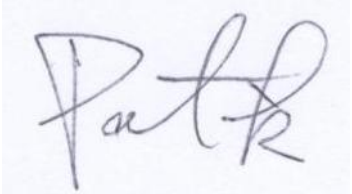
SPECIFICATIONS FOR LCD MODULE

CUSTOMER	**Preliminary Specifications**
CUSTOMER PART NO.	
AMPIRE PART NO.	**AM-320240L8TNQW-00H**
APPROVED BY	
DATE	

☑ **Approved For Specifications**
☐ **Approved For Specifications & Sample**

APPROVED BY	CHECKED BY	ORGANIZED BY
		

RECORD OF REVISION

Revision Date	Page	Contents	Editor
2007/04/13	-	New Release.	Emil
2007/05/09	-	Re-name to AM320240L8TNQW-00H.	Emil
2007/05/09	5,25	Modified interface definition and mechanical drawing.	Emil

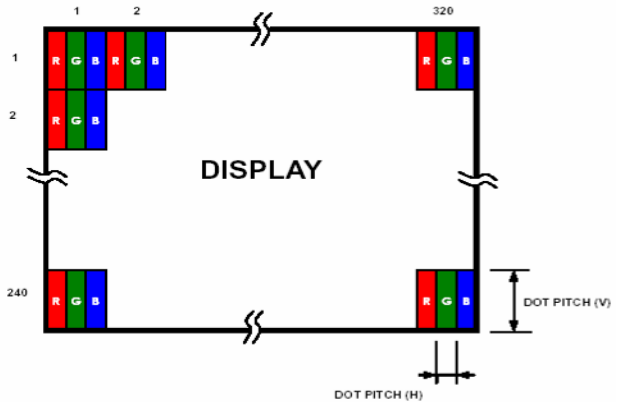
1 General Description and Features

3.5 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module. This module is composed of a 3.5" TFT-LCD panel, a driver circuit and backlight unit.

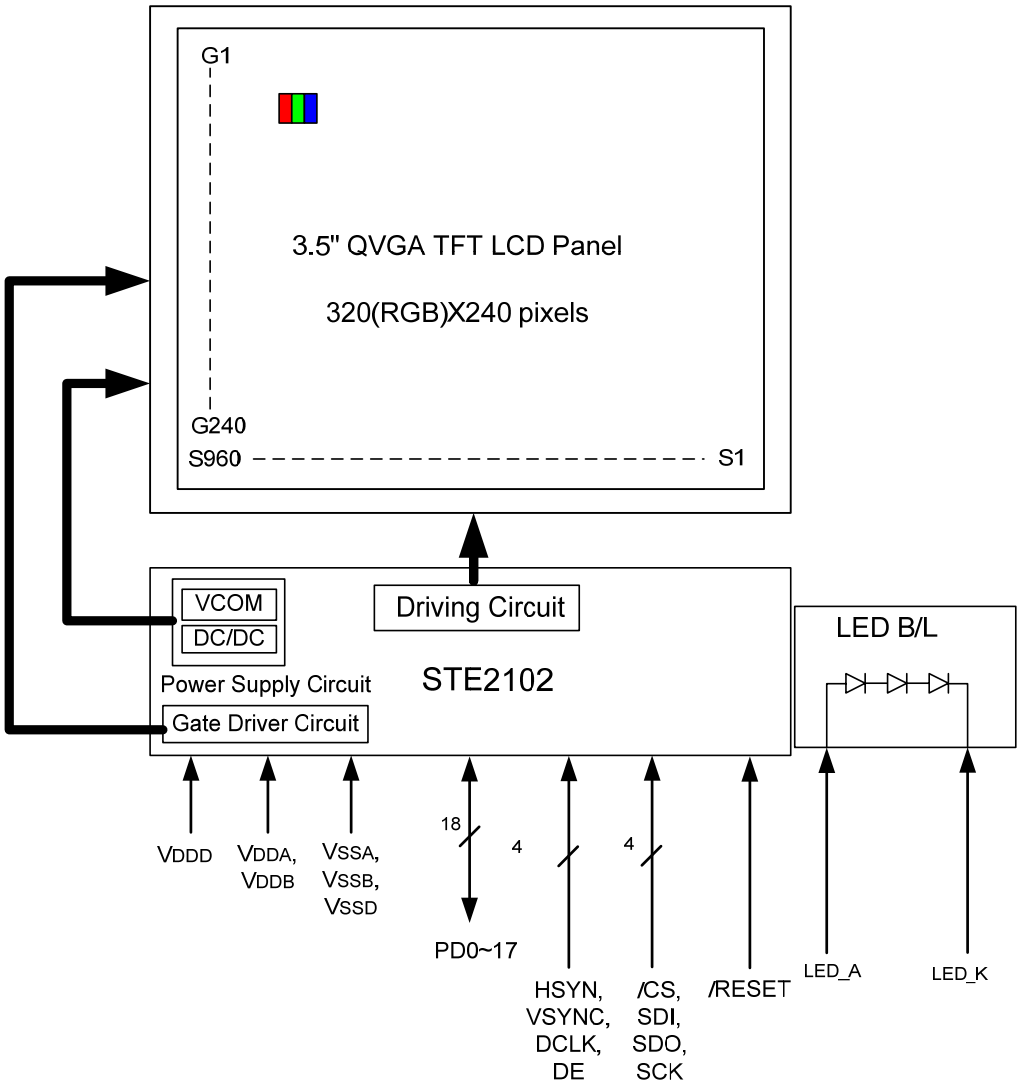
1.1 Construction: 3.5" a-Si color TFT-LCD, White LED Backlight and PCB.
1.2 Resolution (pixel): 320(R.G.B) X240.
1.3 Number of the Colors : 262K colors (R , G , B 6 bit digital each).
1.4 LCD type : Transmissive Color TFT LCD (normally White).
1.5 3-pin Serial Interface (Using for Initialize LCD Driver IC).
1.6 18Bit RGB Interface (DE Mode Only).
1.7 Interface: 40 pin.
1.8 Power Supply Voltage: 3.3V single power input. Built-in power supply circuit.
1.9 LED Type Blacklight.
1.10 IPS (In-Plane Switching) technical LCD Panel.

2 Physical specifications

Item	Specifications	unit
Display Resolution	320(W) x 240(H)	dot
Active area	70.08 x 52.56	mm
Screen size	3.5(Diagonal)	inch
Dot pitch	0.073 (W) x 0.219 (H)	mm
Color configuration	R.G.B – stripe	
Overall Dimension	77.8(W) x 64.5(H) x 6.95(T)	mm
Input interface	digital 18-bits RGB	
Surface Treatment	Anti - glare(AG)	
Backlight unit	White LED	
Display Mode	Normally White/Transmissive	



3 Functional Block Diagram



4 Electrical Specifications

TFT LCD Panel FPC Descriptions

Pin no	Symbol	I/O	Description	Remark
1	LED_A	I		
2	LED_K	I		
3-4	GND		GND terminal	
5	SHUT	I	Shut down the display driver (sleep-in mode) when this pin is high - When driven to VDD : sleep-in mode; - When driven to GND: normal operation.	
6	/RESET	I	Reset Signal L : Reset	
7	SCL	I	Input for Serial Clock	
8	SDO	O	Serial Data Output Pin	
9	SDI	I	Serial Data Input Pin	
10	/CS	I	Chip Select Signal L : Select	
11	DCLK	I	Clock signal. Latching data at the rising edge.	
12	HSYNC	I	Horizontal sync input in digital RGB mode	
13	VSYNC	I	Vertical sync input in digital RGB mode.	
14	DE	I	Input data enable control	
15	GND		GND terminal	
16	R5	I	Red data	
17	R4	I		
18	R3	I		
19	R2	I		
20	R1	I		
21	R0	I		
22	G5	I	Green data	
23	G4	I		
24	G3	I		
25	G2	I		
26	G1	I		
27	G0	I		
28	B5	I	Blue data	
29	B4	I		
30	B3	I		
31	B2	I		
32	B1	I		
33	B0	I		
34	GND		GND terminal	
35	VCC		Power supply for the logic (3.3V)	
36	VCC			
37	YU	I	Touch panel control pad	

38	XL	I		
38	YD	I		
40	XR	I		

5 Basic Display Color and Gray Scale

	Color & Gray Scale	DATA SIGNAL																	
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(0)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(0)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(61)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(31)	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(1)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(61)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(31)	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(1)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(0)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(31)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(0)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

6 Absolute Maximum Ratings

If the operating condition exceeds the following absolute maximum ratings, the TFT LCD module may be damaged permanently.

6.1 Environmental Absolute max. ratings

Item	OPERATING		STORAGE		Remark
	MIN	MAX	MIN	MAX	
Temperature	-20	70	-30	80	Note2,3,4,5,6,7,8
Humidity	Note1		Note1		
Corrosive Gas	Not Acceptable		Not Acceptable		

Note1 : Ta <= 40℃ : 85% RH max

Ta > 40℃ : Absolute humidity must be lower than the humidity of 85%RH at 40℃

Note2 : For storage condition Ta at -30℃ < 48h , at 80℃ < 100h

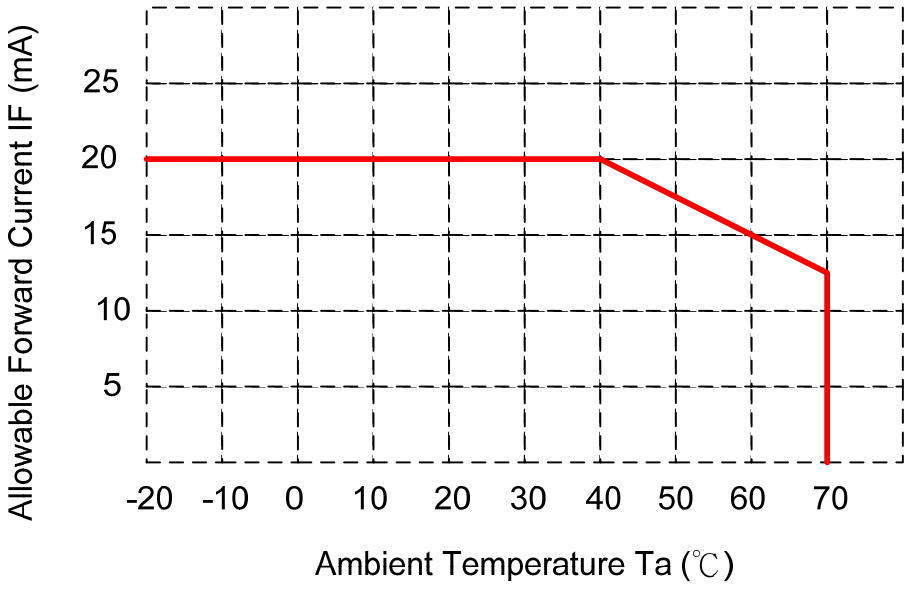
For operating condition Ta at -20℃ < 100h

Note3 : Background color changes slightly depending on ambient temperature. This phenomenon is reversible.

Note4 : The response time will be slower at low temperature.

Note5 : Only operation is guarantied at operating temperature. Contrast , response time, another display quality are evaluated at +25℃

Note6 : When LCM is operated over 40℃ ambient temperature, the I_{LED} of the LED back-light should be follow :



Note7 : This is panel surface temperature, not ambient temperature.

Note8 : When LCM be operated over than 40℃ , the life time of the LED back-light will be reduced.

6.2 Electrical Absolute max. ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	VDD	VSS=0	-0.3	6.0	V	
Input voltege	V_{in}		-0.3	VDD+0.3	V	Note 1

Note1:Hsync, Vsync, DEN, DCLK, R0~R5, G0~G5, B0~B5

7 Electrical Characteristics

7.1 DC Electrical characteristic of the LCD

Typical operting conditions (VSS=0V)

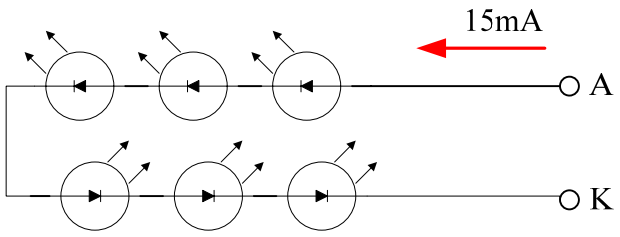
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	3.6	V	
Input Voltage for logic	H Level	V_{IH}	0.7 VDD	-	VDD	V	Note 1
	L Level	V_{IL}	0	-	0.3 VDD	V	
Power Supply current		IDD		(T.B.D)	--	mA	Note 2

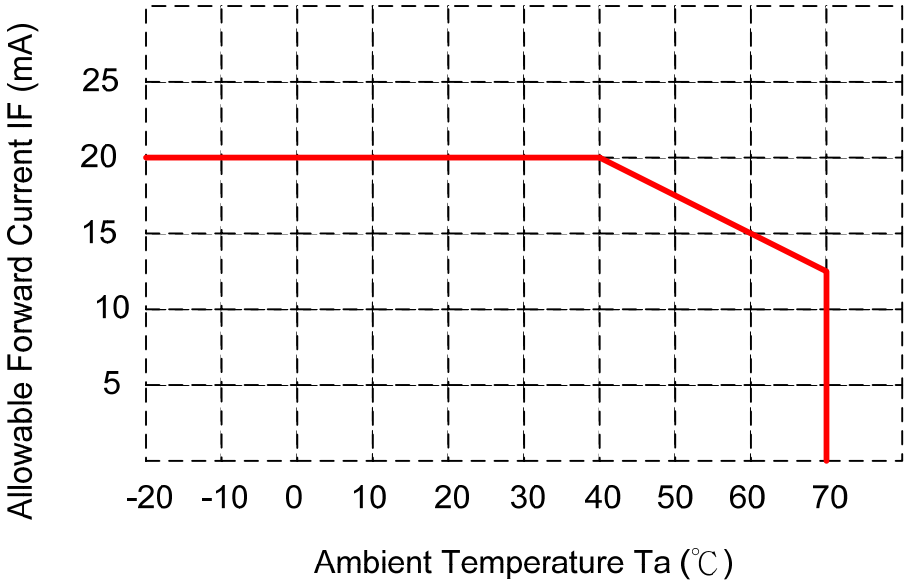
Note1: Hsync, Vsync, DEN, DCLK, R0~R5, G0~G5, B0~B5

Note2: fv =60Hz , Ta=25℃ , Display pattern : All Black

7.2 Electrical characteristic of LED Back-light

Paramenter	Symbol	Min.	Typ.	Max.	Unit	Condiction
LED voltage	V_{AK}	16.8	19.2	22.8	V	I_{LED} =15mA,Ta=25℃
LED forward current	I_{LED}	--	15	20	mA	Ta=25℃
	I_{LED}	--	10	15	mA	Ta=60℃




Allowable Forward Current IF (mA)
25
20
15
10
5
-20
-10
0
10
20
30
40
50
60
70
Ambient Temperature Ta (℃)

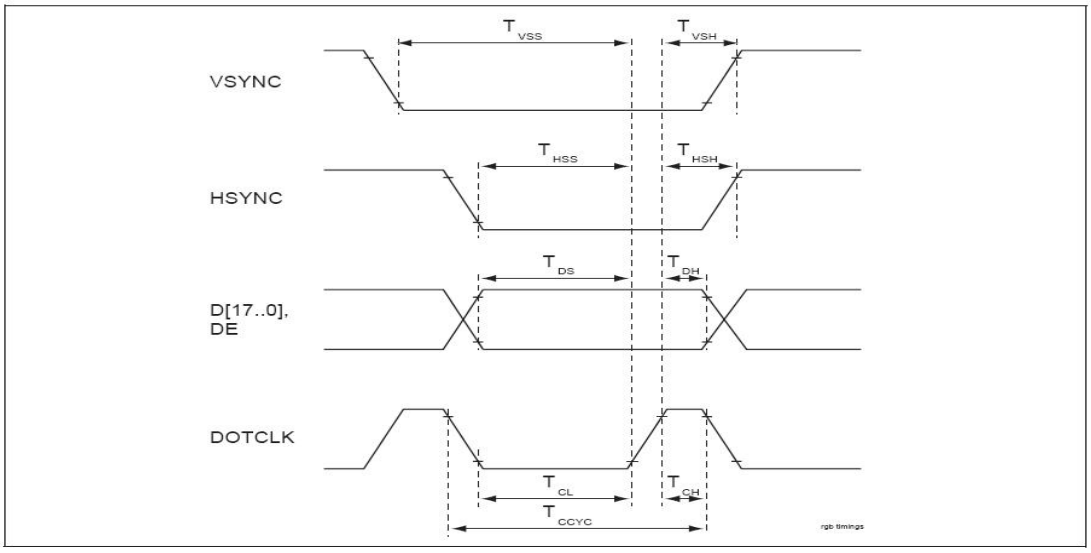
8 AC Timing characteristic of the LCD

RGB Interface Timings

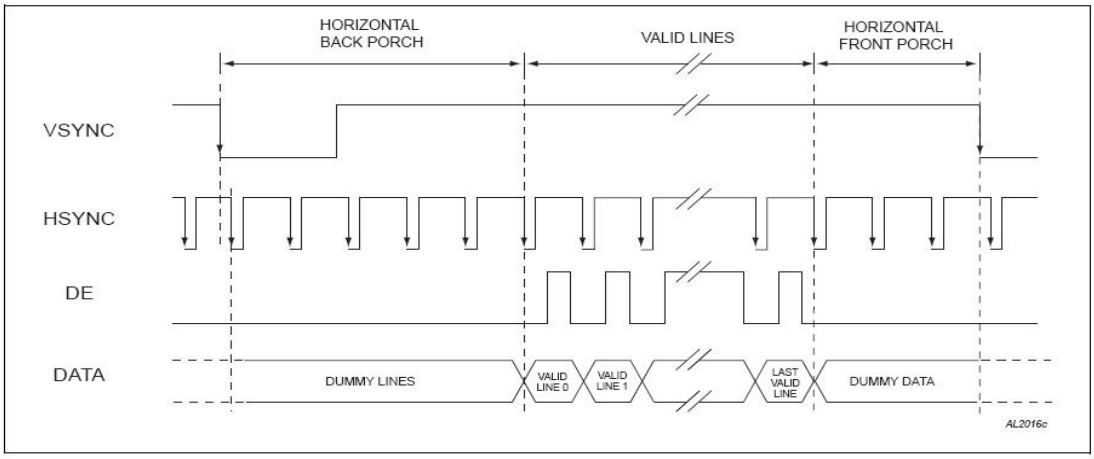
(VDDD = 1.50 to 1.95 V; VDDA/VDDB = 2.2V to 3.6V; VSS/VSSA/VSSB = 0V; Tamb =-40 to 85°C; unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{CCYC}	Dot Clock cycle	60 (3.)		226 (4.)	ns
T_{CL}	Dot Clock pulse width “L”	5			ns
T_{CH}	Dot Clock pulse width “H”	5			ns
T_{VSS}	Vertical Sync Setup time	15			ns
T_{VSH}	Vertical Sync Hold time	15			ns
T_{HSS}	Horizontal Sync Setup time	15			ns
T_{HSH}	Horizontal Sync Hold time	15			ns
T_{DS}	Data and DE Sync Setup time	15			ns
T_{DH}	Data and DE Sync Hold time	15			ns

Notes：1. Signal rise and fall times are equal or less than 20ns.
2. Low state is 0.3xVDDD, high state is 0.7xVDDD.
3. Refresh Rate = 65Hz.
4. Refresh Rate = 50Hz.



Vertical display timing



3-lines SPI Interface

The STE2102 3-lines serial Interface is a bidirectional link between the display driver and the application host. It consists of three lines:
– Data signal (SDAIN and SDAOUT);
– Clock signal (SCL);
– Peripheral enable (/CS).
The serial interface is active only if the /CS line is set to a logic 0. When /CS line is high the serial peripheral is disabled and no data are clocked in.
The STE2102 is always a slave on the communication bus and receive the communication clock on the SCL pin from the master.
Information is exchanged byte-wide. During data transfer, the input data line SDAIN is sampled by the STE2102 on the SCL rising edge while the output data line SDAOUT is written on the SCL falling edge.

Write Mode

The STE2102 is always a slave on the communication bus and receive the communication clock on the SCL pin from the master. Information is exchanged byte-wide. During data transfer, the data line is sampled by the slave unit on the SCL rising edge.

After a falling edge of the /CS signal, the driver interprets the first incoming byte as a command. One of the following options can occur:
– The command is related to an instruction with no parameters: the command is executed and the next incoming byte will be interpreted as a new command;

– The command is related to an instruction with N parameters: the next incoming N bytes will be interpreted as a parameter (or parameters);

– The command belongs to the Protected Mode Area and the Protected Mode is enabled: the command is neglected and the next incoming byte will be interpreted as a new command;

– The byte received is not a valid command: the byte is neglected and the next incoming byte will be interpreted as a new command.
If /CS stays low after the last bit of a command/parameter byte, the serial interface expects the MSB of the next command or parameter byte on the next SCL positive edge.

If the /CS line is forced high after a completed parameter or command transfer, an halt condition (Figure 8-4) occurs and the last command or parameter received is processed.
If /CS line is forced high in the middle of a parameter or command transfer, a break condition (Figure 8-5) occurs and incomplete parameter or command transfers are discarded.
A reset pulse on /RES pin interrupts any transmission.
If /CS is low after the positive edge of /RES, the serial interface is ready to receive data.

Figure 8-1. 3-lines SPI Communication Protocol

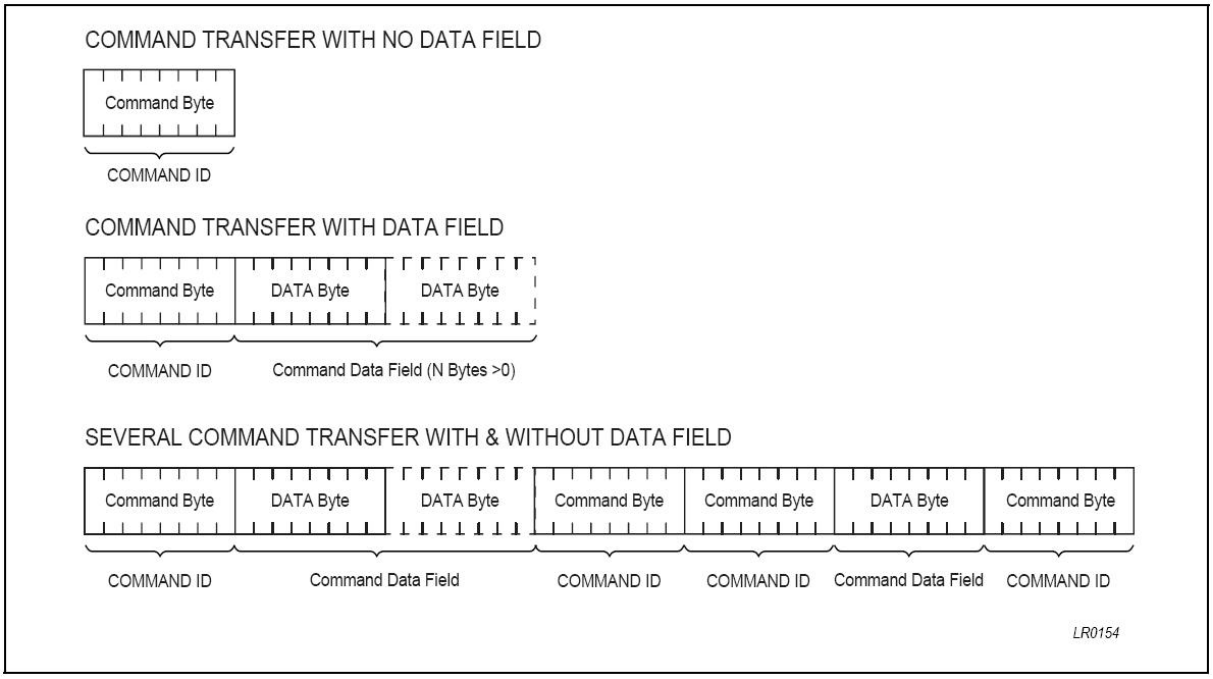


Figure 8-2. 3-lines SPI One Byte Write Cycle

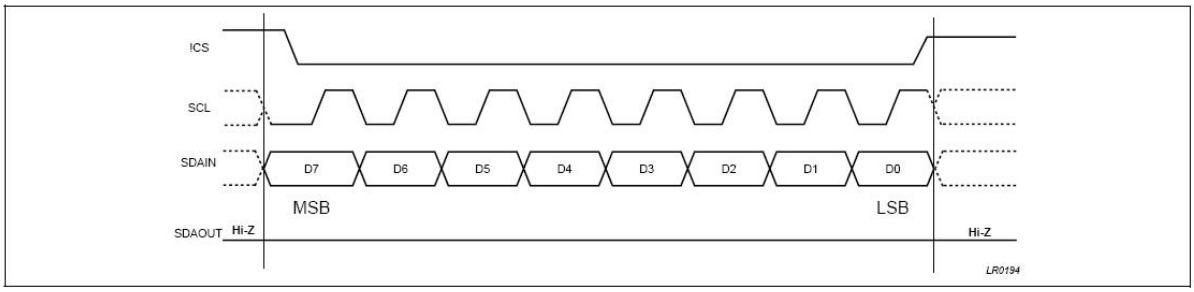


Figure 8-3. 3-lines SPI Several Commands transfer

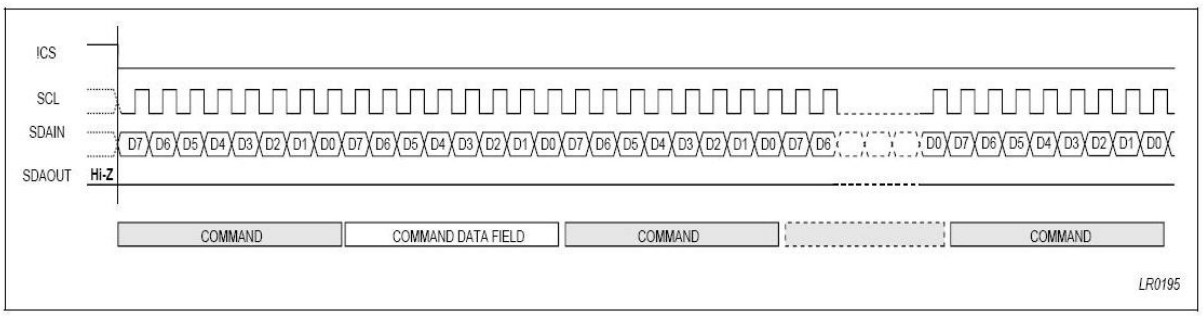


Figure 8-4. 3-lines SPI Halt Data Transfer

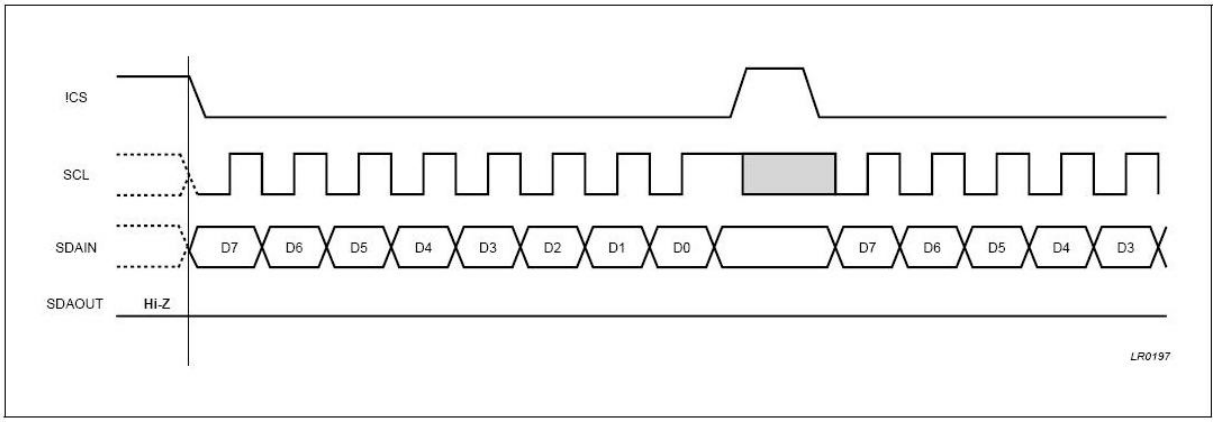
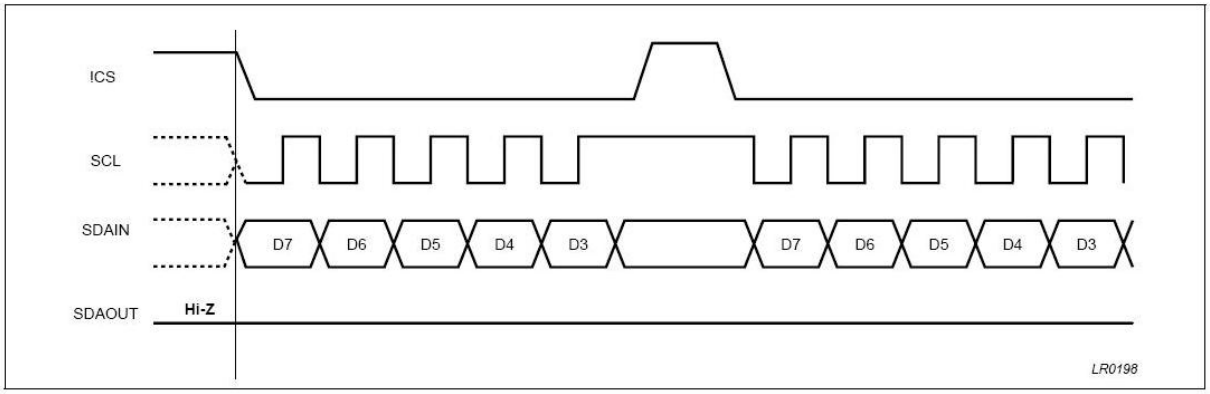


Figure 8-5. 3-lines SPI Break Data Transfer



Read Mode

Throughout SDA is possible to read some registers value (ID Codes, Status Bytes, etc...).
When reading back a 8bit wide value no dummy clock pulse is required (Figure 8-6), while it is required when reading back 24bit (Figure 8-7) and 32bit (Figure 8-8) wide values.
SDA is in High impedance in steady state and during data write.
In Figure 8-6. and Figure 8-7. SDA(IN) shows the Host Controller side, while SDA(OUT) shows the Display Driver side for the same SDA bus.

Figure 8-6. 3-lines SPI 8Bit Read Cycle (no dummy clock)

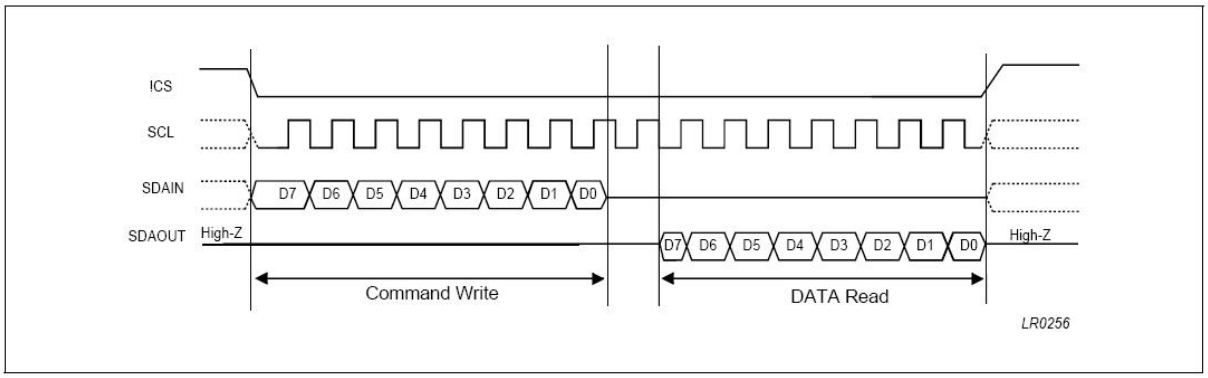


Figure 8-7. 3-lines SPI 24 Bit Read Cycle (dummy clock)

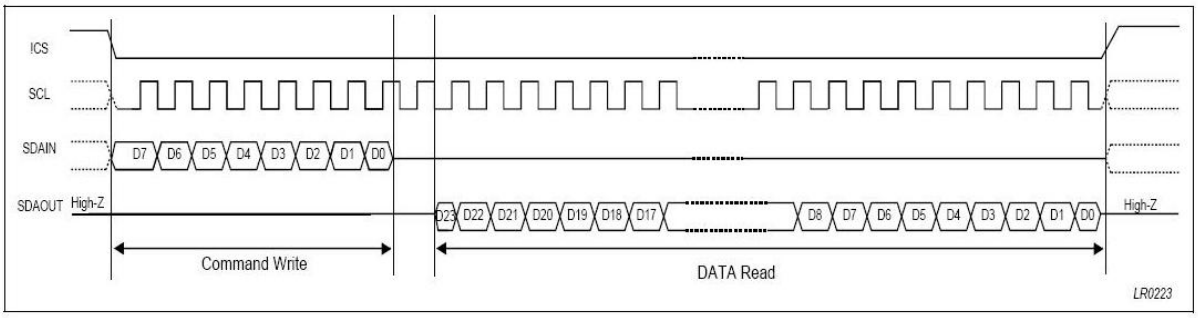
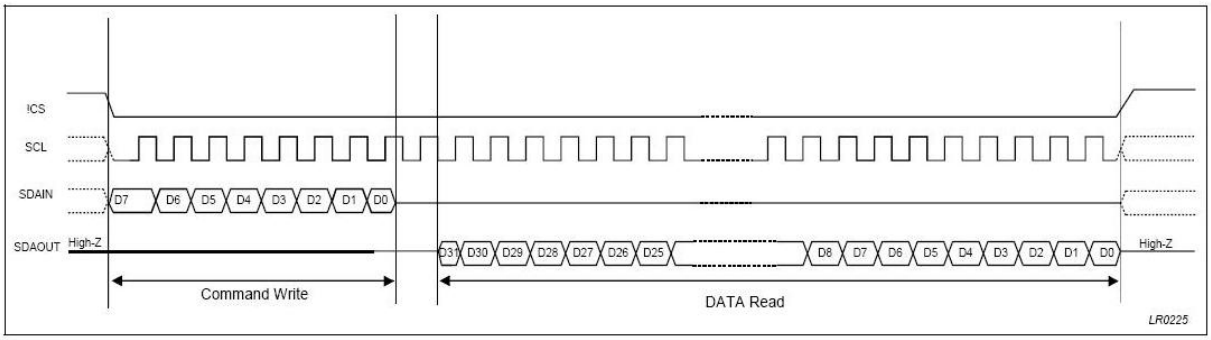


Figure 8-8-lines SPI 32 Bit Read Cycle (dummy clock)



Serial Interfaces Timings

(VDDD = 1.50 to 1.95 V; VDDA/VDDB = 2.2V to 3.6V; VSS/VSSA/VSSB = 0V; Tamb =-40 to 85°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
F_{SCLKW}	Clock Frequency	Write			15	MHz
T_{scycw}	Clock Cycle SCL		66			ns
T_{shw}	SCL pulse width “H”		5			ns
T_{slw}	SCL Pulse width “L”		5			ns
F_{SCLKW}	Clock Frequency	Read			6.7	MHz
T_{scycr}	Clock Cycle SCL		150			ns
T_{shr}	SCL pulse width “H”		0			ns
T_{slr}	SCL Pulse width “L”		0			ns
T_{css}	/CS setup time	Write	10			ns
T_{csh}	/CS hold time		30			ns
T_{chw}	/CS minimum high time		20			ns
T_{cst}	D/!C setup time	Write	10			ns
T_{cht}	D/!C hold time		10			ns
T_{sds}	SDA (Input) setup time		10			ns
T_{sdh}	SDA (Input) hold time		10			ns
T_{acc}	SDA (Output) Access Time	Read	10		50	ns
T_{oh}	SDA (Output) Disable Time		15		50	ns

Notes: 1. Input signal’s rise and fall time is equal to 15ns or less.

2. Output signal’s rise and fall time is equal to 15ns or less.

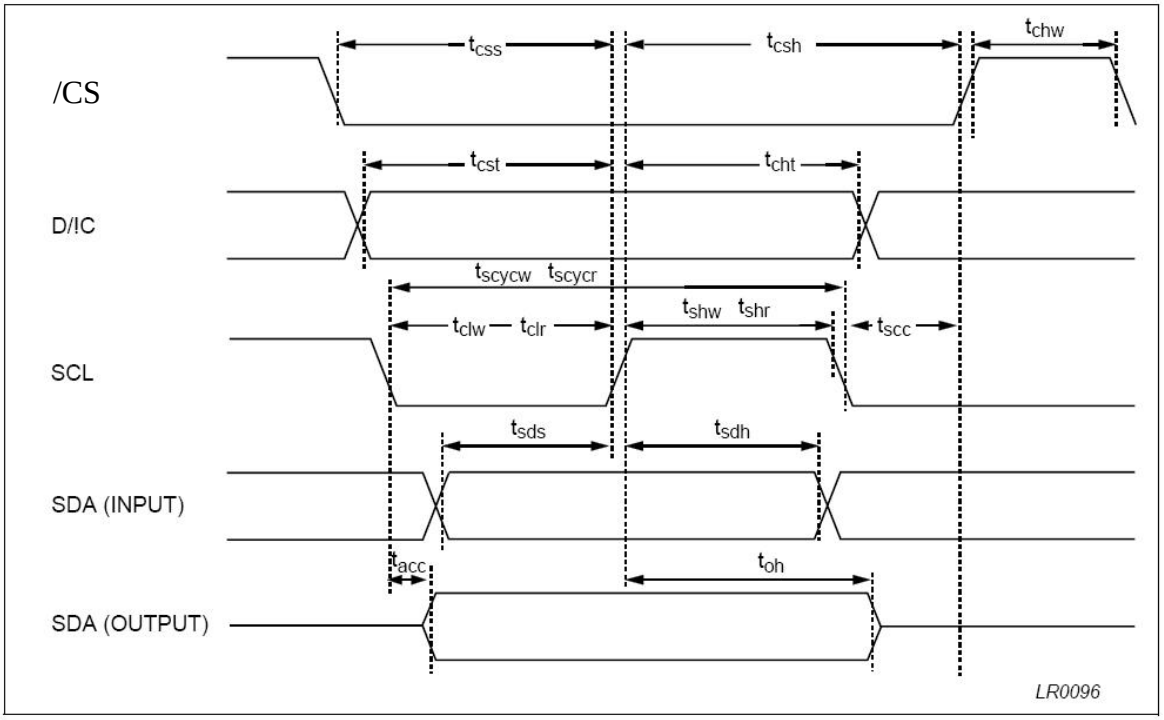


Figure Serial Interface

9 Optical specification

9.1 Optical characteristic of the LCD

Item		Symbol	Conditon	Min.	Typ.	Max.	Unit	Remark
Response Time		T_r+T_f	Θ=0°		25	40	ms	Note 1,2,3,5
Contrast ratio		CR	At optimized viewing angle	-	300	-		Note 1,2,4,5
Viewing Angle	Top Bottom Left Right		CR≧10	- - - -	80 80 80 80	- - - -	deg.	Note1,2, 5,6
Brightness		Y_L	I_{LED}=20mA ,25℃	-	350	-	cd/m²	Note 7
White chromaticity		Xw		-	0.312	-		
		Yw		-	0.333	-		

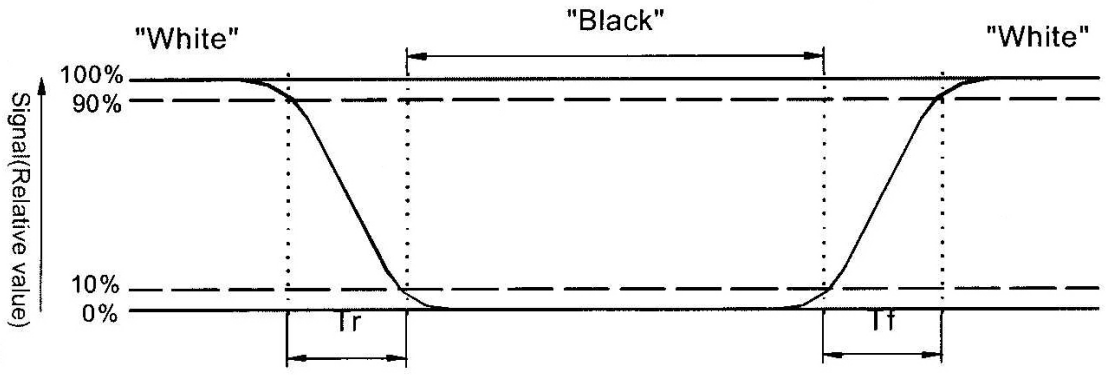
( )For reference only. These data should be update according the prototype.

Note 1: Note 1:Ambient temperature=25℃,and lamp current I_{LED}=20mA.To be measured in the dark room.

Note 2:To be measured on the center area of panel with a viewing cone of 1°by Topcon luminance meter BM-7,after 10 minutes operation.

Note 3.Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black“ to “white”(falling time) and from”white” to “black” (rising time),respectively.The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector Output when LCD is at "Black" state}}$$

Note 5:White $V_i=V_{i50}$ +1.5V

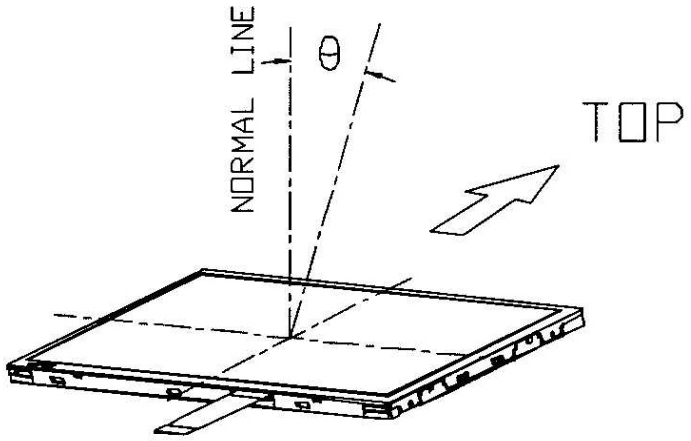
Black $V_i=V_{i50}$ +2.0V

"±"means that the analog input signal swings in phase with V_{COM} signal.

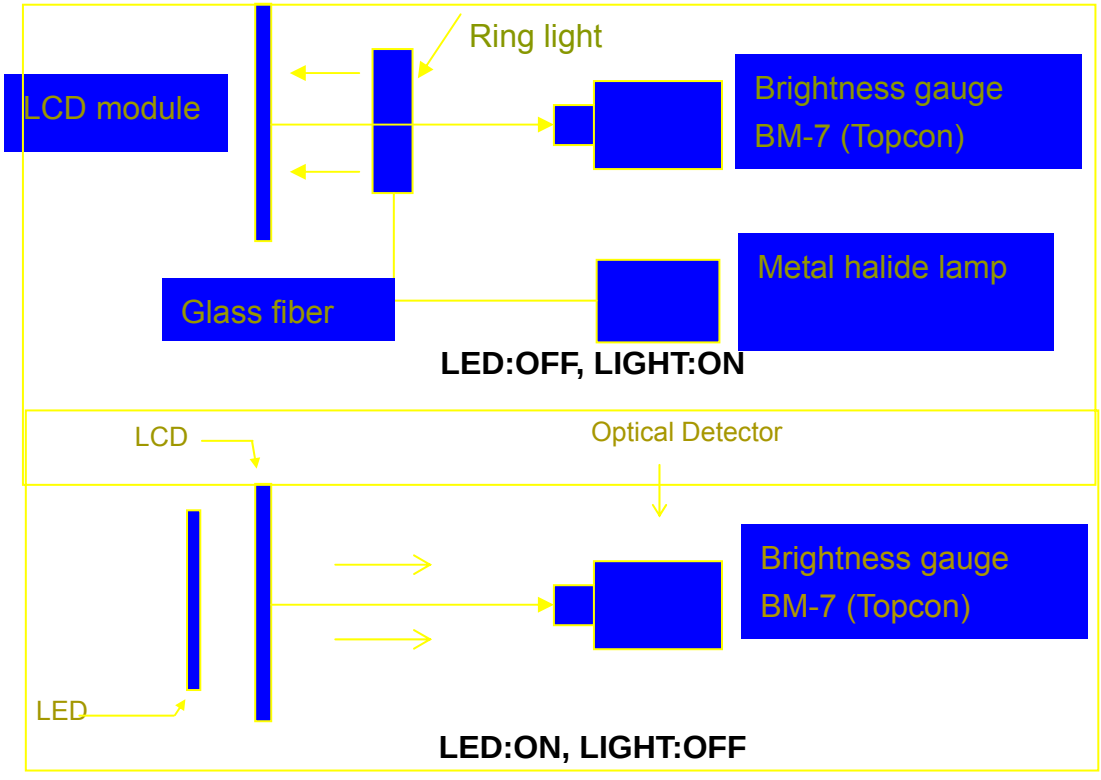
"$\frac{-}{+}$" means that the analog input signal swings out of phase with V_{COM} signal.

V_{i50} : The analog input voltage when transmission is 50%.The 100% Transmission is defined as the transmission of LCD panel when all the Input terminals of module are electrically opened.

Note 6.Definition of viewing angle, Refer to figure as below.



Note 7.Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.



10 QUALITY AND RELIABILITY

10.1 TEST CONDITIONS

Tests should be conducted under the following conditions:

Ambient temperature: 25 ± 5°C

Humidity : 60 ± 25% RH.

10.2 SAMPLING PLAN

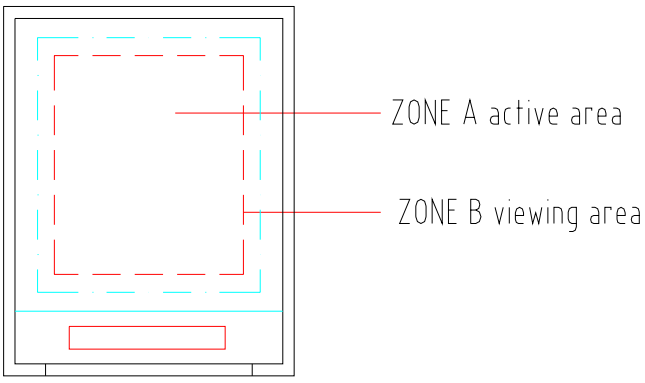
Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

10.3 ACCEPTABLE QUALITY LEVEL

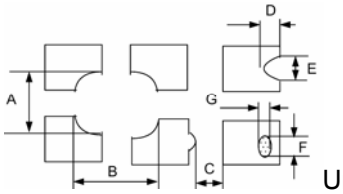
A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

10.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under fluorescent light. The inspection area of LCD panel shall be within the range of following limits.



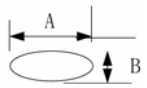
10.5 INSPECTION QUALITY CRITERIA

<table>
<tr><th>No.</th><th>Item</th><th>Criterion for defects</th><th>Defect type</th></tr>
<tr><td>1</td><td>Non display</td><td>No non display is allowed</td><td>Major</td></tr>
<tr><td>2</td><td>Irregular operation</td><td>No irregular operation is allowed</td><td>Major</td></tr>
<tr><td>3</td><td>Short</td><td>No short are allowed</td><td>Major</td></tr>
<tr><td>4</td><td>Open</td><td>Any segments or common patterns that don’t activate are rejectable.</td><td>Major</td></tr>
<tr><td>5</td><td>Black/White spot</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.15</td><td>Ignore</td></tr><tr><td>0.15 < D ≤ 0.20</td><td>3</td></tr><tr><td>0.20 < D ≤ 0.30</td><td>2</td></tr><tr><td>0.30 < D</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>6</td><td>Black/White line</td><td><table><tr><th>Length(mm)</th><th>Width (mm)</th><th>Acceptable number</th></tr><tr><td>10 < L</td><td>0.03 < W ≤ 0.04</td><td>5</td></tr><tr><td>5.0 < L ≤10</td><td>0.04 < W ≤ 0.06</td><td>3</td></tr><tr><td>1.0 < L ≤ 5.0</td><td>0.06 < W ≤ 0.07</td><td>2</td></tr><tr><td>L ≤ 1.0</td><td>0.07 < W ≤ 0.09</td><td>1</td></tr></table></td><td>Minor</td></tr>
<tr><td>7</td><td>Back Light</td><td>1. No Lighting is rejectable
2. Flickering and abnormal lighting are rejectable</td><td>Major</td></tr>
<tr><td rowspan="4">8</td><td rowspan="4">dot defect</td><td>Bright dot</td><td>N≦1</td><td rowspan="4">Minor</td></tr>
<tr><td>Dark dot</td><td>N≦3</td></tr>
<tr><td>Total dot defect
(Bright dot + Dark dot)</td><td>N≦3</td></tr>
<tr><td>Minimum distance between dark dot and dark dot</td><td>L≧5 mm</td></tr>
<tr><td>9</td><td>Display pattern</td><td colspan="2"> 

Unit:mm
<table><tr><td>$\frac{A+B}{2} \le 0.30$</td><td>0 < C</td><td>$\frac{D+E}{2} \le 0.25$</td><td>$\frac{F+G}{2} \le 0.25$</td></tr></table>
Note: 1. Acceptable up to 3 damages
2. NG if there’re to two or more pinholes per dot</td><td>Minor</td></tr>
</table>

<table>
<tr><td>10</td><td>Blemish & Foreign matters

Size:
$D=\frac{A+B}{2}$</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.15</td><td>Ignore</td></tr><tr><td>0.15 < D ≤ 0.20</td><td>3</td></tr><tr><td>0.20 < D ≤ 0.30</td><td>2</td></tr><tr><td>0.30 < D</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>11</td><td>Scratch on Polarizer

  </td><td><table><tr><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable number</th></tr><tr><td>W≤0.03</td><td>Ignore</td><td>Ignore</td></tr><tr><td>0.03<W≤0.05</td><td>L ≤ 2.0</td><td>Ignore</td></tr><tr><td></td><td>L > 2.0</td><td>1</td></tr><tr><td>0.05<W≤0.08</td><td>L > 1.0</td><td>1</td></tr><tr><td></td><td>L ≤ 1.0</td><td>Ignore</td></tr><tr><td>0.08<W</td><td>Note (1)</td><td>Note(1)</td></tr></table>Note(1) Regard as a blemish</td><td>Minor</td></tr>
<tr><td>12</td><td>Bubble in polarizer</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.20</td><td>Ignore</td></tr><tr><td>0.20 < D ≤ 0.50</td><td>3</td></tr><tr><td>0.50 < D ≤ 0.80</td><td>2</td></tr><tr><td>0.80 < D</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>13</td><td>Stains on LCD panel surface</td><td>Stains that cannot be removed even when wiped lightly with a soft cloth or similar cleaning too are rejectable.</td><td>Minor</td></tr>
<tr><td>14</td><td>Rust in Bezel</td><td>Rust which is visible in the bezel is rejectable.</td><td>Minor</td></tr>
<tr><td>15</td><td>Defect of land surface contact (poor soldering)</td><td>Evident crevices which is visible are rejectable.</td><td>Minor</td></tr>
<tr><td>16</td><td>Parts mounting</td><td>1. Failure to mount parts
2. Parts not in the specifications are mounted
3. Polarity, for example, is reversed</td><td>Major
Major
Major</td></tr>
<tr><td>17</td><td>Parts alignment</td><td>1. LSI, IC lead width is more than 50% beyond pad outline.
2. Chip component is off center and more than 50% of the leads is off the pad outline.</td><td>Minor

Minor</td></tr>
<tr><td>18</td><td>Conductive foreign matter (Solder ball, Solder chips)</td><td>1. 0.45< φ ,N≧1
2. 0.30< φ ≤0.45 ,N≧1
φ :Average diameter of solder ball (unit: mm)
3. 0.50<L ,N≧1
L: Average length of solder chip (unit: mm)</td><td>Major
Minor

Minor</td></tr>
<tr><td>19</td><td>Faulty PCB correction</td><td>1. Due to PCB copper foil pattern burnout, the pattern is connected, using a jumper wire for repair; 2 or more places are corrected per PCB.
2. Short circuited part is cut, and no resist coating has been performed.</td><td>Minor

Minor</td></tr>
</table>

10.6 RELIABILITY

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=96 hrs	
Low Temperature Operation	-20±3°C , t=96 hrs	
High Temperature Storage	80±3°C , t=96 hrs	1,2
Low Temperature Storage	-30±3°C , t=96 hrs	1,2
Humidity Test	40°C , Humidity 90%, 96 hrs	1,2
Thermal Shock Test	-30°C ~ 25°C ~ 80°C 30 min. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2
Vibration Test (Packing)	Sweep frequency：10~55~10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2
Static Electricity	150pF 330 ohm ±8kV, 10times air discharge	

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions

(15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

11 USE PRECAUTIONS

11.1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

11.2 Installing precautions

1) To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

11.3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

11.4 Operating precautions

1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.
8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by

the LC drive voltage. Design the contents of the display, considering crosstalk.

11.5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.

12 Mechanical Dimensions