ZARLINK SEMICONDUCTOR

ZL30110
Telecom Rate Conversion DPLL

Data Sheet

November 2006

Features

- Synchronizes to 8 kHz, 2.048 MHz, 8.192 MHz or 16.384 MHz
- Provides a range of output clocks:
  - 65.536 MHz TDM clock locked to the input reference
  - General purpose 25 MHz fan-out to 6 outputs locked to the external crystal or oscillator
  - General purpose 125 MHz and 66 MHz or 100 MHz locked to the external crystal or oscillator
- Provides DPLL lock and reference fail indication
- Automatic free run mode on reference fail
- DPLL bandwidth of 922 Hz for all rates of input reference and 58 Hz for an 8 kHz input reference
- Less than 5 $psec_{rms}$ on 25 MHz outputs, and less than 0.6 ns_{pp} intrinsic jitter on the all other outputs
- Minimal input to output and output to output skew
- 25 MHz external master clock source: clock oscillator or crystal
- Simple hardware control interface

Ordering Information

ZL30110LDE	32 Pin QFN	Tubes Bake & Dry Pack
ZL30110LDE1	32 Pin QFN*	Tubes Bake & Dry Pack

*Pb Free Matte Tin

-40°C to +85°C

Applications

- Clock rate conversion PLL for Telecommunication Equipment
- Small/Medium Enterprise Router / Gateway
- Broadband access (xPON/xDSL) CPE gateway

Description

The ZL30110 clock rate conversion digital phase-locked loop (DPLL) provides accurate and reliable frequency conversion.

The ZL30110 generates a range of clocks that are either locked to the input reference or locked to the external crystal or oscillator.

In the locked mode, the reference input is continuously monitored for a failure condition. In the event of a failure, the DPLL continues to provide a stable free running clock ensuring system reliability.

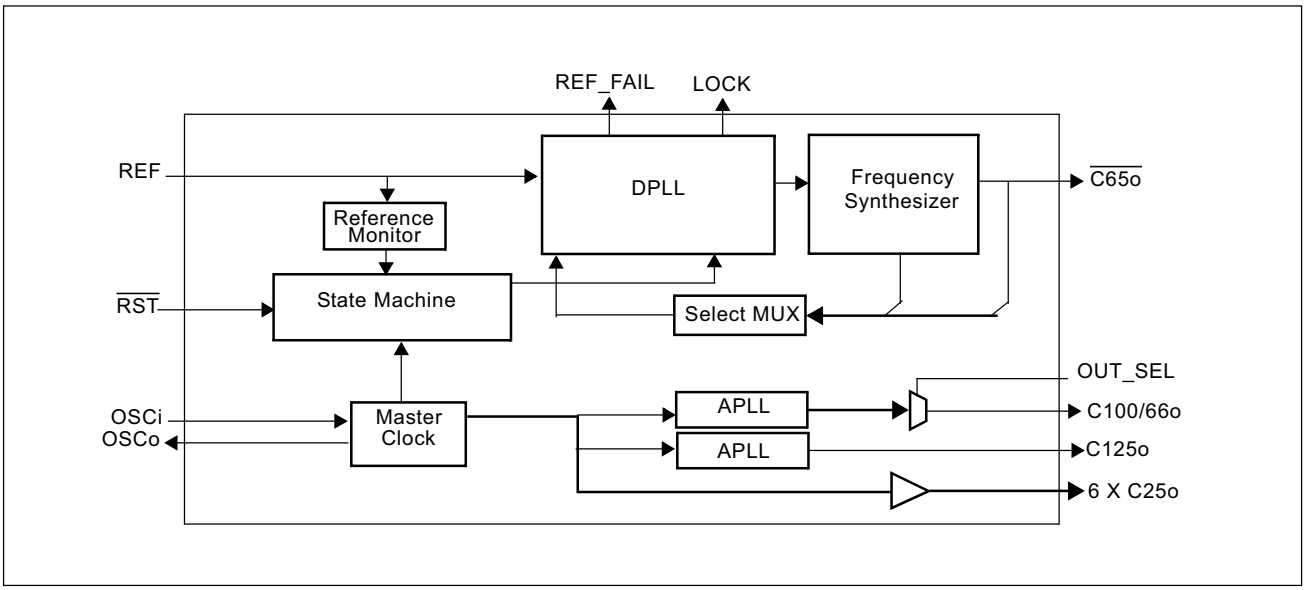

Figure 1 - Functional Block Diagram

1.0 Physical Description

1.1 Pin Connections

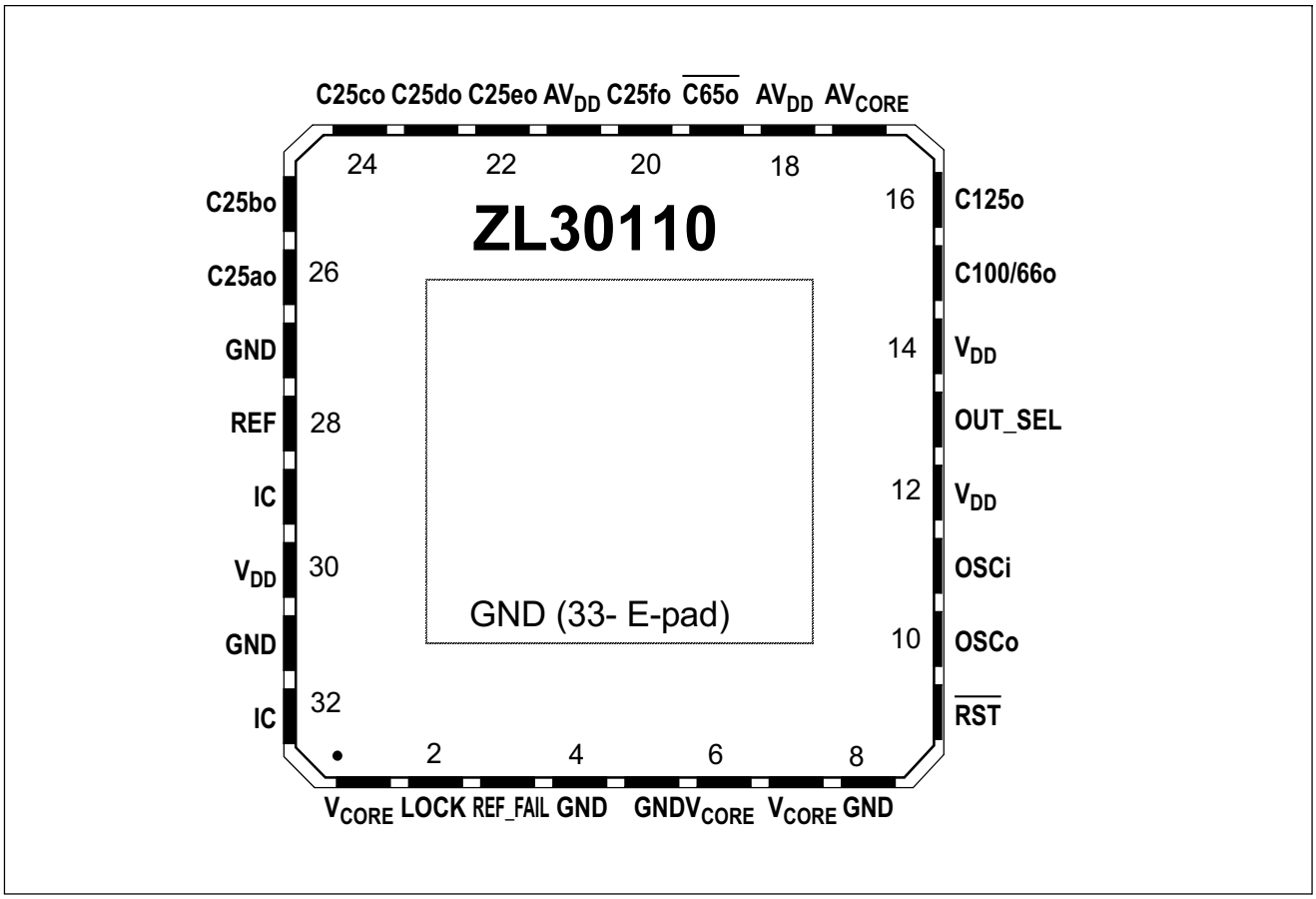

Figure 2 - Pin Connections (32 pin 5 mm X 5 mm QFN with E-pad)