Zarlink's ZL30119 chip is the industry's smallest, lowest power programmable digital/analog PLL for line card clock management in next-generation SONET/SDH multi-service provisioning platforms and multi-service edge products.
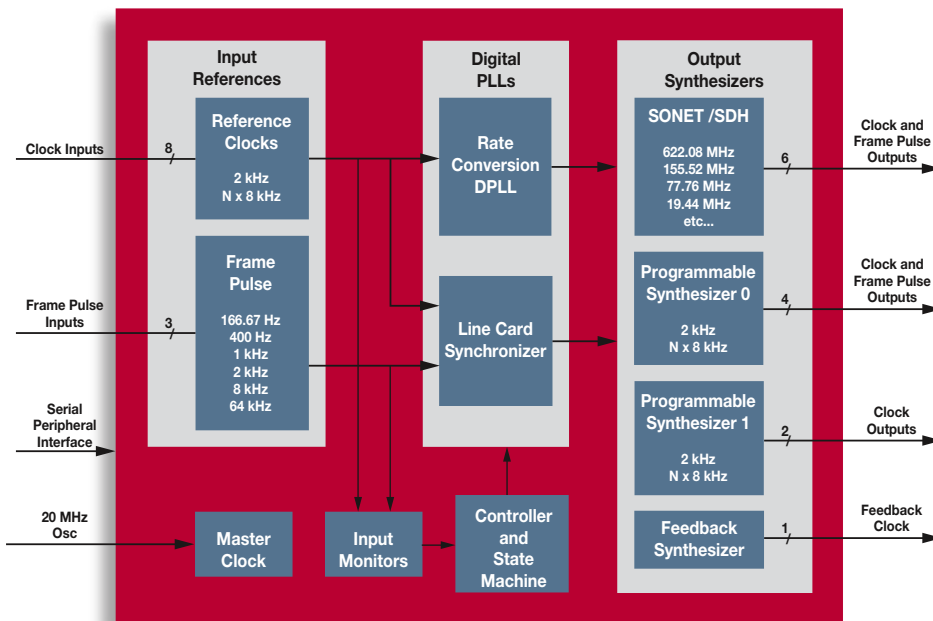
A highly integrated device, the ZL30119 PLL combines the hitless reference switching capabilities of a digital PLL with the jitter performance of an analog PLL. The ZL30119 PLL delivers all of the clocks and clock formatting required to allow existing SONET/SDH infrastructures to carry new Ethernet, VoIP and Fiber Channel services.

The ZL30119 PLL combines backplane interface functions, ultra-low jitter SONET/SDH clock synthesis, programmable clock synthesis and clock formatting in a compact 9 x 9 mm chip. Simplifying design, the device synthesizes SONET/SDH interface clocks, tributary clock families and SBI or Telecom busses without requiring significant board space or the use of multiple PLLs.

ZL30119 Simplified Block Diagram

Integrated Timing Chip for SONET/SDH Line Cards

→ Single-chip integrates reference switching performance of a DPLL with jitter generation of an APLL

→ Jitter attenuation under 1 ps (less than 25% of jitter budget for OC-48/STM-16 interfaces)

→ Two independently configurable DPLLs:
  • DPLL1 provides all features for generating SONET/SDH compliant clocks
  • DPLL2 generates independent, general purpose clocks

→ PLLs operate in free-run, normal and holdover modes and provide automatic hitless reference switching

→ CMOS outputs for 19.44 MHz and 77.76 MHz clocks eliminate external dividers or clock multiplying PLLs

→ Programmable frame pulse formatter replaces CPLD or FPGA gates

→ Selectable output clocks (6.48 MHz, 19.44 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz) eliminate external dividers & clock multiplying DPLLs

→ Programmable output synthesizers generate clock frequencies from any multiple of 8 kHz up to 77.76 MHz and 2 kHz

→ Eight reference inputs supporting clock frequencies in any multiple of 8 kHz up to 77.76 MHz and 2 kHz

→ Meets Telcordia GR-253-CORE and ITU-T G.813 jitter requirements up to OC-48/STM-16

Customer Support

The ZL30119 chip is supported by an evaluation board, reference designs and Zarlink's network of in-house field application and design engineers.

Applications

→ WAN router line cards

→ DSLAM line cards

→ RNC/Mobile switching center line cards

→ ADM line cards

→ Next generation SONET/SDH line cards

→ AdvancedTCA™ line cards

ZARLINK SEMICONDUCTOR

SONET/SDH Line Card Synchronization

Zarlink's ZL30119 is a compact, highly integrated PLL that synthesizes SONET/SDH interface clocks, tributary clock families and SBI or Telecom bus clocks locked to backplane references. Incorporating digital and analog PLLs, the single chip manages line card timing for next-generation SONET/SDH platforms operating at speeds up to OC-48/STM-16. Competing two-chip or module approaches are more than twice the size of the ZL30119 and require external devices to manage high-speed network timing.
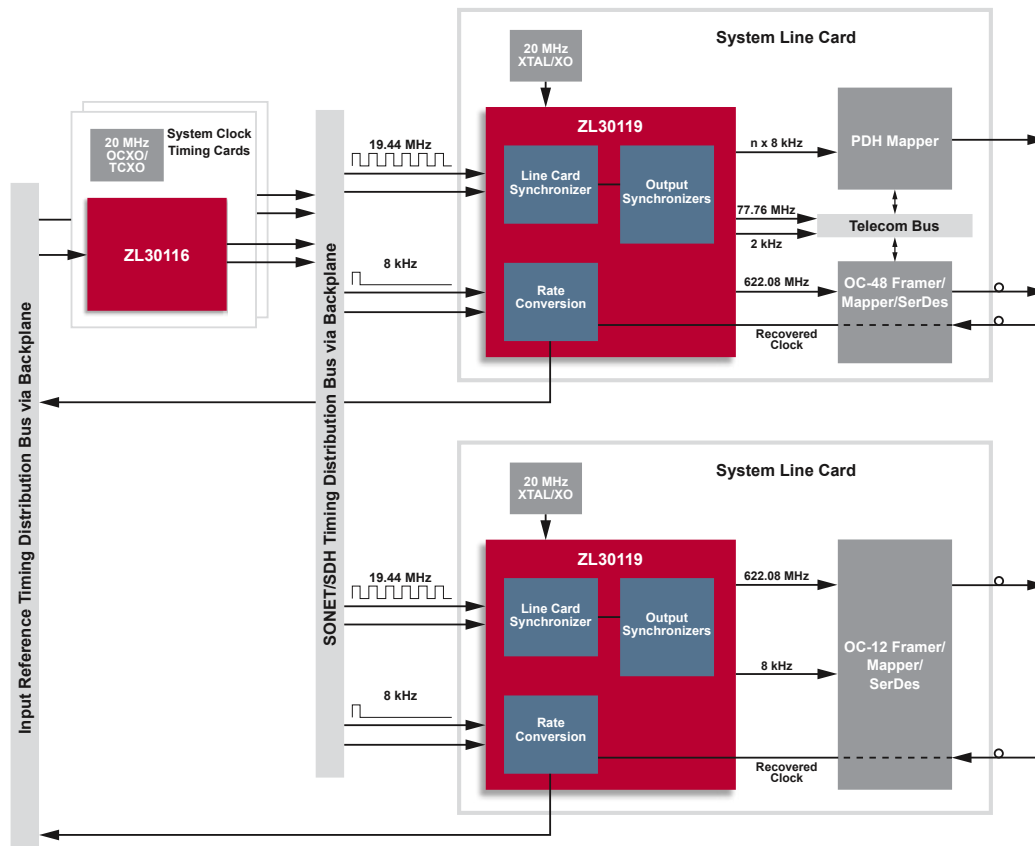
As illustrated below, the ZL30119 can be used as the sole timing source for the most complex line cards, providing all of the required timing functions while meeting jitter requirements up to OC-48/STM-16. The device simultaneously accepts and monitors up to eight input references and three frame pulse (sync) inputs for frequency accuracy, phase irregularity and loss of clock.

The ZL30119 can be configured to manually or automatically switch between valid input references upon reference failure. When using automatic reference switching, reference selection criteria is based on input priority and an optional revertive feature ensures the highest priority valid reference is always selected. When no valid references are available, the device automatically enters holdover mode and continues to generate output clocks based on historical reference frequency data.

The ZL30119 can simultaneously generate 13 output clocks from three independent clock frequency families. Common SONET/SDH clock frequencies, programmable n x 8 kHz clock frequencies and a variety of programmable frame pulses can be generated simultaneously. Programmable phase delay adjustment and programmable frame pulse formatting is also available and both CMOS and differential LVPECL outputs are provided. This means virtually any required frequency can be generated and adjusted as required, eliminating the need for additional oscillators, external dividers, clock multiplying PLLs or level translation devices.

Delivering leading integration, flexibility, programmability and performance, the ZL30119 can be implemented as the sole timing and synchronization source for virtually any line card deployed in multi-service provisioning and multi-service switching platforms.