Circuit Emulation Services (CES)

PACKET PROCESSING & SWITCHING/TDM TO PACKET PROCESSORS

VOICE/DATA

Part #	Features																																Package
				Multiprotocol Engine										TDM Interface						LIU Interface			Clock Recovery			Packet Interface			Micro-processor and Memory								
	Structure CES over Packet	Unstructure CES over Packet	N*64 kbit/s trunking of channels across any stream and channel	Ethernet	Ethernet VLAN	RTP	UDP	IPv4	IPv6	MPLS Tags	PWE3 CESoPSN (Draft)	MEF CES Requirements	QOS support through WFQ & SP	Full Duplex TDM Channels	# of TDM Streams or LIU Interfaces	1k x 1k non-blocking TDM switch	# of Streams at 2 or 8 Mbps	# of Streams programmable at 2/4/8 Mbps	H.100 Compatible TDM Interface	T1/E1 Interfaces	J2 Interfaces	T3/E3 Interfaces	Per Stream DPLL (Unstructure CES)	Integrated 4E PLL for synchronisation	Differential and Adaptive Clock Recovery	# of Packet Interface ports	100 Mb/s MII/RMII	1 Gbps GMII	33MHz 32 bit PCI bus with DMA	On-Chip Memory	Maximum Network latency with Internal Memory (ms)	External Memory type	Maximum Network latency with external Memory (ms)	JTAG	3.3V with 5V tolerent I/O	Maximum Power Dissipation (W)	
MT90880	●		●	●	●		●	●		●				1024	64	●	32/8	32	●					●		2	2		●			PBSRAM ZBT SSRAM		●	●	1	456 ball PBGA
MT90881	●		●	●	●		●	●		●				1024	32		32/8		●					●		2	2		●			PBSRAM ZBT SSRAM		●	●	1	456 ball PBGA
MT90882	●		●	●	●		●	●		●				256	16	●	8/2	8	●					●		2	2		●			PBSRAM ZBT SSRAM		●	●	0.75	456 ball PBGA
MT90883	●		●	●	●		●	●		●				256	8		8/2		●					●		2	2		●			PBSRAM ZBT SSRAM		●	●	0.75	456 ball PBGA
ZL50110	●	●	●	●	●	●	●	●	●	●	●	●	●	256	8		8/2		●	8	2		●	●	●	3	3	2		●	64	ZBT SSRAM	128	●	●		552 ball PBGA
ZL50111	●	●	●	●	●	●	●	●	●	●	●	●	●	1024	32		32/8		●	32	8	2	●	●	●	3	3	2		●	16	ZBT SSRAM	128	●	●		552 ball PBGA
ZL50114	●	●	●	●	●	●	●	●	●	●	●	●	●	128	4		4/1		●	4	1		●	●	●	3	3	2		●	128	ZBT SSRAM	NA	●	●		552 ball PBGA

Application Boards

MEB90880	Evaluation board for the MT90880-1-2-3
ZLE50111	Evaluation board for the ZL50110-1-4