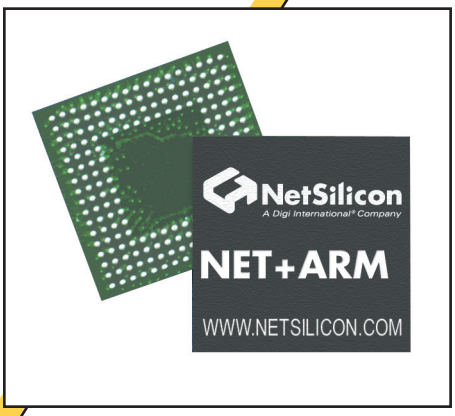
NetSilicon
A Digi International® Company

ADVANCED Product Brief

NET+ARM Processors

- **32-bit, 200MHz NET+ARM processor**
- **0.13µm CMOS process**
- **10/100Base-T Ethernet**
- **Extensive on-chip peripherals**
- **Comprehensive networking software**



NS9750

The NetSilicon NS9750 offers a whole new level of performance to network-attached processing. It provides full duplex 10/100Base-T Ethernet with more than enough additional processing performance and bandwidth to handle sophisticated embedded applications.

The NS9750 is based on the ARM 926EJ-S, ARM's most powerful ARM9 core, which contains both DSP and Java byte code instructions. It operates at up to 200MHz and contains a broad set of industry standard peripherals: USB, PCI, I²C, 1284, serial ports and a high-performance LCD controller.

The NS9750 is the latest member of NetSilicon's award wining NET+ARM family of 32-bit processors exclusively targeted at network enabling embedded electronic equipment. NetSilicon processors are all supported by our NET+Works® software development tool suite. The integrated NET+Works package contains either Green Hills MULTI or Microcross GNU X-Tools, a hardware debugger, Express Logic's ThreadX real time operating system, a TCP/IP stack, networking applications software, utilities, and numerous networking applications examples. NetSilicon is dedicated to making it easy for you to network enable your embedded device.

Features

32-bit high-performance processor

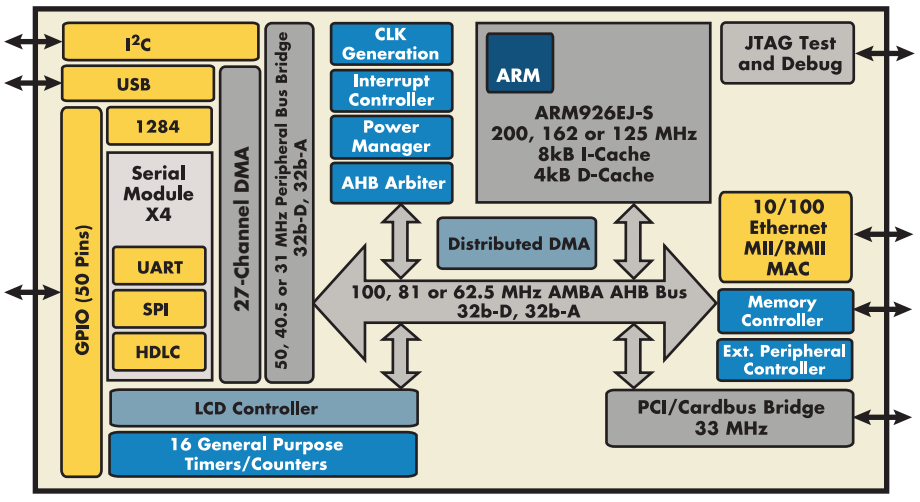
- 200MHz ARM926EJ-S with Harvard architecture 8k/4k Instruction/Data cache
- Integrated full-duplex 10/100Base-T Ethernet MAC
  - 2kB Rx & 256B Tx FIFOs with on-chip buffer descriptor ring SRAM
- 100 MHz memory controller, with glueless connection to SDRAM, DIMM, Flash, EEPROM, & SRAM
- High performance DMA system
- Embedded LCD controller
- PCI/Cardbus port for WLAN or external storage
- USB v2.0 Full-Speed Device or OHCI Host
- 4 multi-function serial ports, selectable UART, HDLC, or Master/Slave SPI mode
- I²C port, master or slave, normal (100kHz) or fast (400kHz) modes with clock stretching
- Programmable high-resolution timers/counters available on I/O
- External bus expansion module
- 50 general-purpose I/O (GPIO) pins
- Highly-configurable power management with sleep mode

Benefits

- Achieve dramatic time-to-market reductions with pre-integrated and tested NET+ARM hardware, NET+Works software, and tools.
- Reduce product unit costs with complete system-on-chip including Ethernet, display support, a robust peripheral set, and the processing headroom to meet the most demanding applications
- Save engineering resources - no networking development required
- Reduce design risk with fully integrated and tested solution

NS9750

352-pin BGA



Making DEVICE NETWORKING easy™

32-bit ARM926EJ-S RISC Processor

- 125, 162, or 200MHz
- 5-stage pipeline
- Harvard architecture
- 8kB I-Cache and 4kB D-Cache
- 32-bit ARM and 16-bit Thumb instruction sets, can be mixed for performance/code density tradeoffs
- MMU to support virtual memory based OS's such as Linux, WinCE/Pocket PC, VxWorks, etc.
- DSP instruction extensions, improved divide, single cycle multiply accumulate
- ARM Jazelle, 1200CM (Coffee Marks) Java Accelerator
- Embedded ICE-RT debug unit
- JTAG boundary scan

External System-Bus Interface

- 32-bit data bus, 32-bit internal address bus, 28-bit external address bus
- Glueless interface to SDRAM, SRAM, EEPROM, buffered DIMM, Flash
- Up to 64MB SDRAM, up to 2GB DIMM
- 4 static and 4 dynamic chip selects
- 0-63 wait states per chip select
- Self-refresh during system sleep
- Automatic dynamic bus sizing to 8-bits, 16-bits, 32-bits
- Burst-mode support with automatic data width adjustment
- 2 external DMA channels for external peripheral support

System Boot

- High-speed boot from 8-bit, 16-bit, or 32-bit ROM or Flash
- Hardware-supported low cost boot from serial EEPROM through SPI port (patent pending)

PCI/CardBus Port

- PCI v.2.2, 32-bit bus, up to 33MHz
- Programmable to:
  - PCI device mode
  - PCI host mode
  - CardBus host mode
- Internal rotating priority PCI bus arbiter, or external arbiter

Optimized 10/100 Ethernet MAC

- MII and RMII PHY interfaces
- Full- or half-duplex
- Station, broadcast, multicast address filtering
- 2kB Rx FIFO
- 256B Tx FIFO with on-chip Buffer Descriptor Ring (eliminates under-runs and decreases bus traffic)
- Separate Tx and Rx DMA channels
- Intelligent receive-side buffer size selection
- Full statistics gathering support
- External CAM filtering support

Flexible LCD Controller

- Supports most commercially available displays
- Active Matrix color TFT displays
  - Up to 24bpp direct 8:8:8 RGB; 16M colors
- Single and dual-panel color STN displays
- Up to 16bpp 4:4:4 RGB; 3375 colors
- Single and dual-panel monochrome STN displays
  - 1, 2, 4bpp palletized grayscale
- Formats image data and generates timing control signals
- Internal programmable palette-LUT and grayscaler support different color techniques
- Programmable panel-clock frequency

USB Ports

- USB v.2.0 Full Speed (12Mbps) and Low Speed (1.5Mbps)
- Configurable to Device or OHCI Host
- USB Host is a bus master
- USB Device supports one bi-directional control endpoint and 11 unidirectional endpoints
- Each endpoint is supported by a dedicated DMA channel, 13 total
- 20B Rx FIFO and 20B Tx FIFO

Serial Ports

- 4 serial modules, each independently configurable to
  - UART mode, HDLC mode, SPI Master mode, or SPI Slave mode
- Bit rates from 75bps to 921.6kbps: asynchronous x16 mode
- Bit rates from 1.2kbps to 6.25Mbps: synchronous mode
- UART provides
  - High-performance hardware and software flow control
  - Odd, even, or no parity
  - 5, 6, 7 or 8 bits
  - 1 or 2 stop bits
  - Receive-side character and buffer gap timers
- Internal or external clock support, digital PLL for Rx clock extraction
- 4 receive-side data match detectors
- 2 dedicated DMA channels per module, 8 total
- 32B Tx FIFO and 32B Rx FIFO per module

I²C Port

- I²C v.1.0, configurable to Master or Slave mode
- Bit rates: fast (400kHz) or normal (100kHz) with clock stretching
- 7-bit and 10-bit address modes

1284 Parallel Peripheral-to-Host Port

- All standard modes:
  - ECP, Byte, Nibble, Compatibility
- RLE (Run Length Encoding) decoding of compressed data in ECP mode
- Operating clock from 100kHz to 2MHz
- 4 dedicated DMA channels
  - 2 for data and 2 for control

System Bus DMA
- Every system bus peripheral is a bus master with dedicated DMA engine
- Intelligent bus bandwidth allocation (patent pending)

Peripheral Bus DMA
- One 13-channel engine supports USB Device
  - 2 DMA channels support control endpoint
  - 11 DMA channels support 11 endpoints
- One 12-channel engine supports
  - 4 serial modules (8 DMA channels)
  - 1284 parallel port (4 DMA channels)
- All DMA channels support fly-by mode

External Peripheral DMA
- One 2-channel DMA engine
- Each DMA channel supports memory-to-memory transfers

Power Management
- Patent pending technology
- Power save during normal operation
  - Disables unused modules
- Power save during sleep mode
  - Sets SDRAM to self-refresh mode
  - Disables all modules except selected wakeup modules
  - Wakeup on valid packets or characters

Vector Interrupt Controller
- Decreased bus traffic and rapid interrupt service
- Hardware interrupt prioritization

General Purpose Timers/Counters
- 16 independent 16-bit or 32-bit programmable timers or counters
  - Each has an I/O pin
- Mode selectable into:
  - Internal timer mode
  - External gated timer mode
  - External event counter
- Can be concatenated
- Can measure minute-range events
- Source clock selectable
  - Internal clock or external pulse event
  - Each can be individually enabled/disabled

System Timers
- Watchdog timer
- System bus monitor timer
- System bus arbiter timer
- Peripheral bus monitor timer

General Purpose I/O
- 50 programmable GPIO pins (muxed with other functions)
- Software-readable power-up status registers for every pin for customer-defined bootstrapping

External Interrupts
- 4 external programmable interrupts
  - Rising or falling - edge sensitive
  - Low or high-level sensitive

Clock Generator
- Low cost external crystal
- Internal phase locked loop (PLL)
- Software programmable PLL parameters
- Optional external oscillator
- Separate PLL for USB

Operating Voltage
- Core: 1.5V ± 0.1V
- I/O ring: 3.3V ± 10%

Operating Frequency
- 125MHz: 0° to 70° C
- 162MHz: -40° to +85° C
- 200MHz: 0° to 70° C

Power Consumption
- 200MHz: 1.9W (max.) - estimated

Package
- 352-pin BGA
- 1.27 mm ball pitch
- 35 mm x 35 mm

NET+Works Software Solutions

NET+Works Integrated Software
NET+ARM network attached processors are the core of the NET+Works Family of solutions that add intelligence and connectivity to electronic devices. NetSilicon offers a variety of solutions to support various applications.

Complete NET+Works Development package includes:
- ThreadX® picokernel RTOS
- Green Hills® MULTI® 2000 IDE or Microcross GNU X-Tools™
- Drivers, protocols and services
- NET+ARM Drivers (10/100Base-T Ethernet, UART, SPI, HDLC, I^2C, DMA, flash, USB host & device, LCD, PCI)

- **Networking protocols:**
  - TCP/IP stack
  - TCP and UDP Sockets API
  - ICMP
  - IGMP
  - PPP for serial communications
  - RARP
  - Ping ARP
  - AutoIP
  - DHCP client
  - BootP
  - Fast IP
  - Fast sockets
  - SSL, TLS

- **NS9750 Development Board and JTAG Probe**

- **Networking services:**
  - FTP server
  - FTP client
  - LDAP agent, for access to network information services
  - HTTP API's for serving basic advanced web pages, HTTPS for security
  - Email (POP and SMTP)
  - SNMP v1/MIBII for remote management
  - SNTP
  - DNS
  - Telnet
  - Multi-homing

- **Utilities:**
  - HTML compilation
  - MIB compilation
  - Download of flash images
  - Code builds
  - Integrated flash file system
  - Code Profiler
  - Boundary Scan Description Language (BSDL)
  - One-year software maintenance and technical support available

Product/Part Number

125MHz	TBD
162MHz	TBD
200MHz	TBD

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