Giantplus
Technology

Design Specification of LCD Module

Product No.: GPM302A0

Customer Approval	

Approved by	Checked by	Organized by
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Approval for specifications only

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1. GENERAL DESCRIPTION

The GPM302A0 is a 128x64 dot-matrix LCD module. It has a FSTN panel composed of 128 segments and 64 commons. The LCM can be easily accessed by microcontroller via interface.

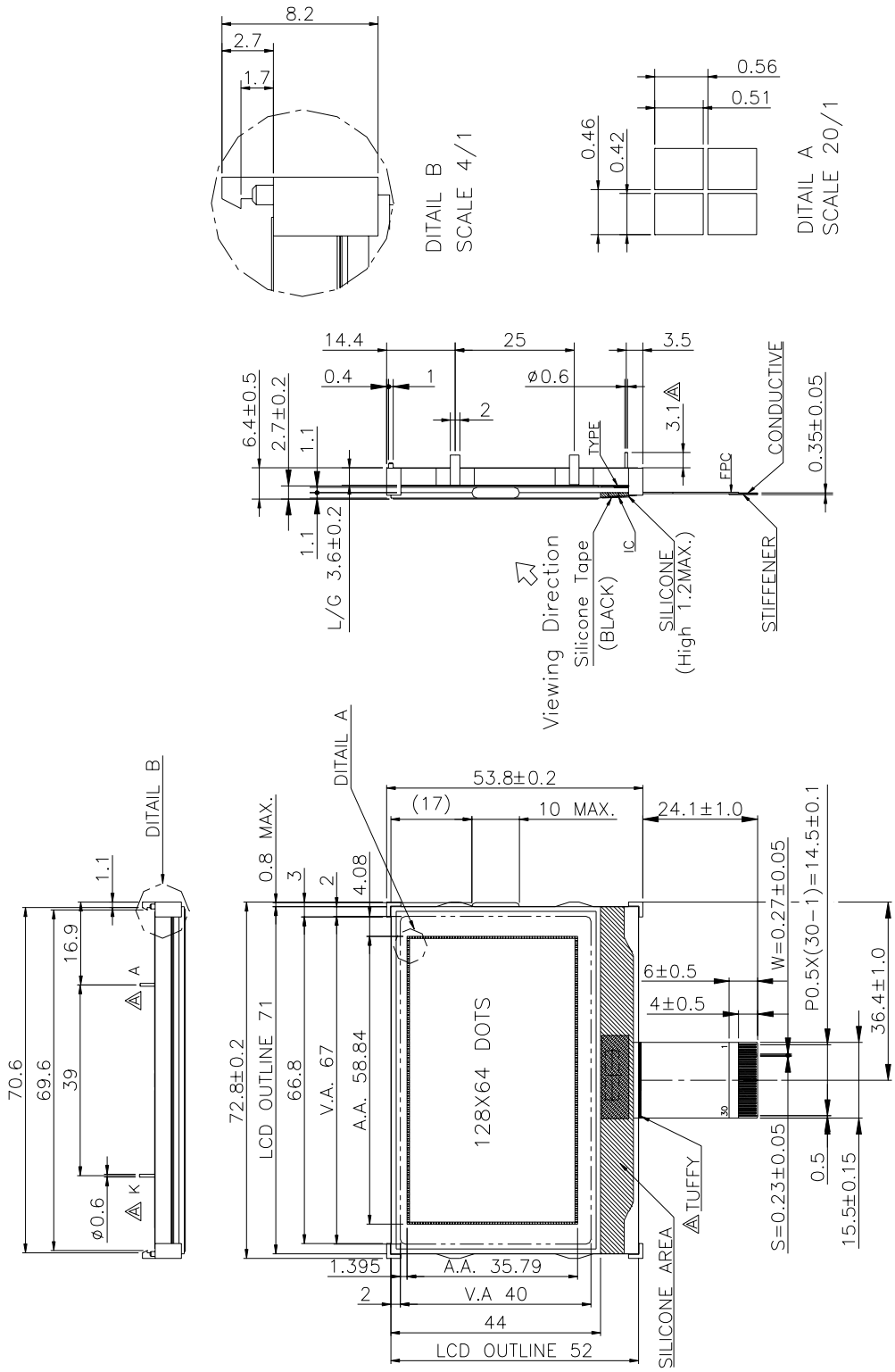
2. FEATURES

Display Mode	Transflective and positive type
	Black/White Mode FSTN LCD
Display Format	Graphic 128 × 64 Dot-matrix
Input Data	68/80 or series data input from MPU
Multiplexing Ratio	1/64 Duty
Viewing Direction	6 O'clock
Backlight	White LED

3. MECHANICAL SPECIFICATION

Item	Specifications	Unit
Outline Dimensional	72.8(W) ×53.8(H) ×6.4(D)	mm
Resolution	128×64	dots
Active area	58.84(W)×35.79(H)	mm
View area	67.0(W)×40.0(H)	mm
Dots pitch	0.46(W)×0.56(H)	mm
Dots size	0.42(W)×0.51(H)	mm

4. MECHANICAL DIMENSION



5. MAXIMUM RATINGS

Item	Symbol	Min	Max	Unit	Note
Supply voltage	V_{DD}	-0.3	7.0	V	
	V_{LCD}	-13.2	0.3	V	
Input Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Operating temperature	T_{OPR}	0	50	℃	
Storage temperature	T_{STR}	-10	60	℃	1
Humidity	-	-	90	%RH	2

6. ELECTRICAL CHARACTERISTICS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	
Supply Voltage	Logic	V_{DD}	-	3.3		5	V	Note1
Input Voltage	H level	V_{IH}	-	$0.7V_{DD}$	-	V_{DD}	V	
	L level	V_{IL}		V_{SS}	-	$0.3V_{DD}$		
Current Consumption		I_{DD}	With internal V_{LCD} generation; V_{DD}=3.3V; V_{LCD}=9.0V; f_{sclk}=0; T_{amb}=25℃; 4x charge pump	-	1.0	1.5	mA	
LCD Driving Voltage		V_{LCD}	Bias=1/9	8.4	8.8	9.2	V	Note2
LED Driving Voltage		V_{LED}	-	-	TBD	-	V	
LED Current Consumption		I_{LED}	V_{LED}=2.1V	-	TBD	--	mA	

Note1:V_{DD} must depend on set-up voltage (2X~4X), (V_{DD} -V_{OUT}) can't be over 13.2V

Note:2

1.The internal resistor ratio is set to 00100100B
2. The Electronic volume register is set to 00011000B
3.VLCD has ± 3 % tolerance , so it can be adjustable by setting two parameters.

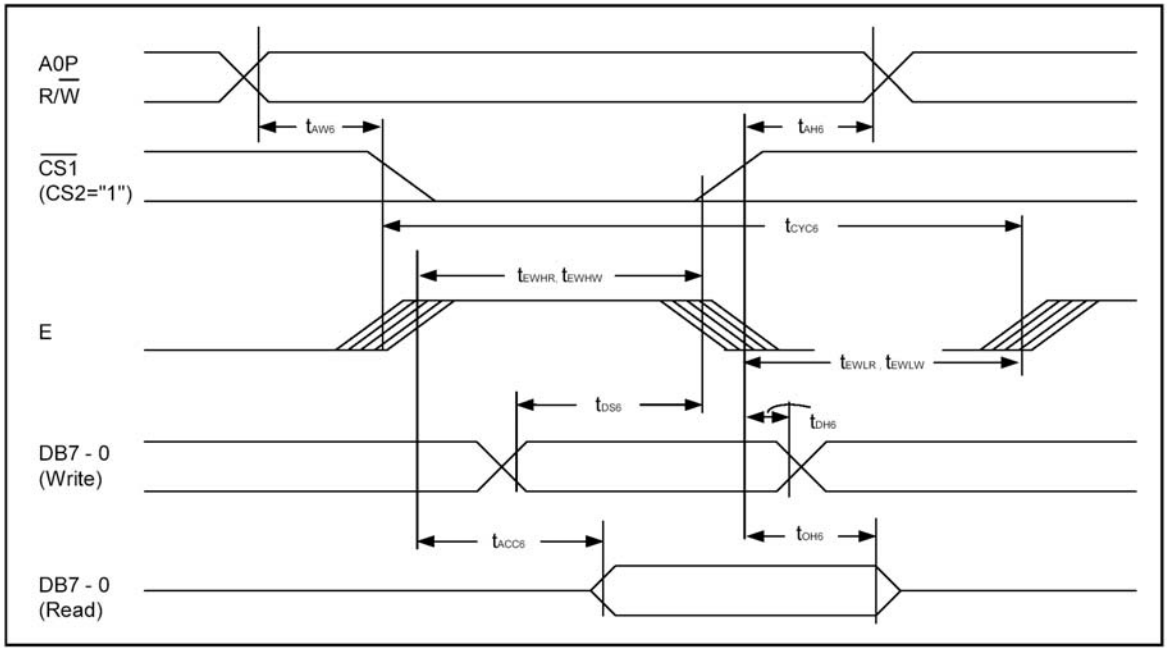
7. MODULE FUNCTION DESCRIPTION

7.1. PIN DESCRIPTION

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1.	/CS1	CHIP SELECT	16.	VOUT	DC/DC VOLTAGE CONVERTER
2.	/RES	RESET SIGNAL	17.	CAP3-	
3.	A0	DATA/COMMAND SELECT	18.	CAP1+	
4.	R/W	READ/WRITE SIGNAL FOR 6800 MPU	19.	CAP1-	
	WR	WRITE SIGNAL FOR 8080 MPU			
5.	EP	ENABLE CLOCK FOR 6800 MPU	20.	CAP2-	
	/RD	READ SIGNAL FOR 8080 MPU			
6.	DB0	8-BITS DATA BUS LINES	21.	CAP2+	
7.	DB1		22.	V1	POWER SUPPLY FOR LCD
8.	DB2		23.	V2	
9.	DB3		24.	V3	
10.	DB4		25.	V4	
11.	DB5		26.	V5	
12.	DB6	8-BITS DATA BUS LINES	27.	VR	OUT VOLTAGE REGULAR TERMINAL
	SCL	SERIAL CLOCK INPUT			
13	DB7	8-BITS DATA BUS LINES	28.	C86	C86=”H”: 6800 MPU SERIES C86=”L”: 8080 MPU SERIES
	SI	SERIAL DATA INPUT			
14	VDD	POWER SUPPLY (LOGIC)	29.	PS	PS=”H”: PARALLEL PS=”L”: SERIAL
15	VSS	POWER SUPPLY (GND)	30.	/IRS	IRS=”H”: USE INTERNAL RESISTOR IRS=”L”: NOT USE INTERNAL RESISTOR

7.2. TIMING CHARACTERISTICS

1.SYSTEM BUS READ/WRITE CHARACTERISTIC (6800 SERIES MPU)



(VDD = 4.5V to 5.5V, T_A = -40 to 85℃)

Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time		A0P	t_{AH6}		0	-	ns
Address setup time			t_{AW6}		0	-	ns
System cycle time		A0P	t_{CYC6}		166	-	ns
Data setup time		DB7 - 0	t_{DS6}	C_L = 100 pF	30	-	ns
Data hold time			t_{DH6}		10	-	ns
Access time			t_{ACC6}		-	70	ns
Output disable time			t_{OH6}		10	50	ns
Enable H pulse time	Read	E	t_{EWHR}		70	-	ns
	Write		t_{EWHW}		30	-	ns
Enable L pulse time	Read	E	t_{EWLR}		30	-	ns
	Write		t_{EWLW}		30	-	ns

(VDD = 2.7V to 4.5V, T_A = -40 to 85℃)

Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time		A0P	t_{AH6}		0	-	ns
Address setup time			t_{AW6}		0	-	ns
System cycle time		A0P	t_{CYC6}		300	-	ns
Data setup time		DB7 - 0	t_{DS6}	C_L = 100 pF	40	-	ns
Data hold time			t_{DH6}		15	-	ns
Access time			t_{ACC6}		-	140	ns
Output disable time			t_{OH6}		10	100	ns
Enable H pulse time	Read	EP	t_{EWHR}		120	-	ns
	Write		t_{EWHW}		60	-	ns
Enable L pulse time	Read	EP	t_{EWLR}		60	-	ns
	Write		t_{EWLW}		60	-	ns

(VDD = 2.4V to 2.7V, T_A = -40 to 85℃)

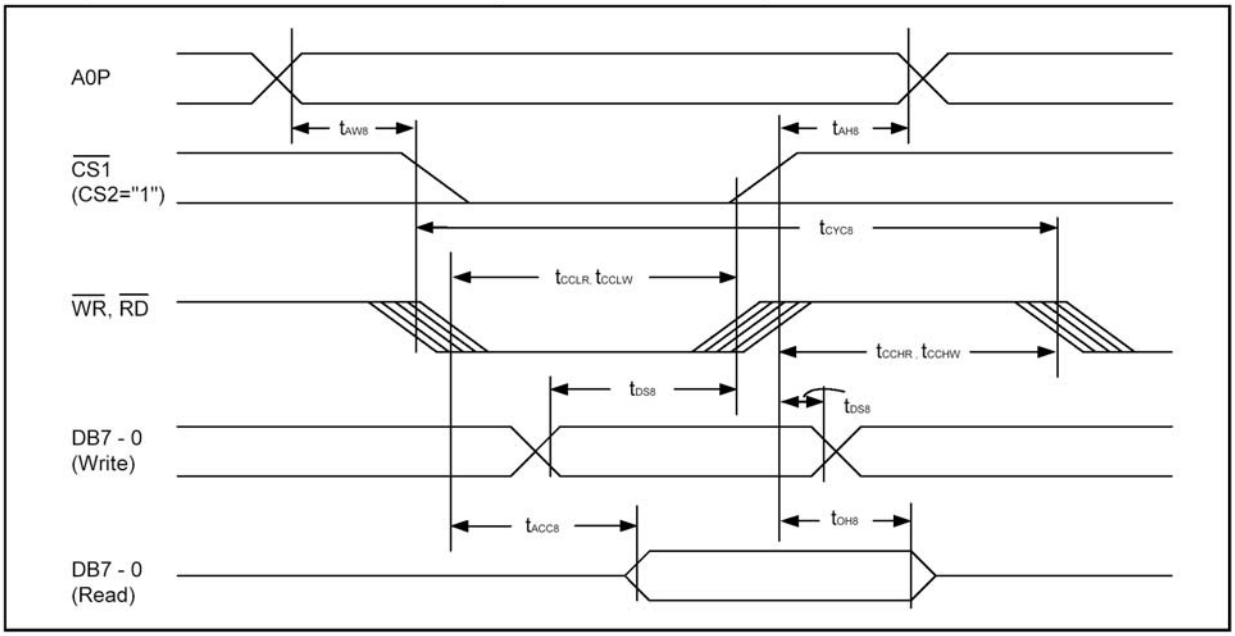
Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time		A0P	t_{AH6}		0	-	ns
Address setup time			t_{AW6}		0	-	ns
System cycle time		A0P	t_{CYC6}		1000	-	ns
Data setup time		DB7 - 0	t_{DS6}	C_L = 100 pF	80	-	ns
Data hold time			t_{DH6}		30	-	ns
Access time			t_{ACC6}		-	280	ns
Output disable time			t_{OH6}		10	120	ns
Enable H pulse time	Read	EP	t_{EWHR}		240	-	ns
	Write		t_{EWHW}		120	-	ns
Enable L pulse time	Read	EP	t_{EWLR}		120	-	ns
	Write		t_{EWLW}		120	-	ns

Note1: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leq (t_{CYC6} - t_{EWLW} - t_{EWHW})$ for $(t_r + t_f) \leq (t_{CYC6} - t_{EWLR} - t_{EWHR})$ are specified.

Note2: All timing is specified using 20% and 80% of VDD as the reference.

Note3: t_{EWLW} and tEWLR are specified as the overlap between CS1 being 'L' (CS2 = 'H') and E.

2.SYSTEM BUS READ/WRITE CHARACTERISTIC (8080 SERIES MPU)



(VDD = 4.5V to 5.5V, T_A = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0P	t_{AH8}		0	-	ns
Address setup time		t_{AW8}		0	-	ns
System cycle time	A0P	t_{CYC8}		166	-	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		30	-	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		70	-	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		30	-	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		30	-	ns
Data setup time	DB7 - 0	t_{DS8}		30	-	ns
Address hold time		t_{DH8}		10	-	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100pF	-	70	ns
Output disable time		t_{OH8}		5.0	50	ns

(VDD = 2.7V to 4.5V, T_A = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0P	t_{AH8}		0	-	ns
Address setup time		t_{AW8}		0	-	ns
System cycle time	A0P	t_{CYC8}		300	-	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		60	-	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		120	-	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		60	-	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		60	-	ns
Data setup time	DB7 - 0	t_{DS8}		40	-	ns
Address hold time		t_{DH8}		15	-	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100pF	-	140	ns
Output disable time		t_{OH8}		10	100	ns

(VDD = 2.4V to 2.7V, T_A = 25℃)

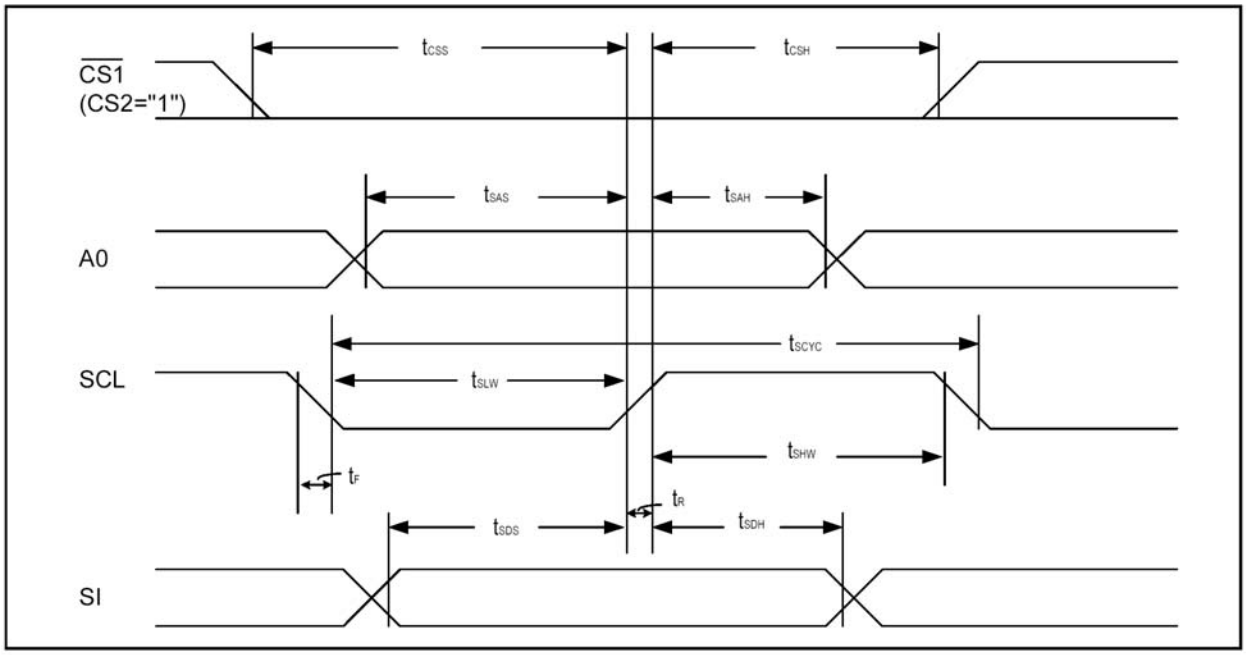
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0P	t_{AH8}		0	-	ns
Address setup time		t_{AW8}		0	-	ns
System cycle time	A0P	t_{CYC8}		1000	-	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		120	-	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		240	-	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		120	-	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		120	-	ns
Data setup time	DB7 - 0	t_{DS8}		80	-	ns
Address hold time		t_{DH8}		30	-	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100pF	-	280	ns
Output disable time		t_{OH8}		10	200	ns

Note1: The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leqq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ for $(t_r + t_f) \leqq (t_{CYC8} - t_{CCLR} - t_{CCHR})$ are specified.

Note2: All timing is specified using 20% and 80% of VDD as the reference.

Note3: t_{CCLW} and t_{CCLR} are specified as the overlap between $\overline{CS1}$ being 'L' (CS2 = 'H') and $\overline{WR}$ and $\overline{RD}$ being at the 'L' level.

3.SYSTEM BUS READ/WRITE CHARACTERISTIC (SERIAL SERIES MPU)



(VDD = 4.5V to 5.5V, T_A = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}	-	200	-	ns
SCL 'H' pulse width		t_{SHW}	-	75	-	ns
SCL 'L' pulse width		t_{SLW}	-	75	-	ns
Address setup time	A0P	t_{SAS}	-	50	-	ns
Address hold time		t_{SAH}	-	100	-	ns
Data setup time	SI	t_{SDS}	-	50	-	ns
Data hold time		t_{SDH}	-	50	-	ns
CS-SCL time	CS	t_{CSS}	-	100	-	ns
		t_{CSH}	-	100	-	ns

(VDD = 2.7V to 4.5V, T_A = 25℃)

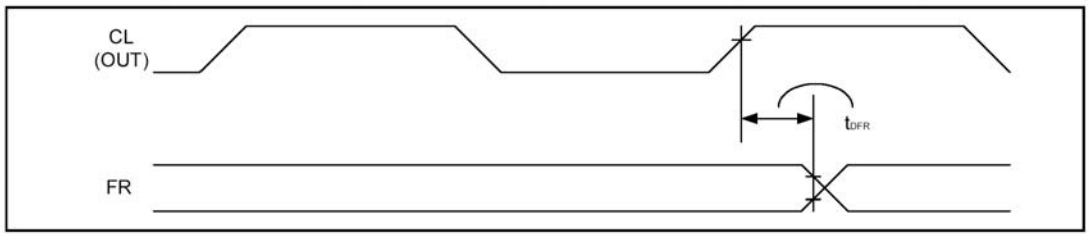
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC	-	250	-	ns
SCL 'H' pulse width		tSHW	-	100	-	ns
SCL 'L' pulse width		tSLW	-	100	-	ns
Address setup time	A0P	tSAS	-	150	-	ns
Address hold time		tSAH	-	150	-	ns
Data setup time	SI	tSDS	-	100	-	ns
Data hold time		tSDH	-	100	-	ns
CS-SCL time	CS	tCSS	-	150	-	ns
		tCSH	-	150	-	ns

(VDD = 2.4V to 2.7V, TA = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}	-	400	-	ns
SCL 'H' pulse width		t_{SHW}	-	150	-	ns
SCL 'L' pulse width		t_{SLW}	-	150	-	ns
Address setup time	A0P	t_{SAS}	-	250	-	ns
Address hold time		t_{SAH}	-	250	-	ns
Data setup time	SI	t_{SDS}	-	150	-	ns
Data hold time		t_{SDH}	-	150	-	ns
CS-SCL time	CS	t_{CSS}	-	250	-	ns
		t_{CSH}	-	250	-	ns

Note1: The input signal rise and fall time (t_r, t_f) are specified at 15 ns or less.
Note2: All timing is specified using 20% and 80% of VDD as the standard.

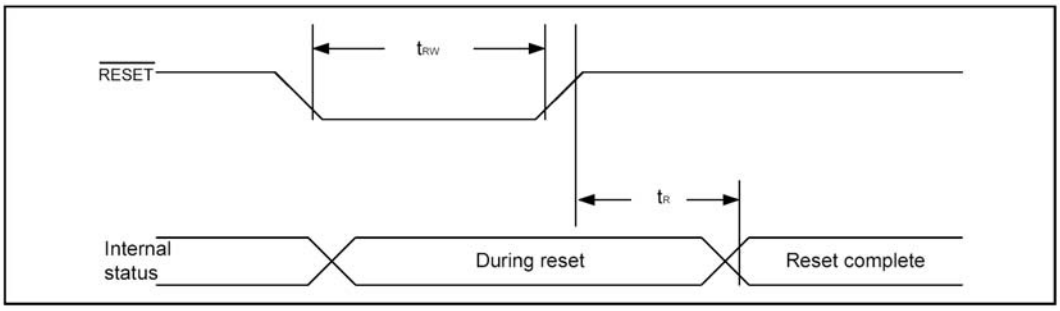
4.DISPLAY CONTROL OUTPUT TIMING



(VDD = 4.5V to 5.5V, T_A = -40 to 85℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L = 50pF	-	10	40	ns

5.RESET TIMING



(VDD = 4.5V to 5.5V, T_A = -40 to 85℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R	-	-	-	0.5	μs
Reset 'L' pulse width	RES	t_{RW}		0.5	-	-	μs

(VDD = 2.7V to 4.5V, T_A = -40 to 85℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R	-	-	-	1.0	μs
Reset 'L' pulse width	RES	t_{RW}		1.0	-	-	μs

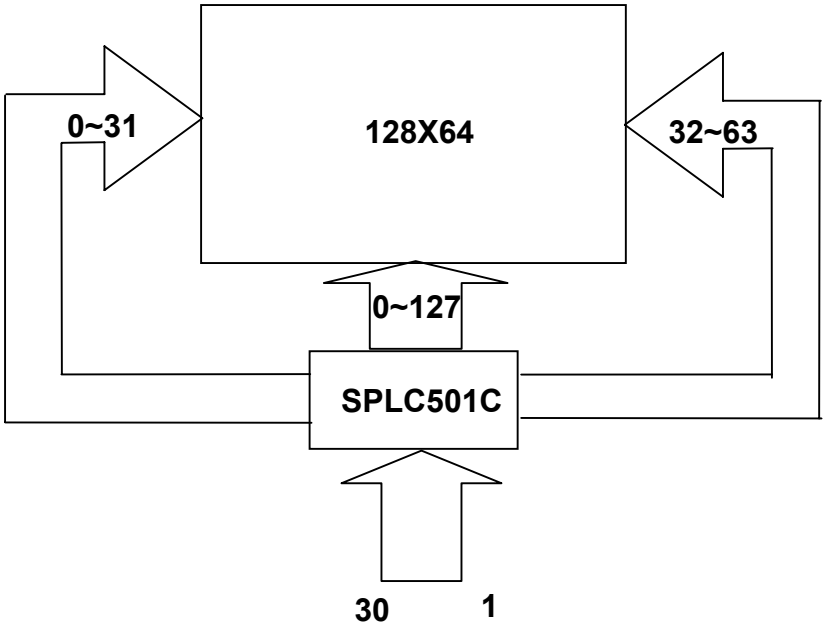
Note2: All timing is based on 20% and 80% of VDD.

(VDD = 2.4V to 2.7V, T_A = -40 to 85℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R	-	-	-	1.5	μs
Reset 'L' pulse width	RES	t		1.5	-	-	μs

Note: All timing is specified with 20% and 80% of VDD as the standard.

7.3. BLOCK DIAGRAM OF LCM



7.4. APPLICATION OF LCM

■ DISPLAY DATA RAM

— Display Data RAM

The display data RAM is a RAM that stores the dot data for the display. It has a 65 (8 page x 8 bit +1) x 132 bit structure. It is possible to access the desired bit by specifying the page address and the column address. Because, as is shown in Figure 3, the DB7 - 0 display data from the MPU corresponds to the liquid crystal display common direction, there are few constraints at the time of display data transfer when multiple SPLC501A chips are used. Therefore, display structures can be created easily and with a high degree of freedom.

Moreover, reading from and writing to the display RAM in the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

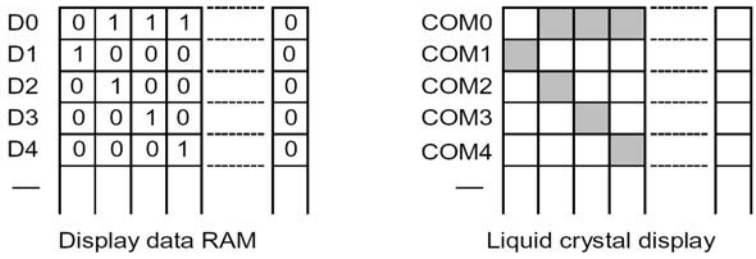


Figure 2

— The Page Address Circuit

As shown in Figure 3, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access. Page address 8 (DB3, DB2, DB1, DB0 = 1, 0, 0, 0) is the page for the RAM region used only by the indicators, and only display data DB0 is used.

— The Column Addresses

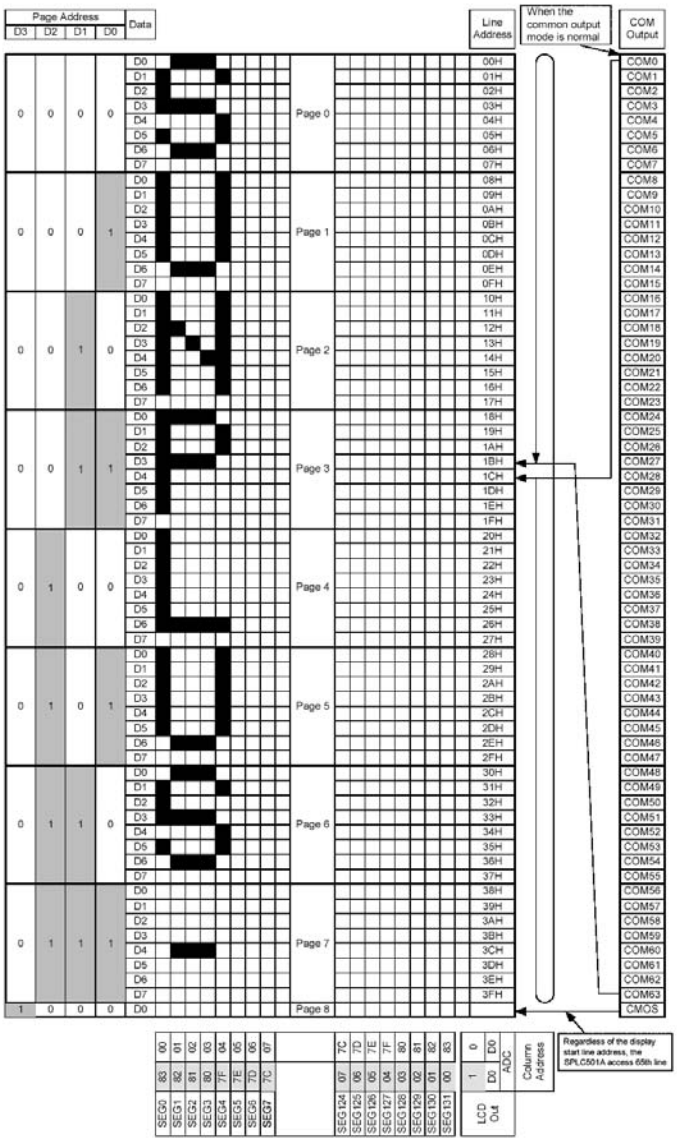
As is shown in Figure 3, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously. Moreover, the increment of column addresses stops with 83H. Because the column address depends on the page address, it is necessary to re-specify both the page address and the column address when moving, for example, from page 0 column 83H to page 1 column 00H. Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized.

Table 4

SEG Output	SEG0 SEG131
ADC '0'	0 (H) → Column Address →83(H)
(DB0) '1'	83(H) ← Column Address ← 0(H)

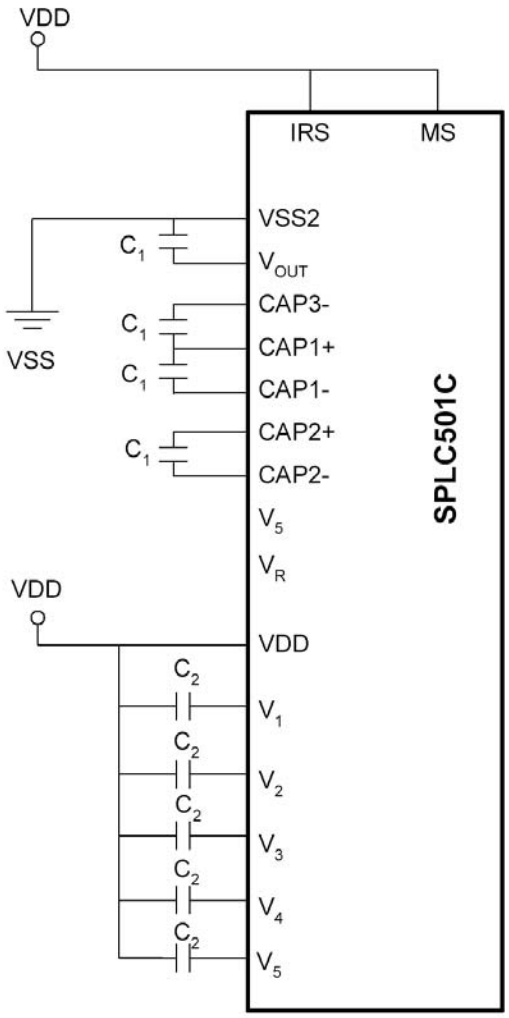
— **The Line Address Circuit**

The line address circuit, as shown in Figure 3, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, which is normally the top line of the display can be specified. This is the COM0 output when the common output mode is normal, and the COM63 output for SPLC501A when the common output mode is reversed. The display area is a 65-line area for the SPLC501A from the display start line address. If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, ...etc. can be performed.



■Reference circuit

When the voltage regulator internal resistor is used.
Example where VSS2 = VSS, with 4x step-up



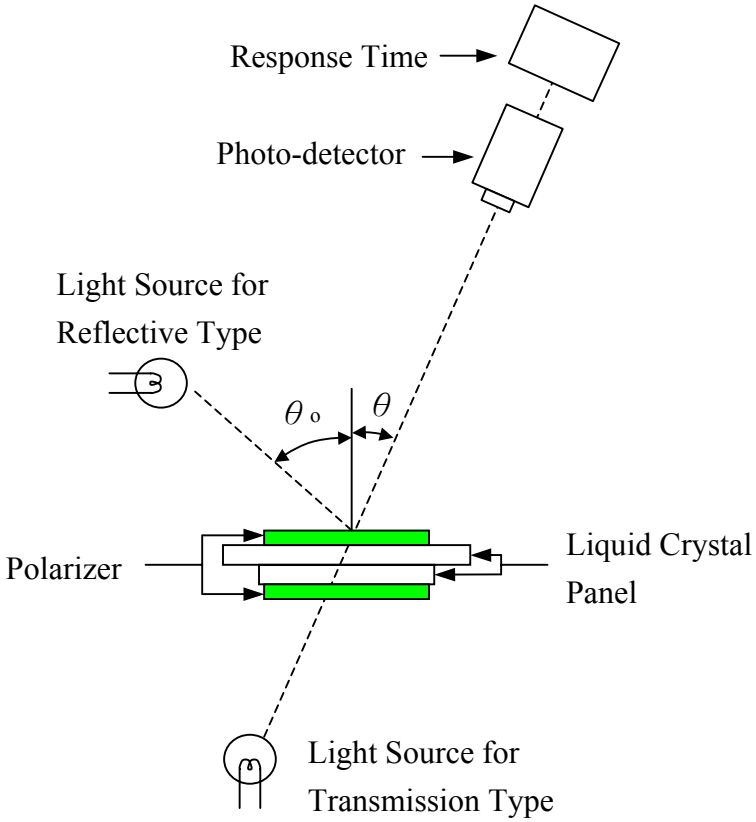
Note: It is recommended that C1=1.0μF ~4.7μF and C2=0.1μF ~1.0μF

8. ELECTRO-OPTICAL CHARACTERISTICS

Item	Symbol	Condition	Temp	Min	Typ	Max	Units	Note
LCD driving voltage	V_{LCD}	$\theta = \phi = 0$	0℃	---	9.0	---	V	
			25℃	8.4	8.8	9.2		
			50℃	---	8.6	---		
Response Time	Rise Time (Tr)	$\theta = \phi = 0$	0℃	---	610	920	msec	
	Decay Time (Td)			---	630	950		
	Rise Time (Tr)		25℃	---	150	230		
	Decay Time (Td)			---	180	270		
	Rise Time (Tr)		50℃	---	80	120		
	Decay Time (Td)			---	90	140		
Contrast Ratio	Cr	$\theta = \phi = 0$	25℃	4	8	---	---	

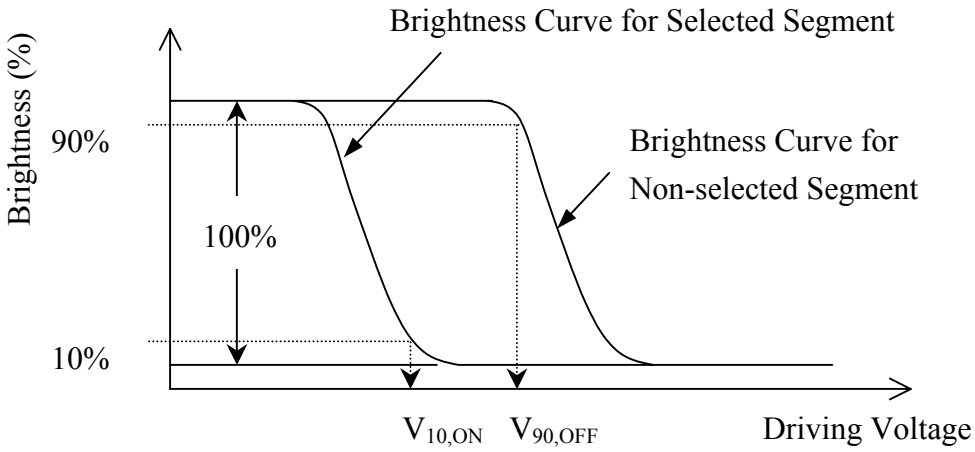
Viewing Angle Range	ϕ = 0° (6”)	ϕ = 90° (3”)	ϕ =180° (12”)	ϕ =270° (9”)	備註
θ (25℃) CR≥2	30	35	55	40	Deg Note3

- Electro-Optical Characteristics Test Method

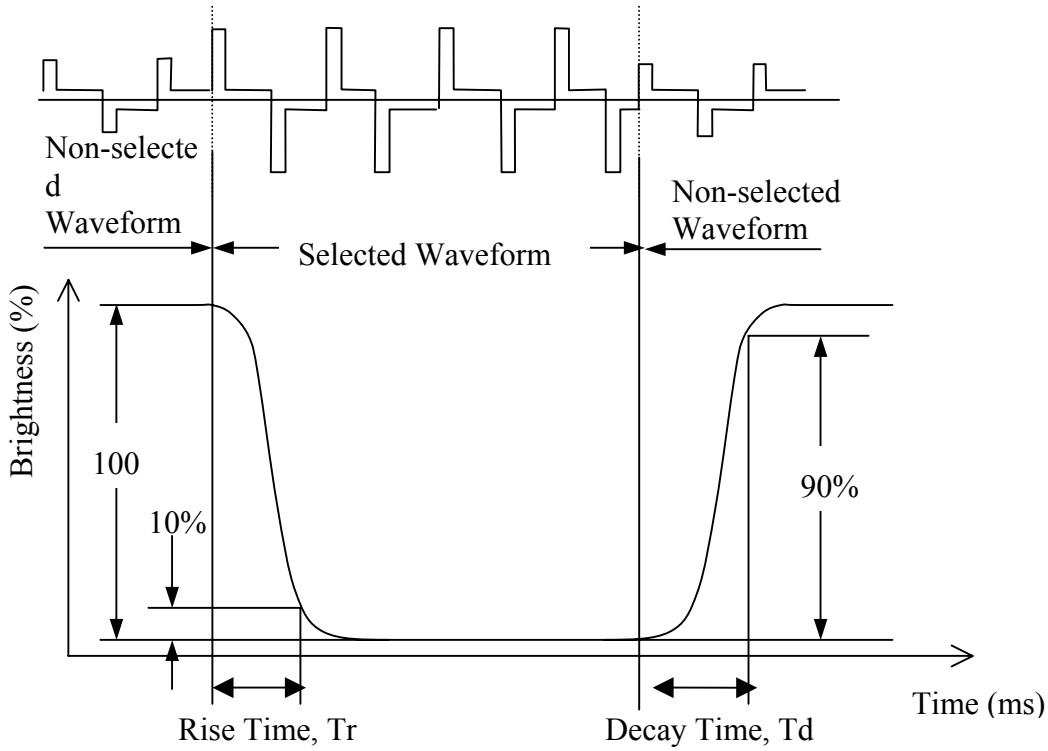


- **Note 1. Definition of Driving Voltage(Vlcd) :**

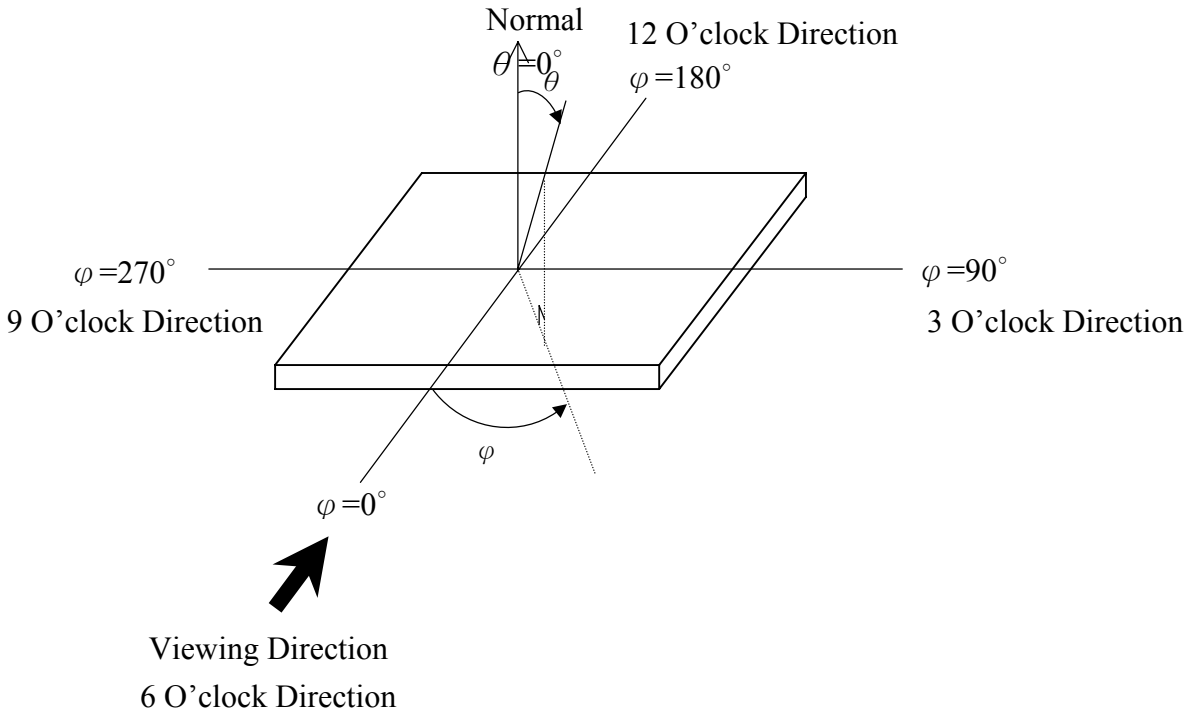
  $Vlcd = (V_{10,ON} + V_{90,OFF})/2$



- **Note 2. Definition of Optical Response Time:**



• Note 3. Definition of Viewing Angle θ and ϕ :



• Note 4. Definition of Contrast ratio (CR):

$$CR = \frac{\text{Brightness of Non-selected Segment (B2)}}{\text{Brightness of Selected Segment (B1)}}$$