SPECIFICATIONS FOR LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	**SED1353 Control Board**
APPROVED BY	
DATE	

APPROVED BY	CHECKED BY	ORGANIZED BY

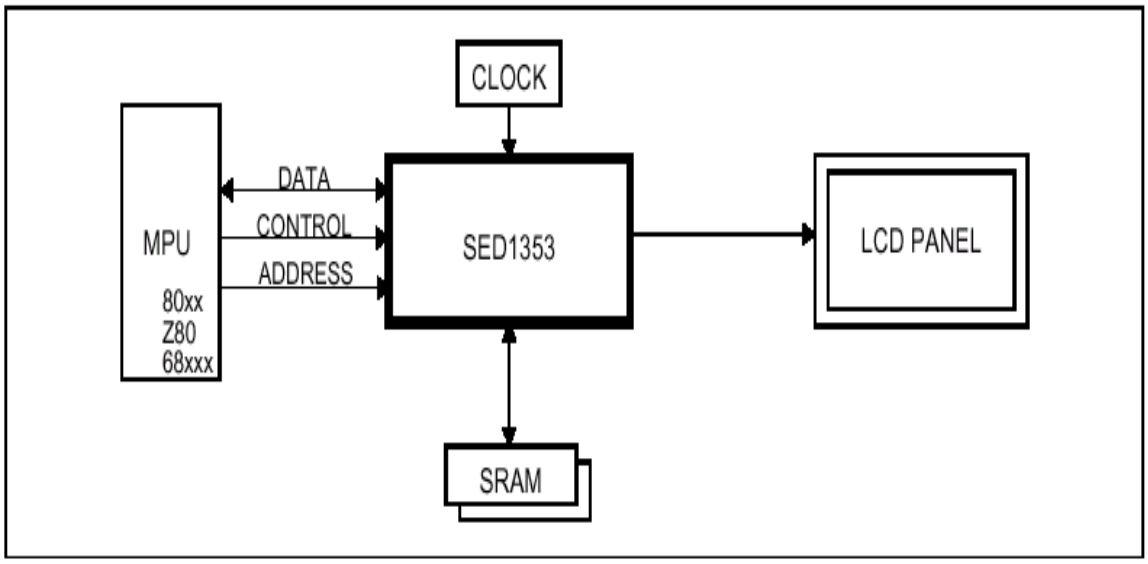
RECORD OF REVISION

Revision Date	Contents
2002/5/23	New Release

1 Features

- Controller: SED1353F1A
- Maximum 25Mhz input clock (or pixel clock).
- Power Supply for Logic : 2.7 V to 5.5 V
- 8 bit MPU interface only.
- 128K bytes using tow 64k x 8 SRAM.
- 2/4/8 bits-per-pixel,4/16/256 level color display modes.
- Two software power-save modes.
- Low power consumption.
- Panel power control switch.
- Example resolution:
  -1024x768 black&white.
  -640x480 with 4 color/grays.
  -640x400 with 16 color/grays.
  -320x240 with 256 colors.

SYSTEM BLOCK DIAGRAM



2 Electrical Characteristics

Maximum Ratings

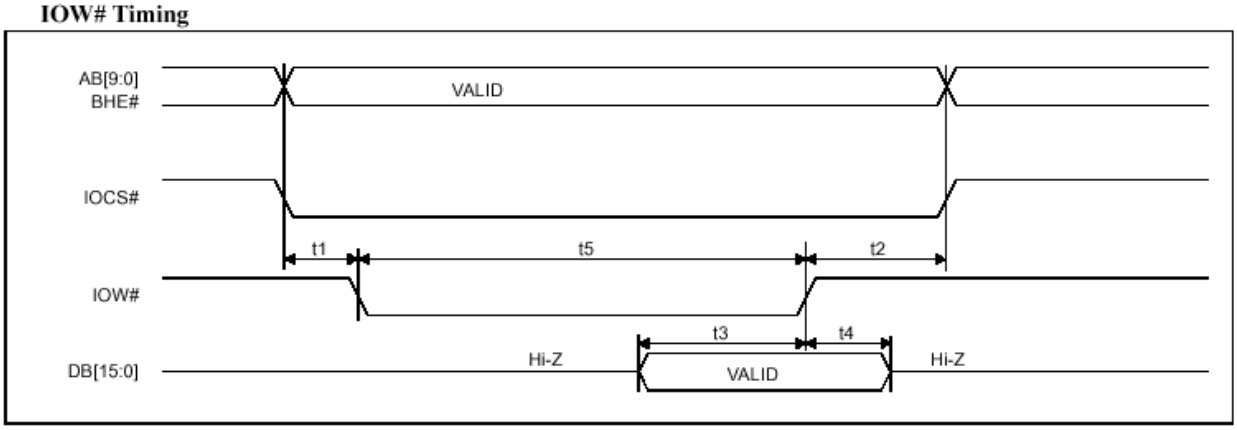
Parameter	Symbol	Condition	Min	Max	Unit
Logic Power Supply	VCC	Ta=25	2.7	5.5	V
Input Voltage Range	VIN		-0.3	VDD+0.3	V
Operating Temperature	Topg		-40	85	Deg.C
Storage Temperature	Tstg		-65	150	Deg.C

Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	VCC	Note4	3.0	3.3	5.5	V
Input Leakage Current	ILI	Note3	-1	-	1	µA
Output Leakage Current	ILO		-1	-	1	µA
Operating Supply Current	Iopr(6Mhz)	Note2		5	11	mA
Oscillator frequency	fosc			-	25.0	MHz

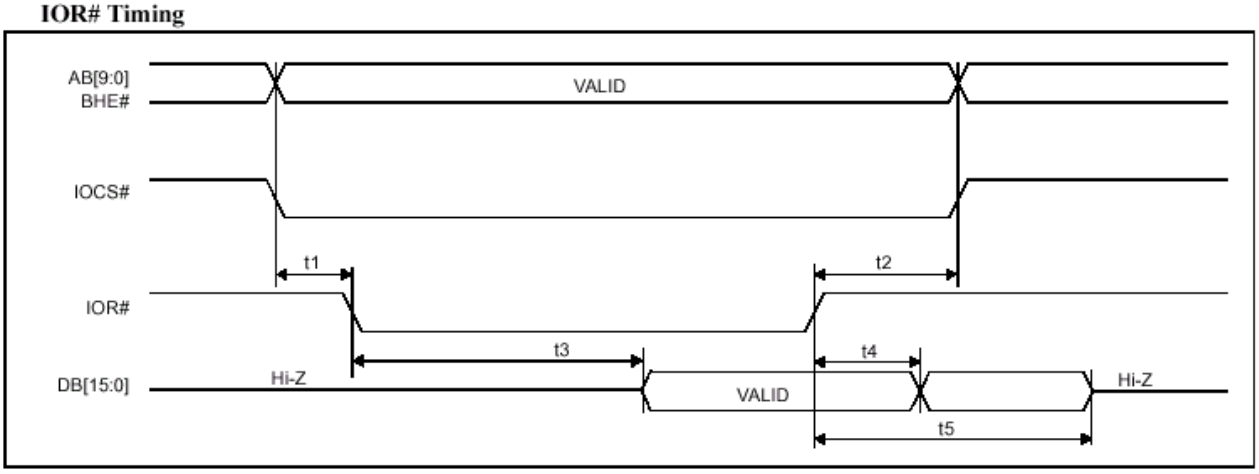
AC Timing Characteristics

IOW# Timing



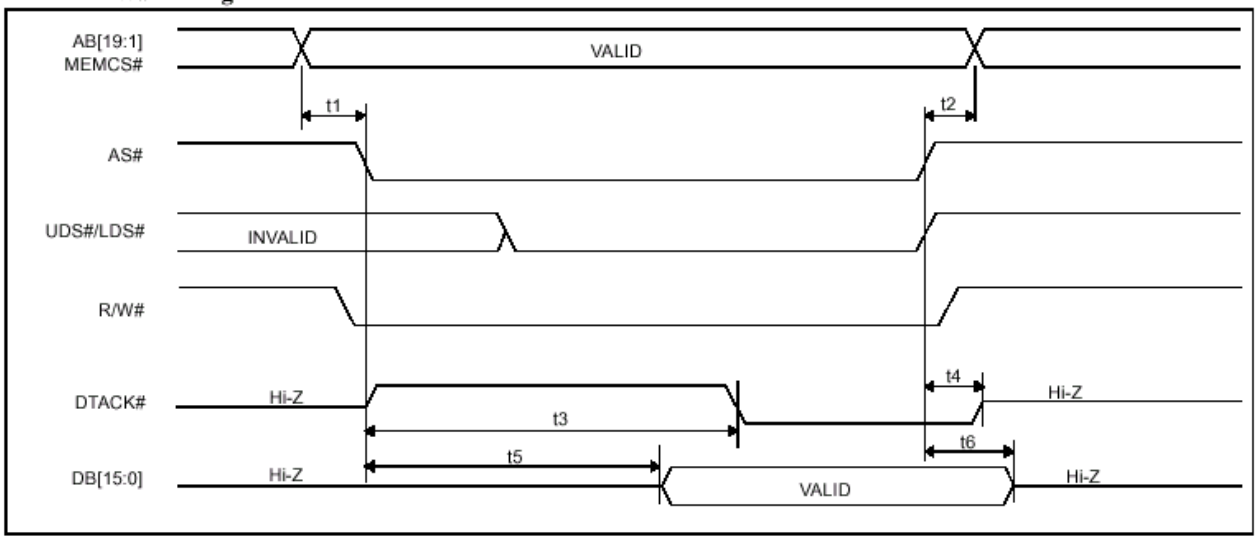
		3V/3.3V		5V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
t1	AB[9:0], BHE# and IOCS# valid before IOW# falling edge	10		0		ns
t2	AB[9:0], BHE# and IOCS# hold from IOW# rising edge	20		10		ns
t3	DB[15:0] setup to IOW# rising edge	20		10		ns
t4	DB[15:0] hold from IOW# rising edge	20		10		ns
t5	Pulse width of IOW#	30		20		ns

IOR# Timing



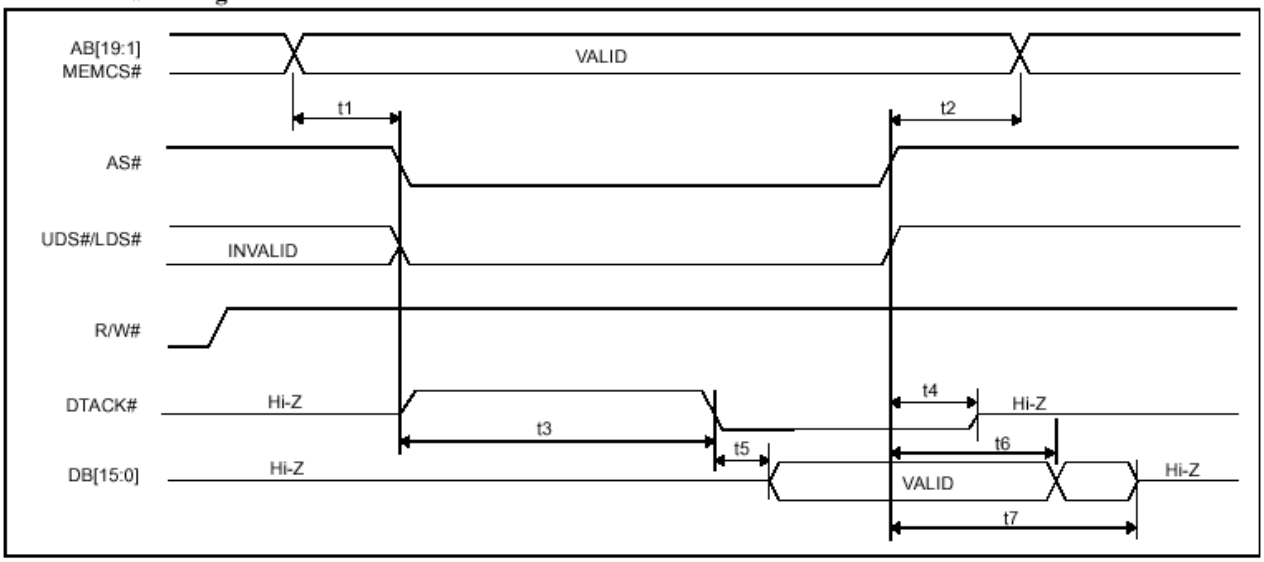
		3V/3.3V		5V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
t1	AB[9:0], BHE# and IOCS# valid before IOR# falling edge	10		0		ns
t2	AB[9:0], BHE# and IOCS# hold from IOR# rising edge	20		10		ns
t3	IOR# falling edge to DB[15:0] valid		60		40	ns
t4	DB[15:0] hold from IOR# rising edge		20		15	ns
t5	IOR# rising edge to DB[15:0] hi-z delay		35		25	ns

MEMW# Timing



		3V/3.3V		5V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
t1	AB[19:1] and MEMCS# valid before AS# falling edge	0		0		ns
t2	AB[19:1] and MEMCS# hold from AS# rising edge	0		0		ns
t3	AS# falling edge to DTACK# falling edge		3.5 * MCLK + 20		3.5 * MCLK + 10	ns
t4	AS# rising edge to DTACK hi-z delay		40		25	ns
t5	AS# falling edge to DB[15:0] valid		MCLK -40		MCLK -20	ns
t6	DB[15:0] hold from AS# rising edge	0		0		ns

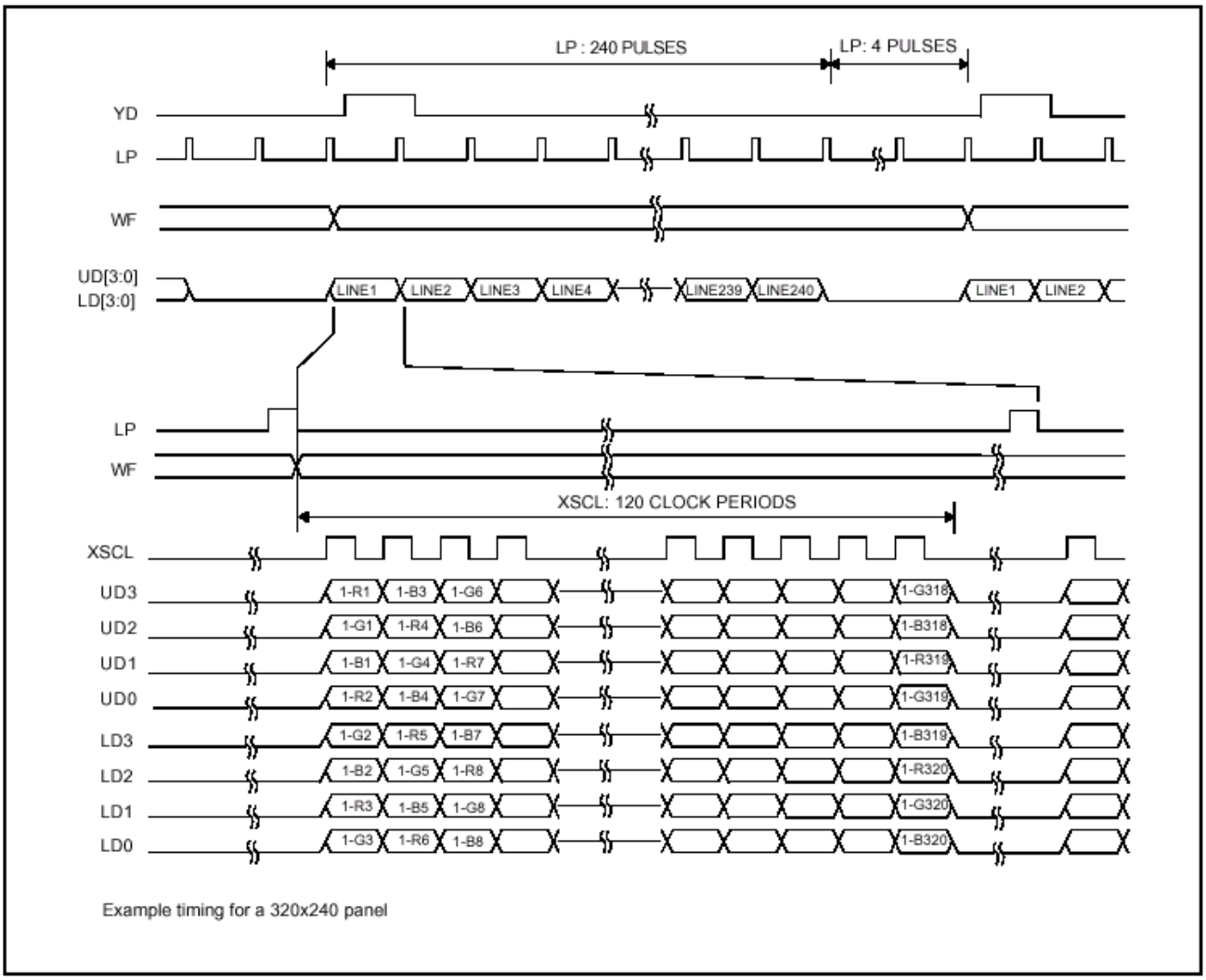
MEMR# Timing



		3V/3.3V		5V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
t1	AB[19:1] and MEMCS# valid before AS# falling edge	0		0		ns
t2	AB[19:1] and MEMCS# hold from AS# rising edge	0		0		ns
t3	AS# falling edge to DTACK# falling edge		3.5 * MCLK + 20		3.5 * MCLK + 10	ns
t4	AS# rising edge to DTACK# hi-z delay		40		15	ns
t5	DTACK# falling edge to DB[15:0] valid		20		15	ns
t6	DB[15:0] hold from AS# rising edge		25		15	ns
t7	AS# rising edge to DB[15:0] hi-z delay		40		30	ns

LCD Interface Time Diagram

.Example for 320x240 Dots (256 Colors).



8-Bit single color panel timing-Format2:AUX[03]Bit3=1 and AUX[01]Bit2=1.

Interface Definition

CN1 Interface:

PIN NO.	SIGNAL	LEVEL	FUNCTION
1~12	AD8~19	H/L	Address Bus, AD8~AD19 Should be set to Low.
13	/ALE	H/L	Latch lower Address bus AD[0~7]from DB[0~7] .
14	/IOCS	H/L	Active low input to select one of sixteen internal
15	/MECS	H/L	Active low input to indicate a memory cycle.
16	/RADY	H/L	Hi –impedance: Data transfer is complete. L: System busy.
17	VADJ	I-	This pin is through PCB connecting to Pin 13 of CN2.
18	VLCD	I-	This pin is through PCB connecting to Pin 12 of CN2.

19	/RESET	H/L	Low : Reset system ; Hi: Normal.
20	/RD	H/L	Read from data bus.
21	/WR	H/L	write to data bus.
22	NC	-	No contacting.
23	NC	-	No contacting.
24~31	DB0~DB7	H/L	Data bus with Address bus depend on /ALE pin
32	VDD	H	Power Supply for logic.
33	VSS	L	Power Supply(Ground:0V)
34	NC	-	No contacting.
35	NC	-	No contacting.
36	NC	-	No contacting.

CN2 Interface:

PIN NO.	SIGNAL	LEVEL	FUNCTION
1	UD0	H/L	Panel display data bus.
2	UD1	H/L	Panel display data bus.
3	UD2	H/L	Panel display data bus.
4	UD3	H/L	Panel display data bus.
5	/DISPOFF	H/L	Data Type Selection
6	FLM	H/L	Data Input(8 bits)
7	M	H/L	Power Supply for Logic
8	LP	H/L	Power Supply(Ground:0V)
9	CP	H/L	Contrast Adjustment Input
10	VDD	H	LC Power Supply
11	VSS	L	H: Display ON L: Display OFF
12	VLCD	O	This pin is through PCB connecting to Pin 18 of CN1.
13	VADJ	O	This pin is through PCB connecting to Pin 17 of CN1.
14	NC	-	No contacting.
15~21	LD0~LD7	H/L	Panel display data bus.
22~25	UD4~UD7	H/L	Panel display data bus.
26~28	NC	-	No contacting.

LCD Signal Connector Pinout

SED1353 Pin Name	Color STN LCD					Mono STN LCD	
	16-bit Single/Dual	8-bit Dual	8-bit Single (Format 1[a]) Aux[03] bit 3 =0, Aux[01] bit 2=1	8-bit Single (Format 2[a]) Aux[03] bit 3 =1, Aux[01] bit 2=1	4-bit	8-bit	4-bit
LD0	LD0	LD0	LD0	LD0		LD0	
LD1	LD1	LD1	LD1	LD1		LD1	
LD2	LD2	LD2	LD2	LD2		LD2	
LD3	LD3	LD3	LD3	LD3		LD3	
UD0	UD0	UD0	UD0	UD0	UD0	UD0	UD0
UD1	UD1	UD1	UD1	UD1	UD1	UD1	UD1
UD2	UD2	UD2	UD2	UD2	UD2	UD2	UD2
UD3	UD3	UD3	UD3	UD3	UD3	UD3	UD3
	LD4[b]						
	LD5[b]						
	LD6[b]						
	LD7[b]						
	UD4[b]						
	UD5[b]						
	UD6[b]						
	UD7[b]						
XSCL	XSCL	XSCL	XSCL	XSCL	XSCL	XSCL	XSCL
WF/XSCL2			XSCL2				
LP	LP	LP	LP	LP	LP	LP	LP
YD	YD	YD	YD	YD	YD	YD	YD

[a] See Section [illegible] for details.
[b] From external logic; see Section 3.5 for details.

Instruction Set

Example 1: Initialize the registers for a 256 color 320 x 240 single panel LCD with 128k of display memory. Afterwards write one pixel to the top left corner of the display.

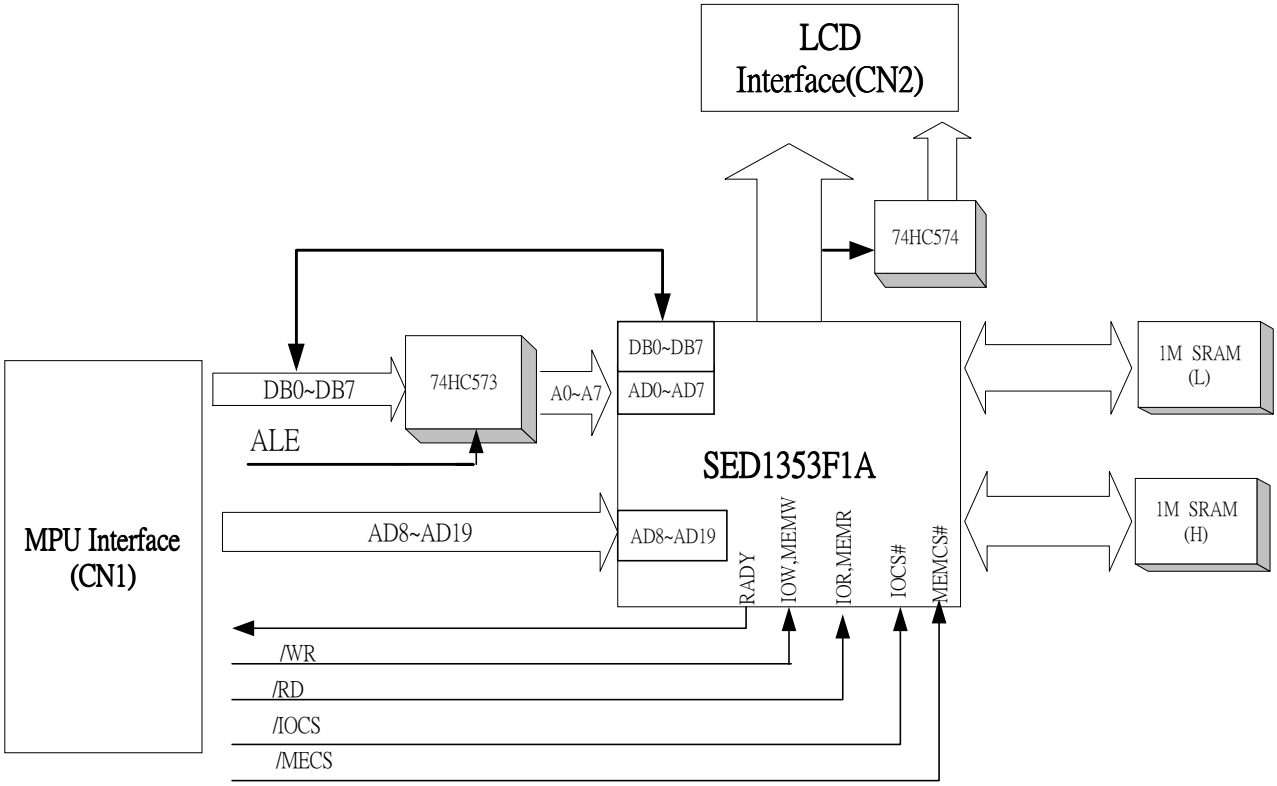
Program SED1353 Registers in the following order with the data supplied:

AUX Register	Data (In Binary)	Notes	See Also
AUX[00h]	0000 0000	• bits 7 and 6 must be zero	
AUX[01h]	0010 1001	• b7 = display off (application specific; the recommended procedure is to turn this bit off during register initialization and afterwards turn this bit on) • b6 = single panel (panel specific) • b5 = XSCL is masked (panel specific) • b4 = LCDE = LCDENB pin = set to disable specific power supply design (for SDU1353B0C, set bit to 0 to disable power supply) (application specific; the recommended procedure is to disable the power supply during register initialization and afterwards enable the power supply) • b3 = N/A for 256 colors (application specific) • b2 = 4 bit LCD data width when combined with AUX[03] bit 3 (panel specific) • b1 = 16 bit Memory Interface (implementation specific) • b0 = RAMS ignored (implementation specific)	
AUX[02h]	1001 1111	• bits 7-0 = bits 7-0 of Line Byte Count • bit 8 of Line Byte Count is bit 0 of AUX[03h]	see Note A at end of Table for calculation
AUX[03h]	0000 0110	• bits 7-6 = Power Save Mode 0 (application specific - for normal operation set to 00b) • bit 5 = LCD interface signals forced low during Power Save (implementation and panel specific) • bit 4 = no LUT bypass (application specific) • bit 3 = 4 bit LCD data width when combined with AUX[01] bit 2 (panel specific) • bit 2 = 256 color mode (application specific) • bit 1 = color panel attached (panel specific) • bit 0 = bit 8 of Line Byte Count (panel specific, see AUX[02h])	see Section 5.6, *"Power Saving"* on page 54
AUX[04h]	1110 1111	• bits 7-0 = bits 7-0 of Total Display Line Count • bits 9-8 of Total Display Line Count in bits 1-0 of AUX[05h]	see Note B and C at end of Table for calculation

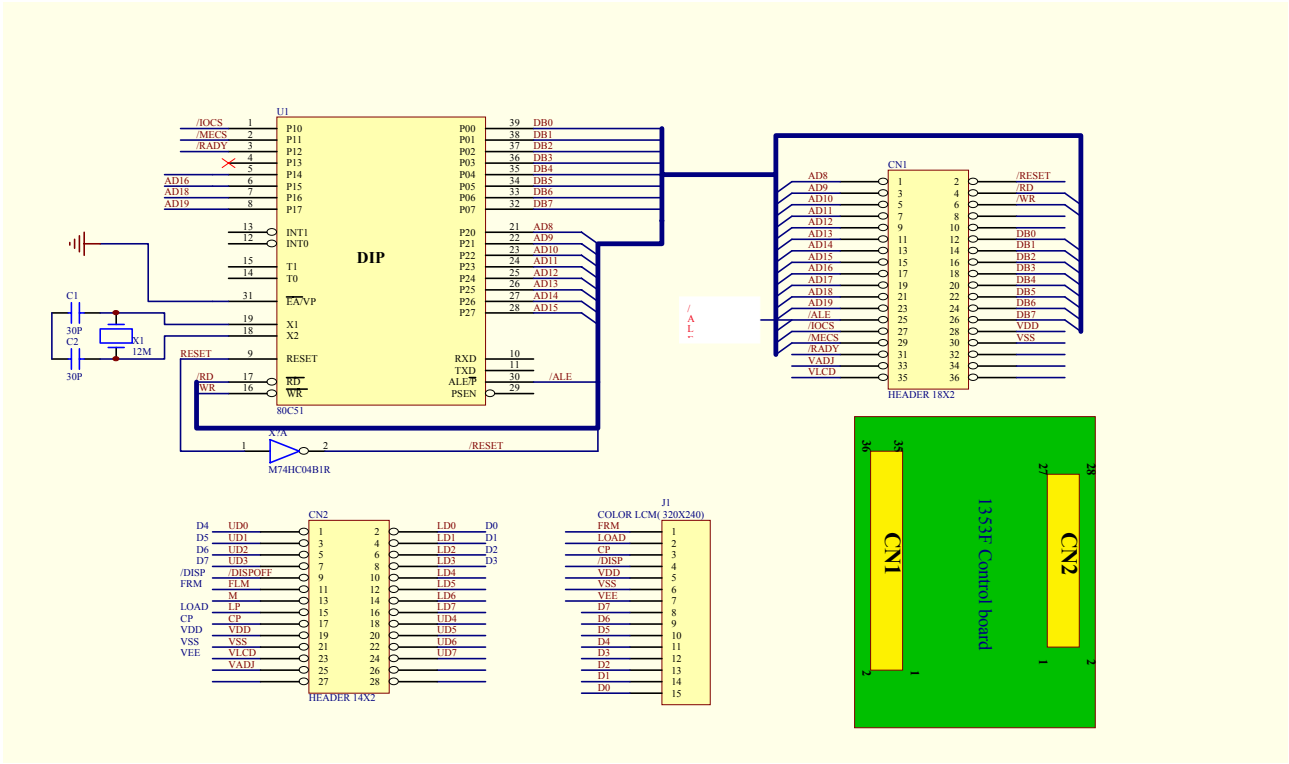
AUX Register	Data (in Binary)	Notes	See Also
AUX[05h]	0000 0000	• bits 7-2: 0 = WF output toggles every frame (panel specific) • bits 1-0 = bits 9-8 of Total Display Line Count (panel specific, see AUX[04h])	
AUX[06h] AUX[07h]	0000 0000 0000 0000	• bits 15-0 of Screen 1 Display Start Address - normally Screen 1 Start Address = 0000h (application and panel specific) bits 7-0 are in AUX[06h] and bits 15-8 are in AUX[07h] when 0000h, Screen 1 Display Start Address is located at D000:0000h, bank 0, on the SDU1353B0C	see Section 4.2.1, *"SDU1353B0C Evaluation Board Display Memory"* on page 36 and Section 4.1, *"Registers"* on page 34
AUX[08h] AUX[09h]	0000 0000 0000 0000	• bits 15-0 of Screen 2 Display Start Address - normally Screen 2 Start Address = 0000h (application and panel specific) bits 7-0 are in AUX[08h] and bits 15-8 are in AUX[09h] when 0000h, Screen 1 Display Start Address is located at D000:0000h, bank 0, on the SDU1353B0C	see Section 4.2.1, *"SDU1353B0C Evaluation Board Display Memory"* on page 36 and Section 4.1, *"Registers"* on page 34
AUX[0Ah]	1110 1111	• bits 7-0 = bits 7-0 of Screen 1 Display Line Count bits 9-8 of Screen 1 Display Line Count in bits 1-0 of AUX[0Bh] Screen 1 Display Line Count is typically the same as Total Display Line Count (AUX[0Ah] = AUX[04h], bits 1-0 of AUX[0Bh] = bits 1-0 of AUX[05h])	see Section 5.4, *"Split Screen"* on page 45
AUX[0Bh]	0000 0000	• bits 7-2 = don't care; recommend clearing bits • bits 1-0 = bits 9-8 of Screen 1 Display Line Count (application specific, see AUX[0Ah])	
AUX[0Ch]	0000 0000	normally programmed to 00h (panel specific) • bits 7-0 = use fixed default non-display period	
AUX[0Dh]	0000 0000	normally programmed to 00h (normal) • bits 7-0 = no address pitch adjustment when 0	see Section 5.1, *"Virtual Displays"* on page 40
AUX[0Eh]	0000 0000	select palette address • bits 7-6 = green bank 0 (application specific) • bits 5-4 = auto increment palette R/W access (application specific) • bits 3-0 = palette address (application specific)	
AUX[0Fh]	0000 0000	write Red data • bits 7-6 = red bank 0 (application specific) • bits 5-4 = blue bank 0 (application specific) • bits 3-0 = palette data (application specific)	
AUX[01h]	1011 1001	program Mode Register bit DISP to 1, and set LCDE to enable power supply 1001 0000b 'OR' {original value for AUX[01h]} • b7 = display on (application specific) • b4 = LCDE = LCDENB pin = set to enable specific power supply design (for SDU1353B0C, set bit to 1 to enable power supply) (application specific)	

Write one pixel to the top left corner of display memory.
If the SDU1353B0C evaluation board is used in indexed I/O mode, there are two video memory banks which begin at D000:0000 (2 banks x 64K per bank; see the following note). If the base port address is 310h, then read from port address 312h. Next, write 0FFh to location D000:0000h; this will be seen as a white pixel at the top left corner of the display.

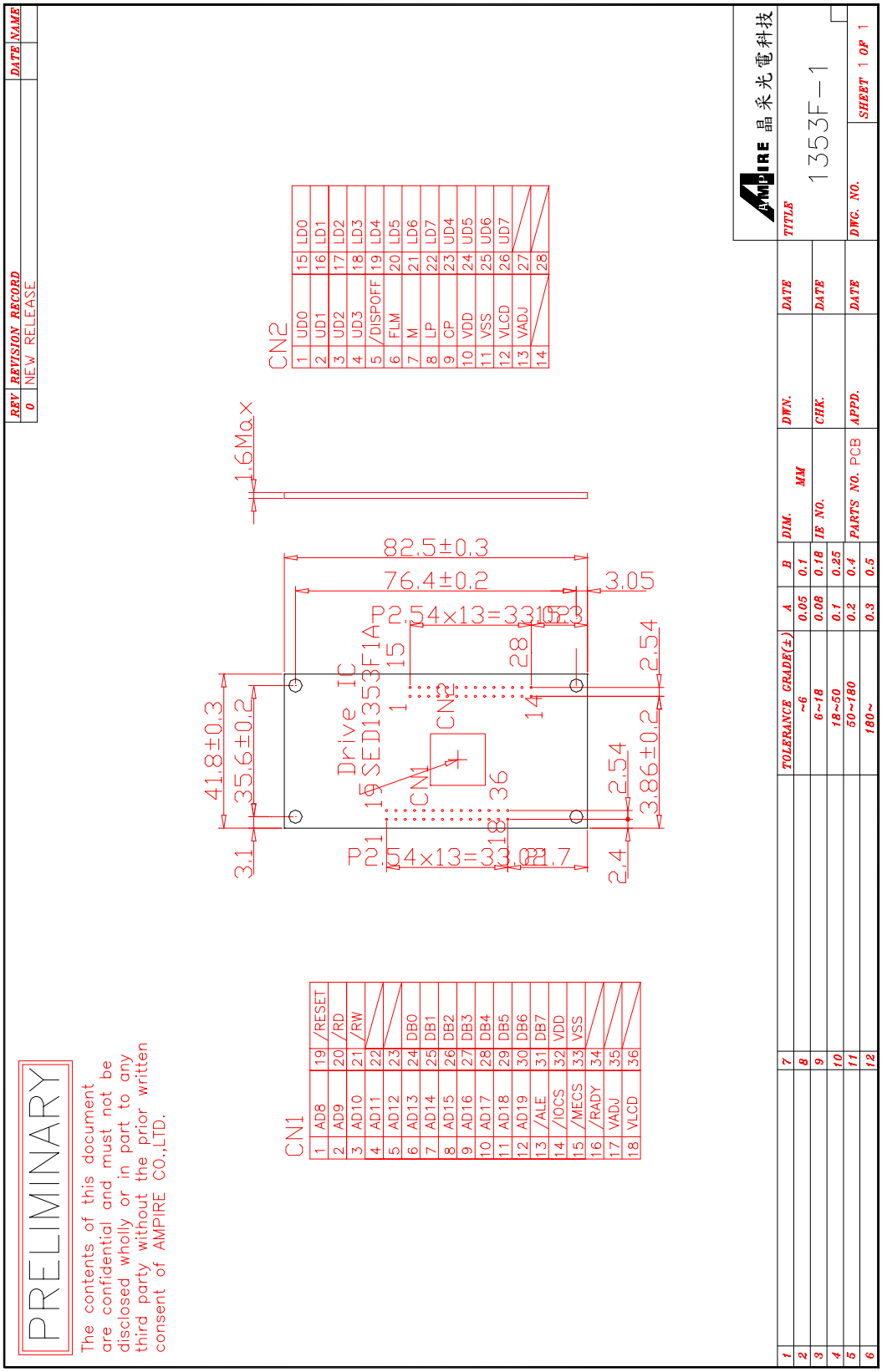
BLOCL DIAGRAM



Application Circuit



Outline Dimension



INITIALIZATION CODE

```
push a
mov    Dly_Time,#2
mov    Dptr,#_TestReg    ;0
mov    a,#00h
call E353Ins
call sDelay
;;
mov    Dptr,#_ModeReg0 ;1
mov    a,#10111101b
call E353Ins
call sDelay
;;
mov    Dptr,#_LineCunt ;2
mov    a,#10011111b
call E353Ins
call sDelay
;;
mov    Dptr,#_ModeReg1    ;3
mov    a,#00001110b
call E353Ins
call sDelay
;;
mov    Dptr,#_TotalLine_L ;4
mov    a,#11101111b
call E353Ins
call sDelay

mov    Dptr,#_TotalLine_H    ;5
mov    a,#00000000b
call E353Ins
call sDelay
;;
mov    Dptr,#_Dsp1Add_L      ;6
mov    a,#00000000b
call E353Ins
call sDelay
```

```
;;
mov    Dptr,#_Dsp1Add_H     ;7
mov    a,#00000000b
call E353Ins
call sDelay
;;
mov    Dptr,#_Dsp2Add_L     ;8
mov    a,#00000000b
call E353Ins
call sDelay
mov    Dptr,#_Dsp2Add_H     ;9
mov    a,#00000000b
call E353Ins
call sDelay
;;
mov    Dptr,#_Dsp1Cunt_L    ;A
mov    a,#11101111b
call E353Ins
call sDelay
mov    Dptr,#_Dsp1Cunt_H    ;B
mov    a,#00000000b
call E353Ins
call sDelay
;;
mov    Dptr,#_HoriNonDsp    ;C
mov    a,#00000000b
call E353Ins
call sDelay
;;
mov    Dptr,#_AddPitchDsp    ;D
mov    a,#00000000b
call E353Ins
call sDelay
;;
mov    Dptr,#Tab256
call LoUpTabSet
pop    a
ret
```

```
;*****************************************

LoUpTabSet:
                mov    2,#8
Lout1:
                mov    a,#00
                movc a,@a+DPTR
                inc    dptr
                push Dph
                push DpL
                mov    Dptr,#000eh
                call E353Ins
                pop    DpL
                pop    Dph
                mov    a,#00
                movc a,@a+DPTR
                inc    dptr
                push Dph
                push DpL
                mov    Dptr,#000fh
                call E353Ins
                pop    DpL
                pop    Dph
                mov    a,#00
                movc a,@a+DPTR
                inc    dptr
                push Dph
                push DpL
                mov    Dptr,#000fh
                call E353Ins
                pop    DpL
                pop    Dph
                mov    a,#00
                movc a,@a+DPTR
                inc    dptr
                push Dph
                push DpL
                mov    Dptr,#000fh
```

```
                call E353Ins
                pop    DpL
                pop    Dph
                djnz r2,Lout1
                ret
;-----------------------------------------------
Tab256:   ;; Add:     Add   R     G     B
                db     00H,00h,00h,00h
                db     01H,03h,04h,07h
                db     02H,05h,08h,0ah
                db     03H,07h,0ah,0fh
                db     04H,09h,0ch,00h
                db     05H,0bh,0dh,07h
                db     06H,0dh,0eh,0ah
                db     07H,0fh,0fh,0fh
```