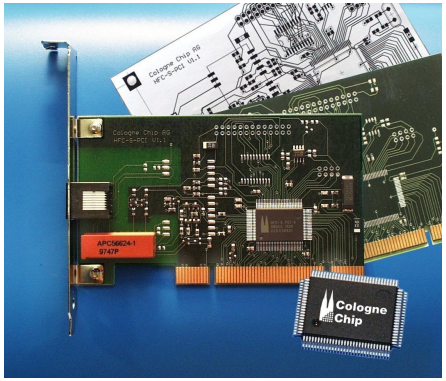
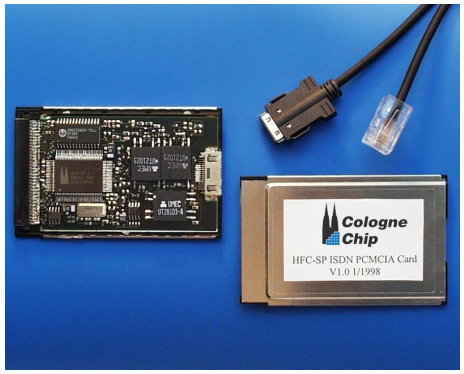
Your contact: www.CODICO.com mailto:office@codico.com phone:+43/1/86 305-0 fax:+43/1/86 305-98





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ISDN Chip Solutions

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[short form catalogue]

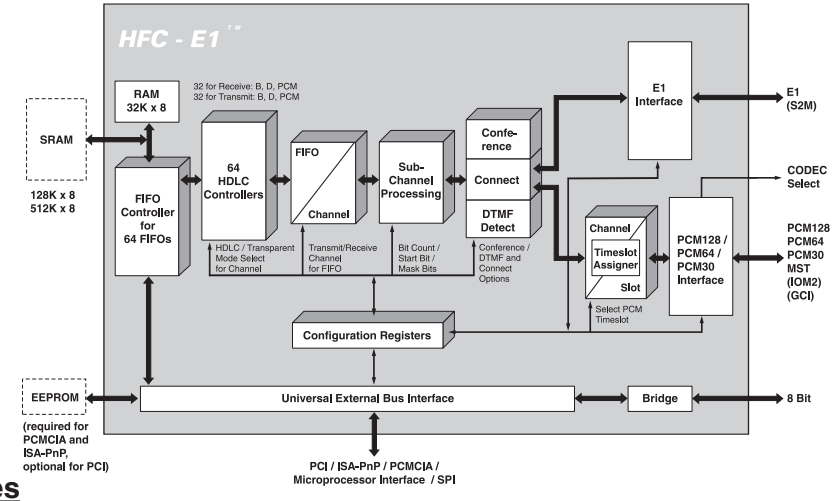
Cologne Chip

The I

ISDN Primary Rate (E1) HDLC FIFO Controller **HFC-E1**

Functions

The HFC-E1 is a HDLC B- and D-channel controller with integrated E1-interface. It can be used for ISDN primary rate lines. All channels are served fully duplex by deep FIFOs. Also implemented is a PCM128 / PCM64 / PCM30 highway interface (which is able to connect to many telecom serial busses) and an universal external bus interface.



Features

- full I.431 ITU E1 (S2M) ISDN support in LT and NT mode
- 32 independent read and write HDLC-channels
  for e.g. 30 ISDN B-channels, 1 ISDN D-channel and 1 timeslot on the PCM interface;
  B-channel transparent mode independently selectable
- up to 64 FIFOs; FIFO size configurable
- each FIFO can be assigned to an arbitrary channel of the E1 or PCM interface
- max. 31 HDLC frames (with 128k or 512k external RAM) or 15 HDLC frames (with 32k built-in RAM) per FIFO
- 1 - 8 bit processing for subchannels selectable
- universal external bus interface configurable into PCI bus, ISA-PnP, PCMCIA or microprocessor interface as well as SPI
- PCM128 / PCM64 / PCM30 interface configurable to interface MITEL ST™ bus (MVIP™) or Siemens IOM2™ and Motorola GCI™ (bearer slots supported only) for inter-chip connection (e.g. external CODECs)
- multiparty audio conferences switchable
- DTMF detection on all B-channels
- CMOS technology 3.3V (5V tolerant inputs), PQFP 208 case

Main Features of HFC-Series

very deep FIFOs

(most of our chips can handle almost 1 full second of ISDN traffic on their own)

integrated S/T interface

(configurable into TE / NT mode by software)

very low power consumption

(e.g.: only 8mA for HFC-S+ at 3.3V power supply)

operating power from 3V to 5V

(pure digital CMOS technology)

built-in switching functionality

(over PCM30 bus by using the built-in time-slot-assigner)

easy connection of telecom CODECs or U-chip

(built-in 2/4/8 MBit serial telecom highway)

excellent price

(1-chip solutions help you to reduce costs)

generic Linux driver support for all chips

Application Matrix for Cologne Chips

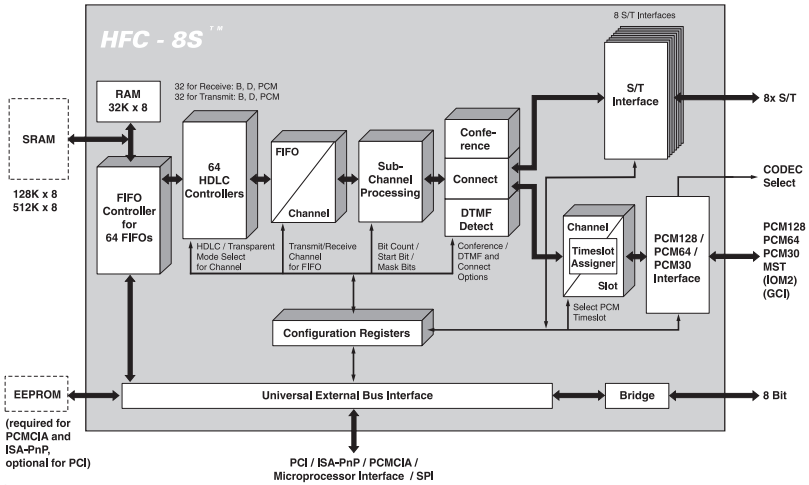
	HFC-S+	HFC-S mini	HFC-SP	HFC-S PCI A	HFC-S USB	HFC-4S	HFC-8S	HFC-E1	HFC-S active
ISA-PnP Cards	✗	✗	✗			✗	✗	✗	
PCI Cards	✗	✗		✗		✗	✗	✗	
PCMCIA Cards	✗	✗	✗			✗		✗	
USB TA	✗	✗			✗				✗
PABX for SOHO	✗	✗			✗	✗			✗
PABX	✗	✗				✗	✗	✗	✗
Smart NTs	✗	✗			✗				✗
Least Cost Router	✗	✗				✗	✗	✗	✗
LAN Routers	✗	✗				✗	✗	✗	✗
POTS TA	✗	✗							✗
Test Equip-ment	✗	✗	✗	✗	✗	✗		✗	✗
Phone, Video-phone	✗	✗			✗				✗

✗ = succeeded by chip with higher functional integration

ISDN S/T HDLC FIFO Controller **HFC-8S**

Functions

The HFC-8S is a HDLC B- and D-channel controller with 8 integrated S/T-interfaces. It can be used for ISDN basic rate lines. All channels are served fully duplex by deep FIFOs. Also implemented is a PCM128 / PCM64 / PCM30 highway interface (which is able to connect to many telecom serial busses) and an universal external bus interface.



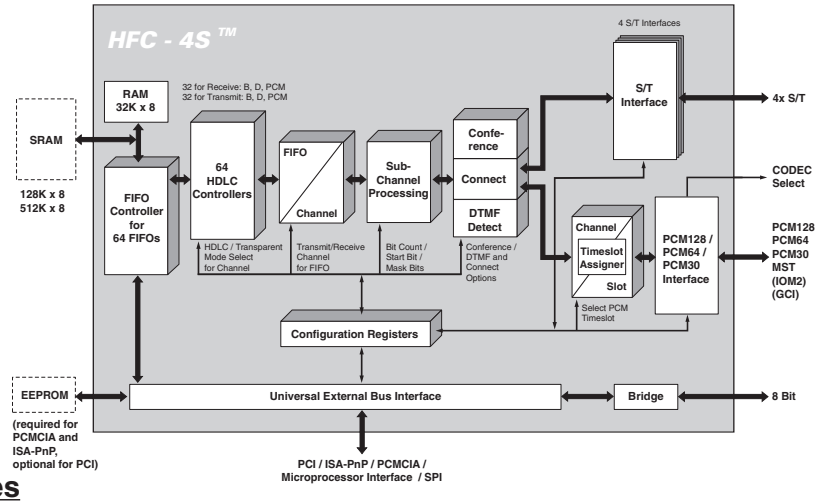
Features

- full I.430 ITU S/T ISDN support in TE and NT mode for 3V - 5V supply power
- 32 independent read and write HDLC-channels
  for e.g. 16 ISDN B-channels, 8 ISDN D-channels and 8 timeslots on the PCM interface; B-channel transparent mode independently selectable
- up to 64 FIFOs; FIFO size configurable
- each FIFO can be assigned to an arbitrary channel of any S/T or PCM interface
- max. 31 HDLC frames (with external 128k or 512k RAM) or 15 HDLC frames (with 32k built-in RAM) per FIFO
- 1 - 8 bit processing for subchannels selectable
- universal external bus interface configurable into PCI bus, ISA-PnP, PCMCIA or microprocessor interface; hot swap for Compact PCI supported
- PCM128 / PCM64 / PCM30 interface configurable to interface MITEL ST™ bus (MVIP™) or Siemens IOM2™ and Motorola GCI™ (bearer slots supported only) for inter-chip connection (e.g. external CODECs)
- multiparty audio conferences switchable
- DTMF detection on all B-channels
- CMOS technology 3.3V (5V tolerant inputs), PQFP 208 case

ISDN S/T HDLC FIFO Controller **HFC-4S**

Functions

The HFC-4S is a HDLC B- and D-channel controller with 4 integrated S/T-interfaces. It can be used for ISDN basic rate lines. All channels are served fully duplex by deep FIFOs. Also implemented is a PCM128 / PCM64 / PCM30 highway interface (which is able to connect to many telecom serial busses) and an universal external bus interface.



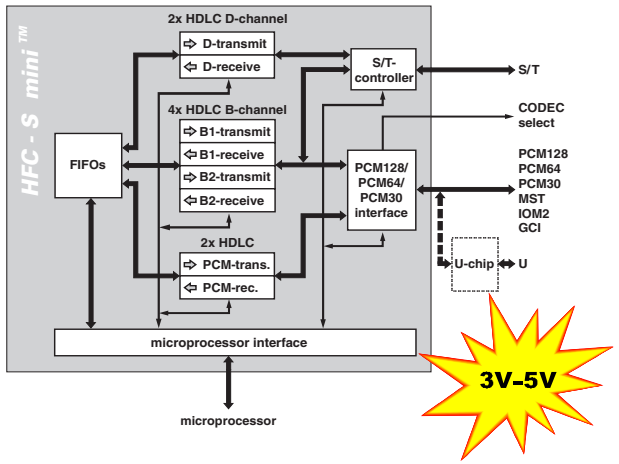
Features

- full I.430 ITU S/T ISDN support in TE and NT mode for 3V - 5V supply power
- 32 independent read and write HDLC-channels
  for e.g. 8 ISDN B-channels, 4 ISDN D-channels and 20 timeslots on the PCM interface; B-channel transparent mode independently selectable
- up to 64 FIFOs; FIFO size configurable
- each FIFO can be assigned to an arbitrary channel of any S/T or PCM interface
- max. 31 HDLC frames (with external 128k or 512k SRAM) or 15 HDLC frames (with 32k built-in RAM) per FIFO
- 1 - 8 bit processing for subchannels selectable
- universal external bus interface configurable into PCI bus, ISA-PnP, PCMCIA or microprocessor interface; hot swap for Compact PCI supported
- PCM128 / PCM64 / PCM30 interface configurable to interface MITEL ST™ bus (MVIP™) or Siemens IOM2™ and Motorola GCI™ (bearer slots supported only) for inter-chip connection (e.g. external CODECs)
- multiparty audio conferences switchable
- DTMF detection on all B-channels
- CMOS technology 3.3V (5V tolerant inputs), PQFP 208 case

ISDN S/T HDLC FIFO Controller **HFC-S mini**

Functions

The HFC-S mini is a single chip ISDN S/T HDLC basic rate controller for embedded applications. The S/T interface, HDLC-controllers, FIFOs and a microprocessor interface are integrated in the HFC-S mini. A PCM128 / PCM64 / PCM30 interface is also implemented which is able to connect to many telecom serial busses. All ISDN channels (2B+1D) and the PCM interface are served fully duplex by the 8 integrated FIFOs.



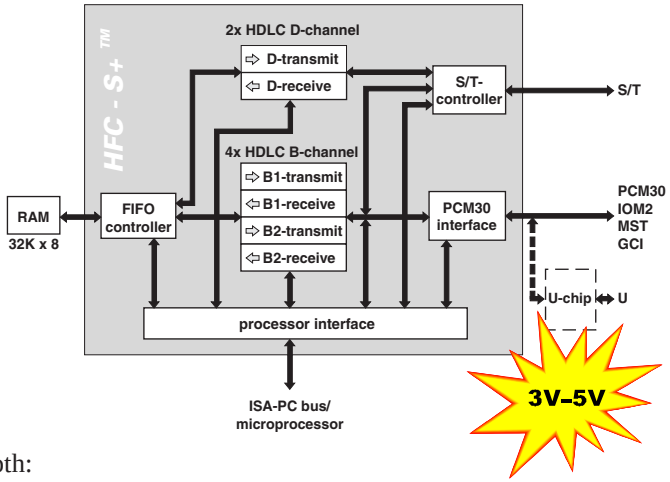
Features

- full I.430 ITU S/T ISDN support in TE and NT mode for 3V - 5V supply power
- independent read/write HDLC-channels for two ISDN B-channels, one ISDN D-channel and one PCM timeslot (or E-channel)
- integrated FIFOs for B1, B2, D and PCM (or E)
- FIFO-Depth: 128 bytes per channel and direction; up to 7 HDLC frames per FIFO
- 56 KBit/s restricted mode for U.S. ISDN lines selectable by software
- PCM128 / PCM64 / PCM30 interface configurable to interface MITEL ST™ bus (MVIP™), Siemens IOM2™ or GCI™ for external CODECs or direct U-chip connection
- integrated microprocessor interface compatible to Motorola bus and Siemens/Intel bus
- timer with interrupt capability
- CMOS technology 3V - 5V
- PQFP 48 case
- Generic Linux driver for Linux and embedded Linux

ISDN S/T HDLC FIFO Controller **HFC-S+**

Functions

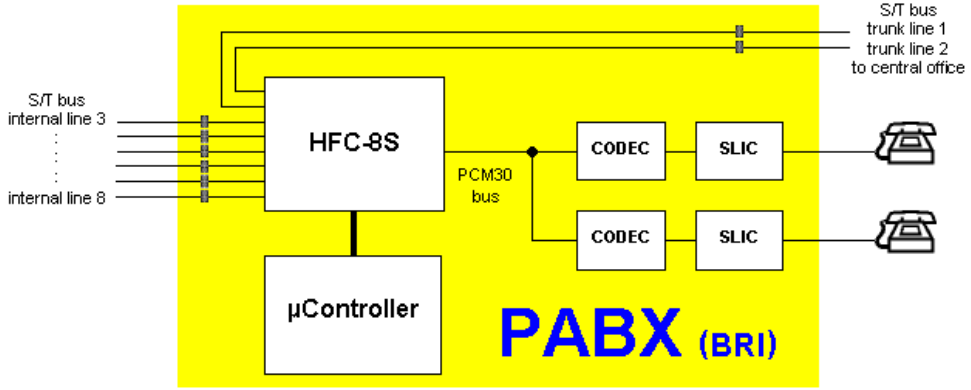
The HFC-S+ is a HDLC B- and D-channel controller with integrated S/T interface. It can be used for ISDN basic rate lines. All channels (2B+D) are served full duplex by six deep FIFOs. Also implemented is a PCM30 highway interface, which is able to connect to many telcom serial buses and a microprocessor interface.

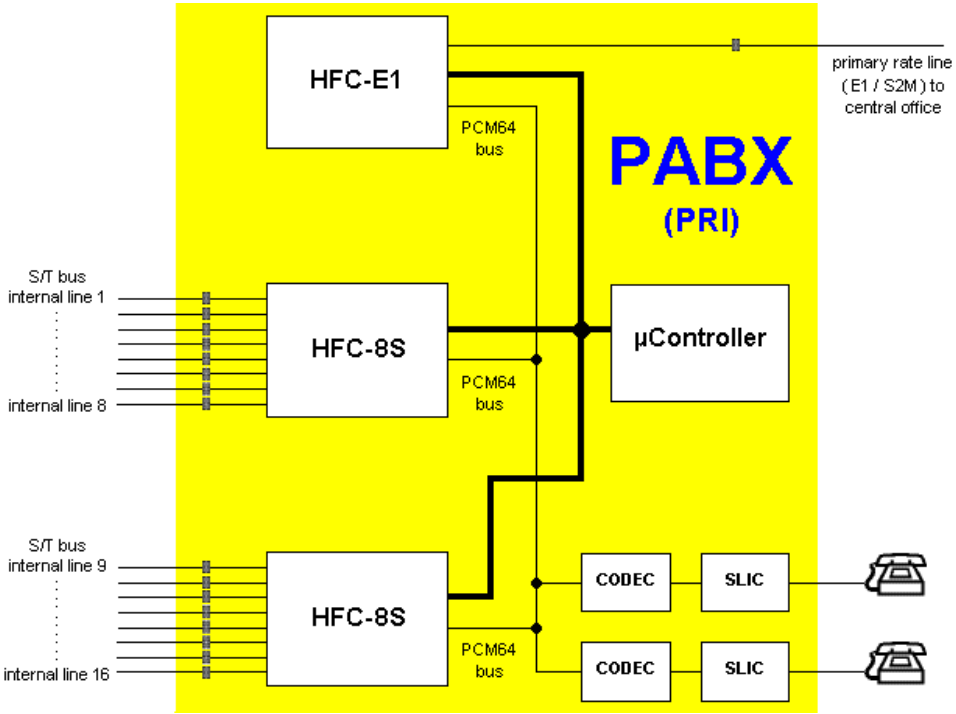


Features

- FIFO-Depth:
  B-channel: 4x 7,5 KByte, maximum 31 HDLC frames per FIFO
  D-channel: 2x 512 Byte, maximum 15 HDLC frames per FIFO
- independent read/write HDLC-channels for two ISDN B-channels and one ISDN D-channel
- 56 KBit/s restricted mode for U.S. ISDN lines selectable by software
- full I.430 ITU S/T ISDN support in TE and NT mode for 3.3V and 5V supply power
- PCM30 interface configurable to interface MITEL ST™ bus (MVIP™), Siemens IOM2™ or GCI™ for external codecs or direct U-chip connection
- direct 8 bit ISA-PC bus interface with buffers for ISA data bus; one of 6 interrupt channels selectable by software
- microprocessor interface compatible to Motorola bus and Siemens/Intel bus
- only 2 I/O addresses used on ISA-PC bus; I/O addresses programmable (no memory mapping, no DMA)
- CMOS technology 3-5V
- PQFP 100 case
- Generic Linux driver for Linux and embedded Linux

Applications for **HFC-4S**, **HFC-8S** and **HFC-E1**

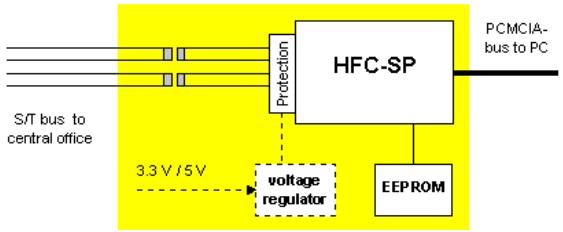




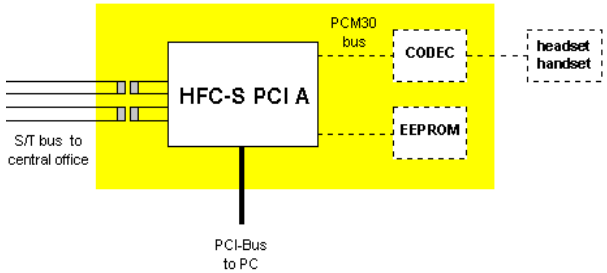
Applications for **HFC-SP**, **HFC-S PCI A** and **HFC-S USB**

Terminal Adapters for PCs - Internet Access

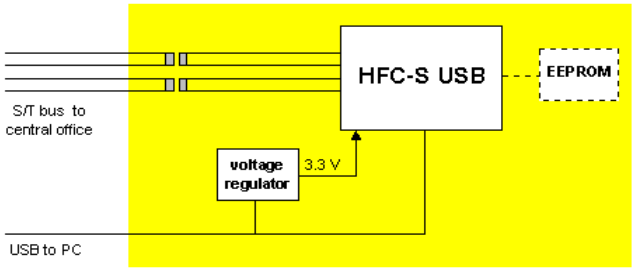
semi-active PCMCIA card



semi-active PCI PC card



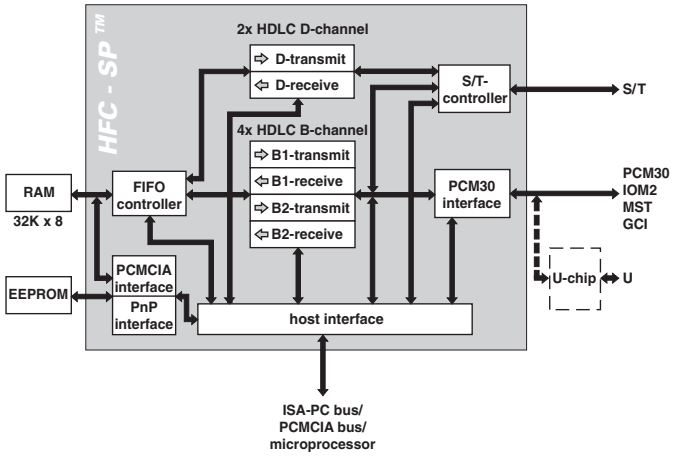
USB device



ISDN S/T HDLC FIFO Controller **HFC-SP**

Functions

The HFC-SP is a HDLC B- and D-channel controller with integrated S/T interface. It can be used for ISDN basic rate lines. All channels (2B+D) are served full duplex by six deep FIFOs. The HFC-SP has an integrated ISA Plug and Play and a PCMCIA interface. Also implemented is a PCM30 highway interface (which is able to connect to many of telecom serial buses) and a microprocessor interface.



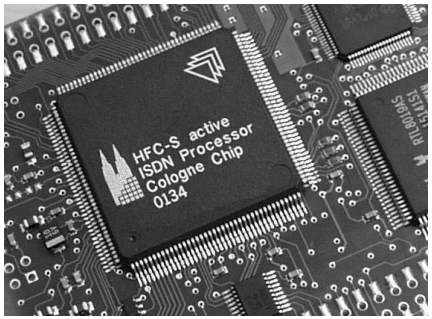
Features

- FIFO-Depth:
  B-channel: 4x 7,5 KByte, maximum 31 HDLC frames per FIFO
  D-channel: 2x 512 Byte, maximum 15 HDLC frames per FIFO
- independent read/write HDLC-channels for two ISDN B-channels and one ISDN D-channel
- 56 KBit/s restricted mode for U.S. ISDN lines selectable by software
- full I.430 ITU S/T ISDN support in TE and NT mode for 3.3V and 5V supply power
- PCM30 interface configurable to interface MITEL ST™ bus (MVIP™), Siemens IOM2™ or GCI™ for external codecs or direct U-chip connection
- integrated ISA Plug and Play;
  direct 8 bit ISA-PC bus interface with buffers for ISA data bus
- integrated PCMCIA interface
- microprocessor interface compatible to Motorola bus and Siemens/Intel bus
- CMOS technology 3-5V
- PQFP 100 case

Product Overview of **HFC-S active**

Functions at a glance

The HFC-S active is an ISDN telecommunication microprocessor system on a single chip (SoC). This new product of Cologne Chip is based on an ARM7 CPU. It is especially designed for applications such as ISDN telephones, PABX and ISDN terminal adapters. Besides additional external SRAM, also cost effective SDRAM is supported.



Moreover the HFC-S active has a S/T interface with HDLC controllers for the D and both B-channels as well as a full speed USB interface.

The two integrated telecom CODECs comply with the G.711 standard. They allow the connection of telephone hand sets or POTS ports in PABX applications. The CODECs have a programmable power-down mode and a processor controlled power management is supported. A programmable PLL allows to vary the system clock in the range from 12.288 MHz to 49.152 MHz.

Applications

- ✔ ISDN PABX and ISDN POTS terminal adapters
- ✔ ISDN telephones with/without data port
- ✔ ISDN USB terminal adapters
- ✔ Intelligent ISDN NTs with POTS ports and data port
- ✔ ISDN RS232 terminal adapters

Evaluation Kit

Cologne Chip also offers an evaluation board for the new ISDN processor. It contains a µC-Linux which was ported to the HFC-S active, including the ISDN protocol software of the ISDN4Linux developers group. An additional Ethernet chip is implemented in the evaluation system in order to enable an easy communication over TCP/IP via LAN. The source code of the protocol stacks is part of the evaluation kit and can also be used for commercial ISDN developments at no costs under the regulations of GPL (GNU Public License).

Therefore the evaluation kit is not only an excellent test environment for the new ISDN controller, but can also function as a basis for product developments with short time-to-market.

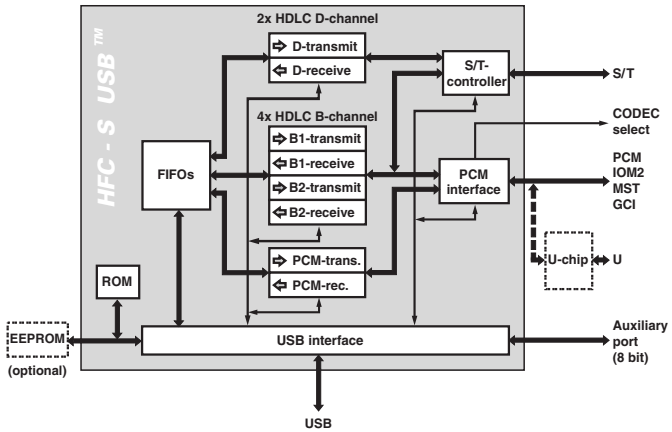
ISDN S/T HDLC FIFO Controller **HFC-S USB**

Functions

The HFC-S USB is an ISDN S/T HDLC basic rate controller for single-chip USB applications. It is based on Cologne's innovative "passive USB" technology: As the USB protocol engine is implemented in hardware, code development for a microcontroller becomes unnecessary.

USB passive Without Firmware

HFC-S USB only requires an external EEPROM to store the USB configuration data (USB descriptors) if the default data from the internal ROM shall not be used. As it is a single-chip solution, the S/T interface, HDLC-controllers, FIFOs and the USB interface are integrated in the HFC-S USB. A PCM128 / PCM64 / PCM30 interface is also implemented which is able to connect to many telecom serial busses. All ISDN channels (2B+1D) and the PCM interface are served fully duplex by the 8 integrated FIFOs. The integrated 8 bit auxiliary port enables the HFC-S USB to be used as USB bridge.



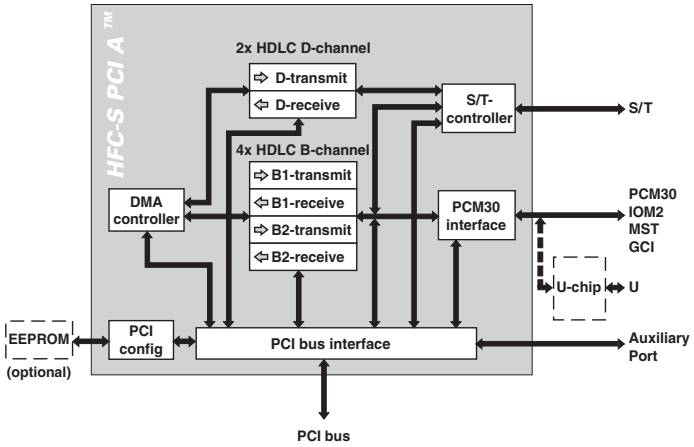
Features

- FIFO size: 128 bytes per channel and direction; maximum 7 HDLC frames per FIFO
- integrated FIFOs for B1, B2, D and PCM (or E)
- independent read/write HDLC-channels for two ISDN B-channels, one ISDN D-channel and one PCM timeslot (or E-channel)
- 56 KBit/s restricted mode for U.S. ISDN lines selectable by software
- full I.430 ITU S/T ISDN support in TE and NT mode
- PCM128 / PCM64 / PCM30 interface configurable to interface MITEL ST™ bus (MVIP™), Siemens IOM2™ or GCI™ for external codecs or direct U-chip connection
- integrated full speed 12 MBps USB interface (USB specification 1.1 compliant)
- integrated auxiliary port (USB bridge)
- CMOS technology 3-5V
- PQFP 48 case

ISDN S/T HDLC FIFO Controller **HFC-S PCI A**

Functions

The HFC-S PCI A is a HDLC B- and D-channel controller with integrated S/T interface. It can be used for ISDN basic rate lines. All channels (2B+D) are served full duplex by six deep FIFOs. The HFC-S PCI A has an integrated PCI bus interface. Also implemented is a PCM30 highway interface, which is able to connect to many telecom serial busses.



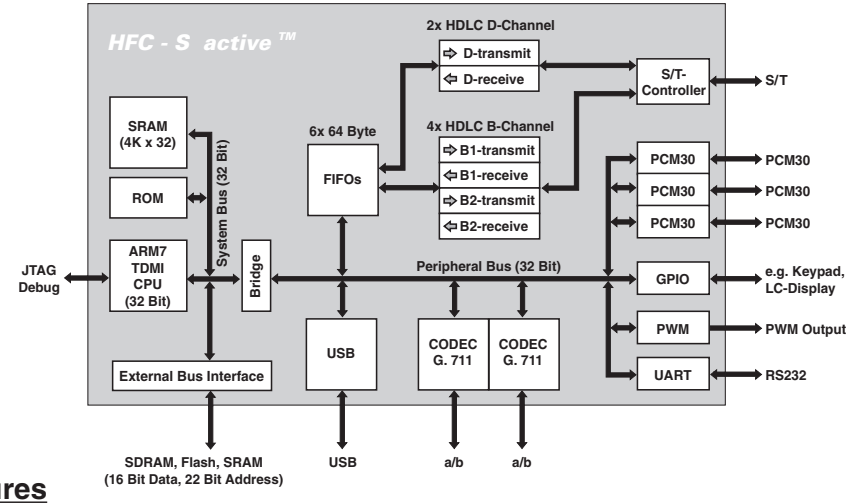
Features

- FIFO memory window:
  B-channel: 4x 7,5 KByte, maximum 31 HDLC frames per FIFO
  D-channel: 2x 512 Byte, maximum 15 HDLC frames per FIFO
- independent read/write HDLC-channels for two ISDN B-channels and one ISDN D-channel
- 56 KBit/s restricted mode for U.S. ISDN lines selectable by software
- full I.430 ITU S/T ISDN support in TE and NT mode for 3.3V and 5V supply
- PCM30 interface configurable to interface MITEL ST™ bus (MVIP™), Siemens IOM2™ or GCI™ for interface to U-chip or external CODECs
- direct access to PCM30 interface for tone synthetisation
- integrated PCI Spec. 2.2 bus interface (power management included, ACPI ready) for 3.3V and 5V bus signal environment
- CMOS technology 3-5V
- PQFP 100 case

ISDN Telecommunication Processor **HFC-S active**

Functions

The HFC-S active is an ISDN telecommunication microprocessor system on a single chip (SoC) based on a 32 bit ARM7TDMI RISC processor with 16- and 32 bit instruction set. It has a S/T interface with HDLC controllers for D and both B channels as well as a full speed USB interface. The CPU can boot from external Flash or from the serial port. Three PCM30 highways make external communication ICs accesible to the HFC-S active.



Features

- contains a powerful 32-bit ARM7TM RISC controller with a 32-bit address-space
- internal 16 KBytes SRAM (zero wait states)
- supports 8/16-bit SRAM/Flash/SDRAM external memory
- advanced SDRAM controller with minimum wait states (full column burst mode)
- integrated ISDN S/T-controller with B- and D-channel HDLC support
- full I.430 ITU S/T ISDN support in TE and NT mode
- 6 independent read and write HDLC-controllers for B1, B2 and D-channel
- B1, B2 and D-channel transparent mode independently selectable
- integrated FIFOs: 64 bytes per channel and direction
- 2 integrated audio CODECs for connection of analog devices (e.g. phone, fax, answering machine in PABX applications or handset in telephone applications)
- 3 independently programmable PCM highways with switching unit
- Full speed 12 Mbps Universal Serial Bus (USB) interface integrated
- CMOS technology 3.3V
- PQFP 160 case