The NS7520 is a high-performance, highly integrated, 32-bit system-on-a chip ASIC designed for use in intelligent networked devices and Internet appliances. The NS7520 is based on the standard architecture in the NET+ARM family of devices.

The NS7520 can support most any networking scenario, and includes a 10/100 BaseT Ethernet MAC and two independent serial ports (each of which can run in UART, HDLC, or SPI mode).

The CPU is an ARM7TDMI (ARM7) 32-bit RISC processor core with a rich complement of support peripherals and memory controllers including:

- Glueless connection to various types of memory (including flash, SDRAM, EEPROM, and others)
- Programmable timers
- 13-channel DMA controller
- External bus expansion module
- 16 general purpose input/output (GPIO) pins

NET+ARM is the hardware foundation for the NET+Works family of integrated hardware and software solutions for device networking. These comprehensive platforms include drivers, popular operating systems, networking software, development tools, APIs, and complete development boards.

NS7520 Overview

Figure 1 shows the NS7520 modules. Dashed lines indicate shared pins.

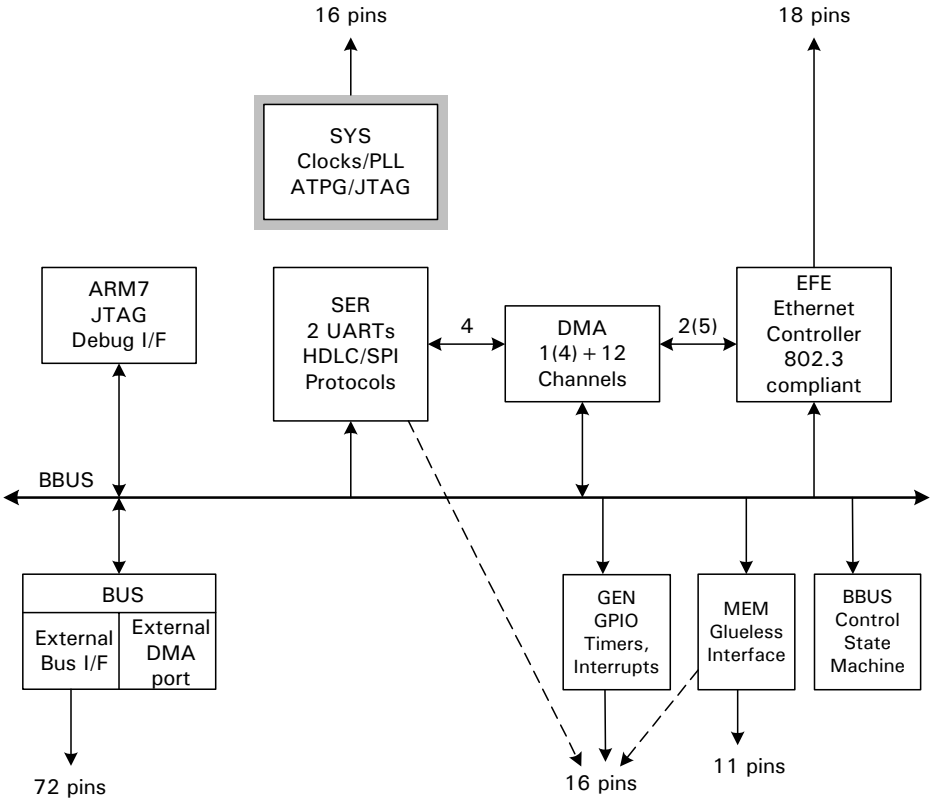


Figure 1: NS7520 modules

Key Features

Table 1 lists the key features of the NS7520.

CPU core

- ARM7 32-bit RISC processor
- 32-bit internal bus
- 16-bit Thumb mode
- 15 general purpose 32-bit registers
- 32-bit program counter (PC) and status register
- Five supervisor modes, one user mode

Integrated 10/100 Ethernet MAC

- 10/100 MII-based PHY interface
- 10 Mbit ENDEC interface
- TP-PMD and fiber-PMD device support
- Full-duplex and half-duplex modes
- Optional 4B/5B coding
- Full statistics gathering (SNMP and RMON)
- Station, broadcast, and multicast address detection and filtering
- 512-byte transmit FIFO, 2 Kbytes receive FIFO
- Intelligent receive-side buffer selection

13-Channel DMA controller

- Two channels dedicated to Ethernet transmit and receive
- Four channels dedicated to serial transmit and receive
- Four channels for external peripherals. Only two channels — either 3 and 5 or 4 and 6 — can be configured at one time.
- Three channels available for memory-to-memory
- Flexible buffer management

Programmable Timers

- Two independent timers (2µs–20.7 hours)
- Watchdog timer (interrupt or reset on expiration)
- Programmable bus monitor or timer

General purpose I/O pins

- 16 programmable I/O interface pins
- 4 pins programmable with level-sensitive interrupt

Operating frequency

- 32, 46, or 55 MHz internal clock operation from 18.432 MHz crystal
- f_{MAX} = 32, 46, or 55 (version–dependent)
- System clock source by external crystal or clock signal
- Programmable PLL, which allows a range of operating frequencies from 10 to f_{MAX}
- Maximum operating frequency from external clock or using PLL multiplication f_{MAX}

Table 1: NS7520 key features

Serial ports

- Two fully-independent serial ports (UART, HDLC, SPI)
- Digital phase lock loop (DPLL) for receive clock extractions
- 32-byte transmit/receive FIFOs
- Internal programmable bit-rate generators
- Bit rates 75–230400 in 16X mode
- Bit rates 1200 bps–4 Mbps in 1X mode
- Flexible baud rate generator, external clock for synchronous operation
- Receive-side character and buffer gap timers
- Four receive-side data match detectors

Bus interface

- Five independent programmable chip selects with 256 Mb addressing per chip select
- Chip select support for SRAM, FP/EDO DRAM, SDRAM, flash, and EEPROM without external glue
- Support 8-, 16-, and 32-bit peripheral support
- External address decoding and cycle termination
- Dynamic bus sizing
- Internal DRAM/SDRAM controller with address multiplexer and programmable refresh frequency
- Internal refresh controller (CAS before RAS)
- Burst-mode support
- 0–63 wait states per chip select
- Bootstrap support

Power and Operating Voltages

- 500 mW maximum at 55 MHz (all outputs switching)
- 418 mW maximum at 46 MHz (all outputs switching)
- 291 mW maximum at 32 MHz (all outputs switching)
- 3.3 V — I/O
- 1.5 V — Core

Table 1: NS7520 key features

Operating frequency

The NS7520 is available in grades operating at three speeds: 32 MHz, 46 MHz, and 55 MHz. The operating frequency is set during bootstrap initialization, using pins A[8:0]. These address pins load the PLL Settings register on powerup reset. A[8:7} determines IS (charge pump current); A[6:5] determines FS (output divider), and A[4:0] defines ND (PLL multiplier). Each bit in A[8:0] can be set individually.

To set the operating frequency, add a pulldown resistor to the appropriate A[*n*] bit. Table 2 shows how to set the bits for the operating frequency you want to use:

Speed	Modify	Resulting IS value		Resulting ND value				
55 MHz	Leave all bits as is	1	0	0	1	0	1	1
46 MHz	Add a pulldown resistor to A[1], to change the value from 1 to 0	1	0	0	1	0	0	1

Table 2: Operating frequency

Speed	Modify	Resulting IS value	Resulting ND value
32 MHz	Add pulldown resistors to A[8:7] Add pulldown resistors to A[3:2] and A[0]	0 1	0 0 1 1 0

Table 2: Operating frequency

Note: Operation at frequencies greater than the stated maximum operating frequency is not guaranteed.

Ethernet operating frequency

The maximum frequencies for Ethernet depend on speed and use of PHY:

Ethernet Max	PHY	Mbits
25 MHz	Nibble data from PHY	100
2.5 MHz	Nibble data from PHY	10
10 MHz	None	10

Packaging and pinout

Table 3 provides the NS7520 packaging dimensions. Figure 2 shows the NS7520 pinout and dimensions.

Symbol	Min	Nom	Max
A	—	—	1.4
A1	0.35	0.40	0.45
A2	—	—	0.95
b	0.45	0.50	0.55
D		13.0 BSC	
D1		11.2 BSC	
E		13.0 BSC	
E1		11.2 BSC	
e		0.8 BSC	
aaa		0.1	

Table 3: NS7520 packaging dimensions

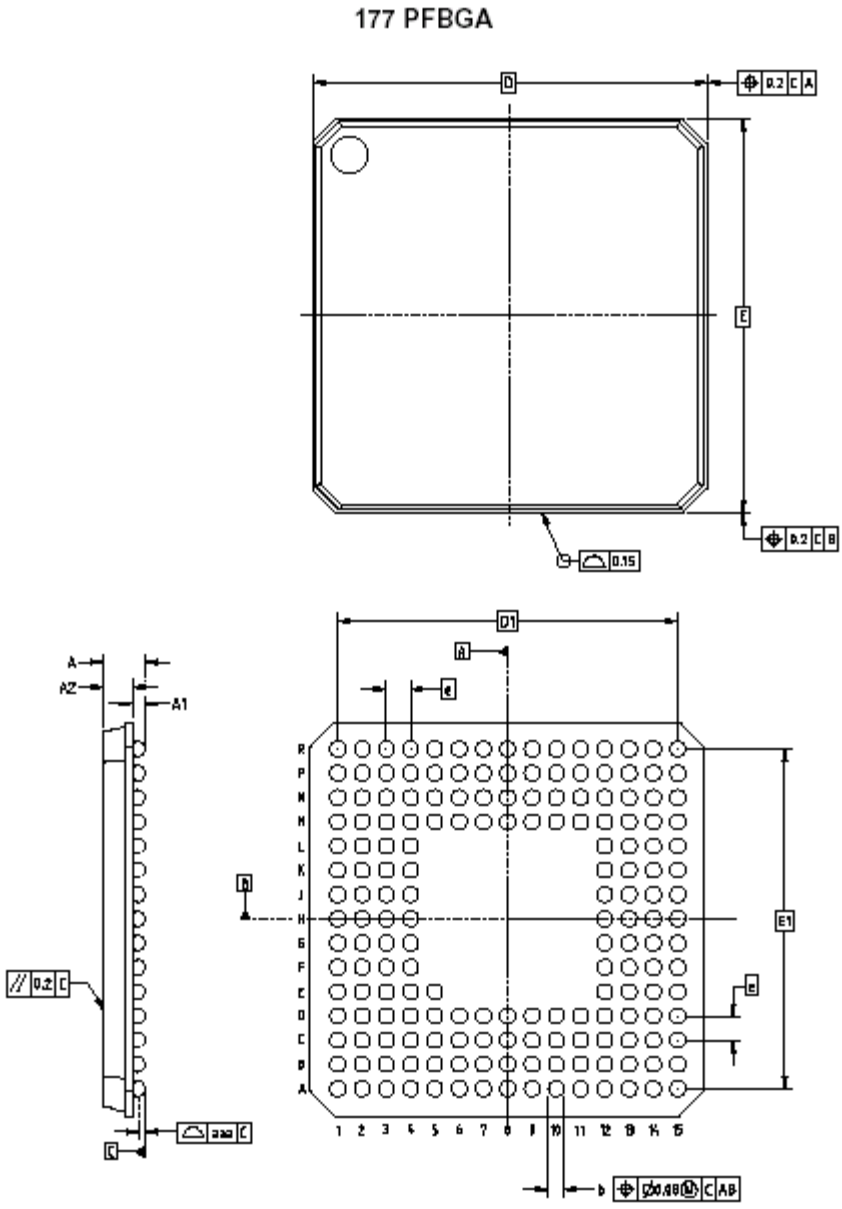


Figure 2: NS7520 pinout and dimensions

Pinout detail tables

Each pinout table applies to a specific interface, and contains the following information:

Signal	The pin name for each I/O signal. Some signals have multiple function modes and are identified accordingly. The mode is configured through firmware using one or more configuration registers.
Pin #	The pin number assignment for a specific I/O signal. **Note**: U or D next to the pin number indicates whether the pin is an input current source (pullup resistor) or an input current sink (pulldown resistor): ■ **U** — Pullup ■ **D** — Pulldown If no value appears next to the pin number, that pin has neither a pullup nor pulldown resistor.
_	An underscore (bar) indicates that the pin is *active low*.
I/O	The type of signal — input, output, or input/output.
OD (output drive)	The output drive strength of an output buffer. The NS7520 uses one of three drivers: ■ 2 mA ■ 4 mA ■ 8 mA

System Bus interface

Symbol		Pin #	I/O	OD	Description	
BCLK		A6	0	8	Synchronous bus clock	
External bus	**Other**				**External bus**	**Other**
ADDR27	CS0OE_	N10 U	I/O	4	Addr bit 27	Logical AND of CS0_ and OE_
ADDR26	CS0WE_	P10 U	I/O	4	Addr bit 26	Logical AND of CS_ and WE_
External bus					**External bus**	
ADDR25		M10 U	I/O	4	Remainder of address bus (through ADDR0)	
ADDR24		R10 U	I/O	4		
ADDR23		N9 U	I/O	4		
ADDR22		R9 U	I/O	4		
ADDR21		M9 U	I/O	4		
ADDR20		N8 U	I/O	4		
ADDR19		P8 U	I/O	4		
ADDR18		M7 U	I/O	4		
ADDR17		R7 U	I/O	4		
ADDR16		N7 U	I/O	4		

Symbol	Pin #	I/O	OD	Description
ADDR15	R6 U	I/O	4	
ADDR14	M6 U	I/O	4	
ADDR13	P6 U	I/O	4	
ADDR12	N6 U	I/O	4	
ADDR11	M5 U	I/O	4	
ADDR10	P5 U	I/O	4	
ADDR9	N5 U	I/O	4	
ADDR8	R4 U	I/O	4	
ADDR7	R3 U	I/O	4	
ADDR6	R2 U	I/O	4	
ADDR5	M4 U	I/O	4	
ADDR4	N4 U	I/O	4	
ADDR3	R1 U	I/O	4	
ADDR2	M3 U	I/O	4	
ADDR1	N2 U	I/O	4	
ADDR0	P1 U	I/O	4	
DATA31	N1	I/O	4	Data bus
DATA30	M1	I/O	4	
DATA29	L3	I/O	4	
DATA28	L2	I/O	4	
DATA27	L4	I/O	4	
DATA26	L1	I/O	4	
DATA25	K3	I/O	4	
DATA24	K2	I/O	4	
DATA23	K1	I/O	4	
DATA22	J2	I/O	4	
DATA21	J3	I/O	4	
DATA20	J1	I/O	4	
DATA19	H3	I/O	4	
DATA18	H4	I/O	4	
DATA17	H1	I/O	4	
DATA16	H2	I/O	4	
DATA15	G4	I/O	4	

Symbol	Pin #	I/O	OD	Description
DATA14	G1	I/O	4	
DATA13	G3	I/O	4	
DATA12	G2	I/O	4	
DATA11	F4	I/O	4	
DATA10	F2	I/O	4	
DATA9	F3	I/O	4	
DATA8	E1	I/O	4	
DATA7	E2	I/O	4	
DATA6	E3	I/O	4	
DATA5	D1	I/O	4	
DATA4	C1	I/O	4	
DATA3	B1	I/O	4	
DATA2	D4	I/O	4	
DATA1	D3	I/O	4	
DATA0	C2	I/O	4	
BE3_	D9	I/O	2	Byte enable D31:D24
BE2_	A9	I/O	2	Byte enable D23:D16
BE1_	C9	I/O	2	Byte enable D15:D08
BE0_	B9	I/O	2	Byte enable D07:D00
TS_	A8	Tie off this pin by adding 15K pullup resistors.		
TA_	D8 U	I/O	8	Data transfer acknowledge
TEA_	C8 U	I/O	8	Data transfer error acknowledge
RW_	D6	I/O	2	Transfer direction
BR_	D7 U	I/O	4	Bus request
BG_	C7 U	I/O	4	Bus grant
BUSY_	B7 U	I/O	4	Bus busy

Chip select controller

Symbol	Pin #	I/O	OD	Description
CS4_	B4	O	4	Chip select/DRAM RAS_
CS3_	A4	O	4	Chip select/DRAM RAS_
CS2_	C5	O	4	Chip select/DRAM RAS_

Symbol	Pin #	I/O	OD	Description
CS1_	B5	O	4	Chip select/DRAM RAS_
CS0_	D5	O	4	Chip select (boot select)
CAS3_	A1	O	4	FP/EDO DRAM column strobe D31:D24/SDRAM RAS_
CAS2_	C4	O	4	FP/EDO DRAM column strobe D23:D16/SDRAM CAS_
CAS1_	B3	O	4	FP/EDO DRAM column strobe D15:D08/SDRAM WE_
CAS0_	A2	O	4	FP/EDO DRAM column strobe D07:D00/SDRAM A10(AP)
WE_	C6	O	4	Write enable for NCC Ctrl'd cycles
OE_	B6	O	4	Output enable for NCC Ctrl'd cycles

Ethernet interface MAC

Note: ENDEC values for General Purpose Output and TXD refer to bits in the Ethernet General Control register. ENDEC values for General Purpose Input and RXD refer to bits in the Ethernet General Status register.

In this table, *GP* designates *general purpose*.

Symbol		Pin #	I/O	OD	Description	
MII	**ENDEC**				**MII**	**ENDEC**
MDC	GP output	D10	O	2	MII clock	State of (LPBK bit XOR (Mode = SEEQ))
MDIO	GP output	B10 U	I/O	2	MII data	State of UTP_STP bit
TXCLK		C10	I		TX clock	
TXD3	GP output	A12	O	2	TX data 3	State of AUI_TP[0] bit
TXD2	GP output	B11	O	2	TX data 2	State of AUI_TP[1] bit
TXD1	GP output	D11	O	2	TX data 1	Inverted state of PDN bit, open collector
TXD0	TXD	A11	O	2	TX data 0	TX data
TXER	GP output	A13	O	2	TX code err	State of LNK_DIS_ bit
TXEN		B12	O	2	TX enable	
TXCOL		A14	I		Collision	
RXCRS		D12	I		Carrier sense	
RXCLK		C12	I		RX clock	
RXD3	GP input	D14	I		RX data 3	Read state in bit 12
RXD2	GP input	B15	I		RX data 2	Read state in bit 15
RXD1	GP input	A15	I		RX data 1	Read state in bit 13
RXD0	RXD	B13	I		RX data 0	RX data

Symbol		Pin #	I/O	OD	Description	
MII	**ENDEC**				**MII**	**ENDEC**
RXER	GP input	C15	I		RX error	Read state in bit 11
RXDV	GP input	D15	I		RX data valid	Read state in bit 10

"No connect" pins

Pin #	Description
R13	Tie to V_{CC}
P12	Tie to V_{CC}
N12	XTALB1: Tie to V_{CC}
R15	XTALB2: Tie to V_{CC}

General Purpose I/O

GPIO Signal	Serial Signal	Other Signal	Pin#	I/O	OD	Serial Channel Description	Other Description
PORTA7	TxDA		J14 U	I/O	2	Channel 1 TxD	
PORTA6	DTRA_	DREQ1_	J13 U	I/O	2	Channel 1 DTR_	DMA channel 3/5 Req
PORTA5	RTSA_		J15 U	I/O	2	Channel 1 RTS_	
PORTA4	RxCA/RIA_/ OUT1A_		J12 U	I/O	2	Pgm'able Out/ Channel 1 RxCLK/ Channel 1 ring signal/Channel 1 SPI clock (CLK)	
PORTA3	RxDA	DACK1_	H15 U	I/O	2	Channel 1 RxD	DMA channel 3/5 Ack
PORTA2	DSRA_	AMUX	H12 U	I/O	2	Channel 1 DSR_	DRAM Addr Mux
PORTA1	CTSA_	DONE1_ (O)	H13 U	I/O	2	Channel 1 CTS_	DMA channel 3/5 DONE_Out
PORTA0	TxCA/ OUT2A_/ DCDA	DONE1_ (I)	G12 U	I/O	2	Pgm'able Out/ Channel 1 DCD/ Channel 1 SPI enable (SEL_)/ Channel 1 TxCLK	DMA channel 3/5 DONE_In
PORTC7	TxDB		G13 U	I/O	2	Channel 2 TXD	GEN interrupt out
PORTC6	DTRB_	DREQ2_	G14 U	I/O	2	Channel 2 DTR_	DMA Channel 4/6 Req

GPIO Signal	Serial Signal	Other Signal	Pin#	I/O	OD	Serial Channel Description	Other Description
PORTC5	RTSB_	REJECT_	F15 U	I/O	2	Channel 2 RTS_	CAM reject
PORTC4	RxCB/RIB_/ OUT1B_	RESET_	F12 U	I/O	2	Pgm'able Out/ Channel 2 RxCLK/ Channel 2 ring signal/Channel 2 SPI clock (CLK)	RESET output
PORTC3*	RxDB	LIRQ3/ DACK2_	F13 U	I/O	2	Channel 2 RxD	Level sensitive IRQ / DMA channel 4/6 Ack
PORTC2*	DSRB_	LIRQ2/RPSF_	E15 U	I/O	2	Channel 2 DSR_	Level sensitive IRQ/ CAM request
PORTC1*	CTSB_	LIRQ1/ DONE2_(O)	E12 U	I/O	2	Channel 2 CTS_	Level sensitive IRQ / DMA channel 4/6 Done_Out
PORTC0*	TxCB/ OUT2B_/ DCDB_	LIRQ0/ DONE2_(I)	E14 U	I/O	2	Pgm'able Out/ Channel 2 DCD/ Channel 2 SPI enable (SEL_)/ Channel 2 TxCLK	Level sensitive IRQ / DMA channel 4/6 Done_In

* PORTC[3:0] pins provide level-sensitive interrupts. The inputs do not need to be synchronous to any clock. The interrupt remains active until cleared by a change in the input signal level.

System clock

Symbol	Pin #	I/O	OD	Description
XTALA1	K14	I		ARM/System crystal oscillator circuit
XTALA2	K12	O		
PLLVDD (1.5V)	L15	P		PLL clean power
PLLVSS	L12	P		PLL return

System mode and system reset

Note: PLLTST_, BISTEN_, and SCANEN_ pin encoding determines mode (see Table 4: "NS7520 test modes" on page 18).

Symbol	Pin #	I/O	OD	Description
PLLTST_	N15	I		Encoded with BISTEN_ and SCANEN_
BISTEN_	M15	I		Encoded with PLLTST_ and SCANEN_

Symbol	Pin #	I/O	OD	Description
SCANEN_	L13	I		Encoded with BISTEN_ and PLLTST_
RESET_	A10	I		System reset

JTAG test

JTAG boundary scan allows a tester to check the soldering of all signal pins and tri-state all outputs.

Symbol	Pin #	I/O	OD	Description
TDI	N14 U	I		Test data in
TDO	M13	O	2	Test data out
TMS	M12 U	I		Test mode select
TRST_	M14	I		Test mode reset
TCK	P15	I		Test mode clock

Power supply

Signal	Pin number	Description
Oscillator VCC (3.3V)	N13, C13	Oscillator power supply
Core VCC (1.5V)	R8, L14, C14, C13	Core power supply
I/O VCC (3.3V)	E4, K4, M2, N3, P3, R5, H14, F14, B8, A3	I/O power supply
GND	D2, F1, J4, P4, P7, M8, P9, R11, K15, G15, E13, D13, B14, C11, A7, A5, B2, P2, P14, K13	Ground

NS7520 modules

CPU module

ARM7 provides the CPU module. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, which results in high instruction throughput and impressive real-time interrupt response for a small, cost-effective circuit. For more information about ARM7, see the ARM7TDMI Data Sheet from ARM Ltd. (www.arm.com).

GEN module

The GEN module provides these features:

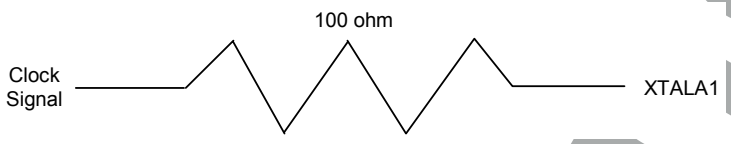
- Two programmable timers with interrupt

- One programmable bus-error timer
- One programmable watch-dog timer
- Two 8-bit programmable parallel I/O ports
- System priority interrupt controller
- Miscellaneous system control functions

System (SYS) module

The system module provides the system clock (SYS_CLK) and system reset (SYS_RESET) resources. The IO_XTALA clock is generated either by tying an external crystal to the XTALA*n* pins and using the internal oscillator or by feeding a clock directly to the XTALA1 pin.

When driving with an external crystal, review the electrical specifications for recommended crystal and external component characteristics. When driven by an external clock, this circuit is recommended:



The frequency of the crystal and the output frequency of the oscillator circuit are called $F_{CRYSTAL}$. The IO_XTALA signal is fed to or through an internal phase locked loop, depending on the state of {PLLTST_, BISTEN_, SCANEN_}. The ARM processor and system interface logic operate off the SYS_CLK signal. The frequency of SYS_CLK is $F_{CRYSTAL}$ when the PLL is disabled; otherwise, the frequency is 1/4 the PLL frequency.

BBus module

The BBus module provides the data path between NS7520 internal modules. This module provides the address and data multiplexing logic that supports the data flow through the NS7520. The BBus module is the central arbiter for all the NS7520 bus masters. Once mastership is granted, the decoding of each address to one (or none) of the NS7520 modules is handled by the BBus.

Memory module (MEM)

The memory module provides a glueless interface to external memory devices such as flash, DRAM, EEPROM, and more. The memory controller contains an integrated DRAM controller that supports five unique chip select configurations.

The memory module monitors the BBus interface for access to the bus module; that is, any access not addressing internal resources. If the address to be used corresponds to an address base register within the memory module, the memory module provides the memory access signals and responds to the BBus with the necessary completion signal.

The memory module can be configured to interface with FP, EDO, or SDRAM (synchronous DRAM). The NS7520 cannot simultaneously interface with more than one of these device types. All chip selects configured for DRAM must be configured with the same style of DRAM.

DMA controller

The NS7520 contains one DMA controller, with 13 DMA channels. Each DMA channel moves data between external memory and internal peripherals in fly-by mode, minimizing CPU intervention.

The DMA controller supports both fly-by operations and memory-to-memory operations:

- When configured for fly-by operation, the DMA controller does not touch the data; rather, it controls the flow of data through the BBus and provides the external address for a single data transfer operation.
- When configured for memory-to-memory operations, the DMA controller uses a temporary holding register between read and write operations. Two memory cycles are executed.

Ethernet controller

The Ethernet controller provides an IEEE 802.3u compatible Ethernet interface. The Ethernet interface includes the Ethernet front-end (EFE) and media access controller (MAC).

The Ethernet module supports both MII and ENDEC modes.

The MAC module interfaces to an external physical layer device using the Media Independent Interface (MII) standard, as defined by IEEE 802.3u. The MAC interface includes the MII clock and data signals.

Figure 3 shows a high-level block diagram of the EFE module, which provides the FIFO handling interface between the NS7520 BBus and the MAC modules.

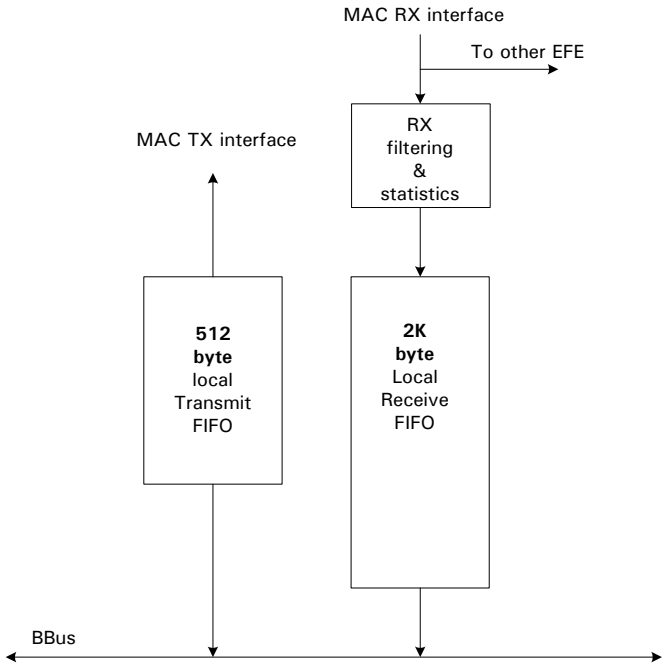


Figure 3: EFE module block diagram

Serial controller

The NS7520 supports two independent universal asynchronous/synchronous receiver/transmitter channels. Each channel supports these features:

- Independent programmable bit-rate generator
- UART, HDLC, SPI (master) modes
- High-speed data transfer:
  - x1 mode: 4Mbits/sec
  - x16 mode: 230Kbits/sec
- 32–byte TX FIFO/32–byte RX FIFO
- Programmable data format:
  - 5 to 8 data bits
  - odd, even, or no parity
  - 1, 2 stop bits
- Programmable channel modes:
  - Normal
  - Local loopback
  - Remote loopback
  - Control signal support

- Maskable interrupt conditions:
  - Receive break detection
  - Receive framing error
  - Receive parity error
  - Receive overrun error
  - Receive FIFO ready
  - Receive FIFO half-full
  - Transmit FIFO ready
  - Transmit FIFO half-empty
  - CTS, DSR, DCD, RI state change detection
- Clock/data encoding:
  - NRZ
  - NRZB
  - NRZI
  - FM
  - Manchester
- Multi-drop capable

NS7520 bootstrap initialization

Many internal NS7520 features are configured when the RESET pin is asserted. The address bus configures the appropriate control register bits at powerup. This table shows which bits control which functions:

Address bit	Name	Description
ADDR[27]	Endian configuration	0 Little Endian configuration 1 Big Endian configuration
ADDR[26]	CPU bootstrap	0 CPU disabled; GEN_BUSER = 1 1 CPU enabled; GEN_BUSER = 0
ADDR[24:23]	CS0/MMCR[19:18] setting	00 8-bit SRAM, 63 wait-states/2'b00 01 32-bit SRAM, 63 wait-states/2'b00 10 32-bit SRAM, 63 wait-states/2'b11 11 16-bit SRAM, 63 wait-states/2'b00
ADDR[19:9]	GEN_ID setting	GEN_ID = A[19:09],Default = 'h3ff
ADDR[8:7]	PLL IS setting	IS = A[8:7]*xnor'b10*,Default = 'b10
ADDR[6:5]	PLL FS setting	FS = A[6:5]*xnor'b00*,Default = 'b00
ADDR[4:0]	PLL ND setting	IS = A[4:0]*xnor'd11*,Default = 'd11

Test modes and PLL operation

The PLLTST_, BISTEN_, and SCANEN_ primary inputs control various test modes for both functional and manufacturing test operations. Table 4 shows how these inputs are encoded.

{PLLTST_, BISTEN_, SCANEN_}	Conditions	Test Modes	Normal Operation	JTAG TAP controller
0	Reserved for factory test			
1	Reserved for factory test			
2	Reserved for factory test			
3	All outputs normal function, PLL disabled	None	PLL bypassed using crystal or external clock	Boundary scan
4	All outputs normal, PLL enabled	None	PLL operational using crystal or external clock	Boundary scan
5	Reserved for factory test			
6	All outputs normal function, PLL enabled	None	PLL operational using crystal or external clock	ARM JTAG debugger
7	All outputs normal function, PLL disabled	None	PLL bypassed using crystal or external clock	ARM JTAG debugger

Table 4: NS7520 test modes

JTAG

The NS7520 provides full support for 1149.1 JTAG boundary scan testing. All NS7520 pins can be controlled using the JTAG interface port. BDSL files (which tell equipment how to test the NS7520 with JTAG) are available. The JTAG interface also provides access to the ARM7 debug module when the appropriate combination of PLLTST_, BISTEN_, and SCANEN_ is selected (as shown in Table 4: "NS7520 test modes" on page 18).

ARM Debug

The ARM7 core uses a JTAG TAP controller that shares the pins with the TAP controller used for 1149.1 JTAG boundary scan testing. To enable the ARM7 TAP controller, {PLLTST_,BISTEN_,SCANEN_} must be set as shown in Table 4: "NS7520 test modes" on page 18.

The NS7520 is compatible with two ICE debuggers:

- Macraigor Systems Raven (aka Blackbird)
- EPI JEENI probe

Factory-tested

The NS7520 is factory-tested using standard BIST techniques, including flip-flop ATPG chains, internal memory BIST, ARM standard tests for the ARM7 core, and a test isolating the PLL.

DC characteristics and other operating specifications

The NS7520 operates using an internal core V_{DD} supply voltage of 1.5V. The NS7520 operates the I/O pad ring using a V_{DD} supply voltage of 3.3V.

Table 5 provides the DC characteristics for inputs; Table 6 provides the DC characteristics for outputs.

Sym	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high voltage		2.0		3.6	V
V_{IL}	Input low voltage		V_{SS} – 0.3		0.8	V
I_{IL}	Input buffer	$V_{IN} = V_{DD}$	-10		10	µA
	Input buffer with pulldown		10	30	60	µA
I_{IH}	Input buffer	$V_{IN} = V_{SS}$	-10		10	µA
	Input buffer with pullup		-60	-30	-10	µA
V_T	Switching threshold	Any input		1.4		V

Table 5: DC characteristics — inputs

Sym	Parameter	Conditions	Min	Typ	Max	Unit
P	Power consumption	F_{SYSCLK} = 55 MHz			500	Mw
		F_{SYSCLK} = 46 MHz			418	Mw
		F_{SYSCLK} = 32 MHz			291	Mw
V_{OL}	Output low voltage	Outputs & bi-directional	0		0.4	mA
V_{OH}	Output high voltage	Outputs & bi-directional	2.7		V_{DD}	mA

Table 6: DC characteristics — outputs

Table 7 defines the DC operating (thermal) conditions for the NS7520. Operating the NS7520 outside these conditions results in unpredictable behavior.

Sym	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Core supply voltage		1.4	1.5	1.6	V
V_{CC}	I/O supply voltage		3.0	3.3	3.6	V

Table 7: Recommended operating temperatures

Sym	Parameter	Conditions	Min	Typ	Max	Unit
T_{OP}	Ambient temperature		-40		85	°C
T_J	Junction temperature				110	V
T_{STG}	Storage temperature		-40		125	V
θ_J	Pkg thermal resistance			50		°C/W
I_{IH}		No pullup With pullup	-10 10		10 200	mA mA
I_{IL}	Input current as “0”	No pullup With pullup	10 10		10 200	mA mA
I_{OZ}	HighZ leakage current	Any input	-10		10	mA
C_{IO}	Pin capacitance	$V_O = 0$			7	pF

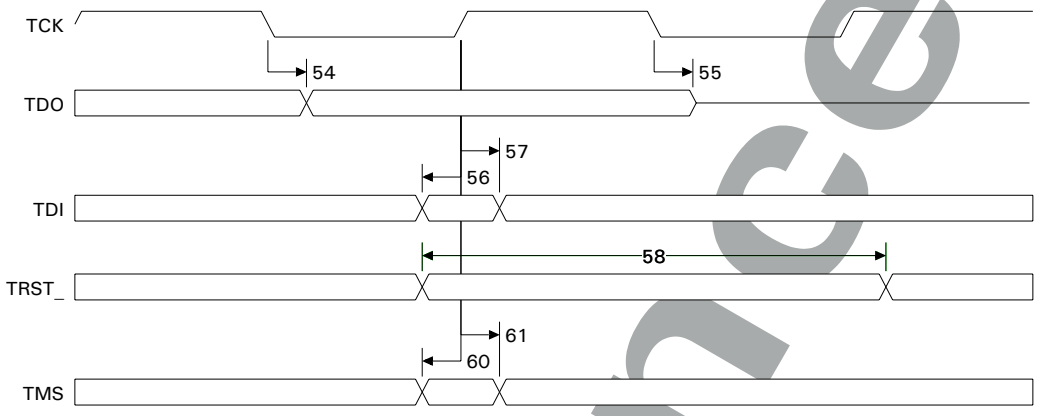
Table 7: Recommended operating temperatures

Timing Diagrams

The timing diagrams are presented in alphabetical order.

arm_ice_jtag timing

The arm_ice_jtag diagram shows the timing for the JTAG interface when used for ARM ICE. The T_{TCK} parameter represents one period of the TCK clock.

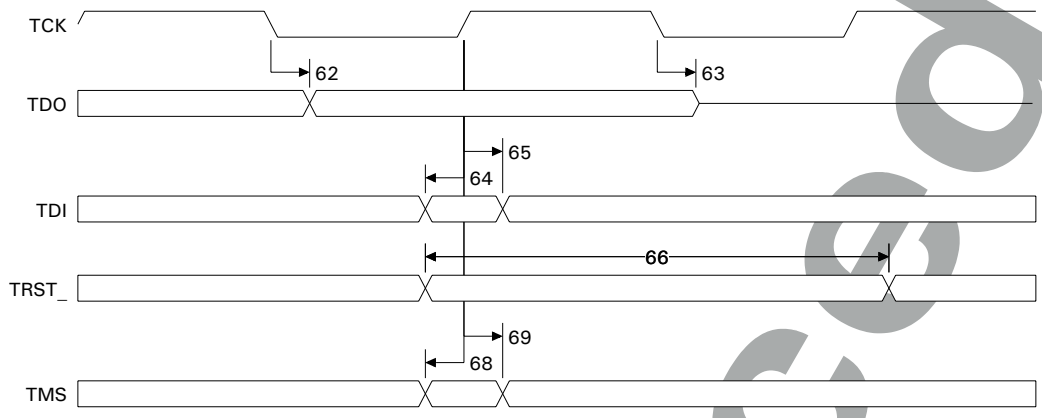


arm_ice_jtag timing parameters

Num	Description	Min	Typ	Max	Units
54	TCK falling to TDO valid			22	ns
55	TCK falling to TDO HighZ			22	ns
56	TDI setup to TCK rising	5			ns
57	TDI hold from TCK rising	0			ns
58	TRST_ period	1			T_{TCK}
60	TMS setup to TCK rising	5			ns
61	TMS hold from TCK rising	0			ns

bscan_jtag timing

The bscan_jtag diagram shows the timing for the JTAG interface when used for boundary scan. The T_{TCK} parameter represents one period of the TCK clock.

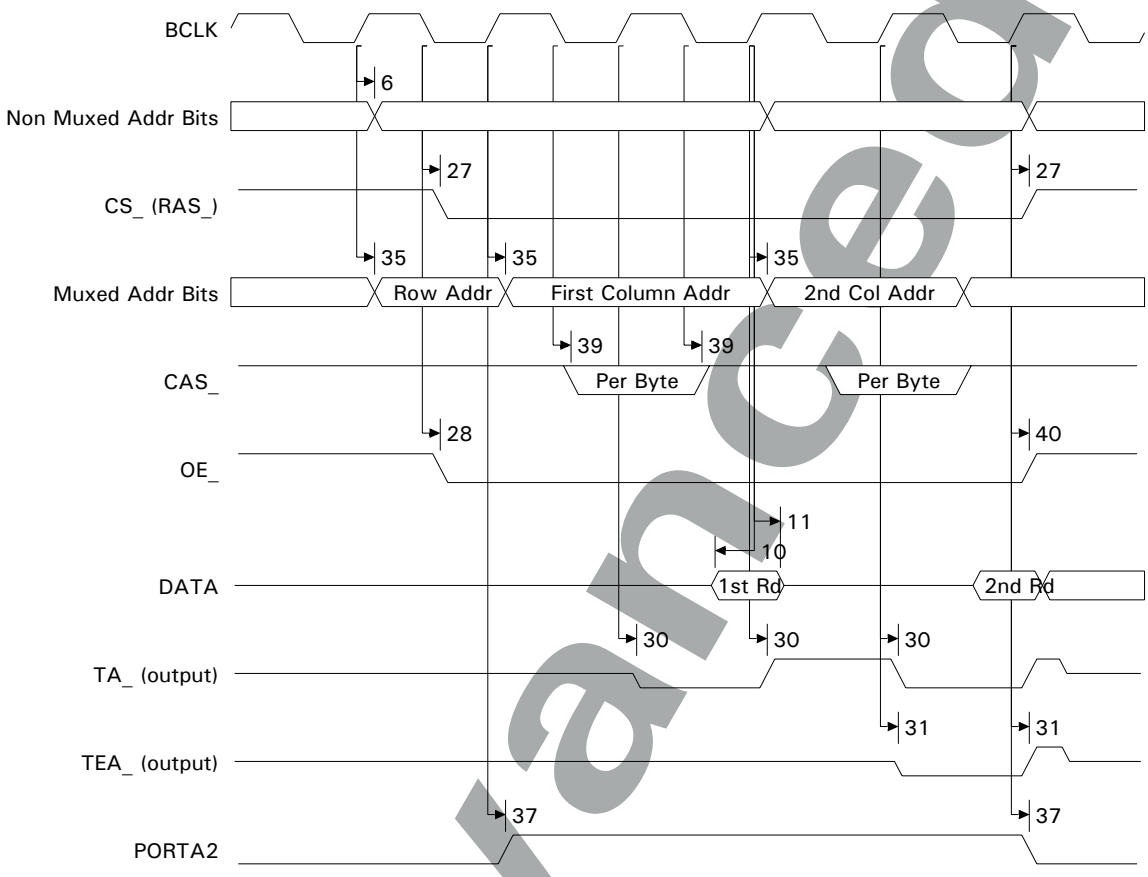


bscan_jtag timing parameters

Num	Description	Min	Typ	Max	Units
62	TCK falling to TDO valid			22	ns
63	TCK falling to TDO HighZ			22	ns
64	TDI setup to TCK rising	5			ns
65	TDI hold from TCK rising	0			ns
66	TRST_ width	1			T_{TCK}
68	TMS setup to TCK rising	5			ns
69	TMS hold from TCK rising	0			ns

edo_dram_read timing

The EDO_DRAM_read timing diagram shows a burst of two. With a single transaction, CS[4:0] is negated two clocks earlier and there is no second read data. With a larger burst, CS[4:0] is extended additional clocks and additional read data.



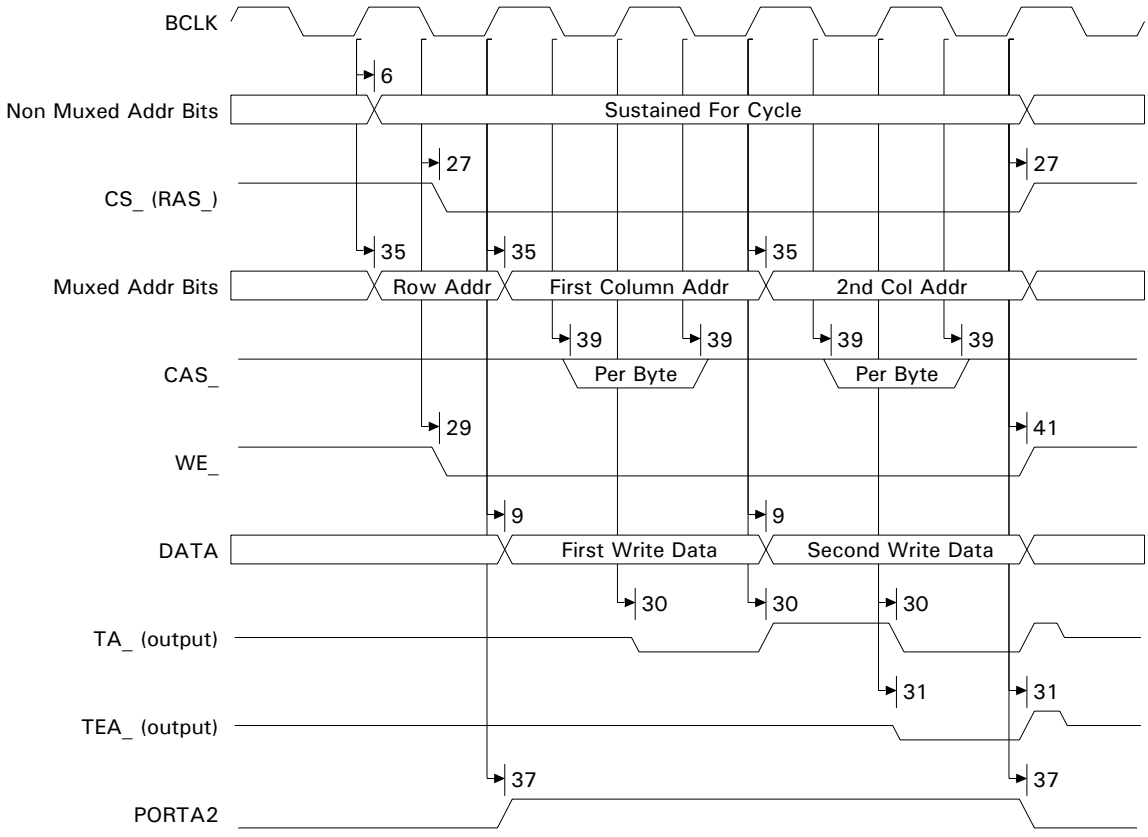
edo_dram_read timing parameters

Num	Description	Min	Typ	Max	Units
6	BCLK to non–multiplexed address valid			12.75	ns
27	BCLK to CS[4:0]_ (RAS_)			14.75	ns
35	BCLK rising to multiplexed address valid			14.75	ns
39	BCLK falling to CAS_			14.75	ns
28	BCLK falling to OE_			15.75	ns
40	BCLK rising to OE_			15.75	ns
10	Read data setup to BCLK rising	10			ns
11	Read data hold from BCLK rising	1			ns
30	BCLK to TA_			15.75	ns

Num	Description	Min	Typ	Max	Units
31	BCLK to TEA_			15.75	ns
37	BCLK to PORTA2			8	ns

edo_dram_write timing

The EDO_DRAM_write timing diagram shows a burst of two. With a single transaction, CS[4:0] is negated two clocks earlier and there is no second write data. With a larger burst, CS[4:0] is extended additional clocks and additional write data.



edo_dram_write timing parameters

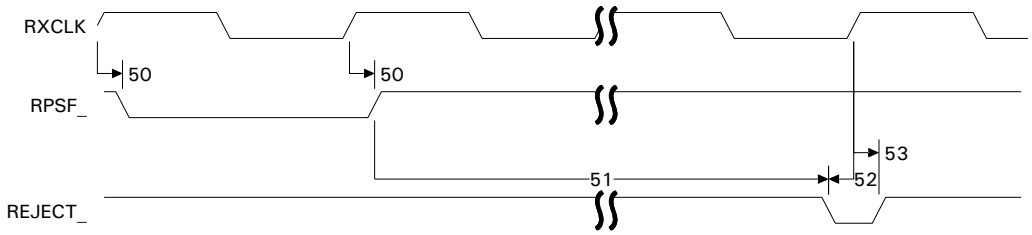
Num	Description	Min	Typ	Max	Units
6	BCLK to non–multiplexed address valid			12.75	ns
27	BCLK falling to CS[4:0]_ (RAS_)			14.75	ns
35	BCLK rising to multiplexed address valid			14.75	ns
39	BCLK falling to CAS_			14.75	ns
29	BCLK falling to WE_			15.75	ns

Num	Description	Min	Typ	Max	Units
41	BCLK rising to WE_			15.75	ns
9	BCLK rising to data valid			14.75	ns
30	BCLK to TA_			15.75	ns
31	BCLK to TEA_			15.75	ns
37	BCLK to PORTA2			8	ns

enet_cam timing

This diagram illustrates Ethernet CAM filter timing:

- The maximum interval between the assertion of RPSF_ and REJECT_ recognition is a function of T_{RXCLK}; that is, a number of RXCLK clock cycles.
- External synchronization typically is required to meet the timing of REJECT_ versus RXCLK.

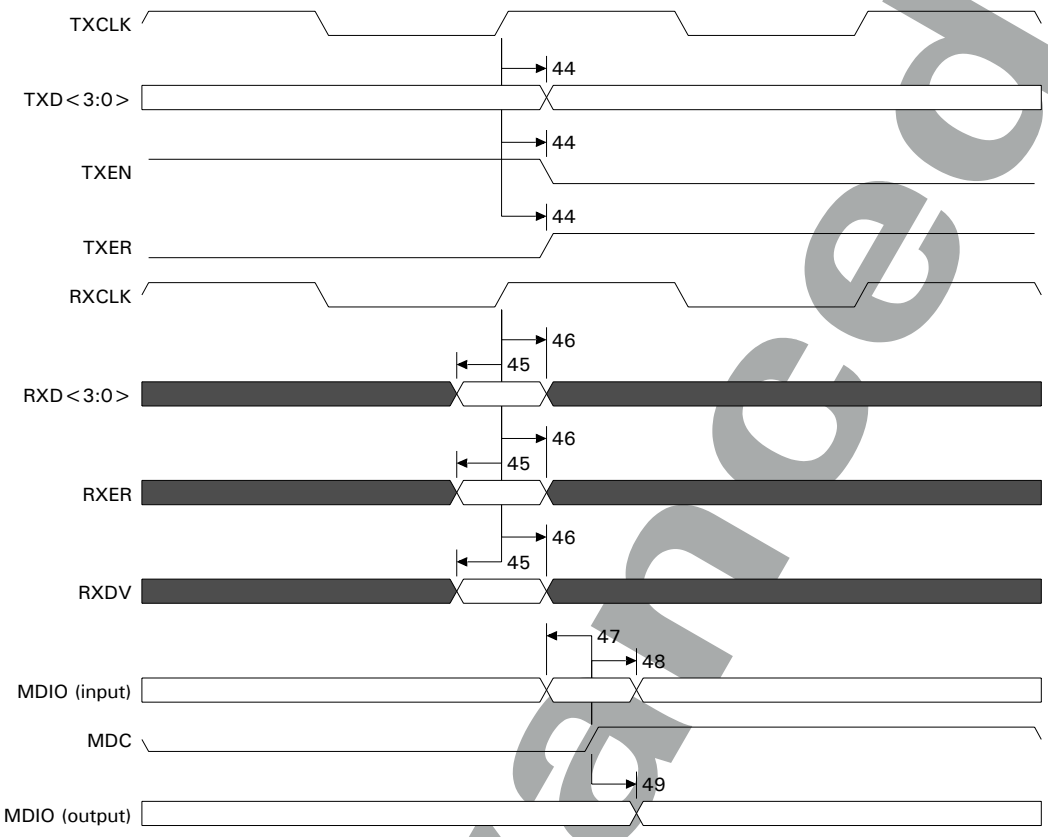


ethernet_cam timing parameters

Num	Description	Min	Typ	Max	Units
50	RXCLK rising to RSPF_			11	ns
51	RPSF_ assertion to REJECT_ assertion			488	T_{RXCLK}
52	REJECT_ setup to RXCLK rising	4			ns
53	REJECT_ hold from RXCLK rising	1			ns

enet_phy timing

The Ethernet_PHY timing diagram shows Ethernet PHY timing requirements. Note that three sets of signals are referenced to three clocks: TXCLK, RXCLK, and MDC.

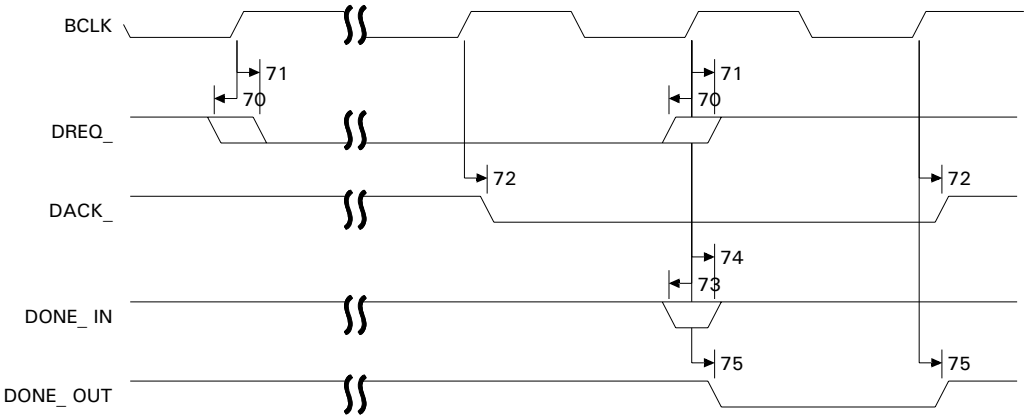


ethernet_phy timing parameters

Num	Description	Min	Typ	Max	Units
44	TXCLK rising to TXD, TXDV, TXER			12.75	ns
45	RXD, RXER, RXDV setup to RXCLK rising	10			ns
46	RXD, RXER, RXDV hold from RXCLK rising	10			ns
47	MDIO (input) setup to MDC rising	10			ns
48	MDIO (input) hold from MDC rising	5			ns
49	MDC rising to MDIO (output)			150	ns

external_dma_timing

This diagram shows timing for external DMA.

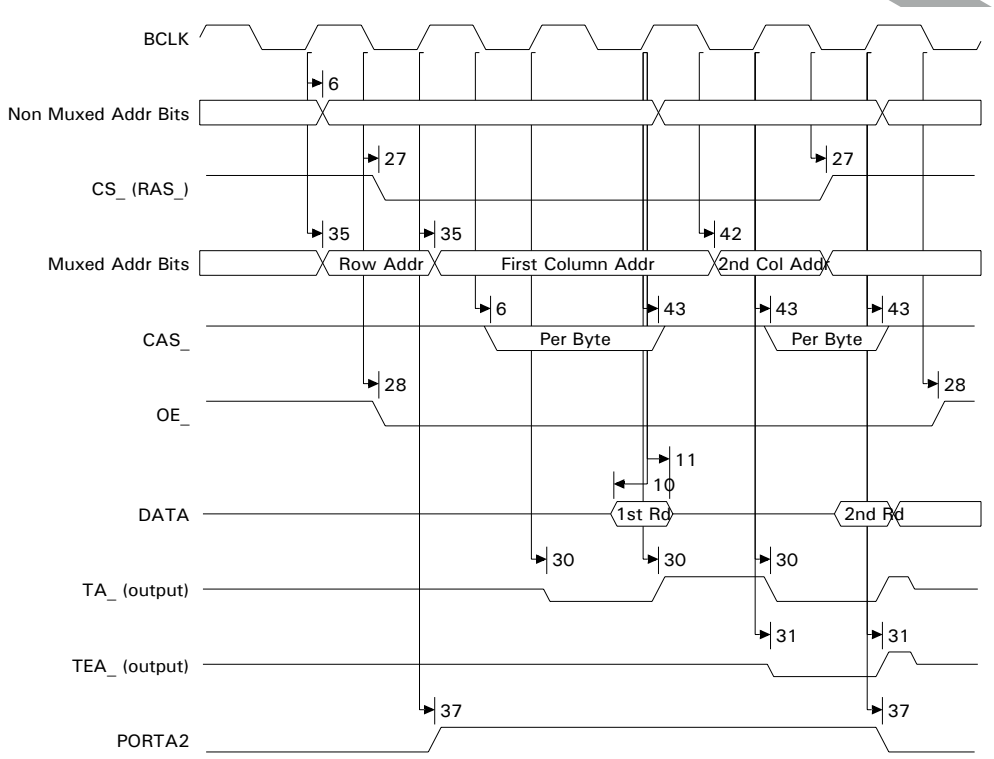


external_dma_timing parameters

Num	Description	Min	Typ	Max	Units
70	DREQ_ setup to BCLK rising	5			ns
71	DREQ_ hold from BCLK rising	0			ns
72	BCLK rising to DACK_			15.75	ns
73	DONE_ “IN” setup to BCLK rising	0			ns
74	DONE_ “IN” hold from BCLK rising	0			ns
75	BCLK rising to DONE_ “OUT”			15.75	ns

fp_dram_read_timing

The FP_DRAM_read timing diagram shows a burst of two. With a single transaction, CS[4:0] is negated two clocks earlier and there is no second read data. With a larger burst, CS[4:0] is extended additional clocks and additional read data.

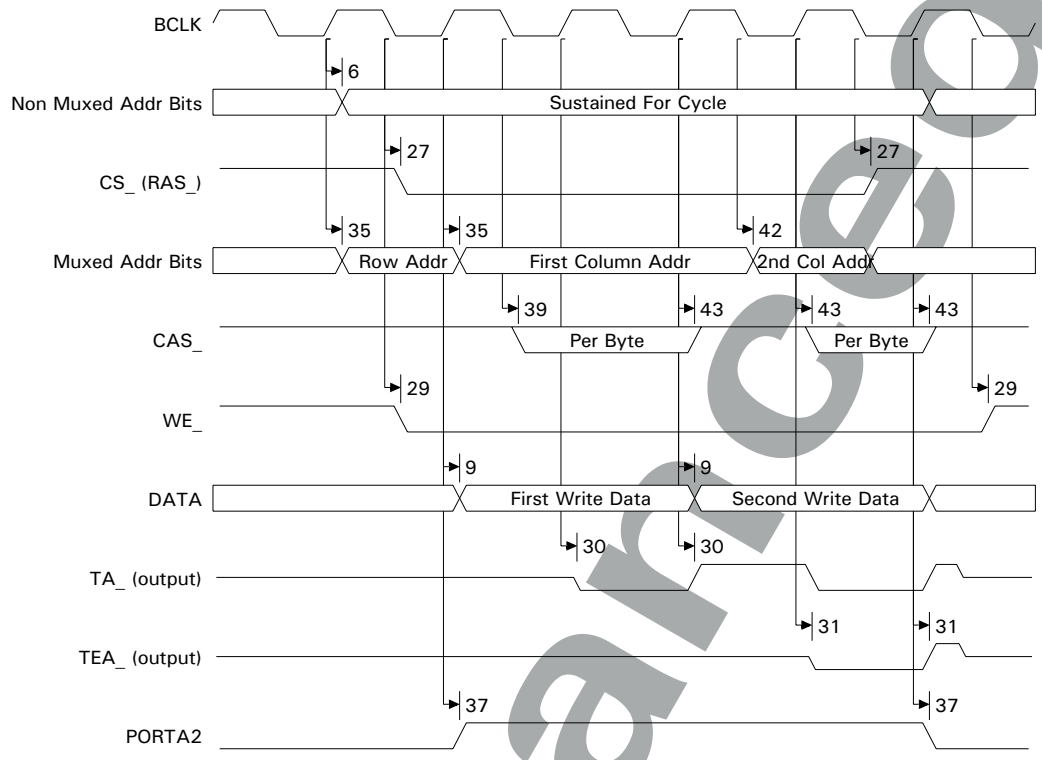


fp_dram_read_timing parameters

Num	Description	Min	Typ	Max	Units
6	BCLK to non–multiplexed address valid			12.75	ns
27	BCLK falling to CS[4:0]_ (RAS_)			14.75	ns
35	BCLK rising to multiplexed address valid			14.75	ns
42	BCLK falling to multiplexed address valid			14.75	ns
39	BCLK falling to CAS_			14.75	ns
43	BCLK rising to CAS_			14.75	ns
28	BCLK falling to OE_			15.75	ns
10	Read data setup to BCLK rising	10			ns
11	Read data hold from BCLK rising	1			NS
30	BCLK to TA_			15.75	ns
31	BCLK to TEA_			15.75	ns
37	BCLK to PORTA2			8	ns

fp_dram_write_timing

The FP_DRAM_write timing diagram shows a burst of two. With a single transaction, CS[4:0] is negated two clocks earlier and there is no second read data. With a larger burst, CS[4:0] is extended additional clocks and additional read data.

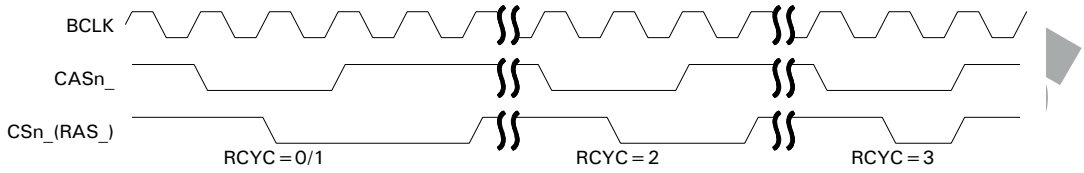


fp_dram_write_timing parameters

Num	Description	Min	Typ	Max	Units
6	BCLK to non-multiplexed address valid			12.75	ns
27	BCLK falling to CS[4:0]_ (RAS_)			14.75	ns
35	BCLK rising to multiplexed address valid			14.75	ns
42	BCLK falling to multiplexed address valid			14.75	ns
39	BCLK falling to CAS_			14.75	ns
43	BCLK rising to CAS_			14.75	ns
29	BCLK falling to WE_			12.75	ns
9	BCLK rising to data valid			14.75	ns
30	BCLK to TA_			15.75	ns
31	BCLK to TEA_			15.75	ns
37	BCLK to PORTA2			8	ns

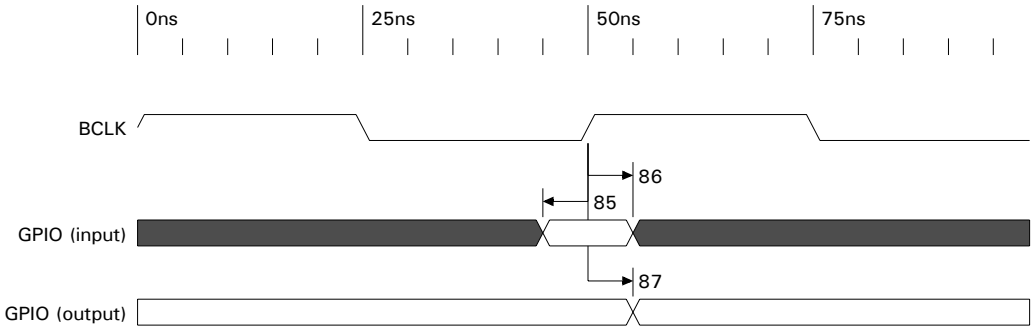
fp_edo_refresh_cycles

This diagram shows RCYC timing as a function of the RCYC field.



gpio_timing

In the GPIO timing diagram, the input specifications define the timing to an internal flop. This internal flop is read by the microprocessor and is further subject to internal bus acquisition and cycle time uncertainty. If timing versus BCLK is not met for a particular transition, the signal may be read with its previous value.



gpio_timing parameters

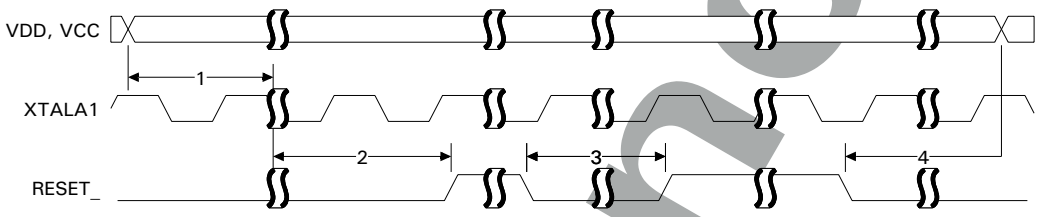
Num	Description	Min	Type	Max	Units
85	GPIO (input) setup to BCLK rising	15			ns
86	GPIO (input) hold from BCLK rising	0			ns
87	BCLK riding to GPIO (output)			15.75	ns

reset_timing

From poweroff, reset must be asserted until all power supplies are above their specified thresholds. An additional 8 microseconds is required for oscillator settling time. After the oscillator is settled and while valid power is maintained, reset must be asserted for three periods of the XTALA1 clock in the following situations:

- Prior to release of reset after application of power
- While valid power is maintained to initiate *hot reset* (reset while power is at or above specified thresholds)
- Prior to loss of valid power during power outage/power down

The PORTC4 output indicates the reset state of the chip. PORTC4 persists beyond the negation of RESET_ for approximately 512 system clock cycles if the PLL is disabled. When the PLL is enabled, PORTC4 persists beyond the negation of RESET_ to allow for PLL lock for 100 microseconds times the ratio of the VCO to XTALA.



reset timing parameters

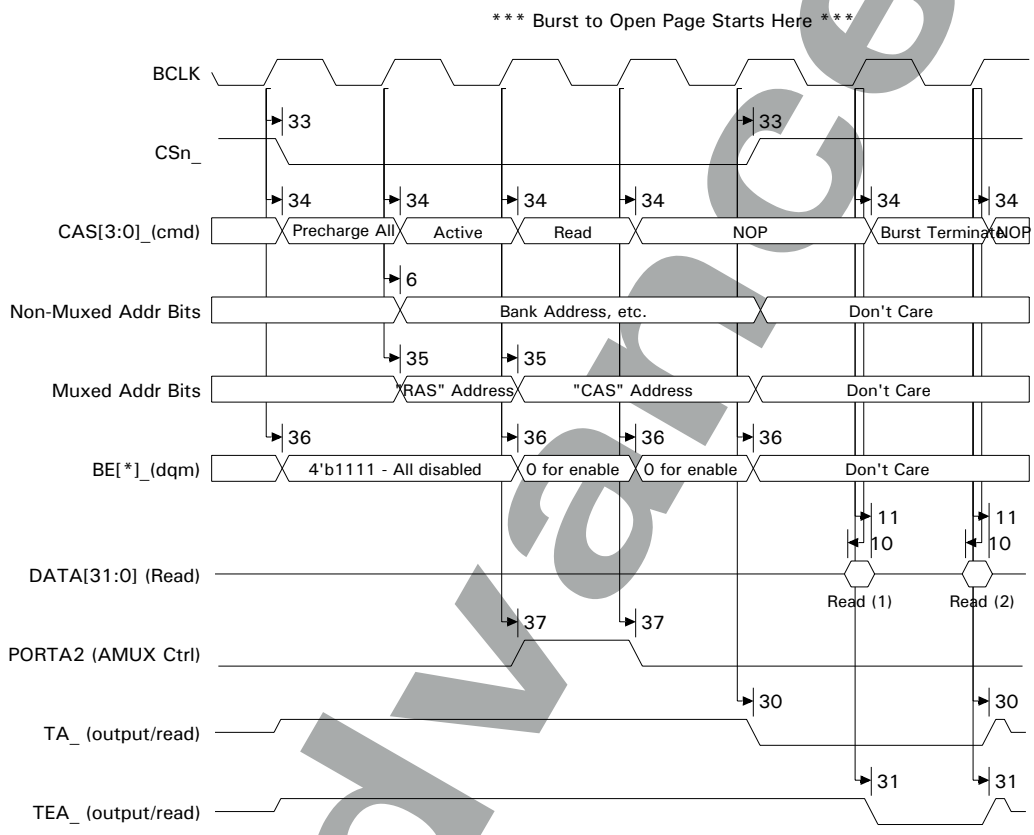
Num	Description	Min	Typ	Max	Units
1	Power valid before reset negated	8			µs
2	Reset asserted after power valid	3			T_{XTALA1}
3	Reset asserted while power valid	3			T_{XTALA1}
4	Reset asserted before power valid	3			T_{XTALA1}

sdram_read_timing

The SDRAM_read timing diagram shows a burst of two. With a single transaction, CS[4:0] is negated one clock earlier and there is no second read data. With a larger burst, CS[4:0] is extended additional clocks and additional read data.

The timing shown is `CAS latency=2`. With different CAS latency values, the point at which read data is valid shifts accordingly but setup/hold time remains constant.

This diagram illustrates the initiation of a burst cycle to non–open page. For a transaction or burst to an open page, the cycle starts with the read command. Note the relationship of the burst terminate command to the output of the last operand by the SDRAM.



sdram_read_timing parameters

Num	Description	Min	Typ	Max	Units
33	BCLK rising to CS[4:0]			14.75	ns
34	BCLK to SDRAM command/A10 valid			14.75	ns
6	BCLK to non–multiplexed address valid			12.75	ns
35	BCLK rising to multiplexed address valid			14.75	ns
36	BCLK to SDRAM BE_ (DQM_)			14.75	ns

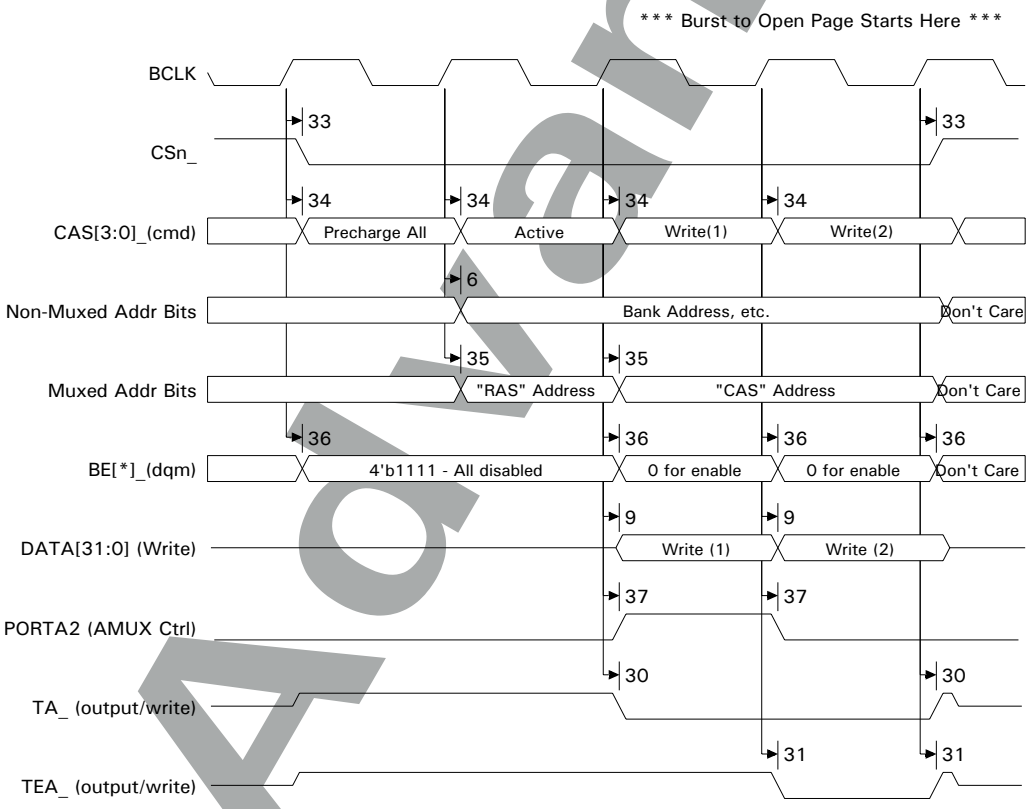
Num	Description	Min	Typ	Max	Units
10	Read data setup to BCLK	10			ns
11	Read data hold from BCLK	1			ns
37	BCLK to PORTA2			8	ns
30	BCLK to TA_			15.75	ns
31	BCLK to TEA_			15.75	ns

sdram_write_timing

The SDRAM_write timing diagram shows a burst of two. With a single transaction, CS[4:0] is negated one clock earlier and there is no second write data. With a larger burst, CS[4:0] is extended additional clocks and additional write data.

The timing shown is independent of CAS latency.

This diagram illustrates the initiation of a burst cycle to non–open page. For a transaction or burst to an open page, the cycle starts with the write command. The NS7520 sets single character write operation of the SDRAM;=. No burst terminate is generated or necessary for write burst cycles.



sdram_write_timing parameters

Num	Description	Min	Typ	Max	Units
33	BCLK rising to CS[4:0]			14.75	ns
34	BCLK to SDRAM command/A10 valid			14.75	ns
6	BCLK to non–multiplexed address valid			12.75	ns
35	BCLK rising to multiplexed address valid			14.75	ns
36	BCLK to SDRAM BE_ (DQM_)			14.75	ns
9	BCLK to write data valid			14.75	ns
37	BCLK to PORTA2			8	ns
30	BCLK to TA_			15.75	ns
31	BCLK to TEA_			15.75	ns

sdram — other commands

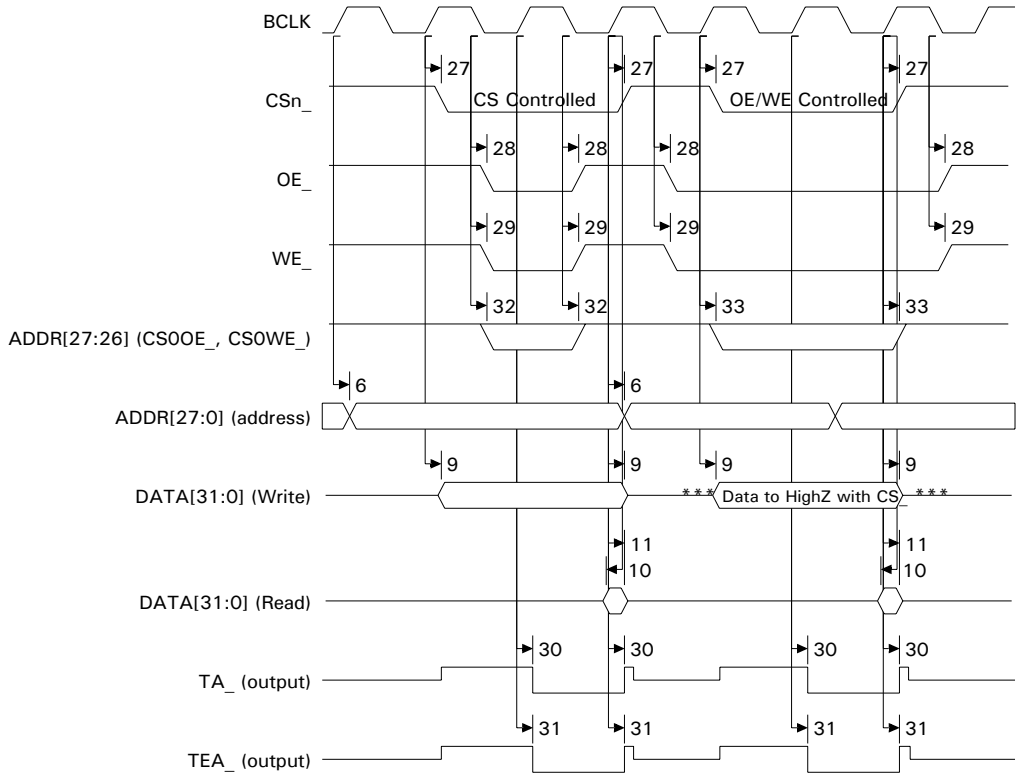
CAS[3:0] timing applies to all SDRAM commands as shown by number 34 in the SDRAM read timing and write timing diagrams. MUXed address bits timing applies to Control Register Load commands as shown by number 35 in the SDRAM read timing and write timing diagrams. All commands follow protocol rules by JEDEC SDRAM standards.

sram_timing

The SRAM timing diagram shows CS–controlled and OE/WE–controlled cycles. The data bus for WE–controlled writes is driven to HighZ before WE_ is negated.

Burst cycles result in additional addresses and the corresponding signalling at the point CS[4:0] is negated. If the EXTTA or OE/WE–controlled options are selected for a chip select, there is no break in the OE_ or WE_ signals between burst transactions.

The TA_ output assertion or the combined output assertion of TA_ and TEA_ correspond to the time that valid data is written or read. The outputs operate only when a chip select is controlling the transaction.



sram_timing parameters

Num	Description	Min	Typ	Max	Units
27	BCLK to CS[4:0]			14.75	ns
28	BCLK to OE_			15.75	ns
29	BCLK to WE_			15.75	ns
32	BCLK to A[27:26] as CS0OE_/CS0WE_			12.75	ns
6	BCLK to non–multiplexed address valid			12.75	ns
9	BCLK to write data valid			14.75	ns
10	Read data setup to BCLK	10			ns
11	Read data hold from BCLK	1			ns
30	BCLK to TA_			15.75	ns
31	BCLK to TEA_			15.75	ns

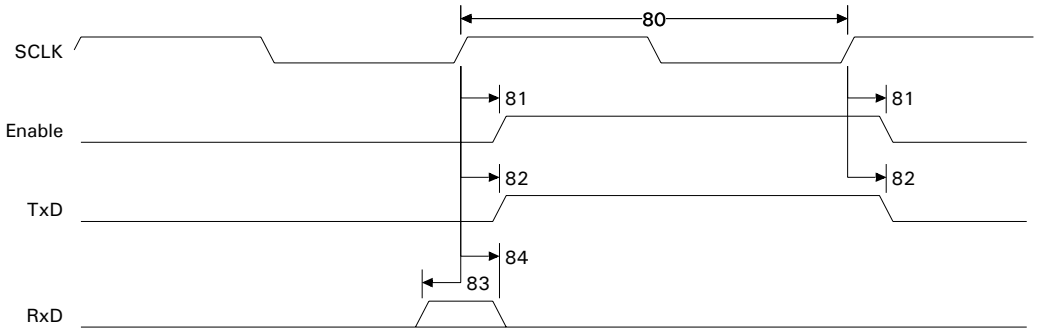
SRAM timing – burst

Burst cycles to an SRAM involve no additional timing parameters. Address, data, and the like change on the BCLK edge where the transaction completes.

- For SRAM using internal TA_/TEA_ generation, this coincides with the edge on which the TA_/TEA_ signals are asserted.
- For SRAM using external TA_/TEA_ generation, this coincides with the BCLK edge that follows the edge on which TA_/TEA_ are asserted, by the selected number of synchronizer stages.
- For CS-controlled cycles, no transitions are seen on CS[4:0] between burst cycle transactions.

sync_serial_ext_clk_timing

The synchronous serial timing – external clock diagram shows synchronous serial timing when the clock is externally generated. This diagram shows a non-inverted clock situation. In an inverted clock situation, the SCLK signal is an inverted version of the signal shown here.



sync_serial_ext_clk_timing parameters

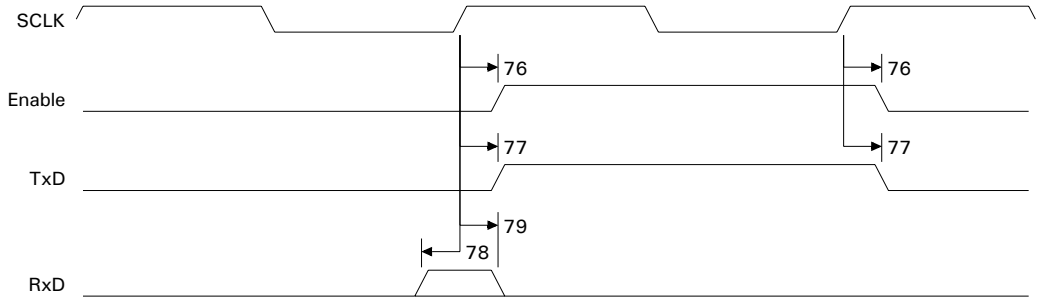
Num	Description	Min	Typ	Max	Units
80	SCLK frequency			10	MHz
	SCLK duty cycle	45		55	%
81	SCLK to enable	1			T_{SCLK}
82	SCLK to TxD			4	ns
83	RxD setup to SCLK	2			ns
84	RxD hold from SCLK	1			ns

sync_serial_int_clk_timing

The synchronous internal timing – internal clock diagram shows synchronous serial timing when the clock is generated internally.

- The T_{SYS} parameter represents one period of the internal system clock.
- The T_{SCLK} parameter represents one period of SCLK.
- SCLK is held inactive between character transfers.
- The enable signal is asserted before SCLK makes its first transition to the active state, and is negated after SCLK is returned to the inactive state.

This diagram shows a non-inverted clock situation. In an inverted clock situation, the SCLK signal is an inverted version of the signal shown here.



sync_serial_int_clk_timing parameters

Num	Description	Min	Typ	Max	Units
76	SCLK to enable	1			T_{SCLK}
77	SCLK to TxD			$3T_{SYS}+4$	ns
78	RxD setup to SCLK	2			ns
79	RxD hold from SCLK	1			ns

timing_specifications

All timing specifications consist of the relationship between a reference clock and a signal:

- There are bussed and non–bussed signals. Non–bussed signals separately illustrate 0–to–1 and 1–to–0 transitions.
- Inputs have setup/hold times versus clock rising.
- Outputs have switching time relative to either clock rising or clock falling.

Note: Timing relationships in this diagram are drawn without proportion to actual delay.