Features

- Incorporates the ARM920T™ ARM® Thumb® Processor
  - 200 MIPS at 180 MHz
  - 16-KByte Data Cache, 16-KByte Instruction Cache, Write Buffer
  - Memory Management Unit
  - In-circuit Emulator including Debug Communication Channel
  - Mid-level Implementation Embedded Trace Macrocell (256-ball BGA Package Only)
- Additional Embedded Memories
  - 16K Bytes of SRAM and 128K Bytes of ROM
- External Bus Interface (EBI)
  - Supports SDRAM, Static Memory, Burst Flash, Glueless Connection to CompactFlash®, SmartMedia™ and NAND Flash
- System Peripherals for Enhanced Performance:
  - Enhanced Clock Generator and Power Management Controller
  - Two On-chip Oscillators with Two PLLs
  - Very Slow Clock Operating Mode and Software Power Optimization Capabilities
  - Four Programmable External Clock Signals
  - System Timer Including Periodic Interrupt, Watchdog and Second Counter
  - Real-time Clock with Alarm Interrupt
  - Debug Unit, Two-wire UART and Support for Debug Communication Channel
  - Advanced Interrupt Controller with 8-level Priority, Individually Maskable Vectored Interrupt Sources, Spurious Interrupt Protected
  - Seven External Interrupt Sources and One Fast Interrupt Source
  - Four 32-bit PIO Controllers with Up to 122 Programmable I/O Lines, Input Change Interrupt and Open-drain Capability on Each Line
  - 20-channel Peripheral Data Controller (DMA)
- Ethernet MAC 10/100 Base-T
  - Media Independent Interface (MII) or Reduced Media Independent Interface (RMII)
  - Integrated 28-byte FIFOs and Dedicated DMA Channels for Receive and Transmit
- USB 2.0 Full Speed (12 M-bits per second) Host Double Port
  - Dual On-chip Transceivers (Single Port Only on 208-lead PQFP Package)
  - Integrated FIFOs and Dedicated DMA Channels
- USB 2.0 Full Speed (12 M-bits per second) Device Port
  - On-chip Transceiver, 2-Kbyte Configurable Integrated FIFOs
- Multimedia Card Interface (MCI)
  - Automatic Protocol Control and Fast Automatic Data Transfers
  - MMC and SD Memory Card-compliant, Supports Up to Two SD Memory Cards
- Three Synchronous Serial Controllers (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I^2S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Four Universal Synchronous/Asynchronous Receiver/Transmitters (USART)
  - Support for ISO7816 T0/T1 Smart Card
  - Hardware and Software Handshaking
  - RS485 Support, IrDA Up To 115 Kbps
  - Full Modem Control Lines on USART1
- Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, 4 External Peripheral Chip Selects
- Two 3-channel, 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- Two-wire Interface (TWI)
  - Master Mode Support, All 2-wire Atmel EEPROMs Supported
- IEEE 1149.1 JTAG Boundary Scan on All Digital Pins
- Power Supplies
  - 1.65V to 1.95V for VDDCORE, VDDOSC and VDDPLL
  - 1.65V to 3.6V for VDDIOP (Peripheral I/Os) and for VDDIOM (Memory I/Os)
- Available in a 208-lead PQFP or 256-ball BGA Package

ARM920T™-based Microcontroller

AT91RM9200 Summary

Rev. 1768FS–ATARM–02/03

Description

The AT91RM9200 is a complete system-on-chip built around the ARM920T ARM Thumb processor. It incorporates a rich set of system and application peripherals and standard interfaces in order to provide a single-chip solution for a wide range of compute-intensive applications that require maximum functionality at minimum power consumption at lowest cost.

The AT91RM9200 incorporates a high-speed on-chip SRAM workspace, and a low-latency External Bus Interface (EBI) for seamless connection to whatever configuration of off-chip memories and memory-mapped peripherals is required by the application. The EBI incorporates controllers for synchronous DRAM (SDRAM), Burst Flash and Static memories and features specific circuitry facilitating the interface for SmartMedia, CompactFlash and NAND Flash.

The Advanced Interrupt Controller (AIC) enhances the interrupt handling performance of the ARM920T processor by providing multiple vectored, prioritized interrupt sources and reducing the time taken to transfer to an interrupt handler.

The Peripheral Data Controller (PDC) provides DMA channels for all the serial peripherals, enabling them to transfer data to or from on- and off-chip memories without processor intervention. This reduces the processor overhead when dealing with transfers of continuous data streams.The AT91RM9200 benefits from a new generation of PDC which includes dual pointers that simplify significantly buffer chaining.

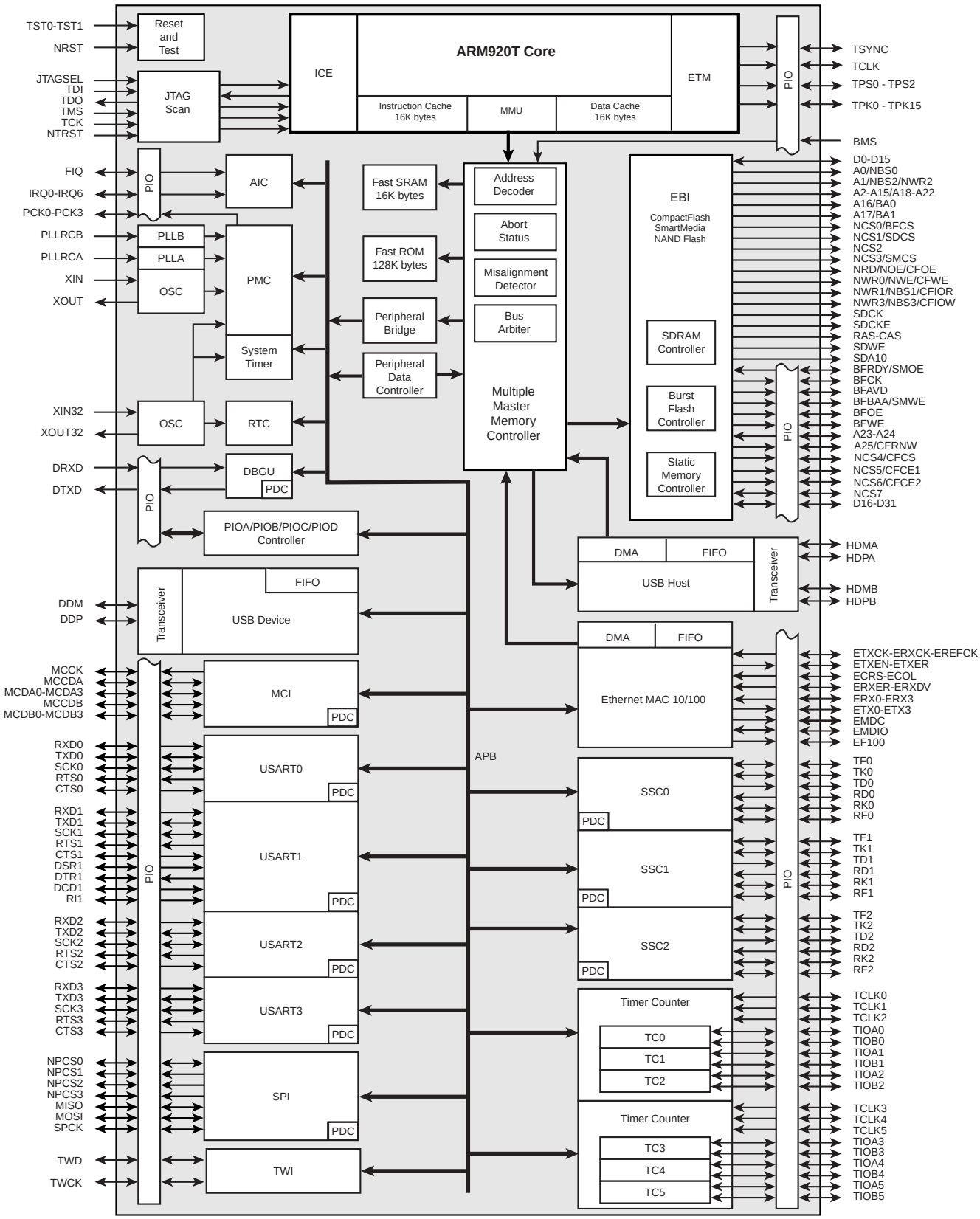
The set of Parallel I/O (PIO) controllers multiplex the peripheral input/output lines with general-purpose data I/Os for maximum flexibility in device configuration. An input change interrupt, open drain capability and programmable pull-up resistor is included on each line.

The Power Management Controller (PMC) keeps system power consumption to a minimum by selectively enabling/disabling the processor and various peripherals under software control. It uses an enhanced clock generator to provide a selection of clock signals including a slow clock (32 kHz) to optimize power consumption and performance at all times.

The AT91RM9200 integrates a wide range of standard interfaces including USB 2.0 Full Speed Host and Device and Ethernet 10/100 Base-T Media Access Controller (MAC), which provides connection to a extensive range of external peripheral devices and a widely used networking layer. In addition, it provides an extensive set of peripherals that operate in accordance with several industry standards, such as those used in audio, telecom, Flash Card, infrared and Smart Card applications.

To complete the offer, the AT91RM9200 benefits from the integration of a wide range of debug features including JTAG-ICE, a dedicated UART debug channel (DBGU) and an embedded real time trace. This enables the development and debug of all applications, especially those with real-time constraints.

Figure 1. AT91RM9200 Block Diagram



Pinout

Table 1. AT91RM9200 Pinout for 208-lead PQFP Package

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
1	PC24	37	VDDPLL	73	PA27	109	TMS
2	PC25	38	PLLRCB	74	PA28	110	NTRST
3	PC26	39	GNDPLL	75	VDDIOP	111	VDDIOP
4	PC27	40	VDDIOP	76	GND	112	GND
5	PC28	41	GND	77	PA29	113	TST0
6	PC29	42	PA0	78	PA30	114	TST1
7	VDDIOM	43	PA1	79	PA31/BMS	115	NRST
8	GND	44	PA2	80	PB0	116	VDDCORE
9	PC30	45	PA3	81	PB1	117	GND
10	PC31	46	PA4	82	PB2	118	PB23
11	PC10	47	PA5	83	PB3	119	PB24
12	PC11	48	PA6	84	PB4	120	PB25
13	PC12	49	PA7	85	PB5	121	PB26
14	PC13	50	PA8	86	PB6	122	PB27
15	PC14	51	PA9	87	PB7	123	PB28
16	PC15	52	PA10	88	PB8	124	PB29
17	PC0	53	PA11	89	PB9	125	HDMA
18	PC1	54	PA12	90	PB10	126	HDPA
19	VDDCORE	55	PA13	91	PB11	127	DDM
20	GND	56	VDDIOP	92	PB12	128	DDP
21	PC2	57	GND	93	VDDIOP	129	VDDIOP
22	PC3	58	PA14	94	GND	130	GND
23	PC4	59	PA15	95	PB13	131	VDDIOM
24	PC5	60	PA16	96	PB14	132	GND
25	PC6	61	PA17	97	PB15	133	A0/NBS0
26	VDDIOM	62	VDDCORE	98	PB16	134	A1/NBS2/NWR2
27	GND	63	GND	99	PB17	135	A2
28	VDDPLL	64	PA18	100	PB18	136	A3
29	PLLRCA	65	PA19	101	PB19	137	A4
30	GNDPLL	66	PA20	102	PB20	138	A5
31	XOUT	67	PA21	103	PB21	139	A6
32	XIN	68	PA22	104	PB22	140	A7
33	VDDOSC	69	PA23	105	JTAGSEL	141	A8
34	GNDOSC	70	PA24	106	TDI	142	A9
35	XOUT32	71	PA25	107	TDO	143	A10
36	XIN32	72	PA26	108	TCK	144	SDA10

Table 1. AT91RM9200 Pinout for 208-lead PQFP Package (Continued)

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
145	A11	161	PC7	177	CAS	193	D10
146	VDDIOM	162	PC8	178	SDWE	194	D11
147	GND	163	PC9	179	D0	195	D12
148	A12	164	VDDIOM	180	D1	196	D13
149	A13	165	GND	181	D2	197	D14
150	A14	166	NCS0/BFCS	182	D3	198	D15
151	A15	167	NCS1/SDCS	183	VDDIOM	199	VDDIOM
152	VDDCORE	168	NCS2	184	GND	200	GND
153	GND	169	NCS3/SMCS	185	D4	201	PC16
154	A16/BA0	170	NRD/NOE/CFOE	186	D5	202	PC17
155	A17/BA1	171	NWR0/NWE/CFWE	187	D6	203	PC18
156	A18	172	NWR1/NBS1/CFIOR	188	VDDCORE	204	PC19
157	A19	173	NWR3/NBS3/CFIOW	189	GND	205	PC20
158	A20	174	SDCK	190	D7	206	PC21
159	A21	175	SDCKE	191	D8	207	PC22
160	A22	176	RAS	192	D9	208	PC23

Note: 1. Shaded cells define the pins powered by VDDIOM.

Figure 2. 208-lead PQFP Pinout

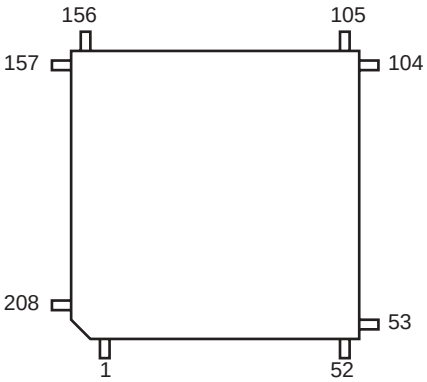


Table 2. AT91RM9200 Pinout for 256-ball BGA Package

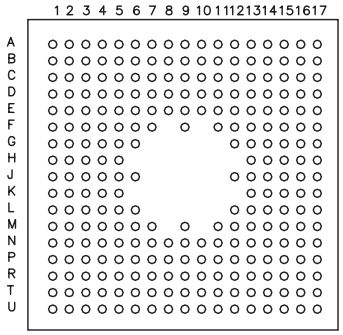
Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	TDI	C3	PD14	E5	TCK	G14	PA1
A2	JTAGSEL	C4	PB22	E6	GND	G15	PA2
A3	PB20	C5	PB19	E7	PB15	G16	PA3
A4	PB17	C6	PD10	E8	GND	G17	XIN32
A5	PD11	C7	PB13	E9	PB7	H1	PD23
A6	PD8	C8	PB12	E10	PB3	H2	PD20
A7	VDDIOP	C9	PB6	E11	PA29	H3	PD22
A8	PB9	C10	PB1	E12	PA26	H4	PD21
A9	PB4	C11	GND	E13	PA25	H5	VDDIOP
A10	PA31/BMS	C12	PA20	E14	PA9	H13	VDDPLLB
A11	VDDIOP	C13	PA18	E15	PA6	H14	VDDIOP
A12	PA23	C14	VDDCORE	E16	PD3	H15	GNDPLLB
A13	PA19	C15	GND	E17	PD0	H16	GND
A14	GND	C16	PA8	F1	PD16	H17	XOUT32
A15	PA14	C17	PD5	F2	GND	J1	PD25
A16	VDDIOP	D1	TST1	F3	PB23	J2	PD27
A17	PA13	D2	VDDIOP	F4	PB25	J3	PD24
B1	TDO	D3	VDDIOP	F5	PB24	J4	PD26
B2	PD13	D4	GND	F6	VDDCORE	J5	PB28
B3	PB18	D5	VDDIOP	F7	PB16	J6	PB29
B4	PB21	D6	PD7	F9	PB11	J12	GND
B5	PD12	D7	PB14	F11	PA30	J13	GNDOSC
B6	PD9	D8	VDDIOP	F12	PA28	J14	VDDOSC
B7	GND	D9	PB8	F13	PA4	J15	VDDPLLA
B8	PB10	D10	PB2	F14	PD2	J16	GNDPLLA
B9	PB5	D11	GND	F15	PD1	J17	XIN
B10	PB0	D12	PA22	F16	PA5	K1	HDPA
B11	VDDIOP	D13	PA21	F17	PLLRCB	K2	DDM
B12	PA24	D14	PA16	G1	PD19	K3	HDMA
B13	PA17	D15	PA10	G2	PD17	K4	VDDIOP
B14	PA15	D16	PD6	G3	GND	K5	DDP
B15	PA11	D17	PD4	G4	PB26	K13	PC5
B16	PA12	E1	NRST	G5	PD18	K14	PC4
B17	PA7	E2	NTRST	G6	PB27	K15	PC6
C1	TMS	E3	GND	G12	PA27	K16	VDDIOM
C2	PD15	E4	TST0	G13	PA0	K17	XOUT

Table 2. AT91RM9200 Pinout for 256-ball BGA Package (Continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
L1	GND	N2	A5	P13	D15	T7	NWR1/NBS1/ CFIOR
L2	HDPB	N3	A9	P14	PC26	T8	SDWE
L3	HDMB	N4	A4	P15	PC27	T9	GND
L4	A6	N5	A14	P16	VDDIOM	T10	VDDCORE
L5	GND	N6	SDA10	P17	GND	T11	D9
L6	VDDIOP	N7	A8	R1	GND	T12	D12
L12	PC10	N8	A21	R2	GND	T13	GND
L13	PC15	N9	NRD/NOE/CFOE	R3	A18	T14	PC19
L14	PC2	N10	RAS	R4	A20	T15	PC21
L15	PC3	N11	D2	R5	PC8	T16	PC23
L16	VDDCORE	N12	GND	R6	VDDIOM	T17	PC25
L17	PLLRCA	N13	PC28	R7	NCS3/SMCS	U1	VDDCORE
M1	VDDIOM	N14	PC31	R8	NWR3/NBS3/ CFIOW	U2	GND
M2	GND	N15	PC30	R9	D0	U3	A16/BA0
M3	A3	N16	PC11	R10	VDDIOM	U4	A19
M4	A1/NBS2/NWR2	N17	PC12	R11	D8	U5	GND
M5	A10	P1	A7	R12	D13	U6	NCS0/BFCS
M6	A2	P2	A13	R13	PC17	U7	SDCK
M7	GND	P3	A12	R14	VDDIOM	U8	CAS
M9	NCS1/SDCS	P4	VDDIOM	R15	PC24	U9	D3
M11	D4	P5	A11	R16	PC29	U10	D6
M12	GND	P6	A22	R17	VDDIOM	U11	D7
M13	PC13	P7	PC9	T1	A15	U12	D11
M14	PC1	P8	NWR0/NWE/CFWE	T2	VDDCORE	U13	D14
M15	PC0	P9	SDCKE	T3	A17/BA1	U14	PC16
M16	GND	P10	D1	T4	PC7	U15	PC18
M17	PC14	P11	D5	T5	VDDIOM	U16	PC20
N1	A0/NBS0	P12	D10	T6	NCS2	U17	PC22

Note: 1. Shaded cells define the pins powered by VDDIOM.

Figure 3. 256-ball LFBGA Pinout



Peripheral Multiplexing on PIO Lines

Table 3. Multiplexing on PIO Controller A and PIO Controller B

PIO Controller A		
I/O Line	**Peripheral A**	**Peripheral B**
PA0	MISO	PCK3
PA1	MOSI	PCK0
PA2	SPCK	IRQ4
PA3	NPCS0	IRQ5
PA4	NPCS1	PCK1
PA5	NPCS2	TXD3
PA6	NPCS3	RXD3
PA7	ETXCK/EREFCK	PCK2
PA8	ETXEN	MCCDB
PA9	ETX0	MCDB0
PA10	ETX1	MCDB1
PA11	ECRS/ECRSDV	MCDB2
PA12	ERX0	MCDB3
PA13	ERX1	TCLK0
PA14	ERXER	TCLK1
PA15	EMDC	TCLK2
PA16	EMDIO	IRQ6
PA17	TXD0	TIOA0
PA18	RXD0	TIOB0
PA19	SCK0	TIOA1
PA20	CTS0	TIOB1
PA21	RTS0	TIOA2
PA22	RXD2	TIOB2
PA23	TXD2	IRQ3
PA24	SCK2	PCK1
PA25	TWD	IRQ2
PA26	TWCK	IRQ1
PA27	MCCK	TCLK3
PA28	MCCDA	TCLK4
PA29	MCDA0	TCLK5
PA30	DRXD	CTS2
PA31	DTXD	RTS2

PIO Controller B		
I/O Line	**Peripheral A**	**Peripheral B**
PB0	TF0	RTS3
PB1	TK0	CTS3
PB2	TD0	SCK3
PB3	RD0	MCDA1
PB4	RK0	MCDA2
PB5	RF0	MCDA3
PB6	TF1	TIOA3
PB7	TK1	TIOB3
PB8	TD1	TIOA4
PB9	RD1	TIOB4
PB10	RK1	TIOA5
PB11	RF1	TIOB5
PB12	TF2	ETX2
PB13	TK2	ETX3
PB14	TD2	ETXER
PB15	RD2	ERX2
PB16	RK2	ERX3
PB17	RF2	ERXDV
PB18	RI1	ECOL
PB19	DTR1	ERXCK
PB20	TXD1	
PB21	RXD1	
PB22	SCK1	
PB23	DCD1	
PB24	CTS1	
PB25	DSR1	EF100
PB26	RTS1	
PB27	PCK0	
PB28	FIQ	
PB29	IRQ0	

Table 4. Multiplexing on PIO Controller C and PIO Controller D

PIO Controller C		
I/O Line	**Peripheral A**	**Peripheral B**
PC0	BFCK	
PC1	BFRDY/SMOE	
PC2	BFAVD	
PC3	BFBAA/SMWE	
PC4	BFOE	
PC5	BFWE	
PC6	NWAIT	
PC7	A23	
PC8	A24	
PC9	A25/CFRNW	
PC10	NCS4/CFCS	
PC11	NCS5/CFCE1	
PC12	NCS6/CFCE2	
PC13	NCS7	
PC14		
PC15		
PC16	D16	
PC17	D17	
PC18	D18	
PC19	D19	
PC20	D20	
PC21	D21	
PC22	D22	
PC23	D23	
PC24	D24	
PC25	D25	
PC26	D26	
PC27	D27	
PC28	D28	
PC29	D29	
PC30	D30	
PC31	D31	

PIO Controller D (256-pin Version Only)		
I/O Line	**Peripheral A**	**Peripheral B**
PD0	ETX0	
PD1	ETX1	
PD2	ETX2	
PD3	ETX3	
PD4	ETXEN	
PD5	ETXER	
PD6	DTXD	
PD7	PCK0	TSYNC
PD8	PCK1	TCLK
PD9	PCK2	TPS0
PD10	PCK3	TPS1
PD11		TPS2
PD12		TPK0
PD13		TPK1
PD14		TPK2
PD15	TD0	TPK3
PD16	TD1	TPK4
PD17	TD2	TPK5
PD18	NPCS1	TPK6
PD19	NPCS2	TPK7
PD20	NPCS3	TPK8
PD21	RTS0	TPK9
PD22	RTS1	TPK10
PD23	RTS2	TPK11
PD24	RTS3	TPK12
PD25	DTR1	TPK13
PD26		TPK14
PD27		TPK15

Pin Description

Table 5. Pin Description List

Pin Name	Function	Type	Active Level	Comments
Power				
VDDIOM	Memory I/O Lines Power Supply	Power		1.65V to 3.6V
VDDIOP	Peripheral I/O Lines Power Supply	Power		1.65V to 3.6V
VDDPLL	Oscillator and PLL Power Supply	Power		1.65V to 1.95V
VDDCORE	Core Chip Power Supply	Power		1.65V to 1.95V
VDDOSC	Oscillator Power Supply	Power		1.65V to 1.95V
GND	Ground	Ground		
GNDPLL	PLL Ground	Ground		
GNDOSC	Oscillator Ground	Ground		
Power Management				
XIN	Main Crystal Input	Input		
XOUT	Main Crystal Output	Output		
XIN32	32KHz Crystal Input	Input		
XOUT32	32KHz Crystal Output	Output		
PLLRCA	PLL A Filter	Input		
PLLRCB	PLL B Filter	Input		
PCK0 - PCK3	Programmable Clock Output	Output		
ICE and JTAG				
TCK	Test Clock	Input		
TDI	Test Data In	Input		
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		
NTRST	Test Reset Signal	Input	Low	
JTAGSEL	JTAG Selection	Input		
ETM				
TSYNC	Trace Synchronization Signal	Output		
TCLK	Trace Clock	Output		
TPS0 - TPS2	Trace ARM Pipeline Status	Output		
TPK0 - TPK15	Trace Packet Port	Output		
Reset/Test				
NRST	Microcontroller Reset	Input	Low	No on-chip pull-up
TST0 - TST1	Test Mode Select	Input		Must be tied low for normal operation
BMS	Boot Mode Select	Input		

Table 5. Pin Description List (Continued)

Pin Name	Function	Type	Active Level	Comments
Debug Unit				
DRXD	Debug Receive Data	Input	DRXD	Debug Receive Data
DTXD	Debug Transmit Data	Output	DTXD	Debug Transmit Data
AIC				
IRQ0 - IRQ6	Interrupt Inputs	Input		
FIQ	Fast Interrupt Input	Input		
PIO				
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset
PB0 - PB29	Parallel IO Controller B	I/O		Pulled-up input at reset
PC0 - PC31	Parallel IO Controller C	I/O		Pulled-up input at reset
PD0 - PD27	Parallel IO Controller D	I/O		Pulled-up input at reset
EBI				
D0 - D15	Data Bus	I/O		Pulled-up input at reset
D16 - D31	Data Bus	I/O		Pulled-up input at reset
A0 - A25	Address Bus	Output		0 at reset
SMC				
NCS0 - NCS7	Chip Select Lines	Output	Low	1 at reset
NWR0 - NWR3	Write Signal	Output	Low	1 at reset
NOE	Output Enable	Output	Low	1 at reset
NRD	Read Signal	Output	Low	1 at reset
NUB	Upper Byte Select	Output	Low	1 at reset
NLB	Lower Byte Select	Output	Low	1 at reset
NWE	Write Enable	Output	Low	1 at reset
NBS0 - NBS3	Byte Mask Signal	Output	Low	1 at reset
EBI for CompactFlash Support				
CFCE1 - CFCE2	CompactFlash Chip Enable	Output	Low	
CFOE	CompactFlash Output Enable	Output	Low	
CFWE	CompactFlash Write Enable	Output	Low	
CFIOR	CompactFlash IO Read	Output	Low	
CFIOW	CompactFlash IO Write	Output	Low	
CFRNW	CompactFlash Read Not Write	Output		
CFCS	CompactFlash Chip Select	Output	Low	
EBI for SmartMedia Support				
SMCS	SmartMedia Chip Select	Output	Low	
SMOE	SmartMedia Output Enable	Output	Low	

Table 5. Pin Description List (Continued)

Pin Name	Function	Type	Active Level	Comments
SMWE	SmartMedia Write Enable	Output	Low	
SDRAM Controller				
SDCK	SDRAM Clock	Output		
SDCKE	SDRAM Clock Enable	Output	High	
SDCS	SDRAM Controller Chip Select	Output	Low	
BA0 - BA1	Bank Select	Output		
SDWE	SDRAM Write Enable	Output	Low	
RAS - CAS	Row and Column Signal	Output	Low	
SDA10	SDRAM Address 10 Line	Output		
Burst Flash Controller				
BFCK	Burst Flash Clock	Output		
BFCS	Burst Flash Chip Select	Output	Low	
BFAVD	Burst Flash Address Valid	Output	Low	
BFBAA	Burst Flash Address Advance	Output	Low	
BFOE	Burst Flash Output Enable	Output	Low	
BFRDY	Burst Flash Ready	Input	High	
BFWE	Burst Flash Write Enable	Output	Low	
Multimedia Card Interface				
MCCK	Multimedia Card Clock	Output		
MCCDA	Multimedia Card A Command	I/O		
MCDA0 - MCDA3	Multimedia Card A Data	I/O		
MCCDB	Multimedia Card B Command	I/O		
MCDB0 - MCDB3	Multimedia Card B Data	I/O		
USART				
SCK0 - SCK3	Serial Clock	I/O		
TXD0 - TXD3	Transmit Data	Output		
RXD0 - RXD3	Receive Data	Input		
RTS0 - RTS3	Ready To Send	Output		
CTS0 - CTS3	Clear To Send	Input		
DSR1	Data Set Ready	Input		
DTR1	Data Terminal Ready	Output		
DCD1	Data Carrier Detect	Input		
RI1	Ring Indicator	Input		

Table 5. Pin Description List (Continued)

Pin Name	Function	Type	Active Level	Comments
USB Device Port				
DDM	USB Device Port Data -	Analog		
DDP	USB Device Port Data +	Analog		
USB Host Port				
HDMA	USB Host Port A Data -	Analog		
HDPA	USB Host Port A Data +	Analog		
HDMB	USB Host Port B Data -	Analog		
HDPB	USB Host Port B Data +	Analog		
Ethernet MAC				
EREFCK	Reference Clock	Input		RMII only
ETXCK	Transmit Clock	Input		MII only
ERXCK	Receive Clock	Input		MII only
ETXEN	Transmit Enable	Output		
ETX0 - ETX3	Transmit Data	Output		ETX0 - ETX1 only in RMII
ETXER	Transmit Coding Error	Output		MII only
ERXDV	Receive Data Valid	Input		MII only
ECRSDV	Carrier Sense and Data Valid	Input		RMII only
ERX0 - ERX3	Receive Data	Input		ERX0 - ERX1 only in RMII
ERXER	Receive Error	Input		
ECRS	Carrier Sense	Input		MII only
ECOL	Collision Detected	Input		MII only
EMDC	Management Data Clock	Output		
EMDIO	Management Data Input/Output	I/O		
EF100	Force 100 Mbits/sec.	Output	High	RMII only
Synchronous Serial Controller				
TD0 - TD2	Transmit Data	Output		
RD0 - RD2	Receive Data	Input		
TK0 - TK2	Transmit Clock	I/O		
RK0 - RK2	Receive Clock	I/O		
TF0 - TF2	Transmit Frame Sync	I/O		
RF0 - RF2	Receive Frame Sync	I/O		
Timer/Counter				
TCLK0 - TCLK5	External Clock Input	Input		
TIOA0 - TIOA5	I/O Line A	I/O		
TIOB0 - TIOB5	I/O Line B	I/O		

Table 5. Pin Description List (Continued)

Pin Name	Function	Type	Active Level	Comments
SPI				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
SPCK	SPI Serial Clock	I/O		
NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
NPCS1 - NPCS3	SPI Peripheral Chip Select	Output	Low	
Two-wire Interface				
TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		

Product Overview

Power Supply

The AT91RM9200 has five types of power supply pins:

- VDDCORE pins. They power the core, including processor, memories and peripherals; voltage is between 1.65V and 1.95V, 1.8V nominal.
- VDDIOM pins. They power the External Bus Interface I/O lines; voltage is between 1.65V and 3.6V, 1.8V, 3V or 3.3V nominal.
- VDDIOP pins. They power the Peripherals I/O lines and the USB transceivers; voltage is between 1.65V and 3.6V, 1.8V, 3V or 3.3V nominal.(1)
- VDDPLL pins. They power the PLL cells; voltage is between 1.65V and 1.95V, 1.8V nominal.
- VDDOSC pin. They power both oscillators; voltage is between 1.65V and 1.95V, 1.8V nominal.

Note: 1. Powering VDDIOP with a voltage lower than 3V prevents any use of the USB Host and Device Ports. This also affects the operation of the Trace Port.

Ground pins are common to all power supplies, except VDDPLL and VDDOSC pins. For these pins, GNDPLL and GNDOSC are provided, respectively.

Input/Output Considerations.

After reset, in general-purpose I/O mode, all the PIO lines are enabled except PC7 to PC13. These are memory control signals and must be driven by the EBI at reset.

All pins capable of operating as inputs or outputs, such as the data bus lines and the PIO lines (multiplexed or non-multiplexed), integrate a programmable pull-up resistor of about 100 kΩ. As soon as the reset line NRST is asserted, all pull-up resistors are enabled. By doing so, the AT91RM9200 ensures that the tri-state inputs are held in a valid logic level and, in turn, assures that no oscillation propagates inside the device, thus preventing any unnecessary power consumption.

When the reset line is de-asserted, the pull-up resistors of the data bus lines D0 to D15 are controlled by programming the external bus interface. The pull-up resistors of the I/O lines (including D16 to D31) are individually disabled by programming the PIO controller.

Reset

Reset restores the default states of the user interface registers (defined in the user interface of each peripheral), and forces the ARM920T to perform the next instruction fetch from address zero. Except for the program counter and the Current Program Status Register, the ARM920T registers do not have defined reset states. Reset state also deactivates all internal clocks to prevent any power consumption.

Debug Features

Embedded In-Circuit Emulator

ARM standard embedded in-circuit emulation is supported via the JTAG/ICE port. It is connected to a host computer via an ICE interface. Embedded ICE mode is selected when JTAGSEL is low. It is not possible to switch directly between ICE and JTAG operations. A chip reset must be performed (NRST and NTRST) after JTAGSEL is changed. The test reset input to the Embedded ICE (NTRST) is provided separately to facilitate debug of boot programs.

Debug Unit

The Debug Unit is a system peripheral dedicated to debugging and provides:

- A simple serial port for application trace outputs.
- Interrupt handling of the Debug Communication Channel signals of the ICE.
- A Chip I.D. Register

Embedded Trace Macrocell

The AT91RM9200 features an Embedded Trace Macrocell (ETM), which is closely connected to the ARM9TDMI Processor. The Embedded Trace is a mid-level implementation of the ARM ETM9 module and contains:

- Four pairs of address comparators
- Two data comparators
- Eight memory map decoder inputs
- Two counters
- One sequencer
- Four external inputs
- One external output
- One 18-byte FIFO

The Trace Packet width, equal to 4, 8 or 16, is selected by software as the packet data bus is 16 bits wide.

The Embedded Trace Macrocell of the AT91RM9200 works in half-rate clock mode and thus integrates a clock divider. This allows the maximum frequency of all the trace port signals not to exceed one half of the ARM920T clock speed.

The eight memory map decoder inputs are connected to custom address decoders that provide triggers to the Embedded Trace upon access to the memory areas as defined by the Memory Controller.

IEEE 1149.1 JTAG Boundary Scan

IEEE 1149.1 JTAG boundary scan is enabled when JTAGSEL is high. The functions SAMPLE, EXTEST and BYPASS are implemented. In ICE debug mode, the ARM processor responds with a non-JTAG chip ID that identifies the processor to the ICE system. This is not IEEE 1149.1 JTAG-compliant.

It is not possible to switch directly between JTAG and ICE operations. A chip reset must be performed (NRST and NTRST) after JTAGSEL is changed.

Clock and Power Saving Features

The AT91RM9200 is clocked by several programmable clock signals provided by the Power Management Controller.

The following clock signals are present in the AT91RM9200:

- SLCK. The slow clock with a typical frequency of 32768 Hz, supplied to the System Timer, the Real Time Clock and the Power Management Controller; is the only permanent clock signal in the AT91RM9200.
- PCK. The processor clock with programmable frequency feeds the ARM920T and can be programmed between 512 Hz and 180 MHz.
- MCK. The master clock is a 1-to-4 programmable division of the processor clock and feeds the internal buses and all the peripherals. The acceptable programming range is from 512 Hz to 60 MHz.
- UDPCK and UHPCK. The USB Device and Host Port clocks with a typical frequency of 48 MHz.
- PCK0 - PCK3. These are programmable output clock signals.

The AT91RM9200 also features the Idle Mode and the peripheral clock control, allowing the user to optimize power consumption of the system depending on the application requirements.

ARM920T Functional Overview

ARM920T Features

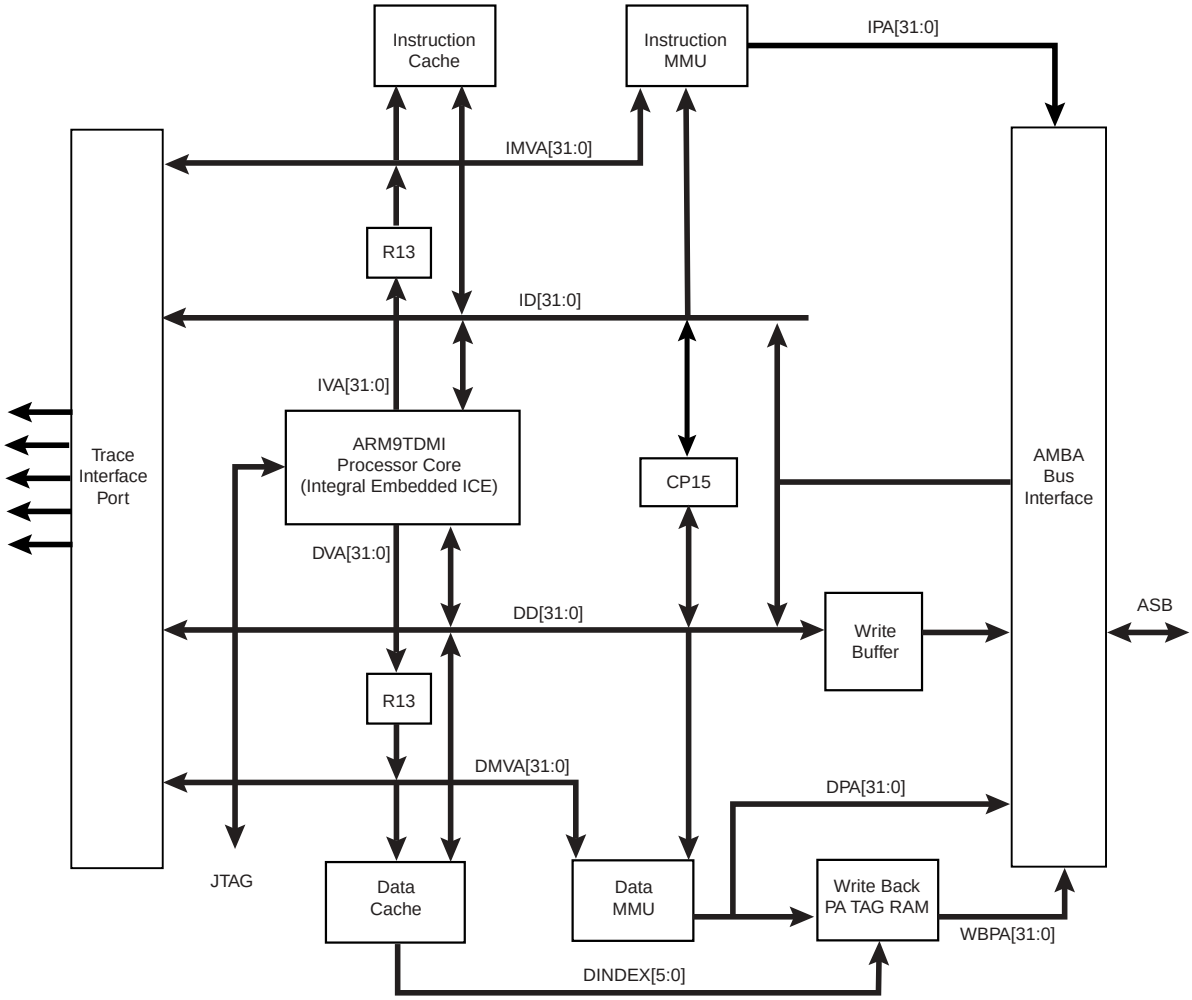
The ARM9TDMI™ processor is a high-performance 32-bit RISC processor described in the *ARM9TDMI Technical Reference Manual* from ARM. Descriptions of the other blocks shown in Figure 4 may be found in the *ARM920T Technical Reference Manual*.

The ARM920T is a member of the ARM9TDMI™ line of general-purpose microprocessors. It comprises an ARM9TDMI processor plus instruction and data cache memory and MMU. See Figure 4.

The ARM9TDMI processor is a Harvard architecture device implemented using a five-stage pipeline consisting of Fetch, Decode, Execute, Memory and Write stages. It supports both the 32-bit ARM®and 16-bit Thumb® instruction sets, allowing the trade-off between high performance and code density.

The ARM920T cache architecture processor is targeted at multi-programmer applications where full memory management, high performance and low power are vitally important. The separate instruction and data caches in this design are each 16K bytes with an 8-word line length. The ARM920T implements two enhanced Memory Management Units (MMU) to provide translation and access permission checks for instruction and data addresses.

Figure 4. Functional Block Diagram of the ARM920T



Multi-master Memory Controller

The AT91RM9200 features a multi-master memory controller that handles the internal bus.

It is made up of:

- A bus arbiter that arbitrates the accesses of the four masters, the ARM920T, the Peripheral Data Controller, the USB Host Port and the Ethernet MAC. Bus master priorities are fully prorgammable.
- An address decoder that splits the 4G bytes of address space into areas to access the SRAM, the ROM and the external memories through the External Bus Interface and the embedded peripherals.
- An Abort Status that enables tracking of the source and the cause of the errors during access to the Memory Controller.
- A Misalignment Detector that detects when a master provides an address that is not consistent with the kind of access required.

The multi-master memory controller handles only little-endian mode accesses. All masters, including the ARM920T, must work in little-endian mode only.

Internal Memories

Internal SRAM

The AT91RM9200 integrates a high-speed, 16-Kbyte internal SRAM. After reset and until the Remap Command is performed, the SRAM is only accessible at address 0x20 0000. After Remap, the SRAM also is available at address 0x0.

Internal ROM

The AT91RM9200 integrates a 128-Kbyte Internal ROM. At any time, the ROM is mapped at address 0x10 0000. It is also accessible at address 0x0 after reset and before the Remap Command if the BMS is tied high during reset.

USB Host Port

The AT91RM9200 integrates a USB Host Port Open Host Controller Interface. The registers of this interface are directly accessible on the ASB Bus and are mapped like a standard internal memory at address 0x30 0000.

External Bus Interface

The External Bus Interface implements the data transfers between several external devices and the embedded memory controllers of an ARM-based microcontroller.

The External Bus Interface contains three external memory controllers, the Static Memory Controller, the SDRAM Controller and the Burst Flash Controller, and is capable of handling several types of external memories and peripheral devices, such as static SRAM, PROM, EPROM, EEPROM, Flash, SDRAM and burst Flash.

The External Bus Interface also supports the CompactFlash, SmartMedia and NAND Flash protocols thanks to integrated programmable circuitry that reduces the requirements for external components to a minimum.

The External Bus Interface handles data transfers with up to eight external devices, each assigned to eight address spaces defined by the embedded memory controller. Data transfers are performed through a 16- or 32-bit data bus, an address bus of up to 26 bits, up to eight chip select lines (NCS0 to NCS7) and several control pins that are generally multiplexed between the different external memory controllers.

Static Memory Controller

The Static Memory Controller (SMC) controls a 16-bit data bus, a 26-bit address bus and the signals that control accesses to external static devices, including up to eight chip select lines.

The Chip Select Register of each of the eight chip select areas configures the behavior of the SMC. It supports byte, half-word and word-aligned accesses. For all chip selects, the user can program:

- Data bus width to 8 bits or 16 bits
- Up to 128 wait states
- Up to 15 data float times (wait time after a read access is finished to prevent any bus contention in case the device is too slow in releasing the bus or latches the data longer after the chip select rising edge)
- With a 16-bit wide data bus, the user can program the SMC to control one 16-bit device (Byte Access Select Type) or two 8-bit devices in parallel that emulate a 16-bit memory (Byte Write Access Type).
- The read and write signal address setup and hold times at up to seven cycles
- An optional address setup and hold time on the Chip Select
- The early read protocol, which allows assertion of the read signal at the beginning of the access and thus facilitates running at 0 wait state with external devices.

SDRAM Controller

The SDRAM controller supports the interface to external 16-bit or 32-bit SDRAM devices. It can address up to 256M bytes. The supported page size ranges from 2048 to 8192 bytes and the number of columns from 256 to 2048. It supports byte, half-word and word accesses.

The SDRAM controller supports a read or write burst. It keeps track of the active row in each bank, thus maximizing SDRAM performance, e.g., the application software may be placed in one bank and data in the other banks.

Additional features include multibank ping-pong access, support of self-refresh and low-power modes, automatic refresh operations with programmable refresh rates and automatic page break when a memory boundary has been reached.

Burst Flash Controller

The Burst Flash Controller provides an interface for external 16-bit burst Flash devices and handles an address space of 256M bytes. It supports byte-, half-word and word-aligned accesses. The BFC also supports data bus and address bus multiplexing.

The Burst Flash Interface supports asynchronous and burst operating modes.

Two protocols are available in Burst Mode, the clock-controlled address advance protocol and the signal-controlled address advance protocol. The clock-controlled address advance protocol automatically increments the address at each clock cycle; in signal-controlled address advance protocol the address is incremented only when the BFBAA signal is active. Address and data bus multiplexing is possible.

The BFC clock speed is programmable to be either Master Clock or Master Clock divided by 2 or 4. Page size handling (16 bytes to 1024 bytes) is supported for burst Flash devices unable to handle continuous burst read.

The Burst Flash Controller can also be programmed to suspend and maintain the current burst. In this mode, the BFC can restart a sequential access without any additional latency.

Boot Program

The AT91RM9200 integrates a ROMed program which operates a bootloader and a boot uploader. The bootloader is started first and searches a sequence of eight valid ARM vectors (either B-Branch or LDR-Load Register) in an external 8-bit device connected on the NCS0, a DataFlash connected on the SPI or an EEPROM connected on the TWI. If any sequence is detected, up to 12K bytes are downloaded into the internal SRAM. This is followed by a jump to the first address of the SRAM.

If no valid ARM vector sequence is found, the boot uploader is started. It initializes the Debug Unit serial port and the USB device port. It then waits for any transaction and downloads through a DFU (Device Firmware Upgrade) protocol a piece of code into the internal SRAM before branching to the first address of the SRAM.

Embedded Software Services

The ROM of the AT91RM9200 embeds code which may be re-used by the programmers. The Boot Program already uses some of these Embedded Software Services, but some others simply target performance optimization as the code is running out of the internal ROM, which is single master clock cycle accessible.

The Embedded Software Services are organized so that the programmers can re-use completely or partially the functions making up a service.

The following Embedded Software Services are embedded in the AT91RM9200:

- DataFlash Service
- XModem Service
- USB Device Enumeration, Communication and DFU Service
- CRC 16/32 Calculation Table
- Sine Wave

Peripherals

The AT91RM9200 integrates a number of peripherals that are classified as either system or user peripherals.

Most of the embedded peripherals are 32-bit accessible by the peripheral Bridge and are programmed with a minimum number of instructions. The peripheral register set is composed of control, mode, data, status and enable/disable/status registers.

An on-chip Peripheral Data Controller (PDC) transfers data between the embedded peripherals and on- and off-chip memory address space without processor intervention.

Peripheral Identifier

Each embedded user peripheral and PIO controller has an identifier between 2 and 31 that corresponds to its interrupt source number and its peripheral clock control number. Identifier 0 is reserved for the FIQ and Identifier 1 is used for one single interrupt source that is the logical OR of all the system peripheral interrupts. Table 6 on page 23 details the peripheral identifiers.

Table 6. Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	MMMC	Multi-master Memory Controller	
	PMC	Power Management Controller	
	ST	System Timer	
	RTC	Real-time Clock	
	DBGU	Debug Unit	
2	PIOA	Parallel I/O Controller A	
3	PIOB	Parallel I/O Controller B	
4	PIOC	Parallel I/O Controller C	
5	PIOD	Parallel I/O Controller D	
6	US0	USART 0	
7	US1	USART 1	
8	US2	USART 2	
9	US3	USART 3	
10	MCI	Multimedia Card Interface	
11	UDP	USB Device Port	
12	TWI	Two-wire Interface	
13	SPI	Serial Peripheral Interface	
14	SSC0	Synchronous Serial Controller 0	
15	SSC1	Synchronous Serial Controller 1	
16	SSC2	Synchronous Serial Controller 2	
17	TC0	Timer/Counter 0	
18	TC1	Timer/Counter 1	
19	TC2	Timer/Counter 2	
20	TC3	Timer/Counter 3	
21	TC4	Timer/Counter 4	
22	TC5	Timer/Counter 5	
23	UHP	USB Host Port	
24	EMAC	Ethernet MAC	
25	AIC	Advanced Interrupt Controller	IRQ0
26	AIC	Advanced Interrupt Controller	IRQ1
27	AIC	Advanced Interrupt Controller	IRQ2
28	AIC	Advanced Interrupt Controller	IRQ3
29	AIC	Advanced Interrupt Controller	IRQ4
30	AIC	Advanced Interrupt Controller	IRQ5
31	AIC	Advanced Interrupt Controller	IRQ6

Peripheral User Interface

Peripheral Access

Most of the peripherals embedded in the AT91RM9200 are connected to the 32-bit wide Advanced Peripheral Bus (APB) only. Peripheral registers are only word accessible. Byte and half-word accesses are not supported. If a byte or a half-word access is attempted, the memory controller automatically masks the lowest address bits and generates a word access.

Each user peripheral is allocated a 16-Kbyte address space.

The system peripherals are all mapped in the highest 4K bytes of address space, between addresses 0xFFFF F000 and 0xFFFF FFFF. Each peripheral has an address space of 256 or 512 bytes, representing 64 or 128 registers.

The USB Host Port peripheral is mapped in the internal memory mapping at address 0x30 0000. Its user interface is compliant with the OHCI standard and thus does not respect the rules defined for the other peripherals.

Peripheral Registers

The following register definitions are common to all peripherals, except the USB Host and Device Ports and the Ethernet MAC:

- Control Register: Write-only register that triggers a command when a one is written to the corresponding position at the appropriate address. Writing a zero has no effect.
- Mode Register: Read/write register that defines the configuration of the peripheral. Usually has a value of 0x0 after a reset.
- Data Registers: Read and/or write register that enables the exchange of data between the processor and the peripheral.
- Status Register: Read-only register that returns the status of the peripheral.
- Enable/Disable/Status Registers are shadow command registers. Writing a one in the Enable Register sets the corresponding bit in the Status Register. Writing a one in the Disable Register resets the corresponding bit and the result can be read in the Status Register. Writing a bit to zero has no effect. This register access method maximizes the efficiency of bit manipulation and enables modification of a register with a single non-interruptible instruction, replacing the costly read-modify-write operation.

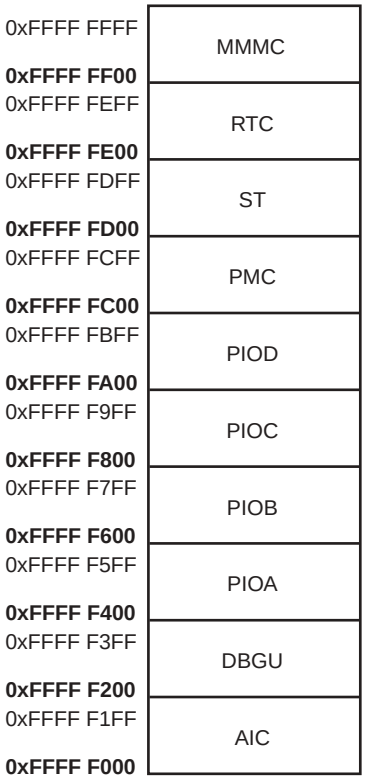
Peripheral Interrupt Control

The Interrupt Control of most of the embedded peripherals originates from the status register using the interrupt mask. The status register bits are ANDed to their corresponding interrupt mask bits and the result is then ORed to generate the Interrupt Source signal to the Advanced Interrupt Controller.

The interrupt mask is read in the Interrupt Mask Register and is modified with the Interrupt Enable Register and the Interrupt Disable Register. The enable/disable/mask makes it possible to enable or disable peripheral interrupt sources with a non-interruptible single instruction. This eliminates the need for interrupt masking at the AIC or processor level in real-time and multi-tasking systems.

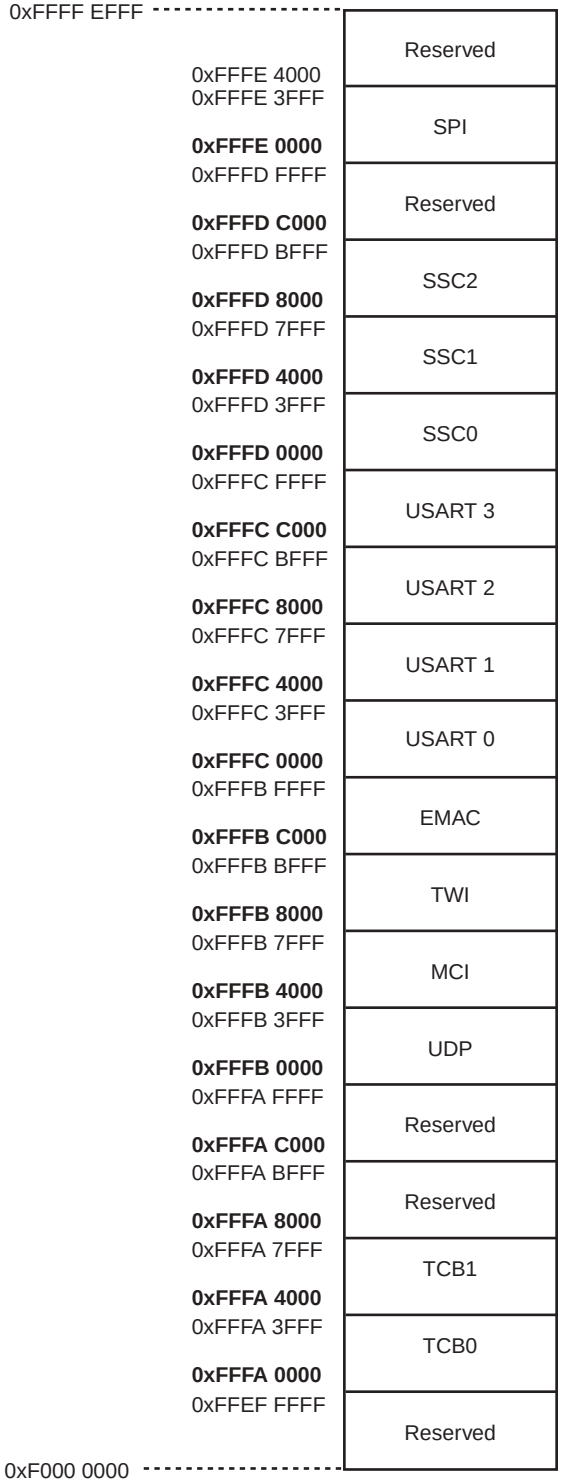
Peripheral Mapping

System Peripheral Mapping



Peripheral Name	Size
Multi-master Memory Controller	256 bytes/64 words
Real-time Clock	256 bytes/64 words
System Timer	256 bytes/64 words
Power Management Controller	256 bytes/64 words
Parallel I/O Controller D	512 bytes/128 words
Parallel I/O Controller C	512 bytes/128 words
Parallel I/O Controller B	512 bytes/128 words
Parallel I/O Controller A	512 bytes/128 words
Debug Unit	512 bytes/128 words
Advanced Interrupt Controller	512 bytes/128 words

User Peripheral Mapping



Peripheral Name	Size
Serial Peripheral Interface	16K Bytes
Serial Synchronous Controller 2	16K Bytes
Serial Synchronous Controller 1	16K Bytes
Serial Synchronous Controller 0	16K Bytes
Universal Synchronous/Asynchronous Receiver/Transmitter 3	16K Bytes
Universal Synchronous/Asynchronous Receiver/Transmitter 2	16K Bytes
Universal Synchronous/Asynchronous Receiver/Transmitter 1	16K Bytes
Universal Synchronous/Asynchronous Receiver/Transmitter 0	16K Bytes
Ethernet MAC	16K Bytes
Two-wire Interface	16K Bytes
Multimedia Card Interface	16K Bytes
USB Device Port	16K Bytes
Timer/Counter Block 1	16K Bytes
Timer/Counter Block 0	16K Bytes

Peripheral Data Controller (DMA)

The AT91RM9200 features a Peripheral Data Controller integrating 20 channels that are dedicated to the following peripherals:

- Debug Unit
- Four USARTs
- Serial Peripheral Interface
- Three Serial Synchronous Controllers
- Multimedia Card Interface

One PDC channel is connected to the receiver and one to the transmitter of each AT91RM9200 peripheral requiring a high data throughput.

The user interfaces (programming registers and status and control bits) of all the PDC channels are integrated into the user interface of the peripheral to which they are assigned.

The current pointer and counter registers typically write the address and the size of the buffer and, when read, show the next transfer address and the remaining transfer number. When a transfer is performed, the address is incremented and the counter decrements.

The next transfer pointer and counter registers permit frames to be chained easily, thus preventing requirement for fast interrupt latency while handling transfers of consecutive data frames. When the current counter reaches 0 and the next counter is not null, the next counter and pointer are loaded in the current registers, thus allowing an uninterrupted transfer rate.

System Peripherals

Power Management Controller

The AT91RM9200 features the Power Management Controller (PMC), which implements the Idle Mode (ARM920T processor clock stopped until the next interrupt) and enables the user to optimize the power consumption of the system to the application requirements (independent peripheral clock control). It also controls the activity and permits programming parameters of the Clock Generator elements, the main oscillator and the PLLs.

It furnishes the Slow Clock (SLCK), the Processor Clock (PCK), the Master Clock (MCK), the USB Clocks (UDPCK and UHPCK) and the Programmable Clock Outputs (PCK0 to PCK3).

System Timer

The AT91RM9200 features a System Timer, which integrates three different free-running timers:

- A Period Interval Timer that sets the base time for an operating system
- A Watchdog Timer that is built around a 16-bit counter and is used to prevent system lock-up if the software becomes trapped in a deadlock. It can generate an internal reset or an interrupt.
- A Real-time Timer that counts elapsed seconds

These timers count using the Slow Clock provided by the Power Management Controller. Typically, this clock has a frequency of 32768 Hz.

Real-time Clock

The AT91RM9200 features a Real-time Clock (RTC) peripheral. It combines a complete time-of-day clock with alarm and a two hundred-year Gregorian calendar, complemented by a programmable periodic interrupt.

The time and calendar values are coded in binary-coded decimal (BCD) format. The time format can be 24-hour mode or 12-hour mode with an AM/PM indicator.

Updating time and calendar fields and configuring the alarm fields is performed with an entry control to avoid loading registers with incompatible BCD-format data or with an incompatible date according to the current month/year/century.

Advanced Interrupt Controller

The AT91RM9200 has an eight-level priority, individually maskable, vectored interrupt controller. This feature substantially reduces the software and real-time overhead in handling internal and external interrupts.

The interrupt controller is connected to the NFIQ (fast interrupt request) and the NIRQ (standard interrupt request) inputs of the ARM920T processor. The NIRQ line can be asserted by the interrupts generated by the on-chip peripherals and the external interrupt request lines: IRQ0 to IRQ6. The processor's NFIQ line can normally be asserted only by the external fast interrupt request input (FIQ).

Internal sources are programmed to be level sensitive or edge triggered. External sources can be programmed to be positive- or negative-edge triggered or high- or low-level sensitive.

Parallel I/O Controller

The AT91RM9200 features four Parallel I/O Controllers, PIOA, PIOB, PIOC and PIOD, each of which controls up to 32 I/O lines. Each I/O line can be assigned to up to two embedded peripherals as defined in Table 3 on page 8 and Table 4 on page 9, or can be used as general-purpose input or output.

For each individual pin the user may:

- read the level
- enable an input change interrupt
- configure the pin in open-drain (driven low only)
- enable a pull-up resistor of about 100 kΩ

When pins are defined as general-purpose output pins, the user can define a mask that allows the levels of several pins of the same port to be changed (set or cleared) in one write instruction.

Debug Unit

The Debug Unit provides a serial interface compatible with the USART, but bonding out only the RXD and TXD pins. These pins are named DRXD and DTXD. A Baud Rate Generator permits the selection of the communication speed and serial asynchronous full duplex data flow. CPU overhead requirements are reduced by the addition of two PDC channels.

The Debug Unit also allows the interrupt handling of the COMMTX and COMMRX signals that come from the ARM920T's ICE Breaker and that trace the activity of the Debug Communication Channel.

Moreover, the Debug Unit integrates two Chip ID registers that contain a unique number for each device of the family. This feature allows identification of the architecture of the device and thus the set of embedded peripherals, the size of the internal memories and the silicon revision, allowing the evolution of the products to be traced.

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User Peripherals

USB Host Port

The AT91RM9200 USB Open Host Controller Interface (Open HCI) provides full-speed serial communication ports at a baud rate of 12 Mbits/s. Up to 127 USB devices (printer, camera, mouse, keyboard, etc.) and USB hubs can be connected to the USB host in the USB “tiered start” topology.

This includes the following features:

- Compliance with USB 2.0 specification
- Compliance with Open HCI Rev 1.0 specification
- Supports both low-speed (1.5 Mbps) and full-speed (12 Mbps) USB device connections
- Root HUB integrated with two downstream USB ports
- Transceiver buffers integrated, over current protection on ports
- Supports power management
- Operates as a master on the ASB bus

The Open HCI host controller initializes master DMA transfer with the ASB bus:

- Fetches endpoint descriptors and transfer descriptors
- Access to endpoint data from system memory
- Access to the HC communication area
- Write status and retire Transfer Descriptor

Ethernet MAC

The Ethernet MAC is the hardware implementation of the MAC sub-layer OSI reference model between the physical layer (PHY) and the logical link layer (LLC). It controls the data exchange between a host and a PHY layer according to Ethernet IEEE 802.3u data frame format. The EMAC contains the required logic and transmit and receive FIFOs for DMA management.

In addition, it is interfaced through MDIO/MDC pins for PHY layer management. The EMAC can transfer data in media-independent interface (MII) or reduced media-independent interface (RMII) modes depending on the pinout configuration.

The EMAC features:

- 10 and 100 Mbits per second data throughput capability
- Full- and half-duplex operation
- MII or RMII interface to the physical layer
- Register interface to Address, Status and Control Registers
- 28-byte transmit and 28-byte receive FIFOs
- Automatic pad and CRC generation on transmitted frames
- Address checking logic to recognize four 48-bit addresses
- Supports promiscuous mode where all valid frames are copied to memory
- Supports physical layer management through MDIO interface control of alarm and update time/calendar data in
- Supports VLAN Protocol IEEE Standard 802.1Q

USB Device Port

The AT91RM9200’s USB Device Port provides a full-speed serial communication port at a baud rate of 12 Mbits/s. It can be connected to a USB host or a USB hub in the USB “tiered start” topology.

It includes the following features:

- USB 2.0 compliant. Can operate at a baud rate of 12 Mbits/s.
- On-chip USB bus transceiver on pins DDM and DDP
- One dual-port SRAM of 2048 bytes accessible in byte mode only as an internal memory
- Programmable endpoint types with support for six control, interrupt, bulk or isochronous endpoints
- Independent interrupt for each endpoint, start-of-frame, reset, suspend and resume events
- Ping-pong transaction supported

Each endpoint can support all types of transfers. A type is suggested according to the fixed size of the DPR allocated to this endpoint:

- Endpoint 0: 8 bytes (suggested type: control transfers)
- Endpoint 1: 64 bytes (supports ping-pong, suggested type: bulk transfers)
- Endpoint 2: 64 bytes (supports ping-pong, suggested type: bulk transfers)
- Endpoint 3: 8 bytes (suggested type: interrupt transfers)
- Endpoint 4: 256 bytes (supports ping-pong, suggested type: isochronous transfers)
- Endpoint 5: 256 bytes (supports ping-pong, suggested type: isochronous transfers)

The external pins dedicated to this interface are DDM and DDP. The USB protocol uses differential signaling between the two pins for half-duplex data transmission. A 1.5 KΩ pull-up resistor is required to be connected to the USB cable's D+ signal to pull the DDP pin high when not driven.

Multimedia Card Interface

The Multimedia Card Interface supports the MultiMediaCard (MMC) Specification v2.2 and the SD Memory Card Specification v1.0.

It can operate at up to Master Clock divided by 2 and supports interfacing up to 16 slots. Each slot may be used to interface with a MultiMediaCard Bus (up to 30 Cards) or with an SD Memory Card. Only one slot can be selected at a time (slots are multiplexed).

The MCI provides a command register, response registers, data registers, time-out counters and error detection logic which automatically handle the transmission of commands and the reception of the associated responses and data with a limited processor overhead. It supports stream, block and multi-block data read and write. It is linked to the PDC making CPU intervention unnecessary for large buffer transfers.

As an energy-saving feature, the MCI is equipped with embedded power management to slow down the clock rate when not being used.

Synchronous Serial Controller

The Synchronous Serial Controller supports many serial synchronous communication protocols generally used in the audio and telecom applications such as I²S, Short Frame Sync, Long Frame Sync, etc.

The SSC contains an independent receiver and transmitter and a common clock divider. The receiver and the transmitter each interface with three signals: the TD/RD signal for the data, the TK/RK signal for the clock and the TF/RF signal for the Frame Sync. Transfers contain up to 16 data of up to 32 bits. They can be programmed to start automatically or on different events detected on the Frame Sync signal.

The SSC's high-level of programmability and its two dedicated PDC channels provide a continuous high bit rate data transfer with minimum processor intervention.

The SSC permits interfacing with low processor overhead to any of the following:

- CODECs in master or slave modes
- DACs through a dedicated serial interface, particularly the I2S
- Magnetic card readers
- Time division multiplexed buses
- Printer and scanner head interfaces

Universal Synchronous/ Asynchronous Receiver/ Transmitter

The AT91RM9200 provides two identical, full-duplex, universal synchronous/asynchronous receiver/transmitters that interface to the APB and are connected to the Peripheral Data Controller.

The main features are:

- Programmable baud rate generator with external or internal clock, as well as slow clock
- Parity, framing and overrun error detection
- Line break generation and detection
- Automatic echo, local loop back and remote loop back channel modes
- Multi-drop mode: address detection and generation
- Two dedicated peripheral data controller channels
- 5-bit, 6-bit, 7-bit, 8-bit and 9-bit character length generation, delay timing and pulse-width modulation.

All USARTs support ISO7816 Smart Card T0 or T1 protocols and manage two signals, RTS and CTS, allowing a hardware handshake.

All USARTs also feature an operating mode supporting the modulation and demodulation IrDA in SIR (Slow Infrared) at up to 115200 baud.

The USART 1 has a complete set of modem signals (RTS/CTS/DSR/DTR/DCD/RI). Outputs can be controlled directly from the USART User Interface and inputs can generate an USART interrupt when changing state.

Serial Peripheral Interface

The AT91RM9200 includes an SPI that provides communication with external devices in master or slave mode. The SPI has four external independently-programmable peripheral chip select lines that can be connected to up to four devices or 15 devices via a decoder. The data length is programmable from 8- to 16-bits, MSB or LSB first, with programmable polarity and phase, and can operate to access at full speed only one peripheral or to communicate through the same buffer with many peripherals. Speed and bit stream delays are fully configurable and independently-definable for each chip select.

The two PDC channels connected to the SPI allow a fast and low CPU overhead communication with serial peripherals.

Two-wire Interface

The Two-wire Interface (TWI) interconnects components on a unique two-wire bus made up of one clock line and one data line with speeds of up to 400 Kbits/s based on a byte-oriented transfer format. It can be used with any Atmel two-wire bus serial EEPROM. The TWI is programmable as a master or a slave with sequential or single-byte access. Multi-master capability is supported. Arbitration of the bus is performed internally and turns the TWI into slave mode automatically if the bus arbitration is lost.

A configurable baud rate generator permits adaptation of the output data rate to a wide range of clock frequencies.

Timer/Counter

The AT91RM9200 features two Timer/Counter blocks, each containing three identical 16-bit Timer/Counter channels. Each channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse-width modulation.

Each Timer/Counter channel has three external clock inputs (TCLK), five internal clock inputs, and two multi-purpose input/output signals (TIOA/TIOB) that can be configured by the user. Each channel drives an internal interrupt signal that can be programmed to generate processor interrupts via the Advanced Interrupt Controller (AIC).

The Timer/Counter block has two global registers that act upon all three TC channels. The Block Control Register allows the three channels to be started simultaneously with the same instruction. The Block Mode Register defines the external clock inputs for each Timer/Counter channel, allowing them to be chained.

Each Timer/Counter block operates independently and has a complete set of block and channel registers.

In waveform mode, each Timer/Counter supports double wave generation or single waveform generation on TIOA with trigger on input TIOB. Up and down counting are both supported and three compare registers are available. Outputs can be configured to be set, cleared or toggled on trigger or compare events. Interrupts can be generated for any event.

In capture mode, two load registers and one compare register are available. Triggers and input event detection are largely programmable, and load events can generate interrupts, stop the operation or disable the channel clock.

Package Drawings

Figure 5. PQFP Package Drawing

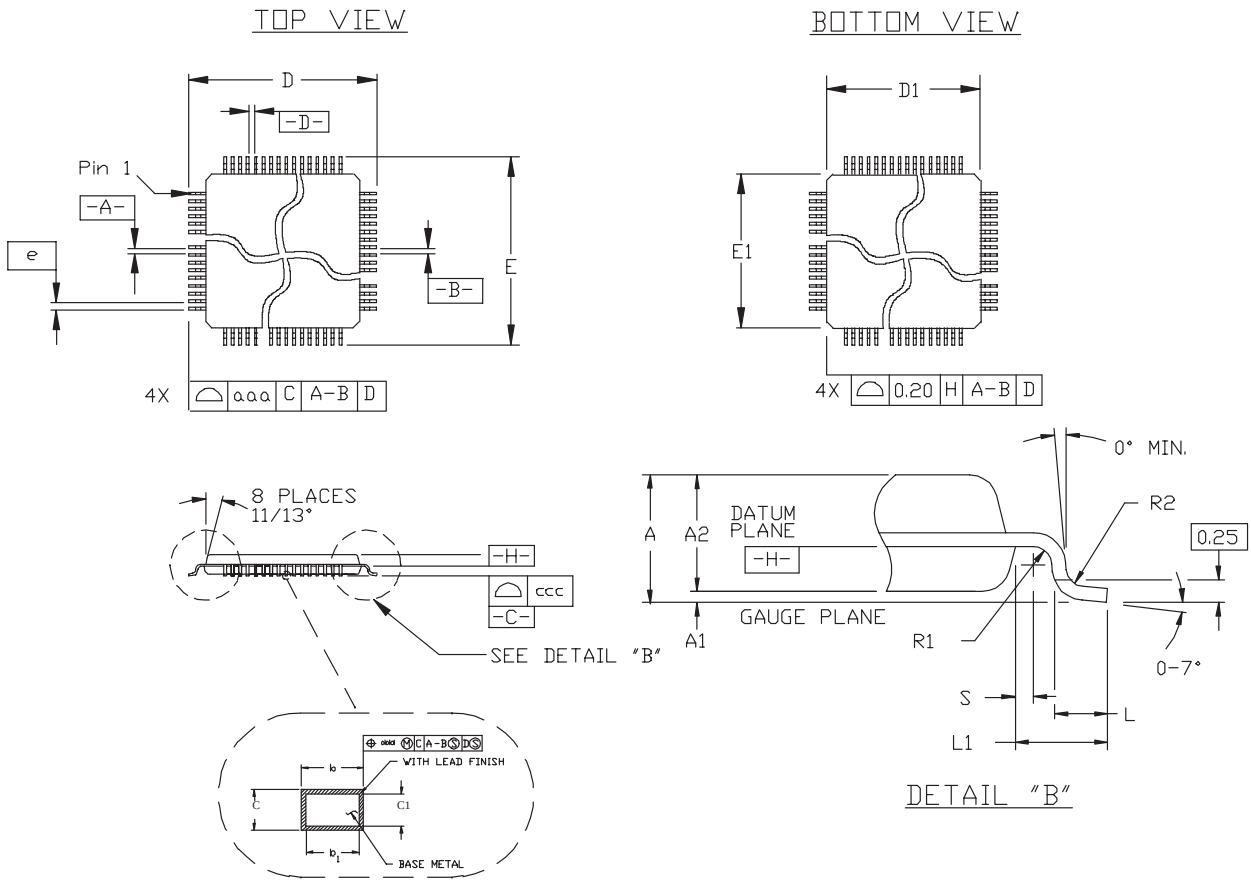
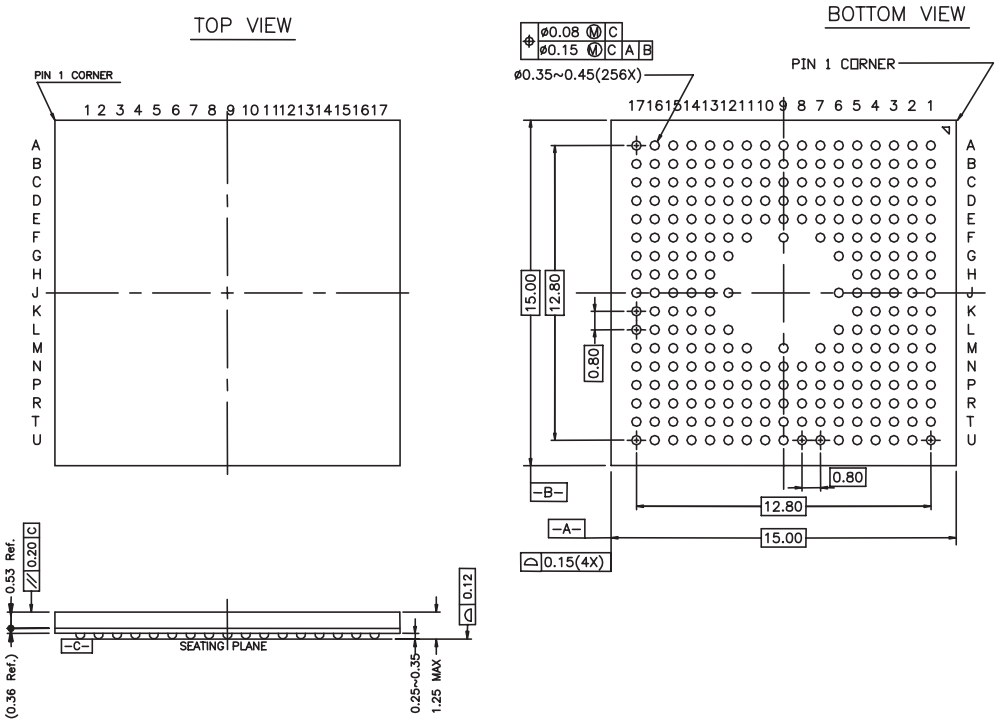


Table 7. 208-lead PQFP Package Dimensions (in mm)

Symbol	Min	Nom	Max	Symbol	Min	Nom	Max
c	0.11		0.23	b1	0.17	0.20	0.23
c1	0.11	0.15	0.19	ddd	0.10		
L	0.65	0.88	1.03	**Tolerances of Form and Position**			
L1	1.60 REF			aaa		0.25	
R2	0.13		0.3	ccc			0.1
R1	0.13			**BSC**			
S	0.4			D	31.20		
A	4.10			D1	28.00		
A1	0.25		0.50	E	31.20		
A2	3.20	3.40	3.60	E1	28.00		
b	0.17		0.27	e	0.50		

Figure 6. LFBGA Package Drawing



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