

Product Specification for model DNSA-141

Stamp Type IoE Module

Version 0.5

2014/2/21

**by
TT Huang**

**Networking Business Unit
Wistron Neweb Corporation**

CONFIDENTIAL

THIS DOCUMENT CONTAINS PROPRIETARY TECHNICAL INFORMATION, WHICH IS THE PROPERTY OF THE WISTRON NEWEB CORPORATION AND SHALL NOT BE DISCLOSED TO OTHERS IN WHOLE OR IN PART, REPRODUCED, COPIED, OR USED AS THE BASIS FOR DESIGN, MANUFACTURING, OR SALE OF APPARATUS WITHOUT WRITTEN PERMISSION OF WISTRON NEWEB CORPORATION.

● Revision History

Version	Change history	Date
V0.4	Initial version	2014/1/22
V0.5	Update RF Tx power and Rx Sensitivity, Antenna pattern based on real module	2014/2/21

● Key Features:

1. QCA4002 IoE solution
2. Internal PA and LNA, no external RFSW
3. 2.4GHz Single band IEEE 802.11b/g/n
4. 11n support HT20 and HT40 Bandwidth
5. On board printed antenna and IPEX connector(use an capacitor to select)
6. GPIO voltage is flexible, can between 1.8~3.3V
7. Single power supply: 3.3V, Low Power Consumption, also support Green Tx and very low power sleep mode for mobile battery operation application. Can be wake up and go to sleep quickly.
8. 25mm x 20mm size, 2-layer, single side component
9. Operation temperature: -40~+85 degrees C(Industry Class Version)
10. TCP/IP offload, include Encryption
11. Easy to use UART or SPI(Slave)
12. Regulatory Compliance: CE, FCC and IC

● System Block Diagram

1. DNSA141 is based on QCA4002 Internet of Everything chip and QCA's SP141 reference board design in stamp form factor.
2. WNC's DNSA141 board is still under production process so in the datasheet we use QCA's SP141's data.
3. Inside the module, there is a QCA4002 main chip which taking care the WLAN RF and BB function, also embedded a small processor which can do the encryption and TCP/IP off load. Only few external components are necessary such as XTAL and Flash. Block Diagram as Fig 1:
4. Flash is only storing the binary code to control the QCA4002. RF calibration data is stored inside QCA4002 OTP not this flash.
5. For complex control or more GPIO demanding, customer has to use a Micro Processor to control this module.

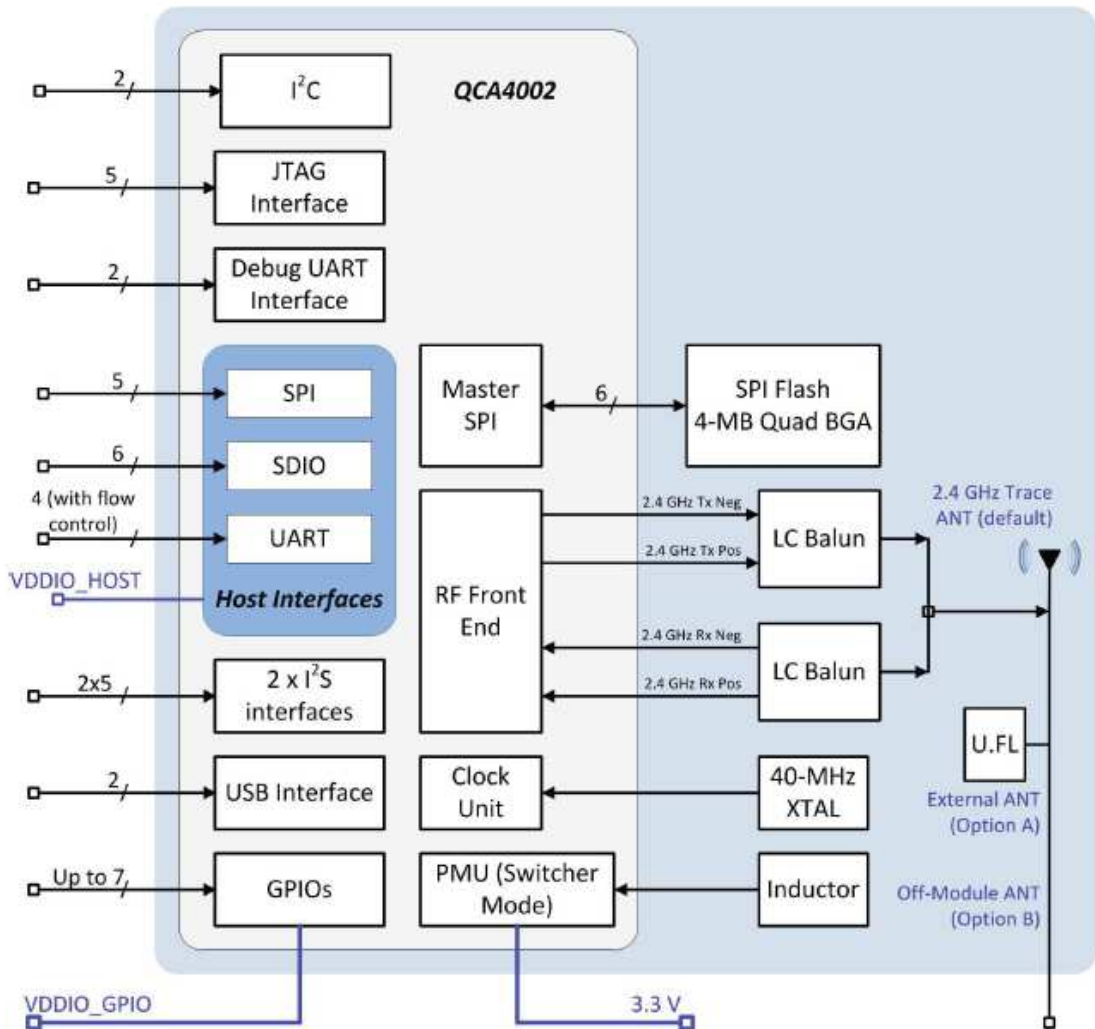


Fig. 1: Block Diagram.

- DNSA-141 Outlook

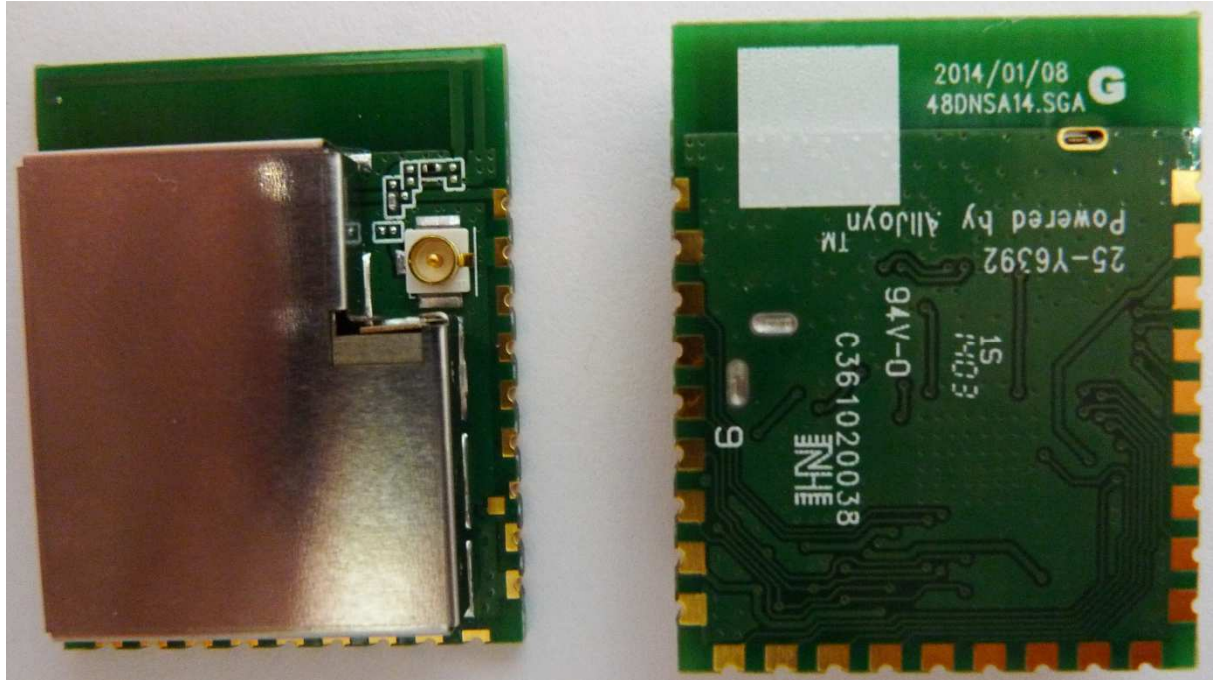


Fig.2: DNSA-141 Outlook(Left: Top side, Right: Bottom side)

- Mechanical Dim and drawing:

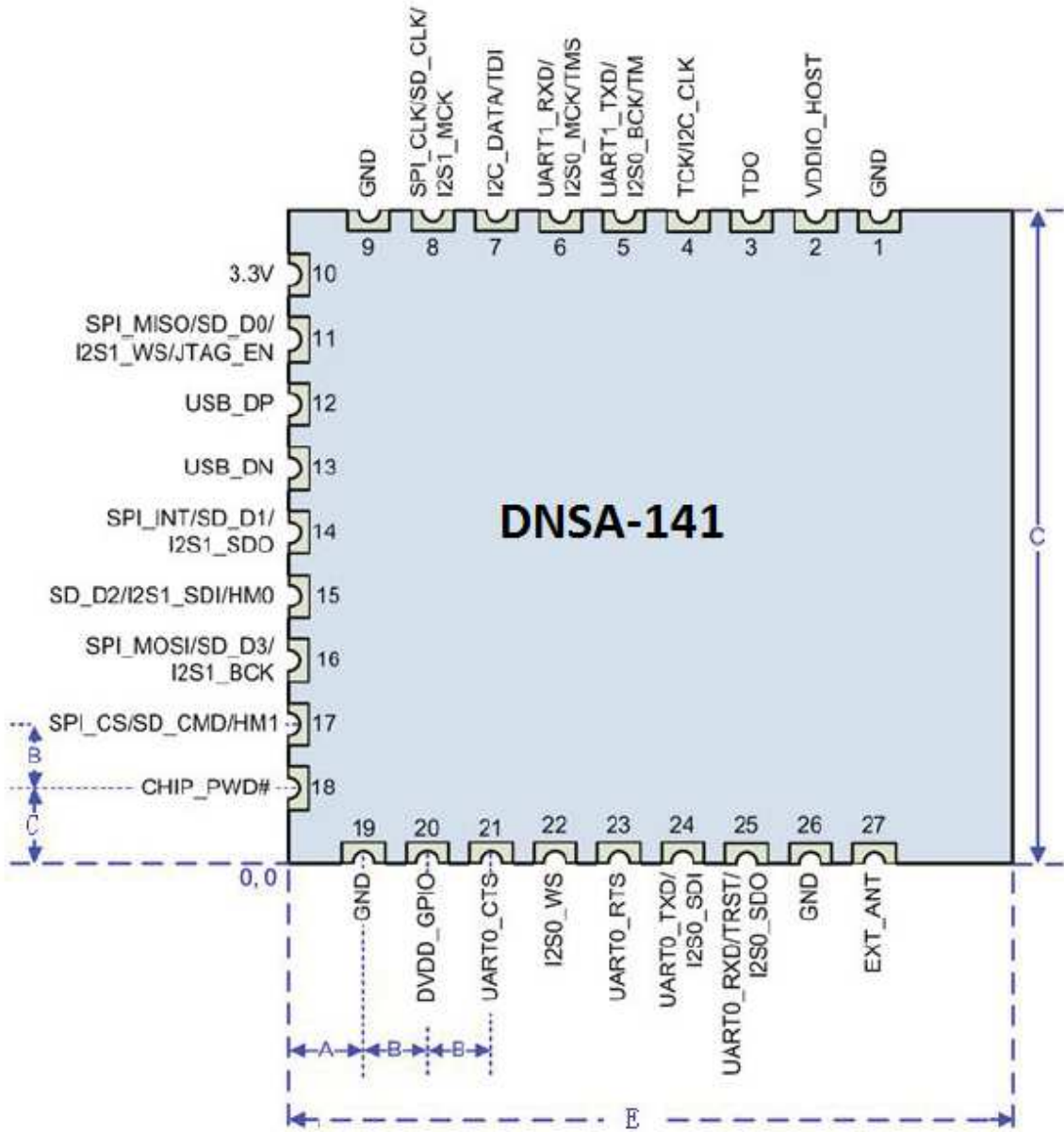


Fig. 3:A:2.5mm, B:2.0mm, C:20mm, D:25mm, total height include is about 4mm(include 3mm height shielding)

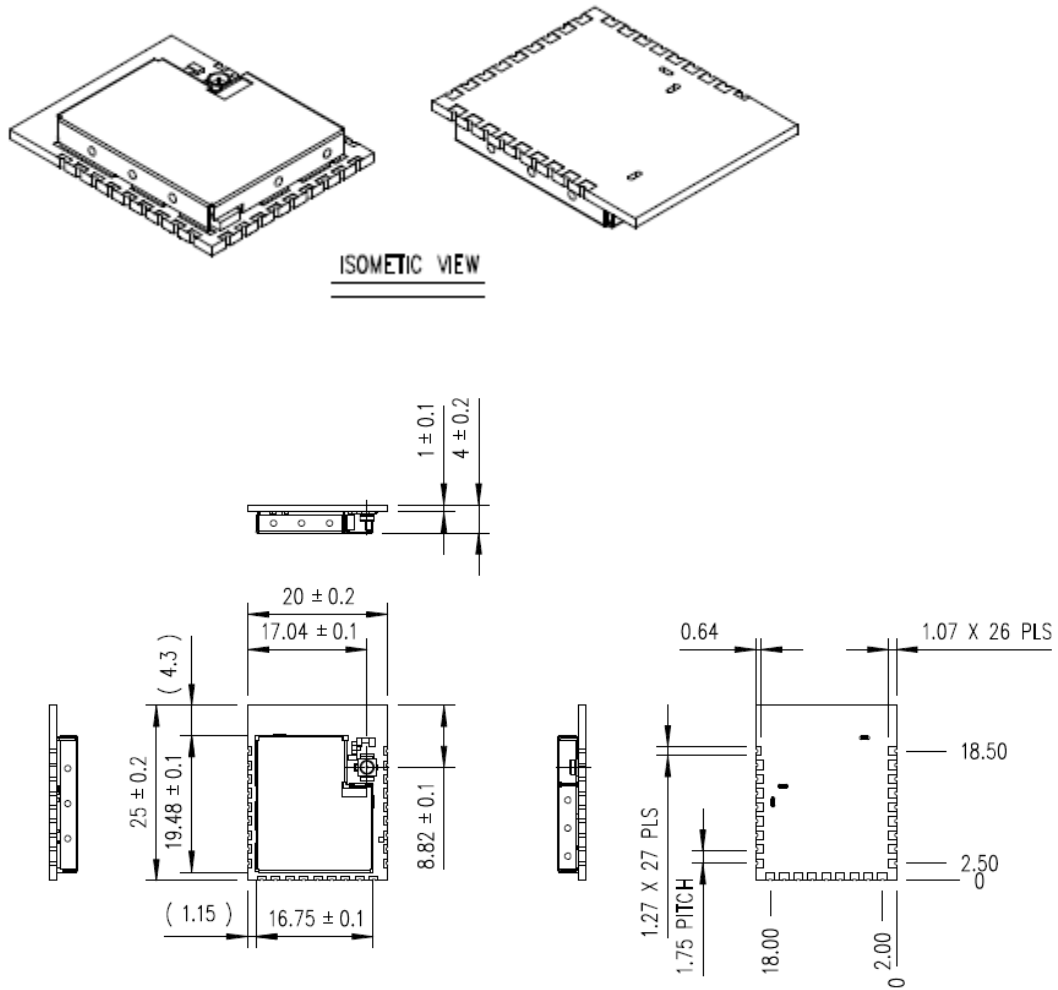


Fig. 4: Mechanical drawing with shielding. (WNC's draft version)

Note: MP without U.FL connector.

- Electrical specification:

(Assume Vcc=3.3V, Room temperature), data is estimate from QCA's SP141.

Condition	Average	Unit
11g continue Tx@1M_18dBm	810	mWatt
11n continue Tx@HT40MCS7_12dBm	600	
11b/g and 11n HT20 continue Rx	about 210	
11n HT40 continue Rx	about 240	
Idle	TBD	
Standby	TBD	

Note A: External IO voltage (DVDD_GPIO) can be 1.8~3.3V.

Note B: QCA4002 need 3.3V and 1.2V supply. For 1.2V supply there are 2 method: Switching and LDO. Inside the QCA4002, there is embedded a switching regulator to convert 3.3V to 1.2V for its chip core voltage supply. Also it has a LDO driver to act as 3.3V->1.2V LDO driver (might need external transistor). In table we consider to use switching regulator method to have better power efficiency. The tradeoff is we have to add a power inductor near QCA4002 chip. Also shielding height has to be caution to prevent the inductor magnetic field interaction with the iron material in the shielding.

Note C: **Absolute Rating: TBD.**

- Module Pin assignment and description.

Signal Name	Pin	Description
USB_DP	12	USB device / manufacturing test and configuration interface
USB_DN	13	
CHIP_PWD#	18	Power down control signal; setting this pin low forces the module in to its lowest power state
TDO	3	GPIO with multiplexed functions.
TCK/I2C_CLK	4	
UART1_TXD/I2S0_BCK/TM	5	
UART1_RXD/I2S0_MCK/TMS	6	
I2C_DATA/TDI	7	
SPI_CLK/SD_CLK/I2S1_MCK	8	
SPI_MISO/SD_D0/I2S1_WS/JTAG_EN	11	
SPI_INT/SD_D1/I2S1_SDO	14	
SD_D2/I2S1_SDI/HM0	15	
SPI_MOSI/SD_D3/I2S1_BCK	16	
SPI_CS/SD_CMD/HM1	17	
UART0_CTS	21	
I2S0_WS	22	
UART0_RTS	23	
UART0_TXD/I2S0_SDI	24	
UART0_RXD/TRST/I2S0_SDO	25	
EXT_ANT	27	Single-ended antenna connection
GND	1, 9, 19, 26	Ground
VDDIO_HOST	2	3.3 V supply for the host I/Os
3.3V	10	Analog 3.3 V supply
DVDD_GPIO	20	VDDIO 3.3 V supply for GPIOs

- RF Tx target power[unit:dBm], IEEE mask and EVM compliance power, not considering FCC/CE's regulation yet.

Mode/Rate	MHz
	2412~2472
11b 1Mbps	17
11b 11Mbps	17
11g 6Mbps	18
11g 54Mbps	14
11n HT20 MCS0	18
11n HT20 MCS7	13
11n HT40 MCS0	16
11n HT40 MCS7	12

- RF Rx sensitivity [unit:dBm]:

Mode/Rate	MHz
	2412~2472
11b 1Mbps	-92
11b 11Mbps	-85
11g 6Mbps	-88
11g 54Mbps	-71
11n HT20 MCS0	-87
11n HT20 MCS7	-67
11n HT40 MCS7	-64

- Antenna performance:
The on board printed antenna VSWR is better than 2.5 and efficiency is around 48%.

	2400	2450	2500	Avg.
Eff.	48%	51%	44%	48%
Avg. Gain	-3.19	-2.92	-3.53	
Peak Gain	0.03	0.44	-0.43	

Unit :Avg. Gain(dB), Peak Gain(dBi)



Fig.5 Antenna VSWR (Testing point is same as Fig.6)

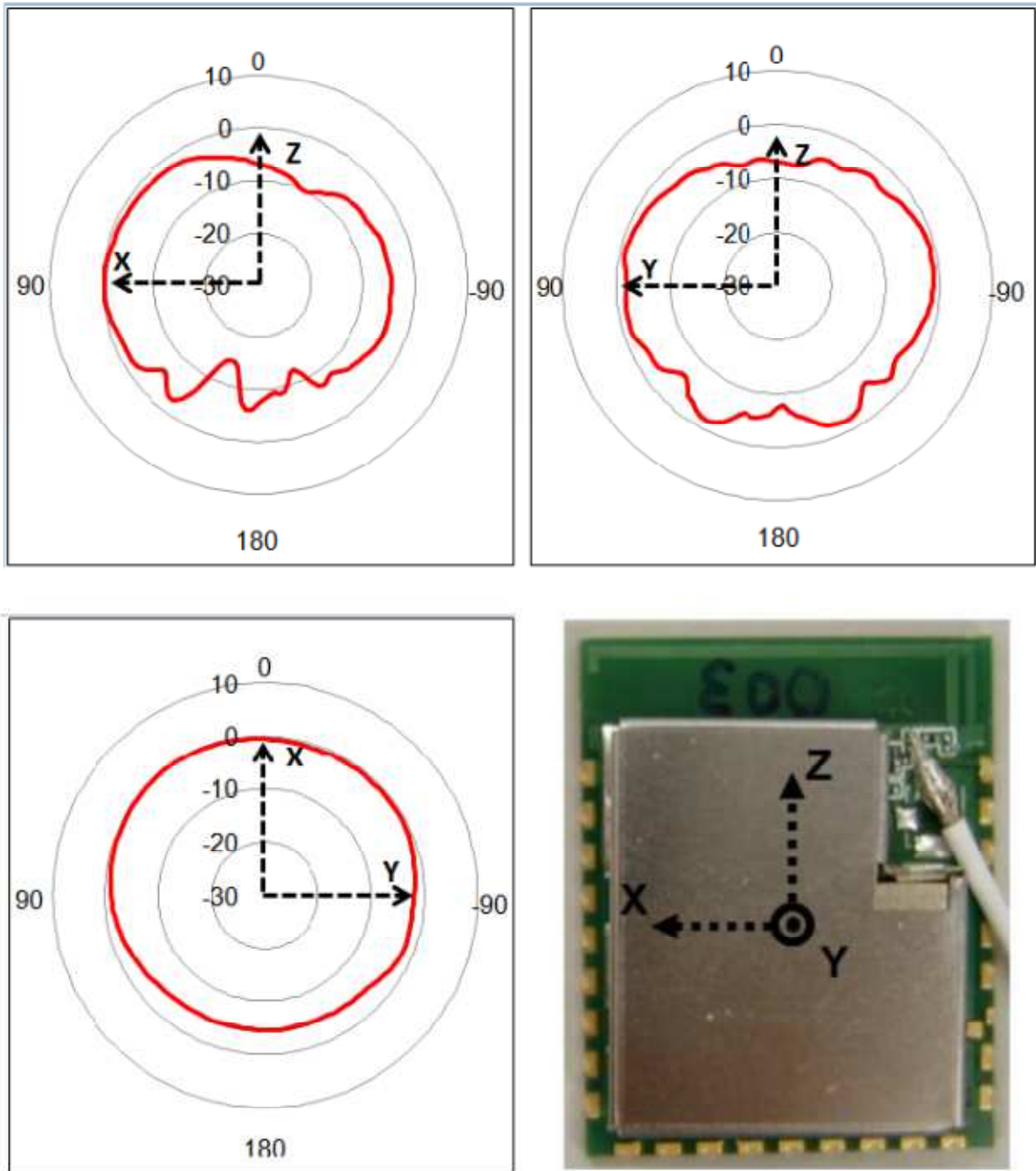
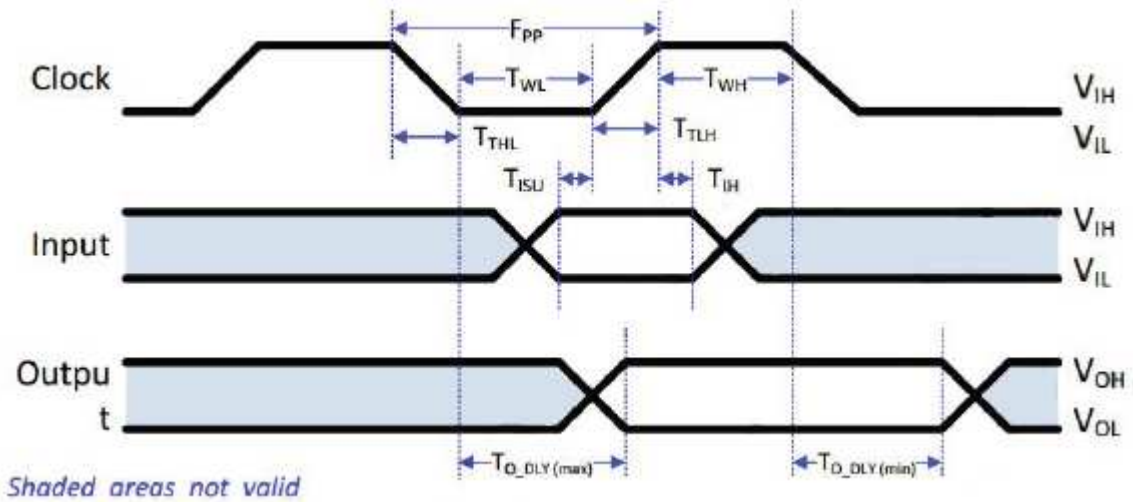


Fig.6: Antenna radiation pattern

- SPI slave interface electrical timing diagram:

Major data port interface for this module is UART and SPI, QCA recommend to use SPI if want to have higher throughput (about 6Mbps when using SPI).



Parameter	Description	Min	Max	Unit
f_{pp}	Clock frequency	0	48	MHz
t_{WL}	Clock low time	8.3	-	ns
t_{WH}	Clock high time	8.33	-	ns
t_{TLH}	Clock rise time	-	2	ns
t_{THL}	Clock fall time	-	2	ns
t_{ISU}	Input setup time	5	-	ns
t_{IH}	Input hold time	5	-	ns
t_{O_DLY}	Output delay	0	5	ns

Fig. 7: SPI slave port timing

- This module has 3 RF path:
 1. On board printed antenna: Please do not cover or put anything close to the antenna otherwise the radiation efficiency will be degraded. Also, since the shielding will be redesigned so we expect some design change on the printed

antenna is necessary after WNC has the 1st version board.

2. On board IPEX (U.FL) connector. This is most stable method if using a cable to attached external antenna.
3. RF PAD: Ideally, this can bridge the RF signal to the device outside the board.
4. Default MP version is on board printed antenna.

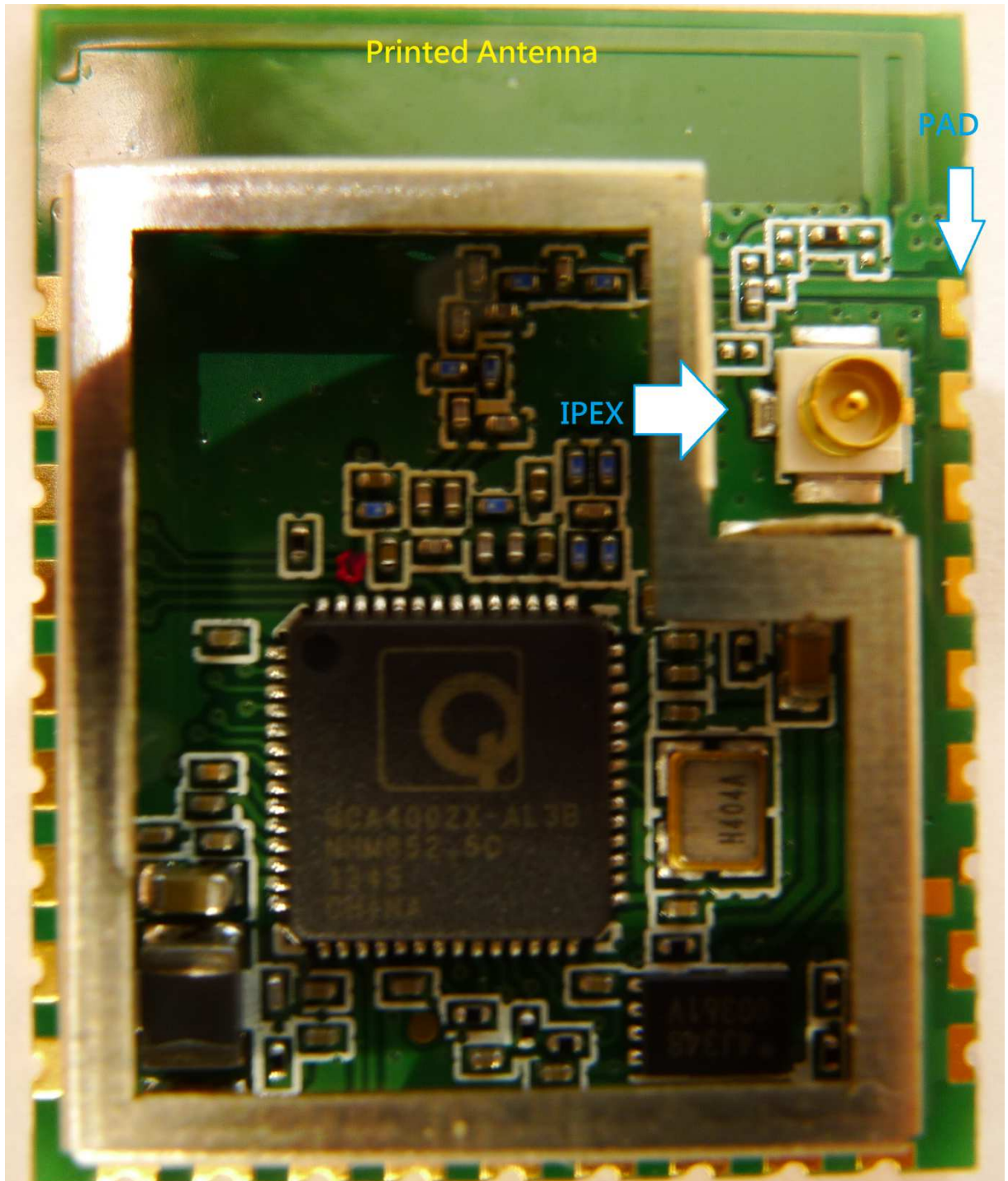


Fig. 8: RF ports and on-board antenna (shielding cover removed, the photo is sample version, final version will merge shielding frame and cover to 1 piece)

- Regulatory Compliance:
Regulatory Compliance: CE, FCC and IC
- Environment policy: All the material used inside this module is Lead Free, RoHS compliant, Halogen-Free(Optional).
- Soldering Reflow Profile: Using WNC's internal SMT line profile. Solder paste: SAC305. Fig.9.

Profile Type Selection		Lead Free Solder	
		(Sn3.0Ag0.5Cu)	
		Lead Free	
		Temperature	Time
Profile Parameter Setting	Max. Rising Slope	<3degree C/sec	
	Soaking Time	140~190degreeC	70~105sec
	Wetting Time	217degree C	70~90sec
	Peak Temperature	230~250degreeC	
	Over Wetting Time	230degree C	40~60sec

Fig.9: Estimate soldering profile for customer to mount the module.

- Ordering Information

Model	Description
DNSA-141(I)	I-temp standard